

AUTONOMOUS AUDIO HEADSET SWITCH

Check for Samples: [TS3A225E](#)

FEATURES

- V_{DD} Range = 2.7 V to 4.5 V
- Break Before Make Stereo Jack Switches
- Ground FET Switches ($<100m\Omega$)
- Autonomous Detection of GND and MIC Connections
- Detection Triggered by I²C or External Trigger Pin
- HDA Compatible MIC Present Indicator
- 1.8V Compatible I²C Switch Control
- ESD Performance Tested Per JESD 22:
 - 2000-V Human-Body Model (A114-B, Class II)
 - 500-V Charged-Device Model (C101)
- ESD Performance (SLEEVE, RING2, TIP)
 - ± 8 -kV Contact Discharge (IEC 61000-4-2)

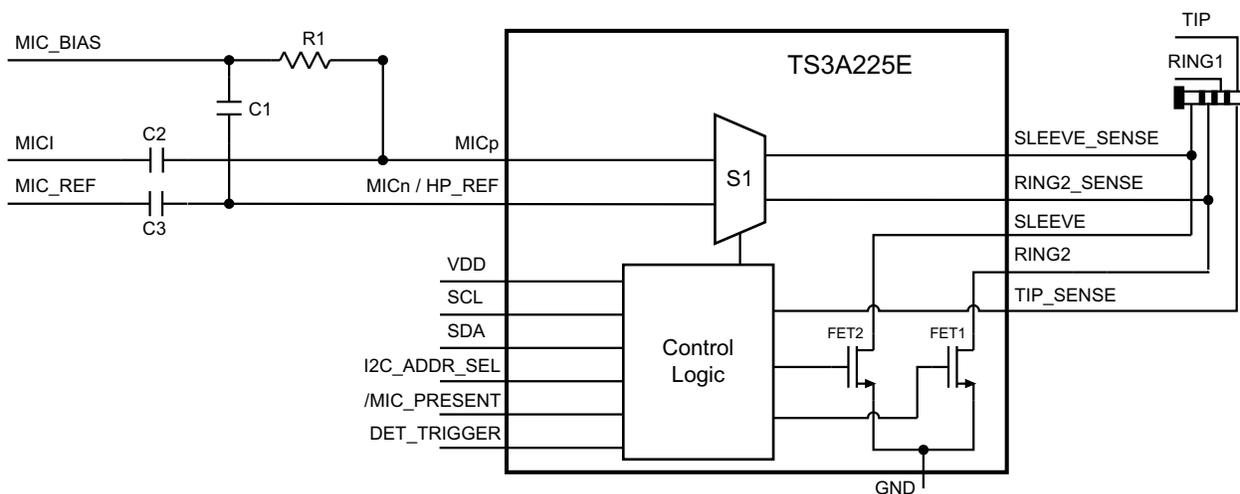
APPLICATIONS

- Mobile Phones/ Tablet PCs
- Notebook Computers

DESCRIPTION

The TS3A225E is an audio headset switch device. The device detects the presence of an analog microphone and switches a system analog microphone pin between different connectors in an audio stereo jack. The microphone connection in a stereo connector can be swapped with the ground connection depending on manufacturer. When the TS3A225E detects a certain configuration, the device automatically connects the microphone line to the appropriate pin. The device also reports the presence of an analog microphone on an audio stereo jack.

In some systems, it is desirable to connect the stereo jack pin to ground. The TS3A225E provides two internal low resistance ($<100m\Omega$) FET switches for ground shorting.



ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	YFF- WCSP	Tape and reel	TS3A225EYFFR	YP225E
-40°C to 85°C	RTE- QFN	Tape and reel	TS3A225ERTER	ZTL

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.



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To request a full data sheet, please send an email to:
signal-switches@list.ti.com

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
HPA02141EYFFR	ACTIVE	DSBGA	YFF	16	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
TS3A225ERTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TS3A225EYFFR	ACTIVE	DSBGA	YFF	16	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

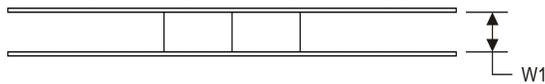
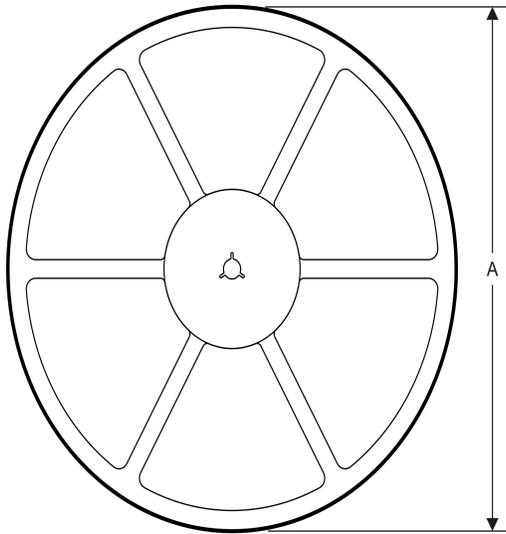
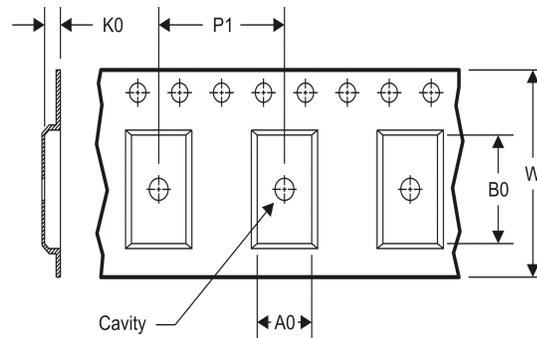
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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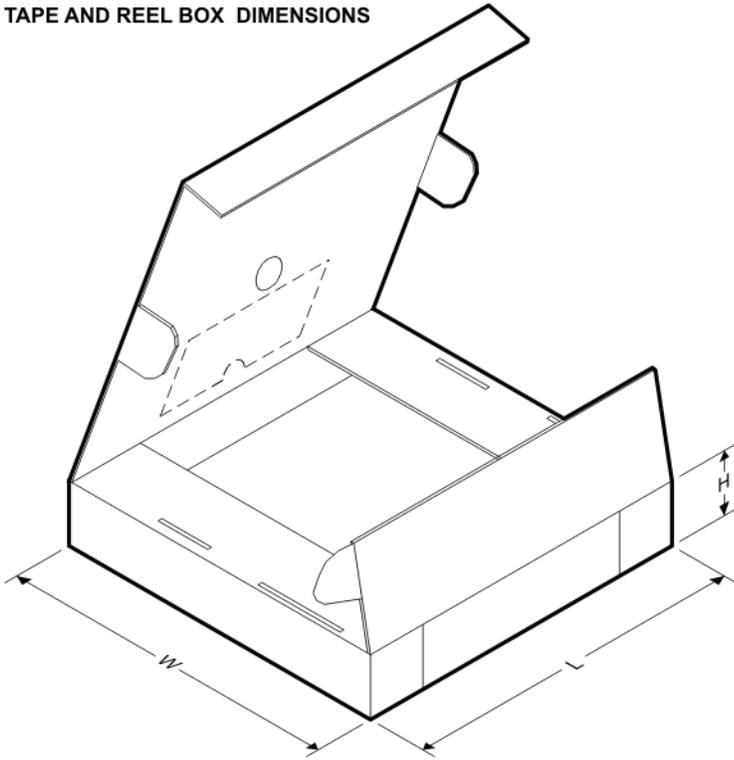
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A225ERTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS3A225EYFFR	DSBGA	YFF	16	3000	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


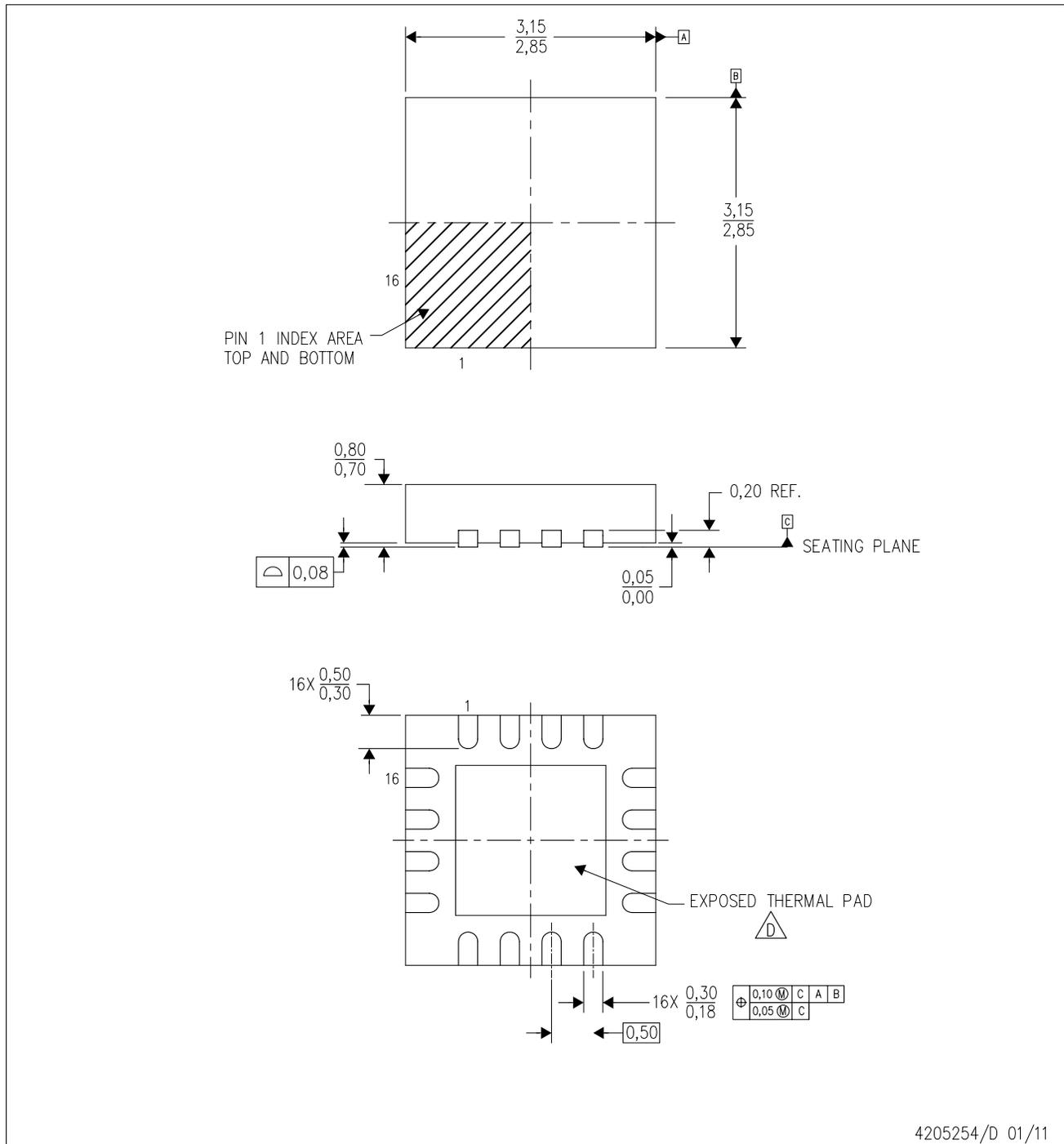
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A225ERTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TS3A225EYFFR	DSBGA	YFF	16	3000	210.0	185.0	35.0

MECHANICAL DATA

RTE (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4205254/D 01/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.

THERMAL PAD MECHANICAL DATA

RTE (S-PWQFN-N16)

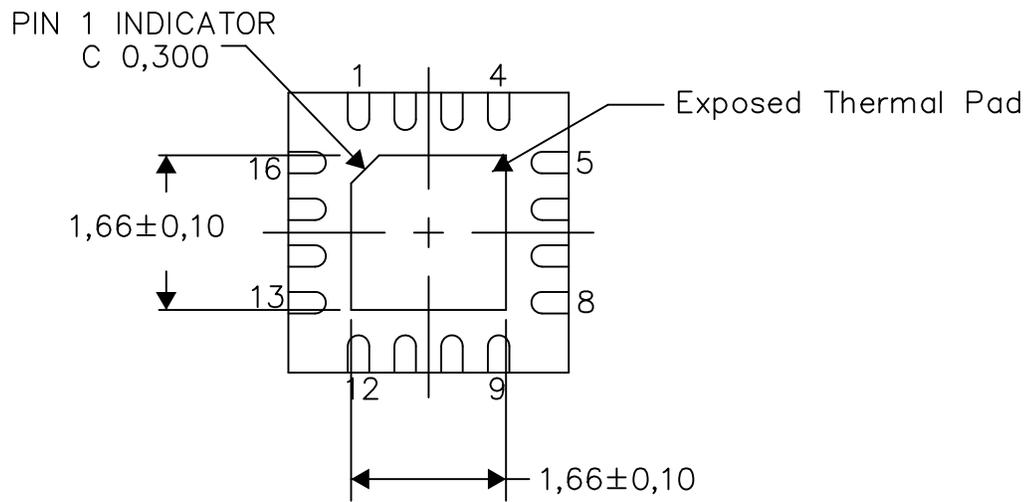
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

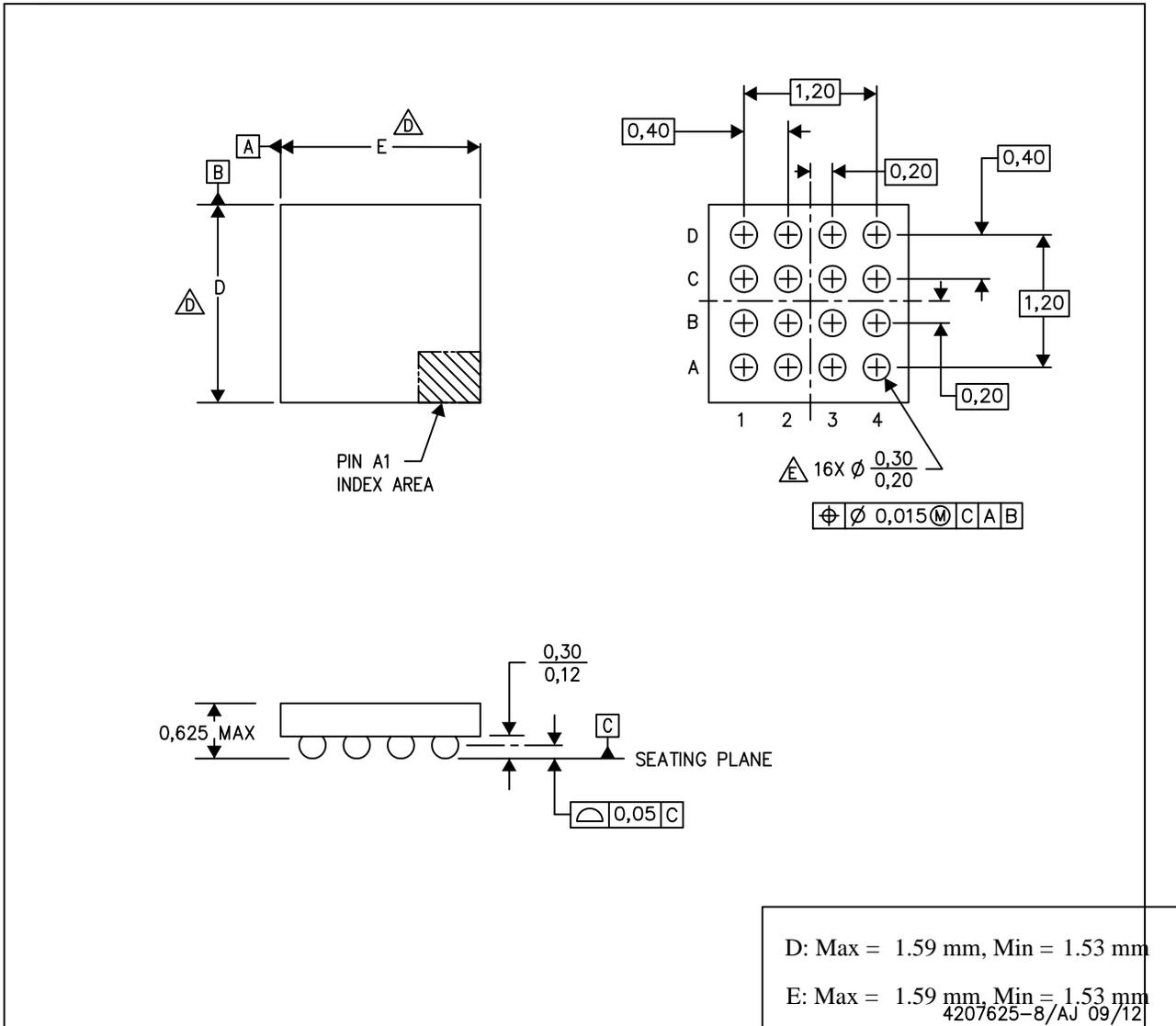
4206446-5/J 05/12

NOTE: A. All linear dimensions are in millimeters

MECHANICAL DATA

YFF (S-XBGA-N16)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 -  The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
 - E. Reference Product Data Sheet for array population.
4 x 4 matrix pattern is shown for illustration only.
 - F. This package contains Pb-free balls.

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