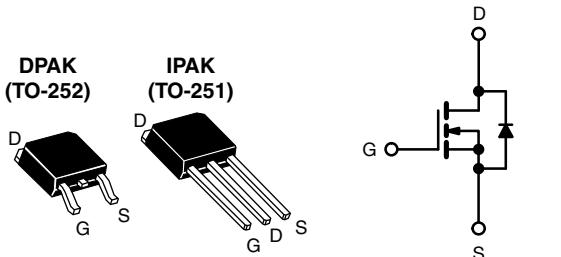


## Power MOSFET

<b>PRODUCT SUMMARY</b>	
V <sub>DS</sub> (V)	500
R <sub>DS(on)</sub> ( $\Omega$ )	V <sub>GS</sub> = 10 V      3.0
Q <sub>g</sub> max. (nC)	17
Q <sub>gs</sub> (nC)	4.3
Q <sub>gd</sub> (nC)	8.5
Configuration	Single



N-Channel MOSFET

### FEATURES

- Low gate Charge Q<sub>g</sub> results in simple drive requirement
- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Effective C<sub>oss</sub> specified
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
**HALOGEN**  
**FREE**  
Available

### APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching

### ORDERING INFORMATION

Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and Halogen-free	SiHFR420A-GE3	SiHFR420ATR-GE3 <sup>a</sup>	SiHFR420ATRL-GE3	SiHFU420A-GE3
Lead (Pb)-free	IRFR420APbF	IRFR420ATRPbF <sup>a</sup>	IRFR420ATRLPbF	IRFU420APbF

#### Note

- a. See device orientation.

### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	500	V
Gate-Source Voltage	V <sub>GS</sub>	± 30	
Continuous Drain Current	I <sub>D</sub>	3.3	A
		2.1	
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>	10	
Linear Derating Factor		0.67	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	E <sub>AS</sub>	140	mJ
Repetitive Avalanche Current <sup>a</sup>	I <sub>AR</sub>	2.5	A
Repetitive Avalanche Energy <sup>a</sup>	E <sub>AR</sub>	5.0	mJ
Maximum Power Dissipation	P <sub>D</sub>	83	W
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	3.4	V/ns
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Soldering Recommendations (Peak temperature) <sup>d</sup>	for 10 s	300	

#### Notes

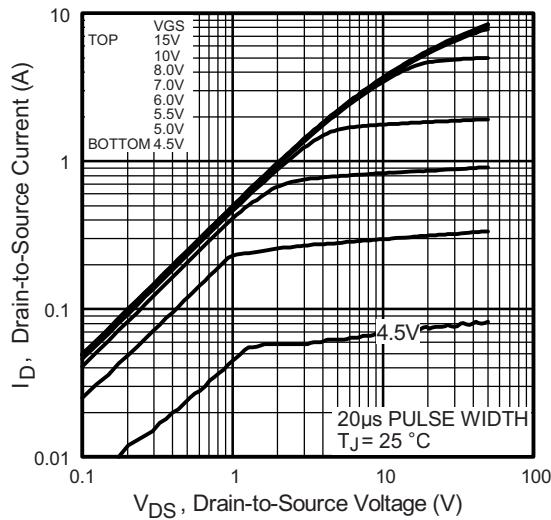
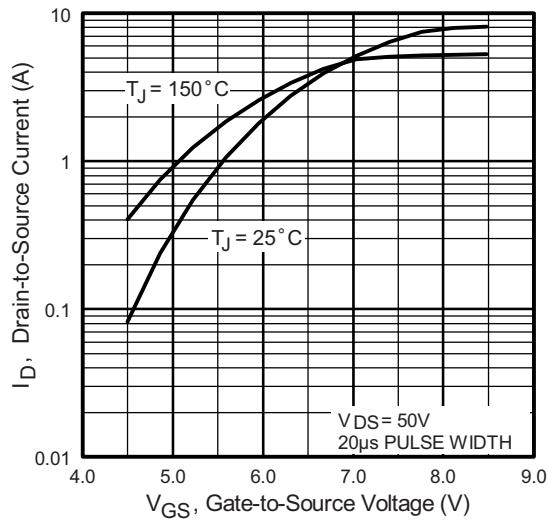
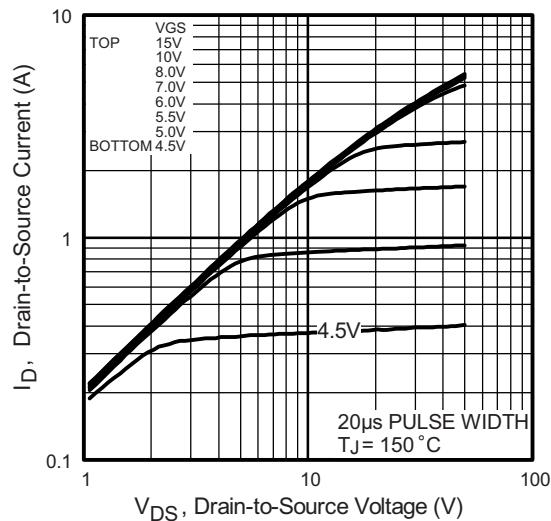
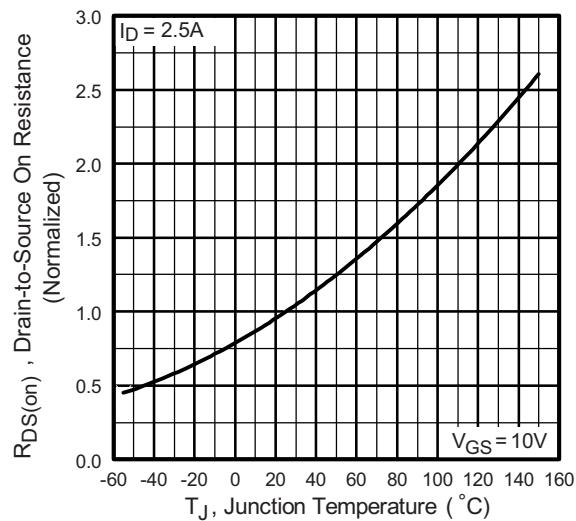
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
b. Starting T<sub>J</sub> = 25 °C, L = 45 mH, R<sub>g</sub> = 25 Ω, I<sub>AS</sub> = 2.5 A (see fig. 12).  
c. I<sub>SD</sub> ≤ 2.5 A, dI/dt ≤ 270 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 150 °C.  
d. 1.6 mm from case.

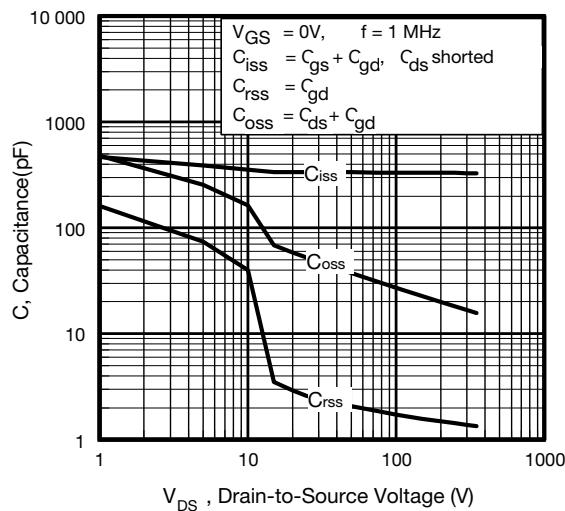
<b>THERMAL RESISTANCE RATINGS</b>				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.5	

<b>SPECIFICATIONS</b> ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$		500	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25^\circ\text{C}$ , $I_D = 1 \text{ mA}$		-	0.60	-	$\text{V}/^\circ\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$		2.0	-	4.5	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30 \text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500 \text{ V}$ , $V_{GS} = 0 \text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 400 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 125^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 1.5 \text{ A}$ <sup>b</sup>	-	-	3.0	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50 \text{ V}$ , $I_D = 1.5 \text{ A}$		1.4	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 25 \text{ V}$ , $f = 1.0 \text{ MHz}$ , see fig. 5		-	340	-	pF
Output Capacitance	$C_{oss}$			-	53	-	
Reverse Transfer Capacitance	$C_{rss}$			-	2.7	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0 \text{ V}$	$V_{DS} = 1.0 \text{ V}$ , $f = 1.0 \text{ MHz}$	-	490	-	pF
			$V_{DS} = 400 \text{ V}$ , $f = 1.0 \text{ MHz}$	-	15	-	
Effective Output Capacitance	$C_{oss\ eff.}$		$V_{DS} = 0 \text{ V}$ to $400 \text{ V}$ <sup>c</sup>	-	28	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10 \text{ V}$	$I_D = 2.5 \text{ A}$ , $V_{DS} = 400 \text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	17	nC
Gate-Source Charge	$Q_{gs}$			-	-	4.3	
Gate-Drain Charge	$Q_{gd}$			-	-	8.5	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250 \text{ V}$ , $I_D = 2.5 \text{ A}$ , $R_g = 21 \Omega$ , $R_D = 97 \Omega$ , see fig. 10 <sup>b</sup>		-	8.1	-	ns
Rise Time	$t_r$			-	12	-	
Turn-Off Delay Time	$t_{d(off)}$			-	16	-	
Fall Time	$t_f$			-	13	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	3.3	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	10	
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}$ , $I_S = 2.5 \text{ A}$ , $V_{GS} = 0 \text{ V}$ <sup>b</sup>		-	-	1.6	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}$ , $I_F = 2.5 \text{ A}$ , $dI/dt = 100 \text{ A}/\mu\text{s}$ <sup>b</sup>		-	330	500	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	760	1140	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

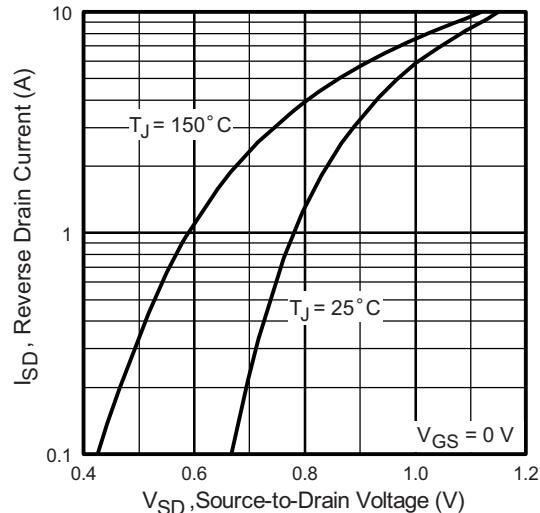
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300 \mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- c.  $C_{oss\ eff.}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .

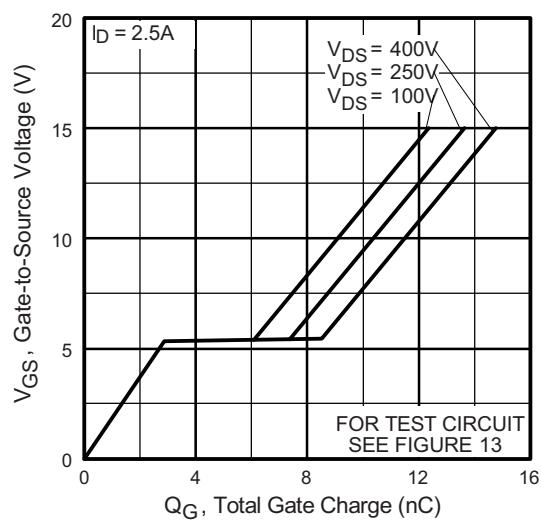
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 2 - Typical Output Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**



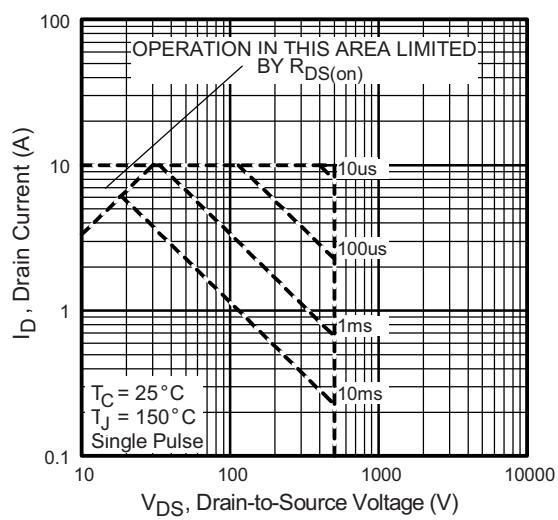
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



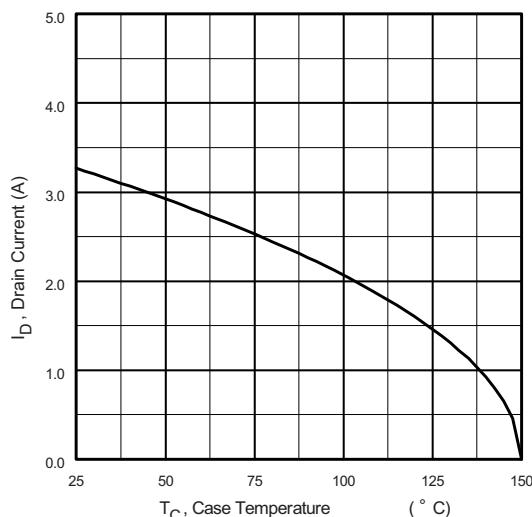
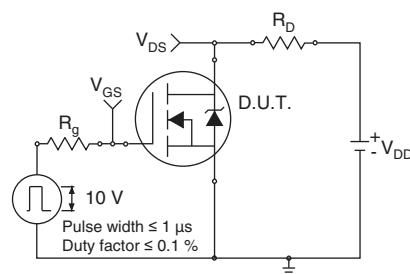
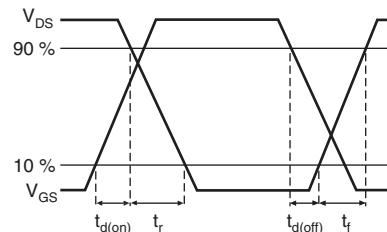
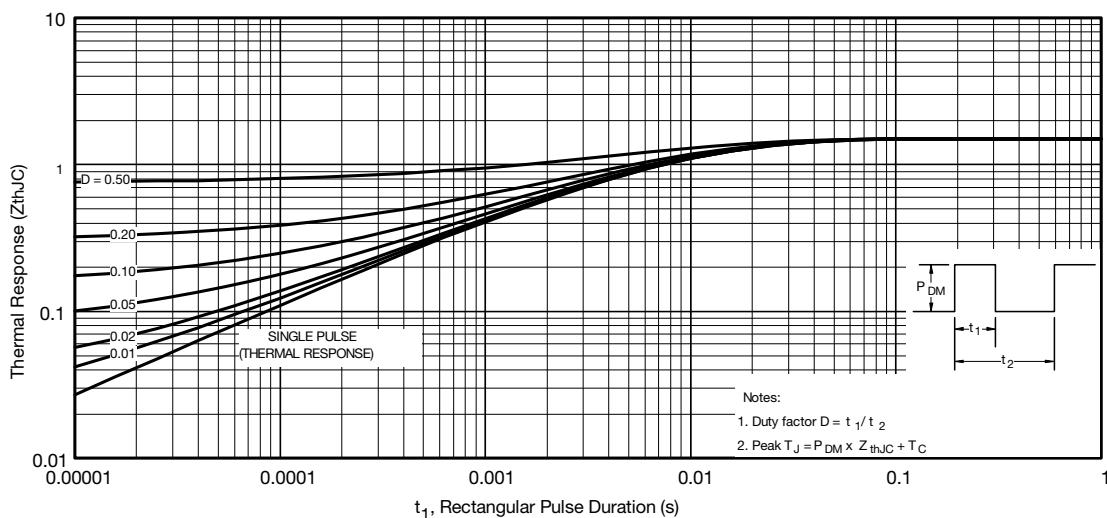
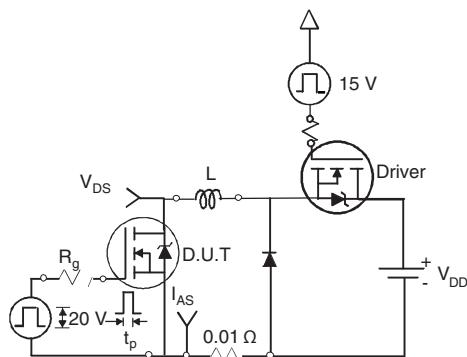
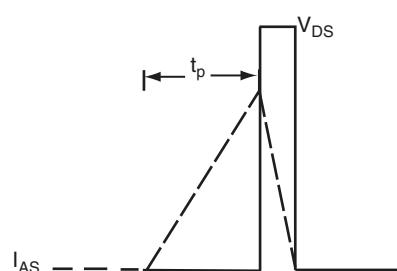
**Fig. 7 - Typical Source-Drain Diode Forward Voltage**



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**



**Fig. 8 - Maximum Safe Operating Area**


**Fig. 9 - Maximum Drain Current vs. Case Temperature**

**Fig. 10a - Switching Time Test Circuit**

**Fig. 10b - Switching Time Waveforms**

**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig. 12a - Unclamped Inductive Test Circuit**

**Fig. 12b - Unclamped Inductive Waveforms**

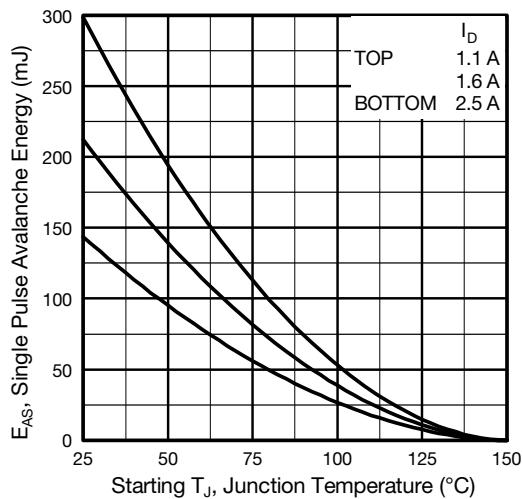


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

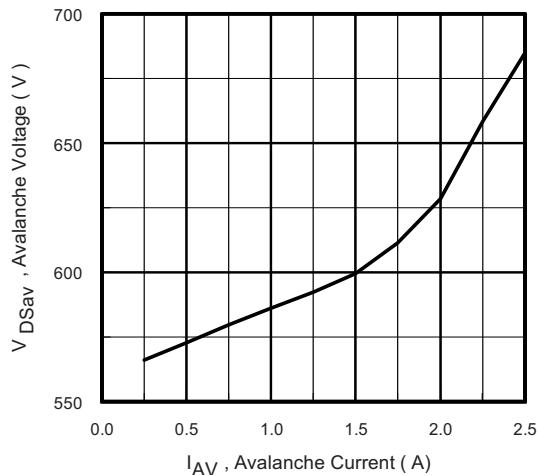


Fig. 12d - Maximum Avalanche Energy vs. Drain Current

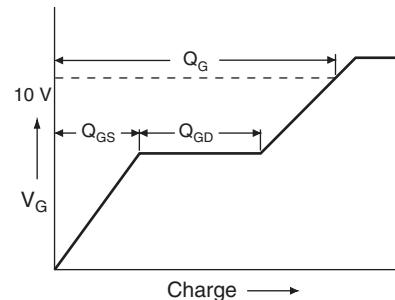


Fig. 13a - Basic Gate Charge Waveform

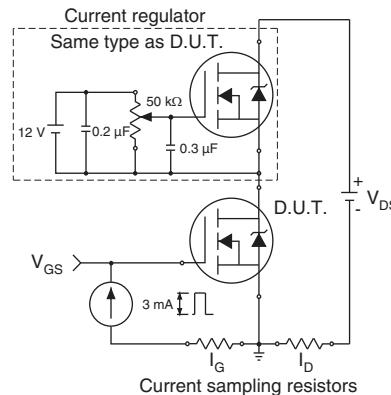
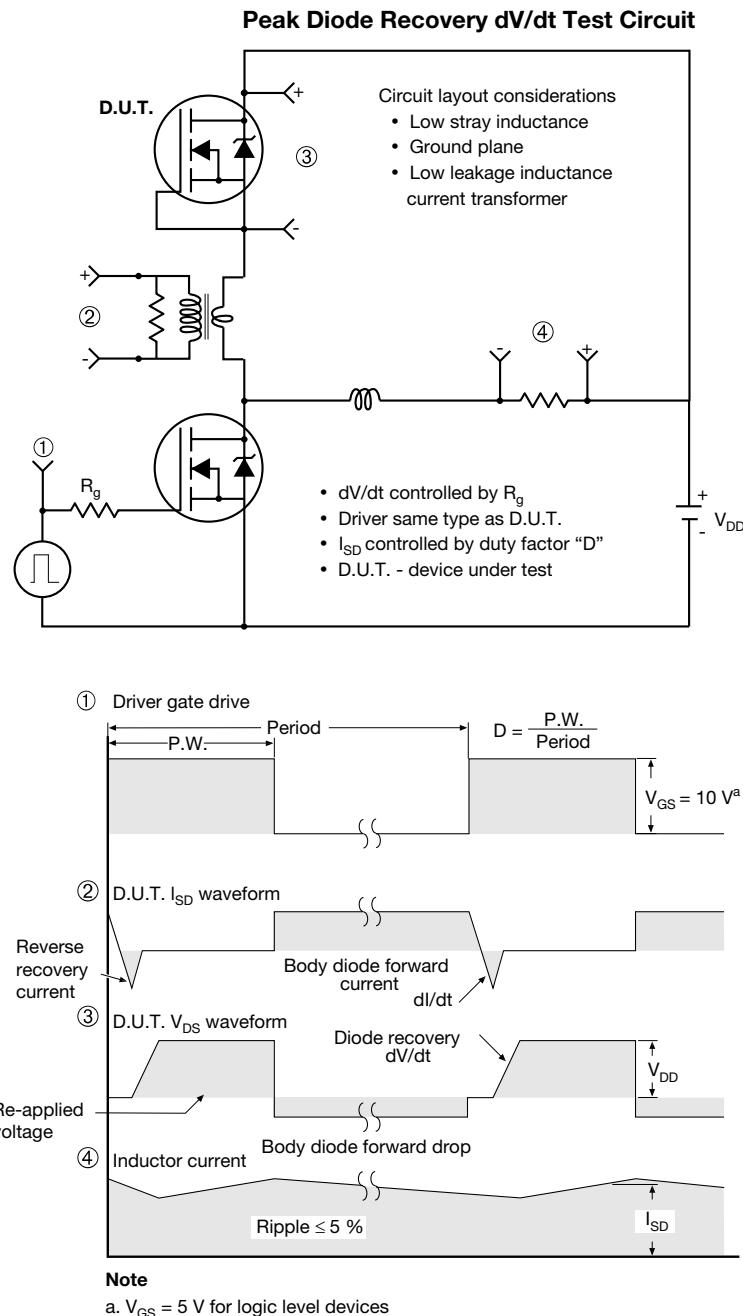
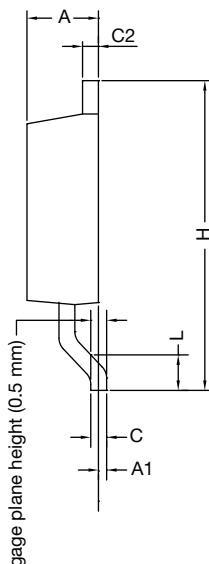
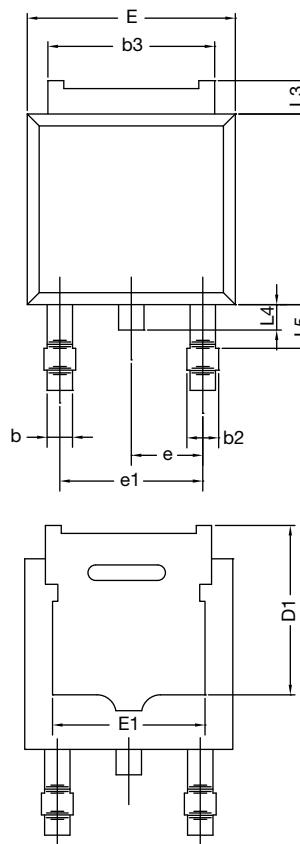


Fig. 13b - Gate Charge Test Circuit


**Fig. 14 - For N-Channel**

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### TO-252AA Case Outline



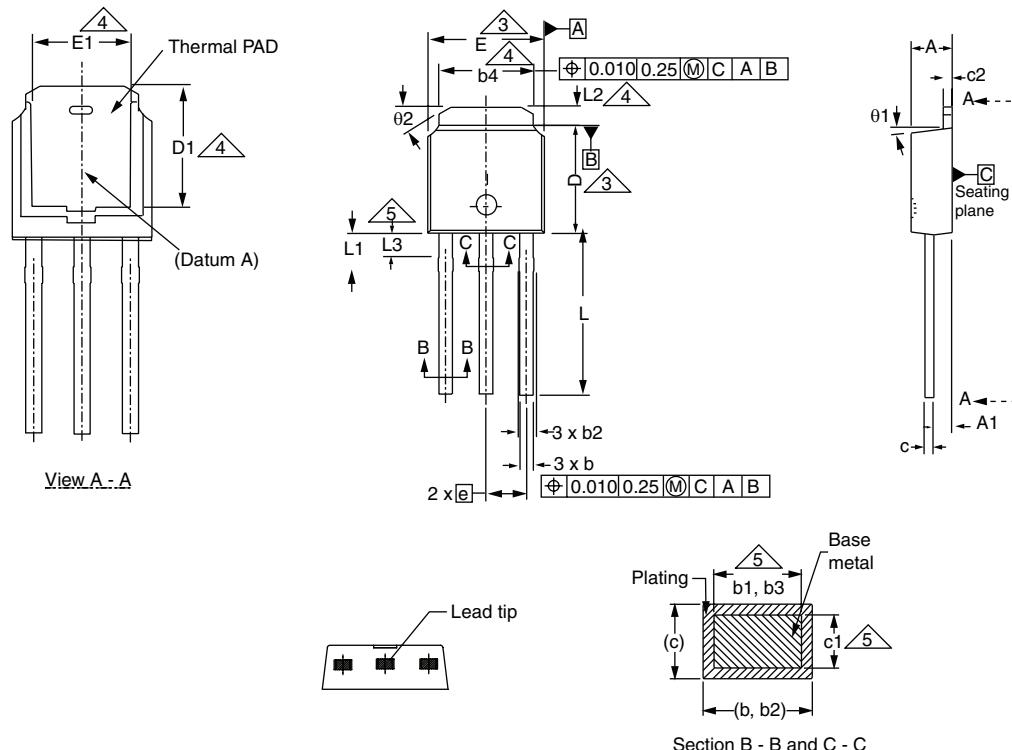
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

ECN: T16-0236-Rev. P, 16-May-16  
DWG: 5347

#### Notes

- Dimension L3 is for reference only.

### TO-251AA (HIGH VOLTAGE)



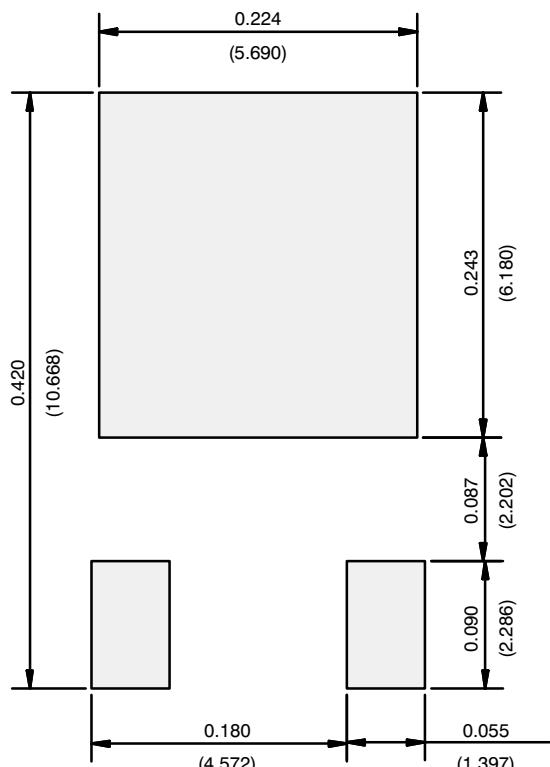
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

ECN: S-82111-Rev. A, 15-Sep-08  
DWG: 5968

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
01	0'	15'	0'	15'
02	25'	35'	25'	35'

#### Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Dimension are shown in inches and millimeters.
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
- Thermal pad contour optional with dimensions b4, L2, E1 and D1.
- Lead dimension uncontrolled in L3.
- Dimension b1, b3 and c1 apply to base metal only.
- Outline conforms to JEDEC outline TO-251AA.

**RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)**

Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)



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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: [org@eplast1.ru](mailto:org@eplast1.ru)

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.