

NVMFD5C478N

Power MOSFET

40 V, 17.0 mΩ, 27 A, Dual N-Channel

Features

- Small Footprint (5 x 6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVMFD5C478NWF – Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	40	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3, 4)	Steady State	$T_C = 25^\circ\text{C}$	I_D	A
		$T_C = 100^\circ\text{C}$	19	
Power Dissipation $R_{\theta JC}$ (Notes 1, 2, 3)		$T_C = 25^\circ\text{C}$	P_D	W
		$T_C = 100^\circ\text{C}$	12	
Continuous Drain Current $R_{\theta JA}$ (Notes 1 & 3, 4)	Steady State	$T_A = 25^\circ\text{C}$	I_D	A
		$T_A = 100^\circ\text{C}$	6.9	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)		$T_A = 25^\circ\text{C}$	P_D	W
		$T_A = 100^\circ\text{C}$	1.5	
Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10\ \mu\text{s}$	I_{DM}	90	A
Operating Junction and Storage Temperature		T_J , T_{stg}	-55 to +175	°C
Source Current (Body Diode)		I_S	19	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 1.4\text{ A}$)		E_{AS}	48	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 3)	$R_{\theta JC}$	6.5	°C/W
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	48.8	

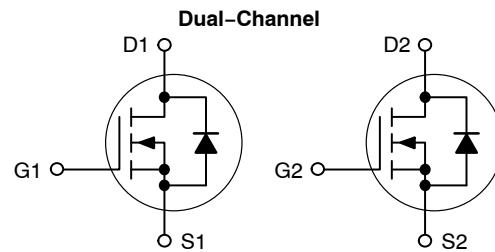
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JEDEC51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
40 V	17.0 mΩ @ 10 V	27 A



MARKING DIAGRAM



DFN8, 5x6
(S08FL)
CASE 506BT

XXXXXX = 5C478N (NVMFD5C478N) or 478NWF (NVMFD5C478NWF)
A = Assembly Location
Y = Year
ZZ = Lot Traceability
WW = Work Week
■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NVMFD5C478N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	40			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 40 V	T _J = 25°C		10	μA
			T _J = 125°C		250	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 20 μA	2.5		3.5	V
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 7.5 A		14	17	mΩ
Forward Transconductance	g _{FS}	V _{DS} = 3 V, I _D = 7.5 A		2		S

CHARGES AND CAPACITANCES

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V		325		pF
Output Capacitance	C _{oss}			165		
Reverse Transfer Capacitance	C _{rss}			10		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 32 V, I _D = 7.5 A		6.3		nC
Threshold Gate Charge	Q _{G(TH)}			1.3		
Gate-to-Source Charge	Q _{GS}			2.0		
Gate-to-Drain Charge	Q _{GD}			1.2		

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V, V _{DS} = 32 V, I _D = 7.5 A, R _G = 1 Ω		7		ns
Rise Time	t _r			13		
Turn-Off Delay Time	t _{d(off)}			14		
Fall Time	t _f			4.5		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 7.5 A	T _J = 25°C		0.84	1.2	V
			T _J = 125°C		0.72		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 7.5 A			18		ns
Charge Time	t _a				7.0		
Discharge Time	t _b				11		
Reverse Recovery Charge	Q _{RR}				6		

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

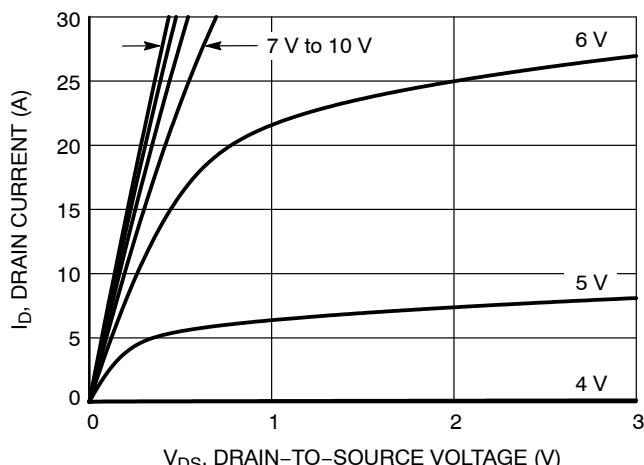


Figure 1. On-Region Characteristics

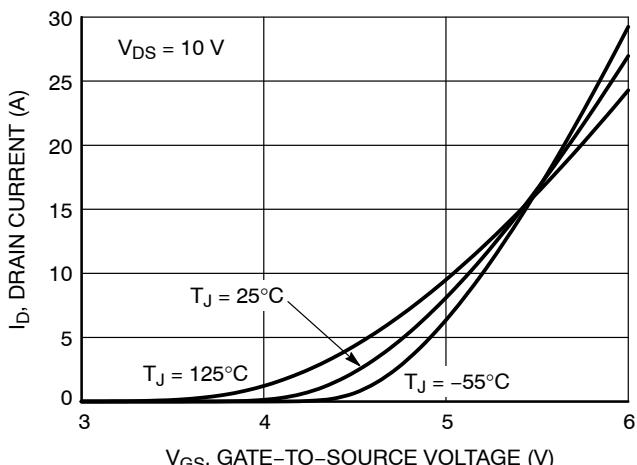


Figure 2. Transfer Characteristics

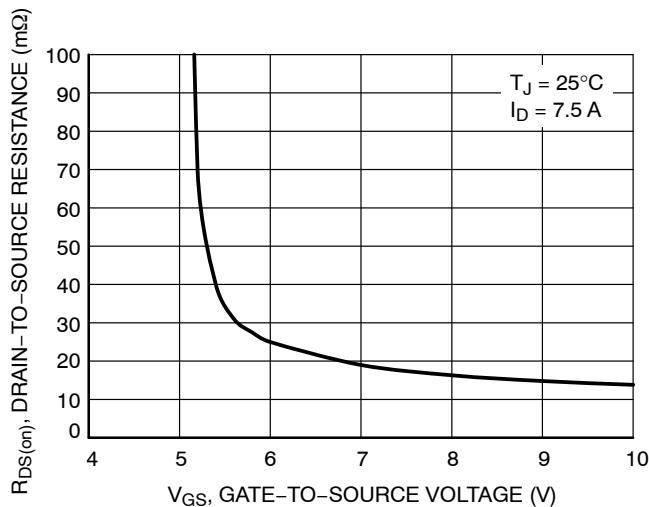


Figure 3. On-Resistance vs. Gate-to-Source Voltage

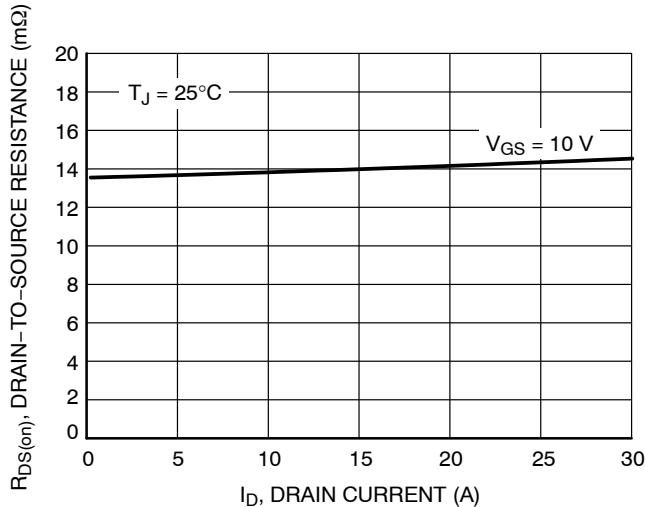


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

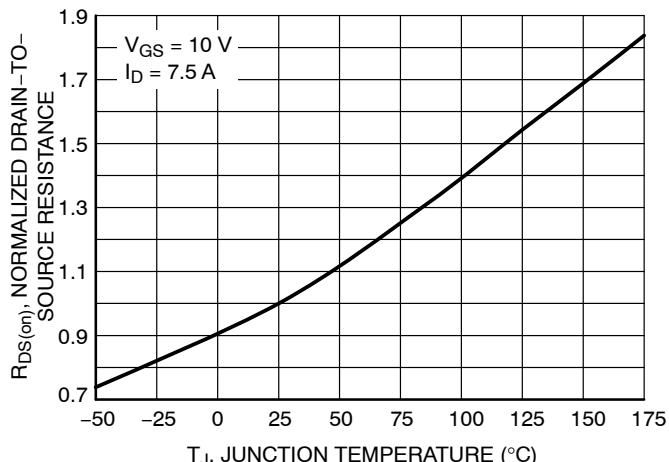


Figure 5. On-Resistance Variation with Temperature

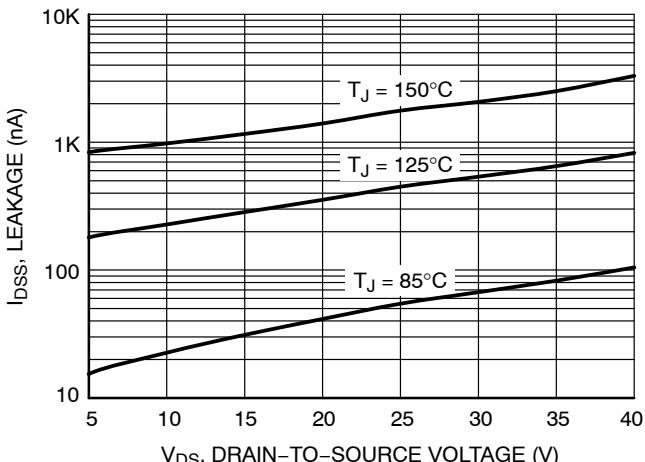
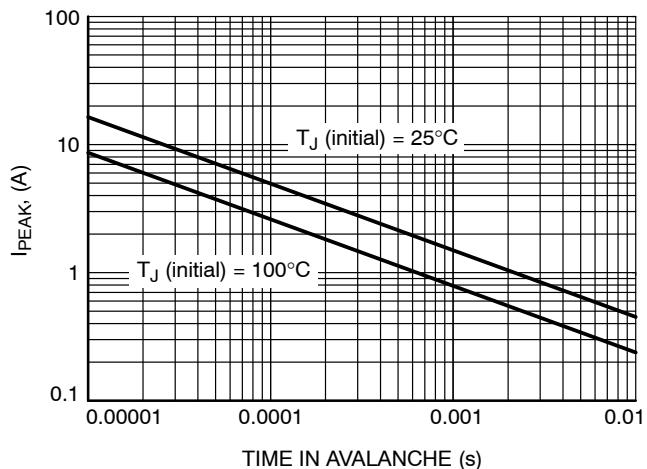
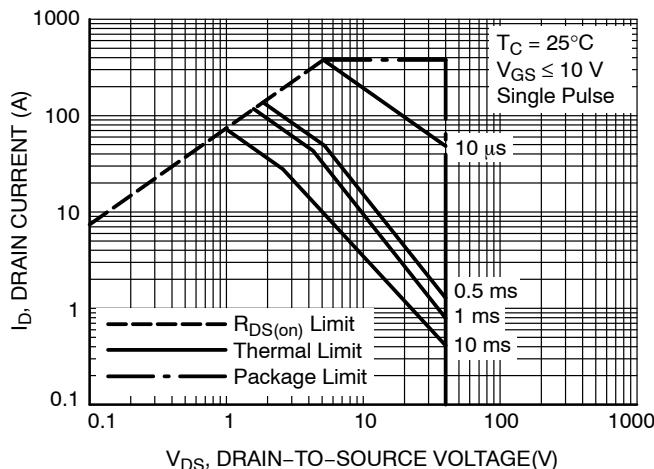
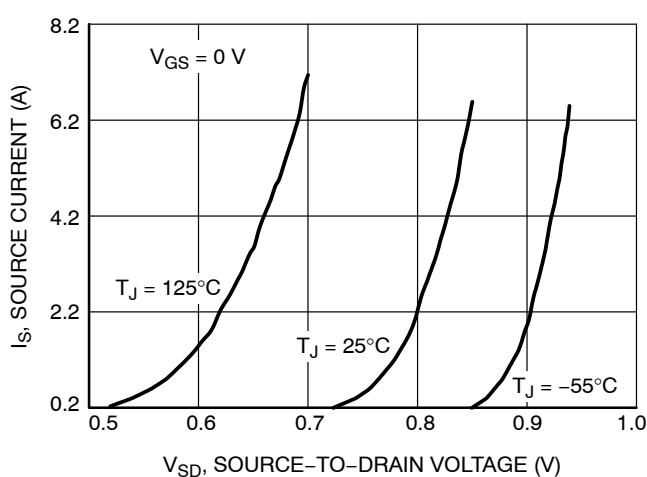
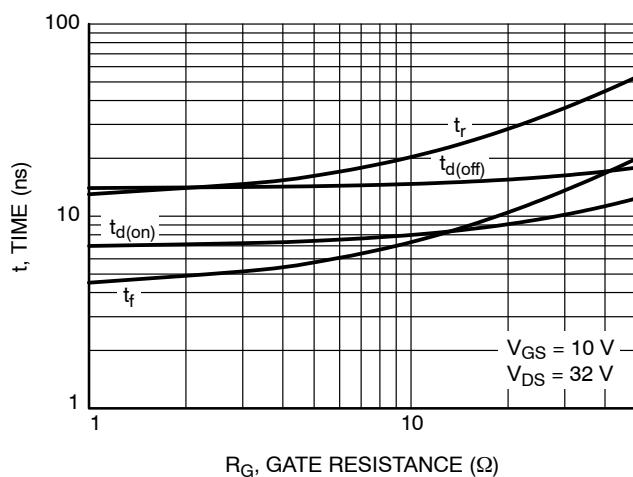
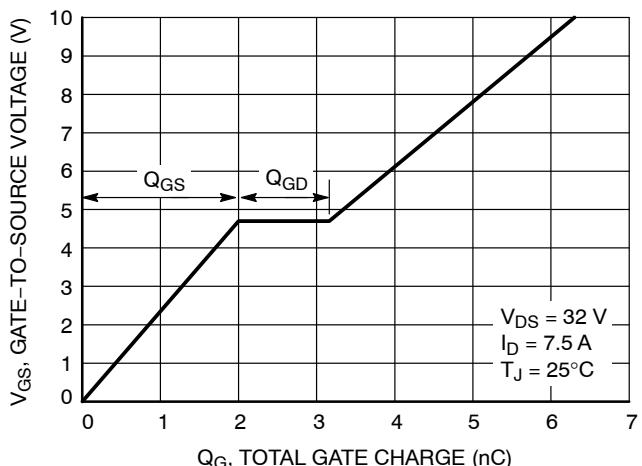
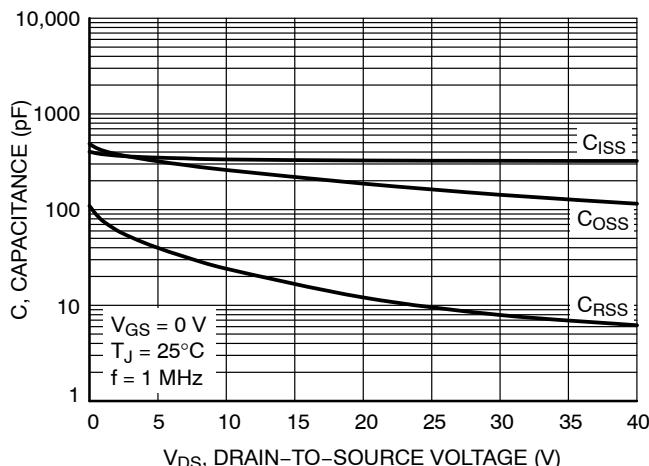
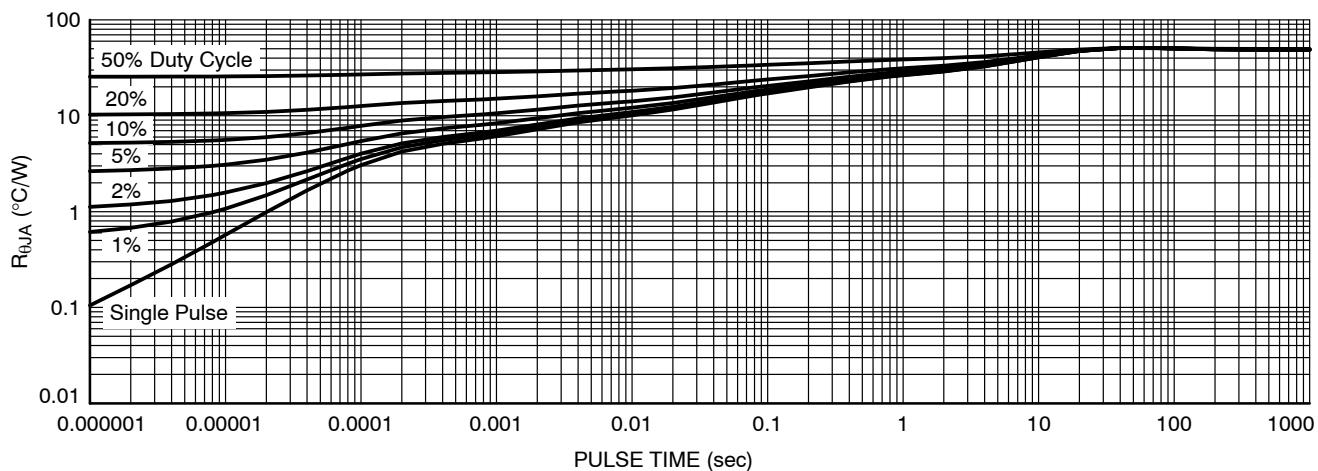


Figure 6. Drain-to-Source Leakage Current vs. Voltage

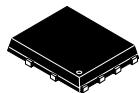
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS**Figure 13. Thermal Characteristics****DEVICE ORDERING INFORMATION**

Device	Marking	Package	Shipping [†]
NVMFD5C478NT1G	5C478N	DFN8 (Pb-Free)	1500 / Tape & Reel
NVMFD5C478NWFT1G	478NWF	DFN8 (Pb-Free)	1500 / Tape & Reel

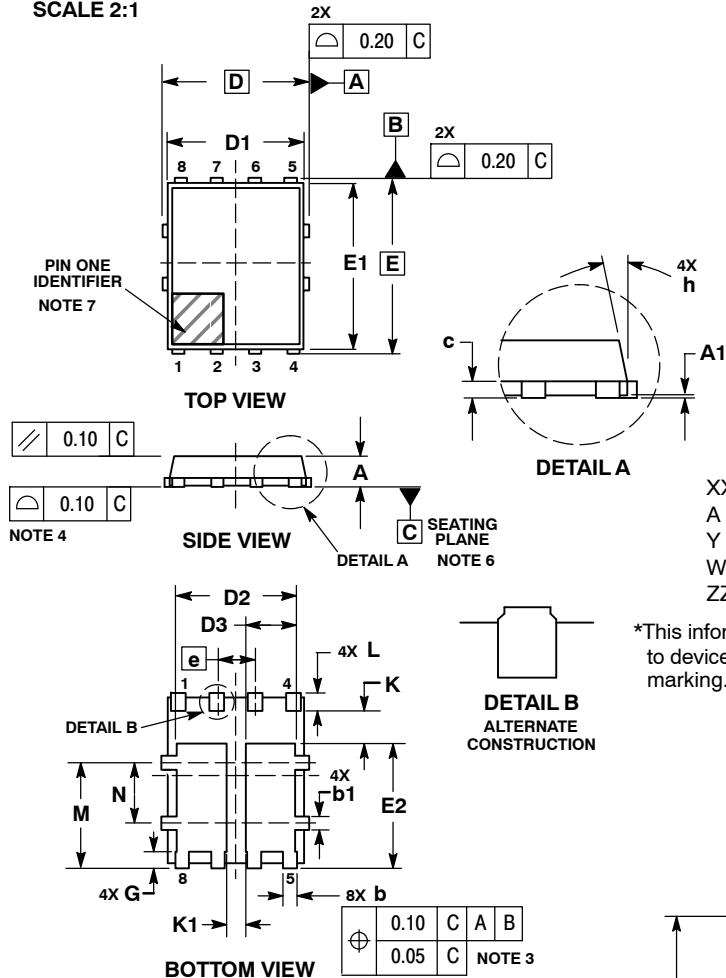
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



1
SCALE 2:1

DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual)
CASE 506BT
ISSUE E

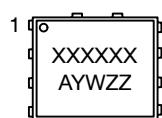
DATE 26 FEB 2013



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.

GENERIC MARKING DIAGRAM*

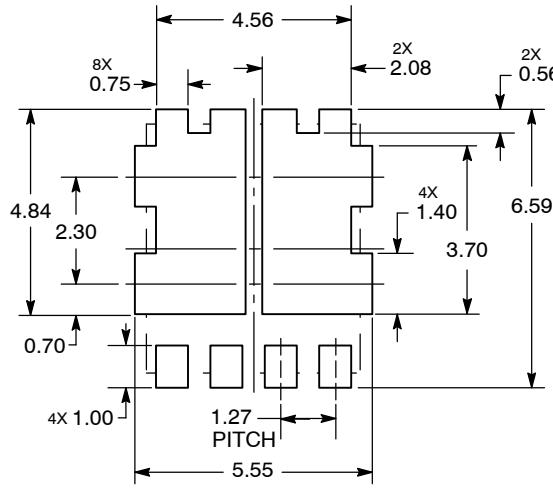


XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking.

DIM	MILLIMETERS		
	MIN	MAX	MAX
A	0.90	---	1.10
A1	---	---	0.05
b	0.33	0.42	0.51
b1	0.33	0.42	0.51
c	0.20	---	0.33
D	5.15 BSC		
D1	4.70	4.90	5.10
D2	3.90	4.10	4.30
D3	1.50	1.70	1.90
E	6.15 BSC		
E1	5.70	5.90	6.10
E2	3.90	4.15	4.40
e	1.27 BSC		
G	0.45	0.55	0.65
h	---	---	12 °
K	0.51	---	---
K1	0.56	---	---
L	0.48	0.61	0.71
M	3.25	3.50	3.75
N	1.80	2.00	2.20

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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NEW STANDARD:		
DESCRIPTION:	DFN8 5X6, 1.27P DUAL FLAG (SO8FL-DUAL)	PAGE 1 OF 2



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PAGE 2 OF 2

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