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### **CMOSIC** 8K-byte FROM and 512-byte RAM integrated

# 8-bit 1-chip microcontroller

### Overview

The LC87F2608A is an 8-bit microcontroller that, centered around a CPU running at a minimum bus cycle time of 100ns, integrates on a single chip a number of hardware features such as 8K-byte flash ROM, 512-byte RAM, an on-chip debugger, two sophisticated 16-bit timers/counters (may be divided into 8-bit timers), a synchronous SIO interface, a high-speed 12-bit PWM, two high-speed pulse width/period counters, a 3-channel AD converter with 12-/8-bit resolution selector, an analog comparator, a watchdog timer, an internal reset circuit, a system clock frequency divider, and a 16-source 10-vector interrupt feature.

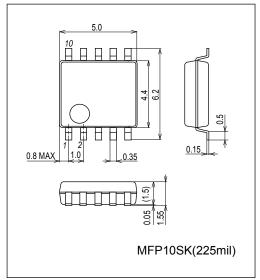
#### **Features**

- Flash ROM
  - 8192 × 8 bits (LC87F2608A)
  - Capable of on-board-programming with wide range of voltage source (3.0 to 5.5V).
  - Block-erasable in 128-byte units
- RAM
  - 512 × 9 bits (LC87F2608A)
- Package Form
  - MFP10SK: Lead-/Halogen-free type
  - MFP14S (for debugging only): Lead-free type
  - MFP10S: Lead-/Halogen-free type (discontinued)

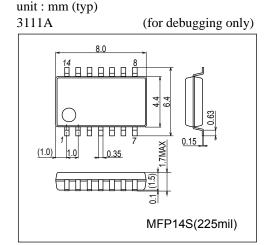
### **Package Dimensions**

unit: mm (typ)

3420



### **Package Dimensions**



### **Package Dimensions**

unit: mm (typ)

3086B (discontinued) 10 6 П П П <u>П П</u> П

(0.5)

MFP10S(225mil)

\* This product is licensed from Silicon Storage Technology, Inc. (USA).

- Minimum Bus Cycle Time (Note1)
  - 100ns (10MHz) V<sub>DD</sub>=2.7 to 5.5V (Note2)
- Minimum Instruction Cycle Time
  - 300ns (10MHz) V<sub>DD</sub>=2.7 to 5.5V (Note2)

Note1: The bus cycle time here refers to the ROM read speed.

Note2: Use this product in a voltage range of 3.0 to 5.5V because the minimum release voltage (PORRL) of the power-on reset (POR) circuit is 2.87V±0.12V.

#### ■ Ports

• I/O ports

Ports whose I/O direction can be designated in 1 bit units: 7 (P10 to P12, P30 to P33)

• Reset pins:  $1 (\overline{RES})$ 

• Power pins: 2 (V<sub>SS</sub>1, V<sub>DD</sub>1)

### ■ Timers

• Timer 0: 16-bit timer/counter with a capture register

Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register)  $\times$  2 channels

Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register)

+ 8-bit counter (with an 8-bit capture register)

Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)

Mode 3: 16-bit counter (with a 16-bit capture register)

• Timer 1: 16-bit timer/counter

Mode 0: 8-bit timer with an 8-bit prescaler + 8-bit timer/counter with an 8-bit prescaler

Mode 2: 16-bit timer/counter with an 8-bit prescaler

#### ■ Serial Interface

- SIO7: 8-bit synchronous serial interface
  - 1) LSB first/MSB first mode selectable
  - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)

### ■ High-speed 12-bit PWM

- System clock/high-speed RC oscillation clock (20MHz or 40MHz) operation selectable
- Duty/period programmable
- Continuous PWM output/specific count PWM output (automatic stop) selectable

#### ■ High-speed Pulse Width/Period Counter

- HCT1: High-speed pulse width/period counter 1
  - 1) System clock/high-speed RC oscillation clock (20MHz or 40MHz) operation selectable
  - 2) H-level width/L-level width/period measurement modes selectable
  - 3) Input triggering noise filter
- HCT2: High-speed pulse width/period counter 2
  - 1) System clock/high-speed RC oscillation clock (20MHz or 40MHz) operation selectable
  - 2) Can measure both L-level width and period simultaneously.
  - 3) Input triggering noise filter
  - 4) Input trigger selectable (from 3 signals, i.e., P11/HCT2IN, P31/HCT2IN, and analog comparator output)

- $\blacksquare$  AD Converter: 12 bits  $\times$  3 channels
  - 12-/8-bit AD converter resolution selectable

#### ■ Analog Comparator

- Sends output to the P32/CMPO port (polarity selectable).
- Edge detection function (shared with INTC and also allows the selection of the noise filter function)

#### ■ Watchdog Timer

- Can generate the internal reset signal on a timer overflow monitored by the WDT-dedicated low-speed RC oscillation clock (30kHz).
- Allows selection of continue, stop, or hold mode operation of the counter on entry into the HALT/ HOLD mode.

#### ■ Interrupt Source Flags

- 16 sources, 10 vector addresses
- 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
- 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INTA
2	0000BH	X or L	INTB
3	00013H	H or L	INTC/T0L/INTE
4	0001BH	H or L	INTD/INTF
5	00023H	H or L	T0H/SIO7
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	HCT1
8	0003BH	H or L	HCT2
9	00043H	H or L	ADC/HPWM automatic stop/HPWM cycle
10	0004BH	H or L	None

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.
- Subroutine Stack Levels: 256 levels maximum (The stack is allocated in RAM.)

#### ■ High-speed Multiplication/Division Instructions

- 16 bits  $\times$  8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

#### ■ Oscillation Circuits

- Medium speed RC oscillation circuit (internal): For system clock (1MHz)
- Low speed RC oscillation circuit (internal): For watchdog timer (30kHz)
- High speed RC oscillation circuit (internal): For system clock (20MHz or 40MHz)
  - 1) 2 source oscillation frequencies (20MHz or 40MHz) selectable for the high-speed RC oscillation circuit by optional configuration.

### ■ System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2μs, 2.4μs, 4.8μs, 9.6μs, 19.2μs, 38.4μs, and 76.8μs (when high speed RC oscillation is selected for system clock.).

#### ■ Internal Reset Circuit

- Power-on reset (POR) function
  - 1) POR reset is generated only at power-on time.
  - 2) The POR release level can be selected from 3 levels (2.87V, 3.86V, and 4.35V) by optional configuration.
- Low-voltage detection reset (LVD) function
  - 1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
  - 2) The use or disuse of the LVD function and the low voltage threshold level (3 levels: 2.81V, 3.79V, and 4.28V) can be selected by optional configuration.

#### ■ Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  - 1) Oscillation is not halted automatically.
  - 2) There are the following three ways of resetting the HALT mode.
    - (1) Setting the Reset pin to the low level
    - (2) Generating a reset signal via the watchdog timer or brown-out detector
    - (3) Having an interrupt generated
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  - 1) The medium- and high-speed RC oscillation circuits automatically stop operation.
  - 2) There are the following four ways of resetting the HOLD mode.
    - (1) Setting the Reset pin to the low level
    - (2) Generating a reset signal via the watchdog timer or brown-out detector
    - (3) Setting at least one of the INTA, INTB, INTC, INTD, INTE, and INTF pins to the specified level (INTA and INTB HOLD mode reset is available only when level detection is set.)
    - (4) Applying input signals to the IN+ and IN- pins so that the analog comparator output is set to the specified level (when the analog comparator output is assigned to the INTC input)

#### ■ On-chip Debugger Function

• Supports software debugging with the IC mounted on the target board (selectable from 3 series).

1) LC87D2708A: All terminal function of LC87F2608A can be used.

2) LC87F2708A : All terminal function of LC87F2608A can be used. The debug feature is limited.

3) LC87F2608A : The debugger terminal function when an On-chip debugger is used cannot be used.

The debug feature is limited.

• Two channels of on-chip debugger pins are available (LC87F2608A).

#### ■ Data Security Function (Note3)

• Protects the program data stored in flash memory from unauthorized read or copy.

Note3: This data security function does not necessarily provide absolute data security.

### ■ Development Tools

• On-chip debugger: 1) TCB87-Type B + LC87D2708A or LC87F2708A

2) TCB87-Type B + LC87F2608A

3) TCB87-Type C (3 wire version) + LC87D2708A or LC87F2708A

4) TCB87-Type C (3 wire version) + LC87F2608A

■ Programming Board

Package	Programming Board
MFP10S	
MFP10SK	W87F27M-DBG
MFP14S	

■ Flash ROM Programming Board

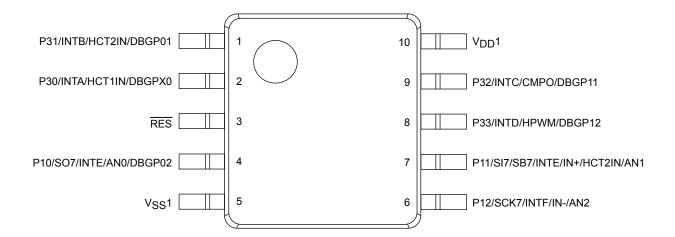
Maker		Model	Version	Device	
Flash Support Group, Inc. (FSG)	In-circuit	AF9101/AF9103 (Main body) (FSG models)		LC87F2608A	
+ Our company (Note 4)	Programmer	SIB87 (Inter Face Driver) (Our company model)	Rev.01.01 or later		
	Single/Gang Programmer	OW PRO T	Application Version		
Our company	In-circuit/ Gang Programmer	SKK-DBG Type B (Sanyo FWS)	1.04 or later Chip Data Version 2.10 or later	LC87F2608A	

For information about AF-series:

Flash Support Group, Inc. TEL: +81-53-459-1050 E-mail: sales@j-fsg.co.jp

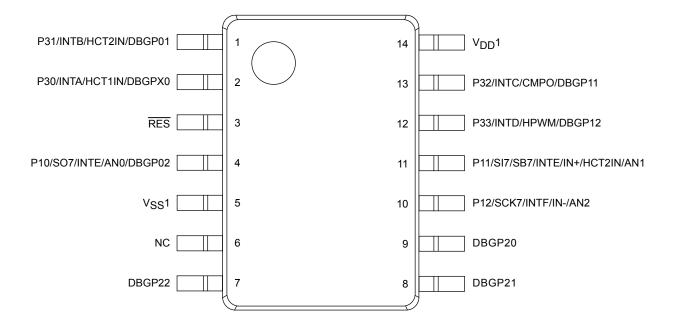
Note4: On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from Our company (SIB87) together can give a PC-less, standalone on-board-programming capabilities.

## **Pin Assignment**



MFP10S "Lead-/Halogen-free type" MFP10SK "Lead-/Halogen-free type"

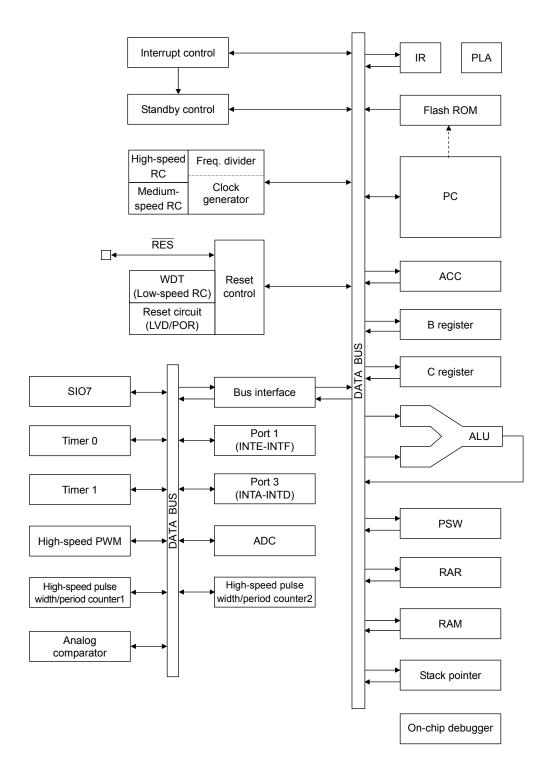
MFP10S MFP10SK	NAME
1	P31/INTB/HCT2IN/DBGP01
2	P30/INTA/HCT1IN/DBGPX0
3	RES
4	P10/SO7/INTE/AN0/DBGP02
5	V <sub>SS</sub> 1
6	P12/SCK7/INTF/IN-/AN2
7	P11/SI7/SB7/INTE/IN+/HCT2IN/AN1
8	P33/INTD/HPWM/DBGP12
9	P32/INTC/CMPO/DBGP11
10	V <sub>DD</sub> 1



MFP14S (for debugging only) "Lead-free type"

MFP14S	NAME
1	P31/INTB/HCT2IN/DBGP01
2	P30/INTA/HCT1IN/DBGPX0
3	RES
4	P10/SO7/INTE/AN0/DBGP02
5	V <sub>SS</sub> 1
6	NC
7	DBGP22
8	DBGP21
9	DBGP20
10	P12/SCK7/INTF/IN-/AN2
11	P11/SI7/SB7/INTE/IN+/HCT2IN/AN1
12	P33/INTD/HPWM/DBGP12
13	P32/INTC/CMPO/DBGP11
14	V <sub>DD</sub> 1

### **System Block Diagram**



# **Pin Description**

Pin Name	I/O			Descr	ription			Option
V <sub>SS</sub> 1	-	- power supply	pin					No
V <sub>DD</sub> 1	-	+ power supply	pin					No
PORT1 P10 to P12	1/0	Pull-up resists     Multiplexed pi     P10: SIO7 dat         INTE inp         timer 0L     P11: SIO7 da         high-spec     INTE inp         timer 0L     P12: SIO7 clo     INTF inpi     timer 0L     AD converter     Analog compa     On-chip debug	<ul> <li>3-bit I/O port</li> <li>I/O specifiable in 1-bit units</li> <li>Pull-up resistors can be turned on and off in 1-bit units</li> <li>Multiplexed pins</li> <li>P10: SIO7 data output/</li></ul>					
		INTE	Rising enable enable	Falling enable enable	Rising & Falling enable enable	H level disable disable	L level disable disable	
PORT3 P30 to P33	1/0	Multiplexed pi P30: INTA inp high-spe P31: INTB inp high-spe P32: INTC inp timer 0L P33: INTD inp timer 0H On-chip debug On-chip debug Interrupt ackn  INTA	ors can be turned ons ut/HOLD release i led pulse width/per out/HOLD release led pulse width/per out/HOLD release capture input/anal out/HOLD release i capture input/high gger pin 1: DBGP>	nput/timer 0L ca riod counter 1 in input/timer 0H c riod counter 2 in input/timer 0 eve log comparator of input/timer 0 eve in-speed PWM ou to to DBGP01 (F	pture input/ put apture input/ put ent input/ output ent input/ utput 230 to P31)	H level	L level	Yes
RES	I/O	INTB INTC INTD	enable enable enable	enable enable enable	disable enable enable	enable disable disable	enable disable disable	No
KES	1/0	External reset in	nput/internal reset	output				No

### **Port Output Types**

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.

Data can be read into any input port even if it is in the output mode.

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
D10 to D12		1 CMOS		Programmable
P10 to P12	1 bit	2	N-channel open drain	Programmable
D20 to D22	4 1-14	1	CMOS	Programmable
P30 to P33	1 bit	2	N-channel open drain	Programmable

### **On-chip Debugger Pin Processing**

For the processing of the on-chip debugger pins, refer to the separately available documents entitled "RD87 On-chip Debugger Installation" and "LC872000 Series On-chip Debugger Pin Processing."

### **Recommended Unused Pin Connections**

Din Name	Recommended Unused Pin Connections				
Pin Name	Board				
P10 to P12	OPEN	Set output low			
P30 to P33	OPEN Set output low				

### **User Options**

			Option	
Option Name	Option Type	Flash Version	Version Switched in Unit of  Switched in Unit of	Description
			Unit of	
	P10 to P12	onable	1hit	CMOS
Dark autout tona	F10 (0 F12	eriable	TOIL	N-channel open drain
Port output type	D20 to D22		46:4	CMOS
	P30 to P33	enable	TOIT	N-channel open drain
Dan sure as a stant and due as				00000H
Program start address	-	enable	-	01E00H
_	Brown-out detector			Enable: Used
Brown-out detector reset function	function	enable	-	Disable: Not used
Turicuori	Brown-out trip level	enable	-	3 levels
Power-on-reset function	Power-on-reset level	enable	-	3 levels
High-speed RC oscillator	Ossillation for account			20 MHz
circuit	Oscillation frequency	enable	-	40 MHz
				MFP10S: LC87F2608A
Package type	-	enable	-	MFP14S: Debugged by using
				LC87D2708A or LC87F2708A

### Absolute Maximum Ratings at Ta=25°C, $V_{SS}1$ =0V

	Doromotor	Cymhal	Din/Domorko	Conditions			Specific	cation	
	Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
	aximum supply Itage	V <sub>DD</sub> max	V <sub>DD</sub> 1			-0.3	to	+6.5	٧
Inp	out voltage	VI	RES			-0.3	to	V <sub>DD</sub> +0.3	
	out/output Itage	V <sub>IO</sub>	• Port 1 • Port 3			-0.3	to	V <sub>DD</sub> +0.3	
	Peak output current	I <sub>OPH</sub> (1)	Port 1	CMOS output selected     Per applicable pin		-7.5			mA
t		I <sub>OPH</sub> (2)	Port 3	CMOS output selected     Per applicable pin		-10			
High level output current	Mean output current	I <sub>OMH</sub> (1)	Port 1	CMOS output selected     Per applicable pin		-5			
outpu	(Note 1-1)	I <sub>OMH</sub> (2)	Port 3	CMOS output selected     Per applicable pin		-7.5			
igh leve	Total output current	ΣI <sub>OAH</sub> (1)	• Port 10 • Ports 30, 31	Total of currents at all applicable pins		-20			
Ξ		ΣI <sub>OAH</sub> (2)	• Ports 11, 12 • Ports 32, 33	Total of currents at all applicable pins		-20			
		ΣI <sub>OAH</sub> (3)	• Port 1 • Port 3	Total of currents at all applicable pins		-35			
	Peak output	I <sub>OPL</sub> (1)	Port 1	Per applicable pin				15	
	current	I <sub>OPL</sub> (2)	Port 3	Per applicable pin				10	
ent	Mean output	I <sub>OML</sub> (1)	Port 1	Per applicable pin				10	
out curr	current (Note 1-1)	I <sub>OML</sub> (2)	Port 3	Per applicable pin				7.5	
Low level output current	Total output current	Σl <sub>OAL</sub> (1)	• Port 10 • Ports 30, 31	Total of currents at all applicable pins				25	
Low le		Σl <sub>OAL</sub> (2)	• Ports 11, 12 • Ports 32, 33	Total of currents at all applicable pins				35	
		Σ <sub>IOAL</sub> (3)	• Port 1 • Port 3	Total of currents at all applicable pins				55	
Po	wer dissipation	Pd max(1)	MFP10S	Ta=-40 to +85°C Independent package				100	mW
		Pd max(2)		Ta=-40 to +85°C  Mounted on thermal test board (Note 1-2)				237	
		Pd max(3)	MFP10SK	Ta=-40 to +85°C Independent package				100	
		Pd max(4)		Ta=-40 to +85°C  Mounted on thermal test board (Note 1-2)				237	
	perating ambient	Topr				-40	to	+85	°C
Sto	orage ambient	Tstg				-55	to	+125	

Note 1-1: Mean output current refers to the average of output currents measured for a period of 100ms.

Note 1-2: Thermal test board used conforms to SEMI (size: 76.1×114.3×1.6tmm, glass epoxy board).

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Conditions at Ta= -40 to +85°C, VSS1=0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
Parameter				V <sub>DD</sub> [V]	min	typ	max	unit
Operating supply voltage (Note 2-1)	V <sub>DD</sub>	V <sub>DD</sub> 1	0.272μs ≤ tCYC ≤ 100μs		2.7		5.5	V
Memory sustaining supply voltage	V <sub>HD</sub>	V <sub>DD</sub> 1	RAM and register contents sustained in HOLD mode		2.0		5.5	
High level input voltage	V <sub>IH</sub> (1)	• Port 1 • Port 3	Output disabled	2.7 to 5.5	0.3V <sub>DD</sub> +0.7		V <sub>DD</sub>	
	V <sub>IH</sub> (2)	RES		2.7 to 5.5	0.75V <sub>DD</sub>		$V_{DD}$	
Low level	V <sub>IL</sub> (1)	• Port 1	Output disabled	4.0 to 5.5	$V_{SS}$		0.1V <sub>DD</sub> +0.4	
input voltage		• Port 3		2.7 to 4.0	$V_{SS}$		0.2V <sub>DD</sub>	
	V <sub>IL</sub> (2)	RES		2.7 to 5.5	V <sub>SS</sub>		0.25V <sub>DD</sub>	
Instruction cycle time (Note 2-2)	tCYC			2.7 to 5.5	0.272		100	μs
Oscillation frequency range	FmHRC(1)		High-speed RC oscillation     40MHz selected as option     Ta=-20 to +85°C	4.5 to 5.5	38	40	42	MH z
J	FmHRC(2)		High-speed RC oscillation	4.5 to 5.5	37.6	40	42.4	
	FmHRC(3)		40MHz selected as option	3.5 to 5.5	36.8	40	43.2	
	FmHRC(4)		• Ta=-40 to +85°C	2.7 to 5.5	32	40	43.2	
	FmHRC(5)		High-speed RC oscillation     20MHz selected as option     Ta=-20 to +85°C	3.0 to 5.5	19	20	21	
	FmHRC(6)		High-speed RC oscillation     20MHz selected as option     Ta=-40 to +85°C	2.7 to 5.5	18.7	20	21.3	
	FmRC		Medium-speed RC oscillation	2.7 to 5.5	0.5	1.0	2.0	
	FmSLRC		Low-speed RC oscillation	2.7 to 5.5	15	30	60	kHz
Oscillation stabilization time	tmsHRC		When high-speed RC oscillation state is switched from stopped to enabled.      See Fig. 2.	2.7 to 5.5			100	μs

- Note 2-1: Use this product in a voltage range of 3.0 to 5.5V because the minimum release voltage (PORRL) of the power-on reset (POR) circuit is  $2.87V\pm0.12V$ .
- Note 2-2: Relationship between tCYC and oscillation frequency is as follows:
  - When system clock source is set to medium-speed RC oscillation 3/FmRC at a division ratio of 1/1, 6/FmRC at a division ratio of 1/2, 12/FmRC a division ratio of 1/4, and so forth
  - When system clock source is set to high-speed RC oscillation (40MHz selected by optional configuration) 12/FmHRC at a division ratio of 1/1, 24/FmHRC at a division ratio of 1/2, 48/FmHRC a division ratio of 1/4, and so forth
  - When system clock source is set to high-speed RC oscillation (20MHz selected by optional configuration) 6/FmHRC at a division ratio of 1/1, 12/FmHRC at a division ratio of 1/2, 24/FmHRC a division ratio of 1/4, and so forth

## **Electrical Characteristics** at Ta = -40 to +85°C, $V_{SS}1 = 0V$

Doromotor	Cumbal	Pin/Remarks	Conditions		Specification				
Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit	
High level input current	I <sub>IH</sub> (1)	• Port 1 • Port 3	Output disabled Pull-up resistor off VIN=VDD (including output Tr. off leakage current)	2.7 to 5.5			1	μА	
	I <sub>IH</sub> (2)	RES	V <sub>IN</sub> =V <sub>DD</sub>	2.7 to 5.5			1		
Low level input current	I <sub>IL</sub>	• Port 1 • Port 3	Output disabled Pull-up resistor off VIN=VSS (including output Tr. off leakage current)	2.7 to 5.5	-1				
High level output voltage	V <sub>OH</sub> (1)	CMOS output	I <sub>OH</sub> =-1mA	4.5 to 5.5	V <sub>DD</sub> -1			V	
	V <sub>OH</sub> (2)	type port 1	I <sub>OH</sub> =-0.35mA	2.7 to 5.5	V <sub>DD</sub> -0.4				
	V <sub>OH</sub> (3)	CMOS output	I <sub>OH</sub> =-5mA	4.5 to 5.5	V <sub>DD</sub> -1.5				
	V <sub>OH</sub> (4)	type port 3	I <sub>OH</sub> =-0.7mA	2.7 to 5.5	V <sub>DD</sub> -0.4				
Low level output	V <sub>OL</sub> (1)	Port 1	I <sub>OL</sub> =10mA	4.5 to 5.5			1.5		
voltage	V <sub>OL</sub> (2)		I <sub>OL</sub> =1.4mA	2.7 to 5.5			0.4		
	V <sub>OL</sub> (3)	Port 3	I <sub>OL</sub> =5mA	4.5 to 5.5			1.5		
	V <sub>OL</sub> (4)		I <sub>OL</sub> =0.7mA	2.7 to 5.5			0.4		
Pull-up resistance	Rpu(1)	• Port 1	V <sub>OH</sub> =0.9V <sub>DD</sub>	4.5 to 5.5	15	35	80	kΩ	
	Rpu(2)	• Port 3		2.7 to 4.5	18	50	150		
	Rpu(3)	RES		2.7 to 5.5	216	360	504		
Hysteresis voltage	VHYS	• Port 1 • Port 3 • RES		2.7 to 5.5		0.1V <sub>DD</sub>		V	
Pin capacitance	СР	All pins	VIN=VSS for pins other than that under test  f=1 MHz  Ta=25°C	2.7 to 5.5		10		pF	

### Serial I/O Characteristics at Ta= -40 to $+85^{\circ}C$ , $V_{SS}1$ =0V

### SIO7 Serial I/O Characteristics (Note 4-1-1)

		Doromotor	0	Dia/Damanta	Conditions			Speci	ification	
	٢	Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
		Frequency	tSCK(1)	SCK7(P12)	• See Fig. 4.	2.7 to 5.5	2			tCYC
	Input clock	Low level	tSCKL(1)		(Note 4-1-2)		1			
	ont c	pulse width		_		-				
ock Sk	ū	High level	tSCKH(1)				1			
Serial clock		pulse width Frequency	tSCK(2)	SCK7(P12)	• CMOS output colocted	2.7 to 5.5	4/3			
Seri	ξ		` '	3CK7(P12)	<ul><li>CMOS output selected</li><li>See Fig. 4.</li></ul>	2.7 10 5.5	4/3	4.10		10.014
	rt clc	Low level pulse width	tSCKL(2)		• See Fig. 4.			1/2		tSCK
	Output clock	High level	tSCKH(2)			-		1/2		
		pulse width	. ,							
input	Da	ta setup time	tsDI(1)	SB7(P11), SI7(P11)	Must be specified with respect to Rising edge of SIOCLK.     See Fig. 4.	2.7 to 5.5	0.03			μs
Serial	Serial input	ta hold time	thDI(1)		G		0.03			
output	Input clock	Output delay time	tdDO(1)	SO7(P10), SB7(P11)	<ul> <li>Must be specified with respect to rising edge of SIOCLK.</li> <li>Must be specified as the time to the beginning of output state change in open drain output</li> </ul>	2.7 to 5.5			1tCYC +0.05	
Serial output	Output clock		tdDO(2)		mode. • See Fig. 4.				(1/3)tCYC +0.05	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in transmission/reception mode, the time from SI7RUN being set when serial clock is "H" to the first falling edge of the serial clock must be longer than 1tCYC.

### Pulse Input Conditions at $Ta = -40 \text{ to } +85^{\circ}\text{C}, V_{SS}1=0V$

D	Cumhal	Pin/Remarks	Conditions			Spec	ification	ation	
Parameter	Symbol	PIn/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit	
High/low level pulse width	tPIH(1) tPIL(1)	INTA(P30), INTB(P31), INTD(P33), INTE(P10, P11), INTF(P12)	Interrupt source flag can be set.     Event inputs for timers 0 and 1 are enabled.	2.7 to 5.5	1			tCYC	
	tPIH(2) tPIL(2)	INTC(P32) when noise filter time constant is "none"	Interrupt source flag can be set.     Event inputs for timer 0 are enabled.	2.7 to 5.5	1				
	tPIH(3) tPIL(3)	INTC(P32) when noise filter time constant is "1/16"	Interrupt source flag can be set.     Event inputs for timer 0 are enabled.	2.7 to 5.5	64				
	tPIH(4) tPIL(4)	INTC(P32) when noise filter time constant is "1/32"	Interrupt source flag can be set.     Event inputs for timer 0 are enabled.	2.7 to 5.5	128				
	tPIH(5) tPIL(5)	INTC(P32) when noise filter time constant is "1/64"	Interrupt source flag can be set.     Event inputs for timer 0 are enabled.	2.7 to 5.5	256				
	tPIH(6) tPIL(6)	HCT1IN(P30)	Pulses can be recognized as signals by the high-speed pulse width/period counter 1.	2.7 to 5.5	3			H1CK (Note 5-1)	
	tPIH(7) tPIL(7)	HCT2IN(P11, P31)	Pulses can be recognized as signals by the high-speed pulse width/period counter 2.	2.7 to 5.5	6			H2CK (Note 5-2)	
	tPIL(8)	RES	Resetting is enabled.	2.7 to 5.5	200			μs	

Note 5-1: H1CK denotes the period of the base clock (1 to  $8 \times$  high-speed RC oscillation clock or system clock) for the high-speed pulse width/period counter 1.

Note 5-2: H2CK denotes the period of the base clock (2 to  $16 \times \text{high-speed RC}$  oscillation clock or system clock) for the high-speed pulse width/period counter 2.

### Comparator Characteristics at Ta= -40 to +85°C, $V_{SS}1$ =0V

Barranta	0	Pin/Remarks	Conditions		Specification				
Parameter	Symbol			V <sub>DD</sub> [V]	min	typ	max	unit	
Common mode input voltage range	VCMIN	IN+(P11), IN-(P12)		2.7 to 5.5	V <sub>SS</sub>		V <sub>DD</sub> -1.5	٧	
Offset voltage	VOFF		Within common mode input voltage range	2.7 to 5.5		±10	±30	mV	
Response time	tRT		Within common mode input voltage range     Input amplitude=100mV     Overdrive=50mV	2.7 to 5.5		200	600	ns	
Operation stabilization time (Note 6-1)	tCMW			2.7 to 5.5			1.0	μs	

Note 6-1: The interval after CMPON is set till the operation gets stabilized.

### AD Converter Characteristics at $V_{SS}1=0V$

<12-bit AD conversion mode at Ta=-40 to  $+85^{\circ}C$  >

Parameter	Symbol	Pin/Remarks	Conditions		Specification				
Parameter	Symbol	Pili/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit	
Resolution	N	AN0(P10)		3.0 to 5.5		12		bit	
Absolute accuracy	ET	to AN2(P12)	(Note 7-1)	3.0 to 5.5			±16	LSB	
Conversion time tCAD	See "Conversion time calculation	4.0 to 5.5	38		104.3	μs			
			method." (Note 7-2)	3.0 to 5.5	75.8		104.3		
Analog input voltage range	VAIN			3.0 to 5.5	V <sub>SS</sub>		$V_{DD}$	V	
Analog port input	IAINH		VAIN= V <sub>DD</sub>	3.0 to 5.5			1	μΑ	
current	IAINL		VAIN= V <sub>SS</sub>	3.0 to 5.5	-1				

#### <8-bit AD Converter Mode at Ta=-40 to +85°C >

Danamatan	Comment of	Pin/Remarks	Conditions		Specification				
Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit	
Resolution	N	AN0(P10)		3.0 to 5.5		8		bit	
Absolute accuracy	ET	to AN2(P12)	(Note 7-1)	3.0 to 5.5			±1.5	LSB	
Conversion time	tCAD		See "Conversion time calculation	4.0 to 5.5	23.4		64.3	μs	
			method." (Note 7-2)	3.0 to 5.5	46.7		64.3		
Analog input voltage range	VAIN			3.0 to 5.5	V <sub>SS</sub>		$V_{DD}$	V	
Analog port	IAINH		VAIN= V <sub>DD</sub>	3.0 to 5.5			1	μΑ	
input current	IAINL		VAIN= V <sub>SS</sub>	3.0 to 5.5	-1				

<sup>&</sup>lt;Conversion time calculation method>

12-bit AD conversion mode: tCAD (conversion time) =  $((52/(\text{division ratio})) + 2) \times (1/3) \times \text{tCYC}$ 

8-bit AD conversion mode: tCAD (conversion time) =  $((32/(\text{division ratio})) + 2) \times (1/3) \times \text{tCYC}$ 

#### < Recommended Operating Conditions>

High-speed RC	Supply Voltage	System Clock	Cycle Time	AD Division Ratio	Conversion Time (tCAD)		
Oscillation (FmHRC)	Range (V <sub>DD</sub> )	Division Ratio (SYSDIV)	(tCYC)	(ADDIV)	12-bit AD	8-bit AD	
400411-/000411-	4.0V to 5.5V	1/1	300ns	1/8	41.8µs	25.8µs	
40MHz/20MHz	3.0V to 5.5V	1/1	300ns	1/16	83.4μs	51.4μs	

Note 7-1: The quantization error ( $\pm 1/2$ LSB) is excluded from the absolute accuracy. The absolute accuracy is measured when no change occurs in the I/O state of the pins that are adjacent to the analog input channel during AD conversion processing.

Note 7-2: The conversion time refers to the interval from the time a conversion starting instruction is issued till the time the complete digital conversion value against the analog input value is loaded in the result register.

\*The conversion time is twice the normal value when one of the following conditions occurs:

- The first AD conversion executed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion executed after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode.

### Power-on Reset (POR) Characteristics at Ta= -40 to +85 $^{\circ}$ C, V<sub>SS</sub> 1=0V

					Specification				
Parameter	Symbol	Pin/Remarks	Conditions	Option Selecting Voltage	min	typ	max	unit	
POR release	PORRL		Option selected	2.87V	2.75	2.87	2.99	٧	
voltage			• See Fig. 6.	3.86V	3.73	3.86	3.99		
			(Note 8-1)	4.35V	4.21	4.35	4.49		
Unknown voltage	POUKS		• See Fig. 6.			0.7	0.95		
area			(Note 8-2)						
Power startup time	PORIS		Power startup time				100	ms	
			from V <sub>DD</sub> =0V to 2.8V						

Note 8-1: The POR release voltage can be selected from three levels when the low-voltage detection feature is deselected.

Note 8-2: There is an unpredictable period before the power-on reset transistor starts to turn on.

### Low-voltage Detection (LVD) Characteristics at Ta=-40 to +85°C, $V_{SS}$ 1=0V

						Specification				
Parameter	Symbol	Pin/Remarks	Conditions	Option Selecting Voltage	min	typ	max	unit		
LVD reset voltage		Option selected	2.81V	2.71	2.81	2.91	V			
(Note 9-2)			• See Fig. 7.	3.79V	3.69	3.79	3.89			
		(Note 9-1) (Note 9-3)	4.28V	4.18	4.28	4.38				
LVD voltage	LVHYS		(Note 9-3)	2.81V		60		mV		
hysteresis				3.79V		65				
				4.28V		65				
Unknown voltage area	LVUKS		• See Fig. 7. (Note 9-4)			0.7	0.95	V		
Minimum low voltage detection width (response sensitivity)	tLVDW		• LVDET-0.5V • See Fig. 8.		0.2			ms		

Note 9-1: The LVD reset voltage can be selected from three levels when the low-voltage detection feature is selected.

Note 9-2: The hysteresis voltage is not included in the LVD reset voltage value.

Note 9-3: There are cases when the LVD reset voltage value is exceeded when a greater change in the output level or large current is applied to the port.

Note 9-4: There is an unpredictable period before the low-voltage detection resetting transistor starts to run.

Consumption Current Characteristics at Ta=-40 to +85  $^{\circ}C,\,V_{SS}$  1=0V

Parameter	Symbol	Pin/Remarks	Conditions			Specif	ication		
гагашетег	Symbol	riii/Reiilarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit	
Normal mode consumption current	IDDOP(1)	V <sub>DD</sub> 1	FmHRC=40MHz oscillation mode     System clock set to high-speed RC,     10MHz (1/4 of 40MHz)	4.5 to 5.5		7.8	14	mA	
Note 10-1)	IDDOP(2)		Medium-speed RC oscillation stopped     System clock frequency division ratio     set to 1/1	2.7 to 3.6		4.9	9.4		
	IDDOP(3)		FmHRC=20MHz oscillation mode System clock set to high-speed RC, 10MHz (1/2 of 20MHz)  Medium-speed RC oscillation stopped System clock frequency division ratio set to 1/1 High-speed RC oscillation stopped System clock set to medium-speed RC oscillation mode System clock frequency division ratio set to 1/2	4.5 to 5.5		7.1	12.8		
	IDDOP(4)			2.7 to 3.6		4.5	8.6		
	IDDOP(5)			4.5 to 5.5		0.60	1.9		
	IDDOP(6)			2.7 to 3.6		0.38	1.3		
HALT mode consumption current	IDDHALT(1)		HALT mode  FmHRC=40MHz oscillation mode  System clock set to high-speed RC,	4.5 to 5.5		3.2	5.0		
(Note 10-1)	IDDHALT(2)		<ul> <li>10MHz(1/4 of 40MHz)</li> <li>Medium-speed RC oscillation stopped</li> <li>System clock frequency division ratio set to 1/1</li> </ul>	2.7 to 3.6		2.0	3.1		
	IDDHALT(3)		HALT mode • FmHRC=20MHz oscillation mode • System clock set to high-speed RC,	4.5 to 5.5		2.5	3.9		
	IDDHALT(4)			10MHz (1/2 of 20MHz)     Medium-speed RC oscillation stopped     System clock frequency division ratio     set to 1/1	2.7 to 3.6		1.6	2.5	
	IDDHALT(5)		HALT mode  • High-speed RC oscillation stopped  • System clock set to medium-speed RC	4.5 to 5.5		0.32	1.0		
	IDDHALT(6)		oscillation mode  • System clock frequency division ratio set to 1/2	2.7 to 3.6		0.16	0.55		
HOLD mode	IDDHOLD(1)	-	HOLD mode  • Ta=-10 to +50°C	4.5 to 5.5		0.04	3.0	μΑ	
onsumption urrent	IDDHOLD(2)	-		2.7 to 3.6		0.02	1.8	-	
Note 10-1)	IDDHOLD(3)	-	HOLD mode  • Ta=-40 to +85°C	4.5 to 5.5		0.04	34	ļ	
	IDDHOLD(4)	-		2.7 to 3.6		0.02	22	ł	
	IDDHOLD(5)	-	HOLD mode  • LVD option selected	4.5 to 5.5 2.7 to 3.6		3.1 2.4	4.2	]	
	IDDHOLD(7)	1	Ta=-10 to +50°C  HOLD mode	4.5 to 5.5		3.1	39	1	
	IDDHOLD(8)	-	LVD option selected     Ta=-40 to +85°C	2.7 to 3.6		2.4	25		
	IDDHOLD(9)	-	HOLD mode	4.5 to 5.5		3.4	10		
	IDDHOLD(10)	-	Watchdog timer active Ta=-10 to +50°C	2.7 to 3.6		1.7	6.0		
	IDDHOLD(11)	1	HOLD mode	4.5 to 5.5		3.4	42	Ī	
	IDDHOLD(12)	†   .	Watchdog timer active     Ta=-40 to +85°C	2.7 to 3.6		1.7	27	1	
	IDDHOLD(13)	1	HOLD mode	4.5 to 5.5		110	160	1	
_	IDDHOLD(14)	1	Comparator active     (IN+= V <sub>DD</sub> , IN-= V <sub>SS</sub> )	2.7 to 3.6		65	100	1	

Note 10-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

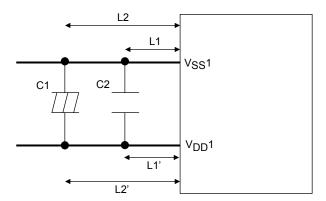
### F-ROM Programming Characteristics at Ta=+10 to +55°C, VSS1=0V

Danamatan	Command and	Pin/Remarks	Conditions		Specification			
Parameter	Symbol			V <sub>DD</sub> [V]	min	typ	max	unit
Onboard programming current	IDDFW	V <sub>DD</sub> 1	Microcontroller consumption current is excluded.	3.0 to 5.5		5	10	mA
Programming	tFW(1)		Erase operation	3.0 to 5.5		20	30	ms
time	tFW(2)		Programming operation			40	60	μs

### Power Pin Treatment Recommendations $(V_{DD}1, V_{SS}1)$

Connect bypass capacitors that meet the following conditions between the V<sub>DD</sub>1 and V<sub>SS</sub>1 pins:

- Connect among the V<sub>DD</sub>1 and V<sub>SS</sub>1pins and bypass capacitors C1 and C2 with the shortest possible heavy lead wires, making sure that the impedances between the both pins and the bypass capacitors are as equal as possible (L1=L1', L2=L2').
- $\bullet$  Connect a large-capacity capacitor C1 and a small-capacity capacitor C2 in parallel. The capacitance of C2 should be approximately  $0.1\mu F.$



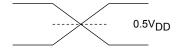
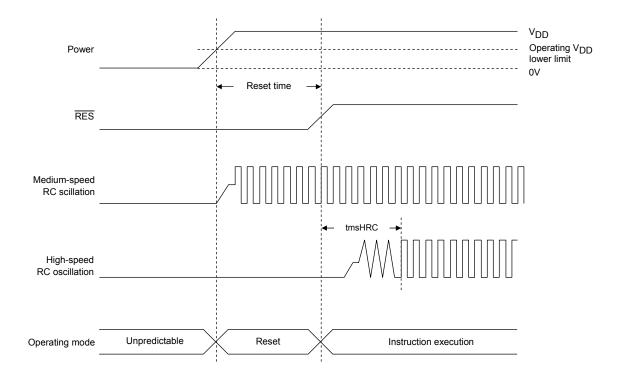
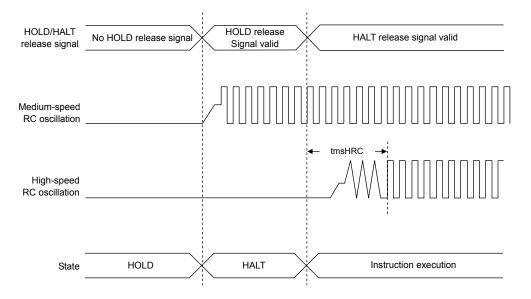


Figure 1 AC Timing Measurement Point

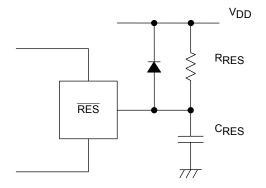


Reset Time and Oscillation Stabilization Time



HOLD Release Signal and Oscillation Stabilization Time

Figure 2 Oscillation Stabilization Times



### Note:

The external peripheral circuit differs depending on the way in which the power-on reset and low-voltage detection reset functions are used. Refer to the Chapter, entitled "Reset Function," of the user's manual.

Figure 3 Sample Reset Circuit

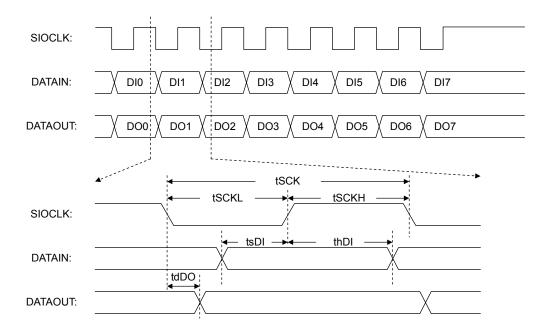


Figure 4 Serial I/O Waveforms

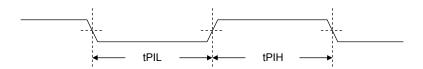


Figure 5 Pulse Input Timing Signal Waveform

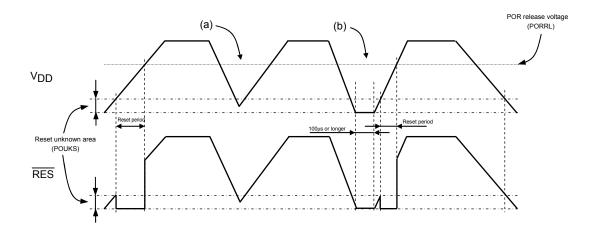


Figure 6 Example of POR Only (LVD Deselected) Mode Waveforms (at Reset Pin with RRES Pull-up Resistor Only)

- The POR circuit generates a reset signal only when the power voltage is raised from the VSS level.
- No stable reset signal is generated if power is turned on again when the power voltage does not go down to the VSS level as shown in (a). If this case is anticipated, use the LVD function as explained below or configure an external reset circuit.
- A reset is effected only when power is turned on again after the power voltage goes down to and remains at the V<sub>SS</sub> level for 100µs or longer as shown in (b).

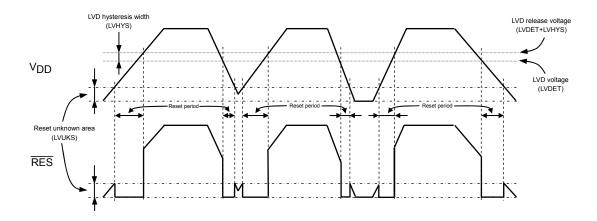


Figure 7 Example of POR + LVD Mode Waveforms (at Reset Pin with RRES Pull-up Resistor Only)

- A reset is effected both when power is turned on and when it goes down.
- The hysteresis width (LVHYS) is introduced in the LVD circuit to prevent the iterations of the IC entering and exiting the reset state near the detection threshold level.

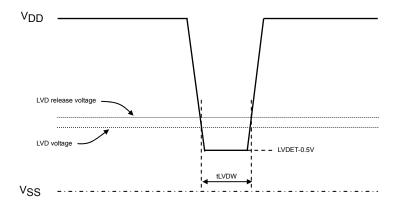


Figure 8 Minimum Low Voltage Detection Width (Example of Short Interruption of Power/ Power Fluctuation Waveform)

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