

N-channel 1050 V, 1.4 Ω typ., 4 A MDmesh™ K5 Power MOSFET in TO-220FP package

Datasheet - production data

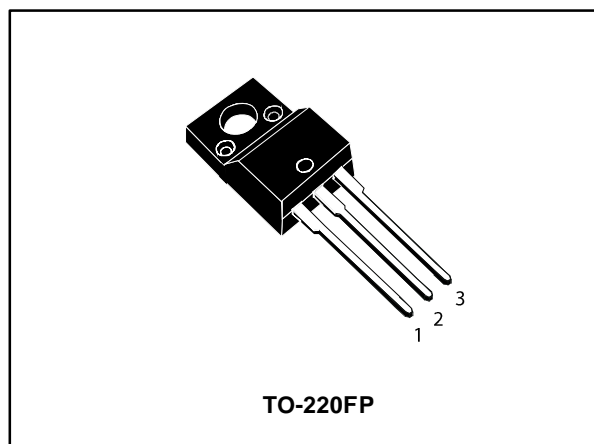
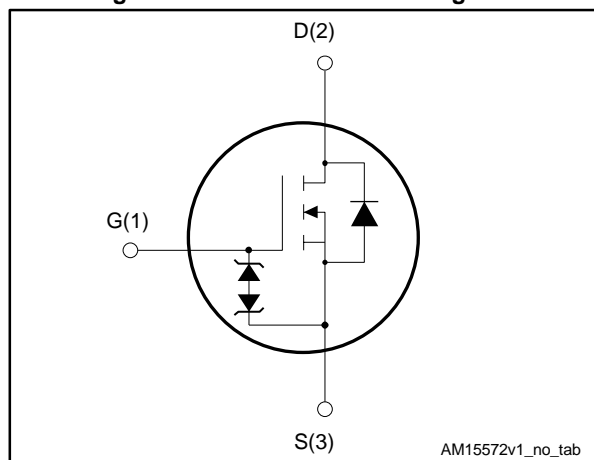


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STF7N105K5	1050 V	2.0 Ω	4 A	25 W

- Industry's lowest R_{DS(on)} x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STF7N105K5	7N105K5	TO-220FP	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate- source voltage	± 30	V
I _D	Drain current (continuous) at T _C = 25 °C	4 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	3 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	16	A
P _{TOT}	Total dissipation at T _C = 25 °C	25	W
I _{AR}	Max. current during repetitive or single pulse avalanche	1.5	A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D =I _{AR} , V _{DD} = 50 V)	132	mJ
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)	2500	V
dv/dt ⁽³⁾	Peak diode recovery voltage slope	4.5	V/ns
dv/dt ⁽⁴⁾	MOSFET dv/dt ruggedness	50	V/ns
T _J	Operating junction temperature range	- 55 to 150	°C
T _{stg}	Storage temperature range		

Notes:

(1)Limited by package.

(2)Pulse width limited by safe operating area.

(3) $I_{SD} \leq 4$ A, $di/dt \leq 100$ A/ μ s, $V_{DS(peak)} \leq V_{(BR)DSS}$; $V_{SD} \leq 840$ V

(4) $V_{DS} \leq 840$ V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case max	5	°C/W
R _{thj-amb}	Thermal resistance junction-amb max	62.5	°C/W

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified).

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	1050			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 1050\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 1050\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			50	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0$, $V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 2\text{ A}$		1.4	2	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	380	-	pF
C_{oss}	Output capacitance		-	40	-	pF
C_{rss}	Reverse transfer capacitance		-	0.65	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }840\text{ V}$	-	47	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	17	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	7	-	Ω
Q_g	Total gate charge	$V_{DD} = 840\text{ V}$, $I_D = 4\text{ A}$	-	11	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\text{ V}$	-	2.8	-	nC
Q_{gd}	Gate-drain charge	<i>Figure 16: "Test circuit for gate charge behavior"</i>	-	5.6	-	nC

Notes:

⁽¹⁾Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

⁽²⁾Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 525 \text{ V}$, $I_D = 2 \text{ A}$, $R_G = 4.7 \text{ } \Omega$, $V_{GS} = 10 \text{ V}$ (see Figure 15: "Test circuit for resistive load switching times" and Figure 20: "Switching time waveform")	-	17.5	-	ns
t_r	Rise time		-	7	-	ns
$t_{d(off)}$	Turn-off delay time		-	43	-	ns
t_f	Fall time		-	25	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4	A
I_{SDM}	Source-drain current (pulsed)				16	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 4 \text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 4 \text{ A}$, $V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$, Figure 17: "Test circuit for inductive load switching and diode recovery times"	-	370		ns
Q_{rr}	Reverse recovery charge		-	3		μC
I_{RRM}	Reverse recovery current		-	16.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 4 \text{ A}$, $V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$, $T_j = 150 \text{ } ^\circ\text{C}$ Figure 17: "Test circuit for inductive load switching and diode recovery times"	-	600		ns
Q_{rr}	Reverse recovery charge		-	4.4		μC
I_{RRM}	Reverse recovery current		-	14.5		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$, $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance the ESD capability of the device. The Zener voltage is appropriate for efficient and cost-effective intervention to protect the device integrity. These integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

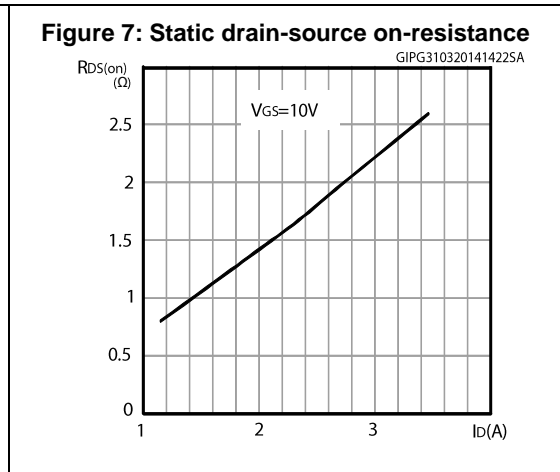
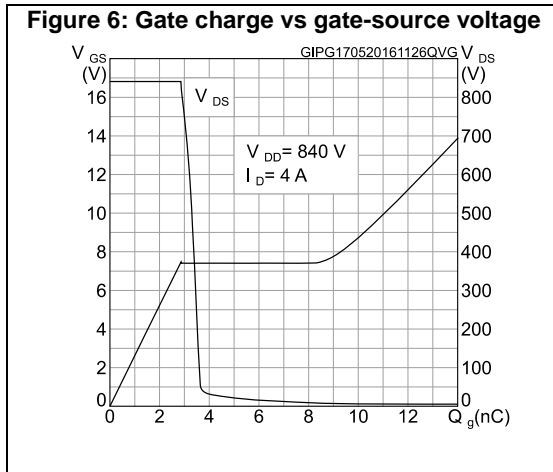
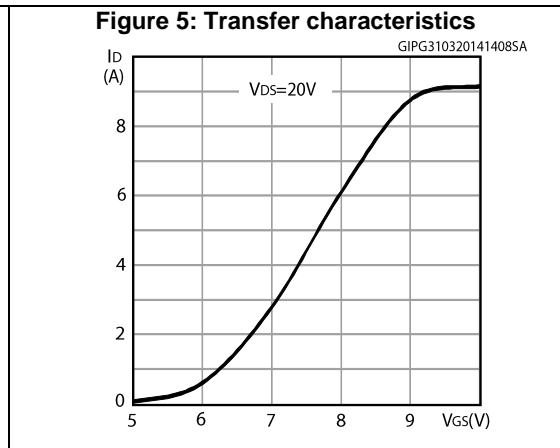
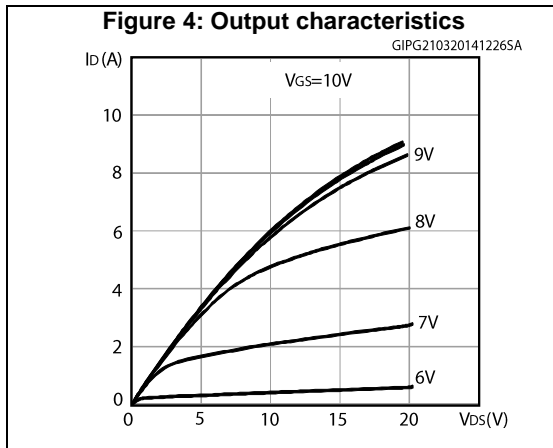
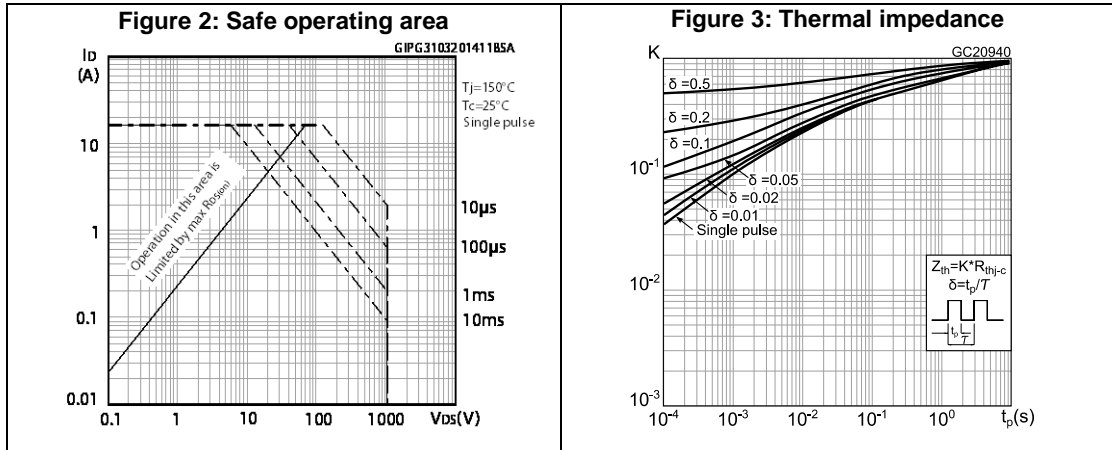


Figure 8: Capacitance variations

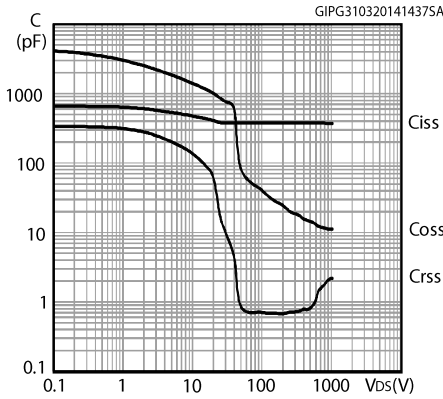


Figure 9: Source-drain diode forward characteristics

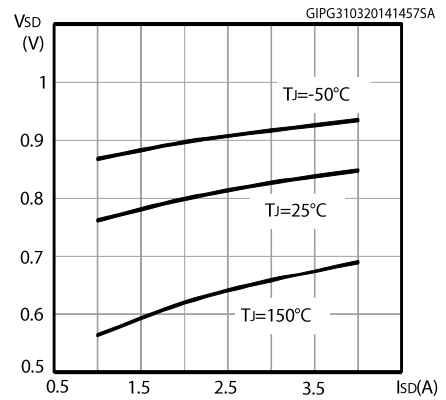


Figure 10: Normalized gate threshold voltage vs temperature

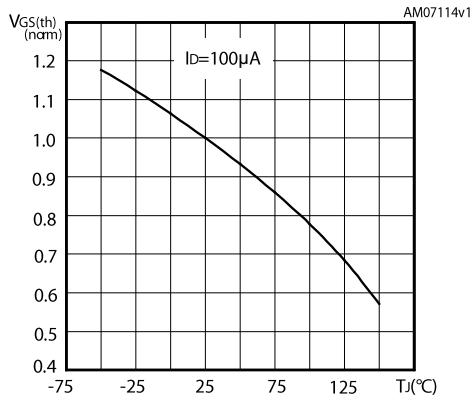


Figure 11: Normalized on-resistance vs temperature

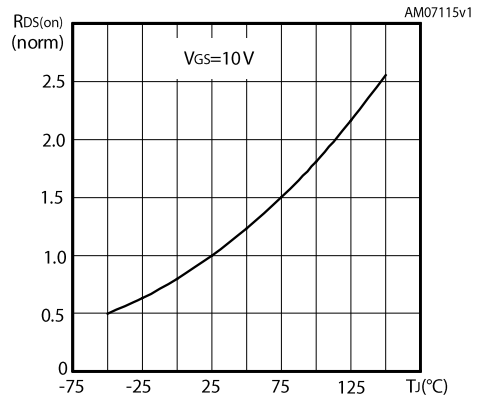


Figure 12: Normalized V(BR)DSS vs temperature

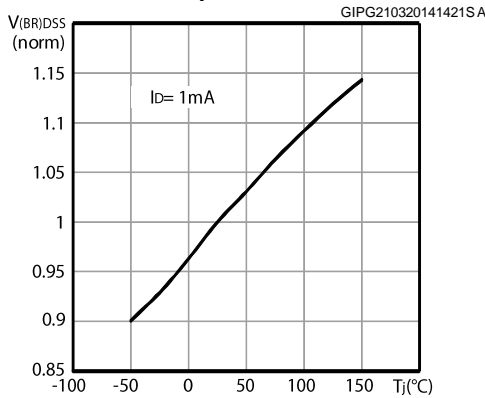


Figure 13: Maximum avalanche energy vs starting Tj

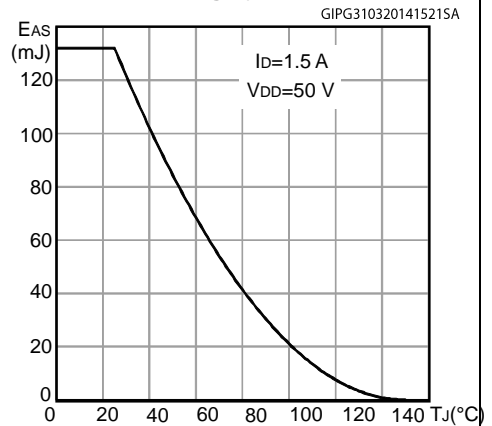
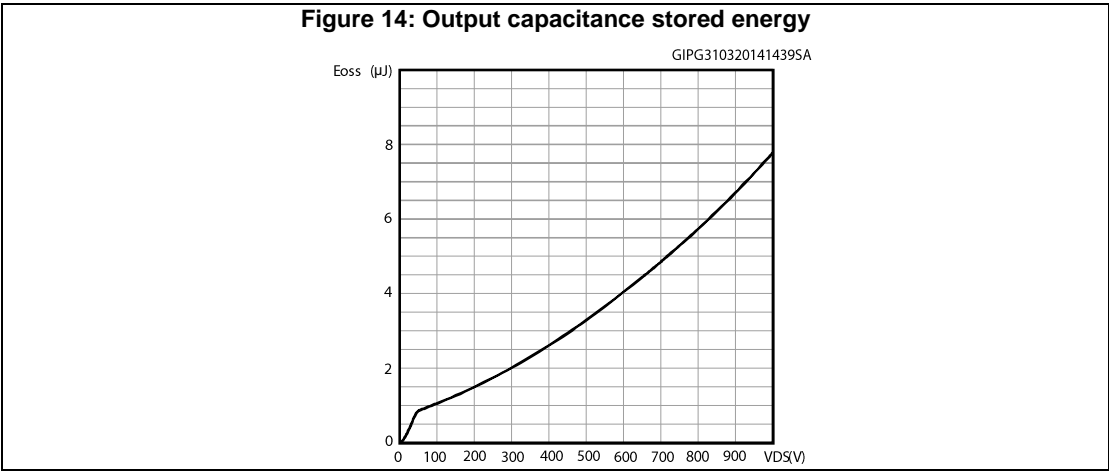
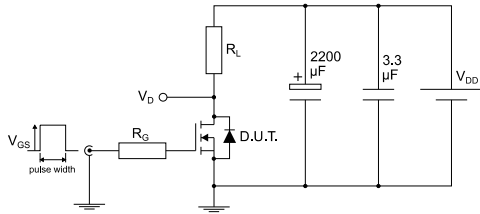


Figure 14: Output capacitance stored energy



3 Test circuits

Figure 15: Test circuit for resistive load switching times



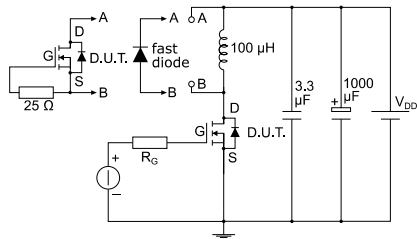
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Figure 16: Test circuit for gate charge behavior



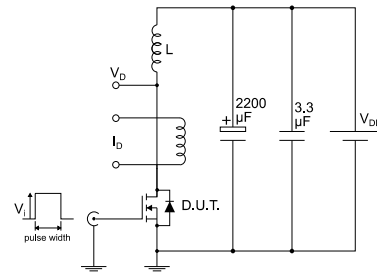
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Figure 17: Test circuit for inductive load switching and diode recovery times



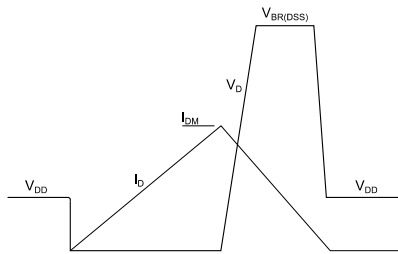
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Figure 18: Unclamped inductive load test circuit



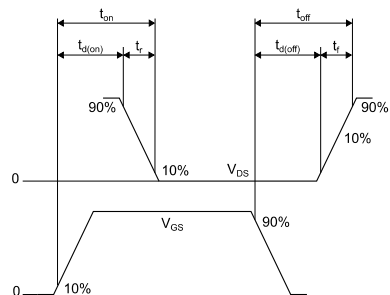
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Figure 19: Unclamped inductive waveform



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Figure 20: Switching time waveform



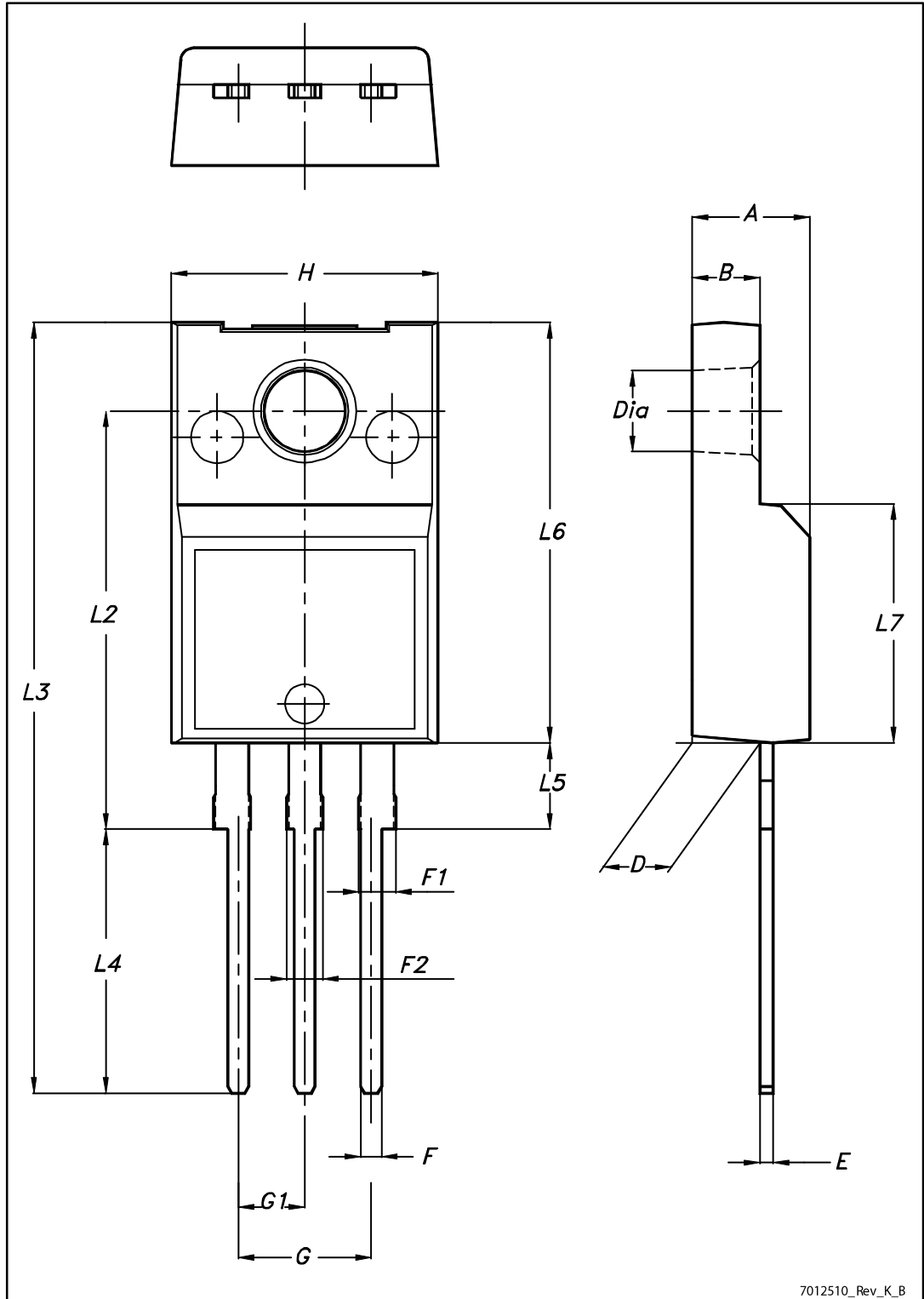
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 21: TO-220FP package outline



7012510_Rev_K_B

Table 9: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
07-Apr-2014	1	First release.
07-Jun-2016	2	Updated <i>Figure 6: "Gate charge vs gate-source voltage"</i> and <i>Table 5: "Dynamic"</i> . Minor text changes.

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