DEMO CIRCUIT 1134
QUICK START GUIDE

LTC4222
Dual Hot Swap Controller with I²C Compatible Monitoring

DESCRIPTION

Demonstration Circuit DC1134A allows evaluation of the performance of the LTC®4222_UF Dual Hot Swap Controller with I2C Compatible Monitoring in +12V/5A and +3.3V/5A applications.

The DC1134A can demonstrate turn-on and turn-off transients as well as the steady state mode of the LTC4222. The Controller responds to fault conditions such as input overvoltage (OV), input undervoltage (UV), output power good (PWRGD) fault and overcurrent fault, and response may be verified by the Fault Alert LED.

The board contains one LTC®4222_UF Controller, two rail channels, input clamps, input and output voltage dividers for setting the UV, OV and PWRGD comparator thresholds, LEDs to indicate the presence of input and output voltages, I2C and ALERT signals, three jumpers ADR0, ADR1, and ADR3 for I2C address programming, jumper TIMER SELECT for timer off period selection, jumper “ON” for ON pin signal selection, jumper “ON CONFIG” for selecting independent or coupled rail operation, two jumpers “ADIN1” and “ADIN2” for selecting ADC1 and ADC2 input signals, two jumpers “EN1 and EN2” for selection EN1 and EN2 pin signals, I2C port and turret terminals for critical signals to facilitate evaluation in a working system. Each rail channel includes a series connected power MOSFET and sense resistor.

The I2C port designed to interface with the DC590A allows providing full control of the DC1134 with LTC's QuickEval software.

Design files for this circuit board are available. Call the LTC factory.

PERFORMANCE SUMMARY

Specifications are at TA = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DDN}	Input Supply Range		2.9		29	V
$V_{DDN(UVL)}$	Input Supply Undervoltage Lockout	V_{DD} Rising	2.34	2.43	2.53	V
$\Delta V_{SENSE(TH)}$	Circuit Breaker Threshold (VV_{DD}-V_{SENSED})		47.5	50	52.5	mV
ΔV_{SENSE}	Current Limit Voltage (VV_{DD}-V_{SENSED})	V_{FB-}=1.3V V_{FB-}=0V Start-Up Timer Expired	46 14 130	50 16.6 150	54 19 165	mV mV mV
V_{DD1}	First Rail Operating Voltage			12		V
V_{DD2}	Second Rail Operating Voltage			3.3		V
I_{LIMIT}	Circuit Breaker Current Limit in both Rails	Steady State Condition, after Power-Up	4.6	5	5.4	A
dU_{OUT}/DT	Both Rails Output Voltage Slew Rate	Rail Current Lower Current Limit Threshold	850	1200	1900	V/s
$V_{INPUT(TH)}$	CONFIG, ENn, FBn, ONn, OVn and UVn Pin Input Threshold	V_{IN} Rising	1.215	1.235	1.255	V

PERFORMANCE SUMMARY

Specifications are at TA = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$I_{GATE(UP)}$	External N-Channel Gate Pull-Up Current	Gate On, V_{GATE} = 0V	8	12	18	µA

OPERATING PRINCIPLES

The LTC4222 is a low voltage dual hot swap controller that has 2.9V to 29V operating range and 35V absolute maximum voltage for the VDD pins. In the DC1134A the first channel operates on the +12V rail and the second channel on the +3.3V rail. Each channel can easily be readjusted for any voltage between 2.9V and 29V by replacing the top resistors in the UV, OV and FB dividers (R1, R2, R7 for the first channel and R101, R102, R107 for the second one). The DC1134 as supplied by the factory is assembled with the Si4864DP MOSFETs in an SO-8 package and with 10mΩ current sense resistors, setting a minimum of 4.6A current limit and 4.75A circuit breaker threshold. The current limit and circuit breaker thresholds can be adjusted by changing the channel's sense resistor (RS1 and RS2). To enable demonstration of higher current applications up to 25A, provisions have been made to replace the provided sense resistor with a 1W, 2512 size and replace Q1 and Q101 with MOSFETs in a PowerPAK SO-8, such as the Si7476ADP. The large turrets may be removed to permit installation of up to a 12 gauge wire for direct, low resistance connections to the board. None of the turrets are swaged.

QUICK START PROCEDURE

Demonstration circuit 1134 is easy to set up to evaluate the performance of the LTC4222. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

The DC1134 is factory set up to operate with 12V and 3.3V rails and up to 5A. If the LTC4222 is to be evaluated at different operating conditions, follow steps 1 through 3 below, otherwise skip to step 4.

1. If evaluating at a voltage other than 12V and 3.3V, R1, R2, R101 and R102 must be adjusted for proper UV and OV comparator response. The values of the bottom resistor in the divider R3 (14.7k) and R103 (4.12k) may be assigned arbitrarily.

Select a voltage divider top resistor R1 and R101 as

$R1 \le 14.7(V_{MAX/12}/1.255)[1\text{-}1.215/V_{MIN12}]k$,

$R101 \le 4.12(V_{MAX3.3}/1.255)[1\text{-}1.215/V_{MIN3.3}]k$.

Select a voltage divider middle resistor R2 and R102 as

$R2 \le 14.7(1.215V_{MAX12}/1.255V_{MIN12}\text{-}1)k$

$R102 \le 4.12(1.215V_{MAX3.3}/1.255V_{MIN3.3}\text{-}1)$ k.

where V_{MIN} and V_{MAX} are the minimum and maximum output voltages expected for normal operation.

Select resistors in the feedback dividers R7 or R107 as

$R = 3.01[V_{MIN}/1.255\text{-}1]k$

where V_{MIN} is the minimum output voltage accepted as a good output.

2. If the DC1134 will operate at other than 5A max, change the value of the sense resistor R_{SENSE}= 0.99•47.5mV/$I_{LOAD(MAX)}$ for a 1% tolerance current sense resistor.

3. If the DC1134 will operate above 10A, replace Q1 with a suitable PowerPAK SO-8 package MOSFET such as the Si7880ADP suitable for up to 20A. The SO-8 pads on the front of the board include the extra heat-sinking area this package requires. Alternately, for low power applications, Q1 may be replaced with a MOSFET in a SSOT-6 package using pads on the back of the board.

4. The "TIMER SELECT" jumper chooses the startup time limit. It may enable either the adjustable timer with external timer capacitor CT or the built in internal timer with a fixed startup time 100ms. CT is stuffed with a 0.68µF capacitor at the factory, which provides a 8ms startup time. To customize the startup time, select CT = T_{START}/12.3(ms/µF).

5. The soft start capacitor, CSS, sets the current ramp rate at which the inrush current will increase when turning on. CSS is stuffed with a 68nF capacitor at the factory, which provides a 5mV/ms inrush sense resistor voltage ramp or 0.5A/ms for both rails.

6. The LTC4222 does not require an RC network on the GATE pin for compensation. However, an RC network may be used to limit the rate at which the GATE rises to provide an inrush current below the internal current limit. Pads for R6, R106, CG1 and CG2 on the back of the board are available for this purpose. R6 and CG1, as well as R106 and CG2 may be stuffed with 100K resistor, and CG = C_{LOAD} * 20uA/I_{INRUSH} for this purpose.

7. The ADIN1 and ADIN2 turrets may be used to provide signals to take 10 bit measurements of any voltage. Jumpers "ADIN1 SELECT" and "'ADIN2 SELECT" choose between measuring the input rail voltage or measuring the voltage on the ADIN1, ADIN2 turrets respectively. The rail input voltages are measured through resistor dividers. The +12V divider is assembled to a 15.4V full scale range to match the range of the Q1 SOURCE voltage measurement. The +3.3V divider is assembled to a 4.3V full scale range to match the range of the Q101 SOURCE voltage measurement. To change the full scale of the input measurement, select R11 or R111 as

   R = V_{RANGE}*12.4k/1.23-12.4k.

   The signals at the ADIN1 and ADIN2 turrets are also measured through a voltage dividers, but the bottom resistor is not stuffed at the factory, defaulting to a 1.28V full scale voltage. To select a larger full scale voltage, choose R17 and R117 as

   R = 12.8/(V_{RANGE}-1.28)k.

8. If the system uses short connector pins to sense board insertion, place "EN1" and "EN2" jumpers to position SHORT PIN1 and SHORT PIN2, respectively. Using the SHORT PIN1 and SHORT PIN2 turrets, connect the aforementioned short pins. Those are direct connections to the LTC4222's EN1 and EN2 pins; if deleterious voltages are anticipated, add a series resistor and clamping. EN1 and EN2 are good for -0.3 to +12V on their own. EN1 and EN2 are also logic compatible with a 1.235V threshold and 130mV hysteresis.

9. The I^2C address, assigned to the board, is selected on the board by using jumpers "ADR0", "ADR1" and "ADR2" to pull the address pins high, low, or allow them to float. An address table is shown in the data sheet. The evaluation software automatically scans and identifies the I2C address, regardless of the setting.

10. After any necessary component changes have been made, connect suitable loads between +12V/5A OUTPUT and GND and +3.3V/5A OUTPUT and GND. This may be a passive resistive load or an active electronic load box. If long leads are present between the DC1134 and load, install 10µF or more at C1 and C101. This should eliminate the chance of MOSFET oscillation and large negative excursions at +12V/5A OUTPUT.

11. Connect power supplies capable of supplying 10A to the +12V INPUT and GND turrets and

the +3.3V INPUT and GND turrets. The minimum current capability of the supply must accommodate the tolerance of the circuit breaker threshold of ±10%. With the 10mΩ, 1%, factory installed sense resistor, the overload circuit breaker will trip at (5.0±0.3)A.

12. Connect the ribbon cable from a DC590 to the I2C PORT on the DC1134. LTC's QuickEval software will automatically recognize the DC1134 and load software to read and write to the LTC4222's registers. During an I2C transaction, D5 and D7 will flicker faintly. If the I2C port (JP7) is disconnected, the turret terminals SDA and SCL can be connected directly to an I2C bus. Power for D4, D5, and D7 is supplied by JP7**,** pin 2, so in this mode the LEDs will not light unless 5V is connected to this pin.

13. The following experiments can be run. Turn on into a nominal load. Turn on into an overload. Turn on into a short circuit. Turn on into a nominal load and increase the load until the LTC4222 trips off. A digital storage scope provides a convenient means of observing the turn-on and overload events. Observe the input or output current using a current probe. A probe ground turret on the board provides a low current connection to the LTC4222's ground.

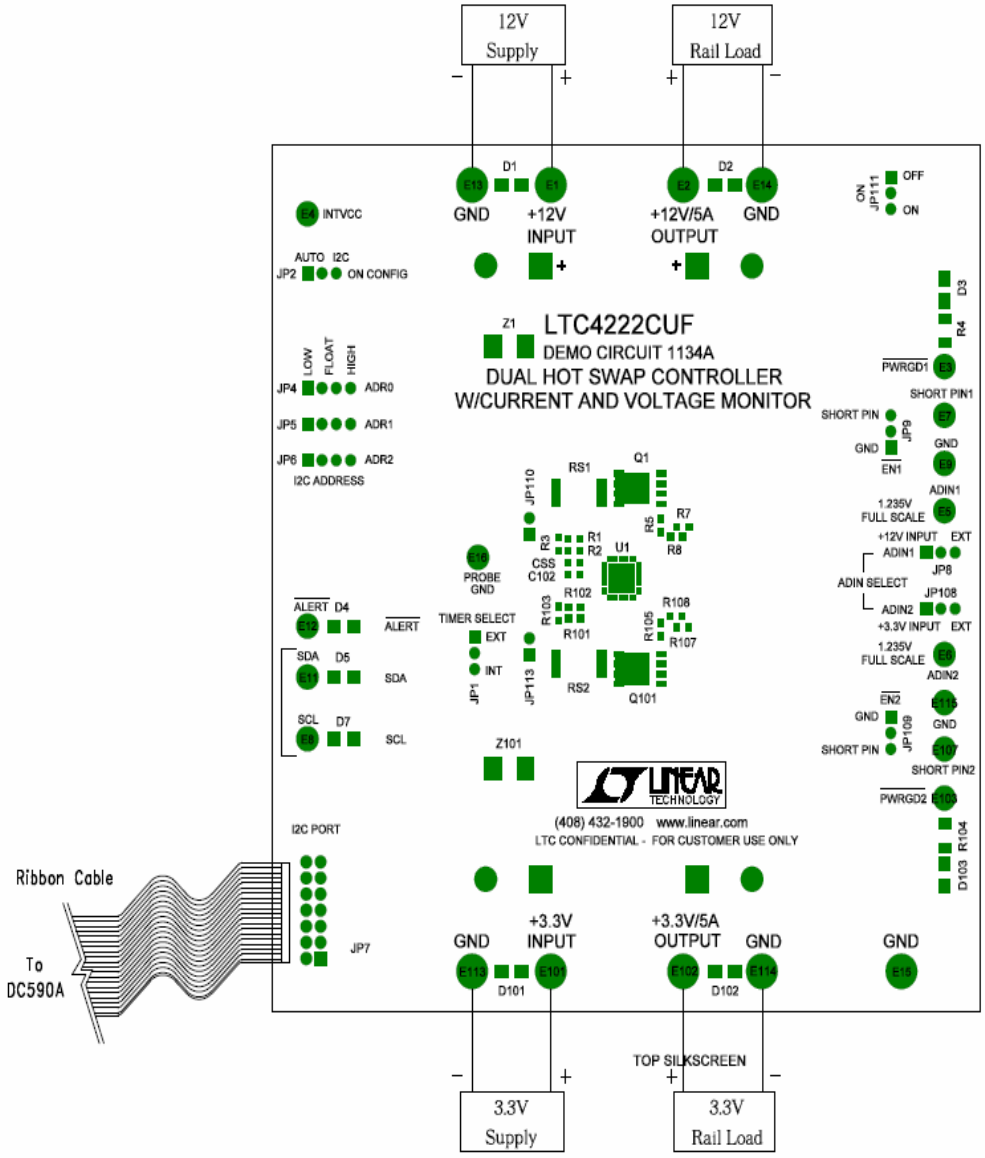


Figure 1. Proper Measurement Equipment Setup

USING THE I²C PORT WITH QUICKEVAL

Demonstration circuit 1134 is easy to set up to evaluate the performance of the LTC4222. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

REGISTER DISPLAY OPTIONS

The content of all Controller registers is displayed in the Register List with symbols “1” and “0” and updated with each refresh of the interface. Additionally there is an option to display CONTROL(A), ALERT(B), STATUS(C), and FAULT(D) registers for both channels with functional bits description. Clicking appropriate register button calls the necessary information. Figures 2 and 3 demonstrate register display options. Checking a box to the left of each bit of the registers CONTROL, ALERT, and FAULT sets the respective bit, while unchecking a box clears the bit. The STATUS register bits are shown after every refresh of the interface. The Clear button for register D clears out the bits in this register.

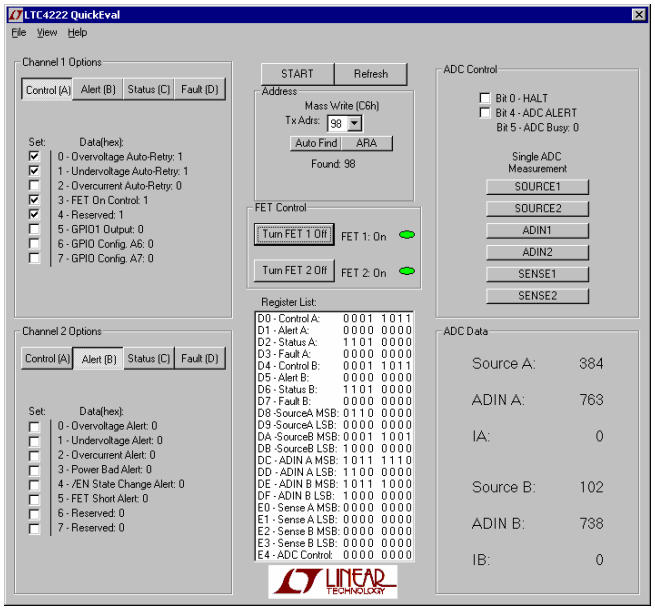


Figure 2.

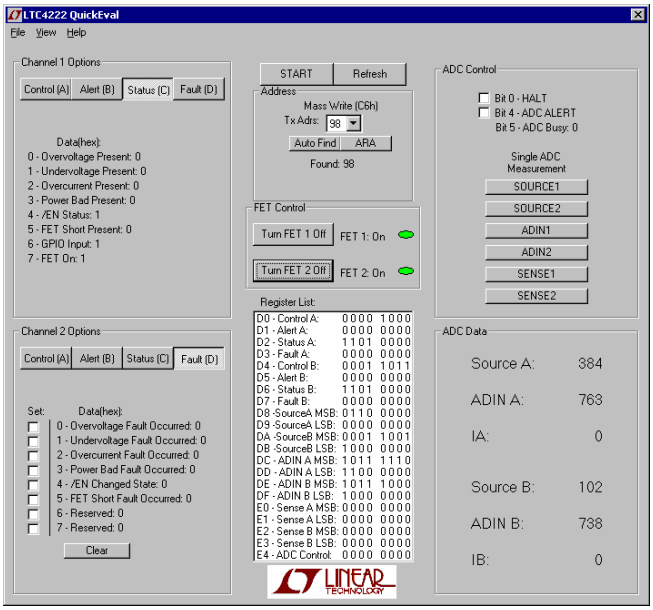


Figure 3.

START / REFRESH BUTTONS

Click on the START button to enable a timer that continuously updates the interface with the latest data from the LTC4222. This button will display STOP when the timer is enabled. Click on STOP to stop the timer. Click on the Refresh button for a single update.

FET CONTROL

The status of the FET is shown with a color display. When the FET On bit (C3) is checked and read as high and the FET On Control bit (A3) is set, the FET is on, the shape display will be green.

Turn FET Off. If C3 is low and A3 is set, the FET is off, the shape display will be red.

Clear Faults. In all other cases, the FET is off, the shape display is red.

Turn FET On. The Turn FET On control button sets bits A3 logic high. Turn FET Off or Clear Faults clears bit A3 to logic low.

ADDRESS SELECTION

Select in the drop down list box the Write address byte of the LTC4222 that is to be communicated with. If multiple LTC4222s are on the bus lines, the Mass Write address BEh can be selected to communicate with all LTC4222s at the same time. The Auto find button will scan through the 27 individual LTC4222 addresses and list which addresses responded with an acknowledge. The ARA button sends the Alert Response protocol and displays the address of the device that replies with its address.

DATA DISPLAY OPTION

Source voltage, ADIN signal, and load current (In) for both channels are displayed in the ADC Data window in the decimal format of the ADC register content.

To translate the register content to the physical value use the following equations:

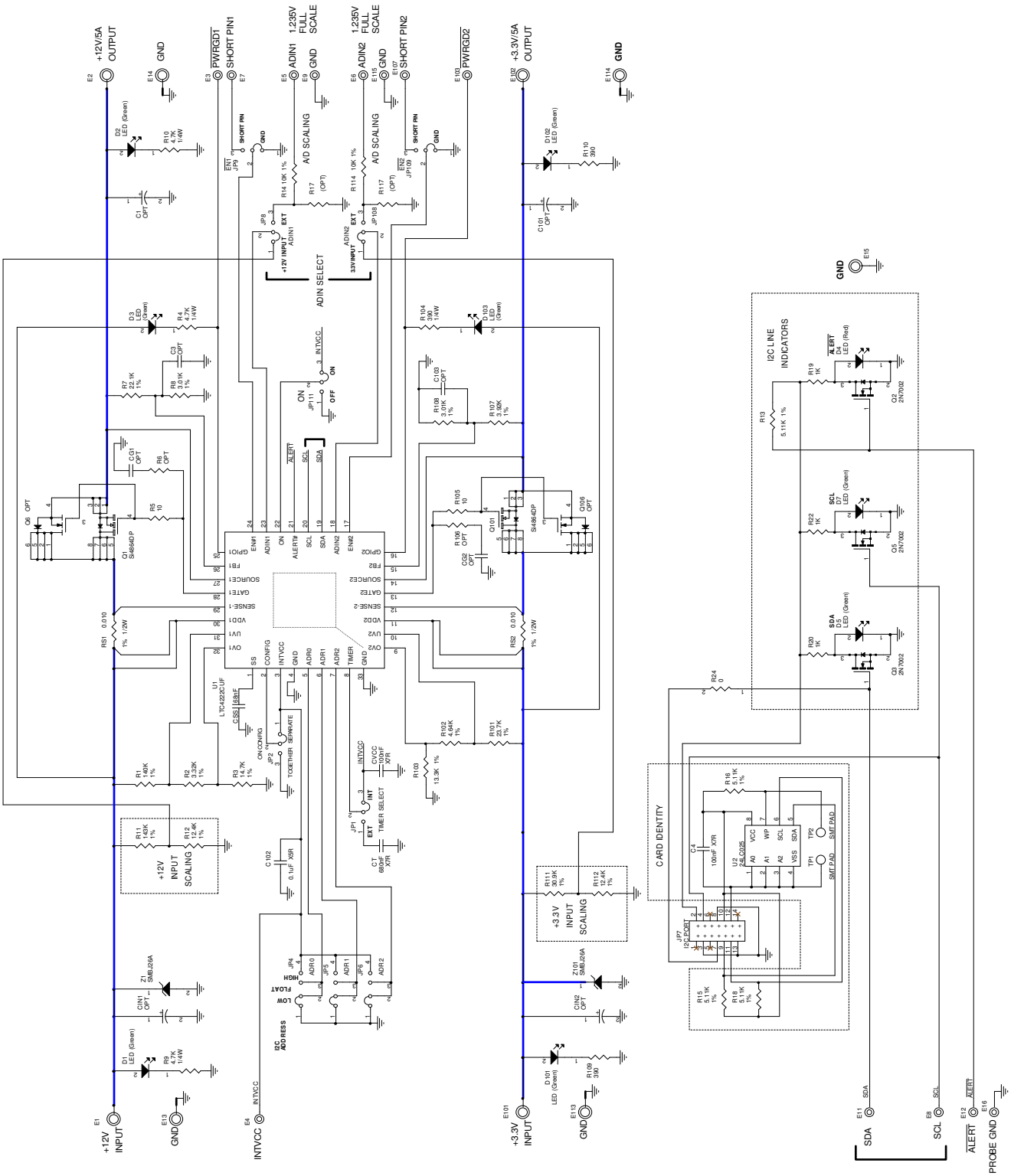
Source voltage = Source(data) * 0.03125V

ADIN voltage = ADIN(data) * 0.00125V

Load Current = Idata * 0.00625V (for 10mΩ sense resistor).

6) ADC Control

The ADC Control window allows the ADC to be placed into the HALT state, facilitating single measurements. Checking ADC_ALERT causes the ALERT pin to be asserted at the end of an ADC conversion.



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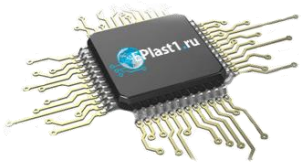

Как с нами связаться

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