



# LMC7101

## Low-Power Operational Amplifier

### Final Information

### General Description

The LMC7101 is a high-performance, low-power, operational amplifier which is pin-for-pin compatible with the National Semiconductor LMC7101. It features rail-to-rail input and output performance in Micrel's IttyBitty™ SOT-23-5 package.

The LMC7101 is a 500kHz gain bandwidth amplifier designed to operate from 2.7V to 12V single-ended power supplies with guaranteed performance at supply voltages of 2.7V, 3V, 5V, and 12V.

This op amp's input common-mode range includes ground and extends 300mV beyond the supply rails. For example, the common-mode range is -0.3V to +5.3V with a 5V supply.

### Features

- Small footprint SOT-23-5 package
- Guaranteed 2.7V, 3V, 5V, and 12V performance
- 500kHz gain-bandwidth
- 0.01% total harmonic distortion at 10kHz (5V, 2kΩ)
- 0.5mA typical supply current at 5V

### Applications

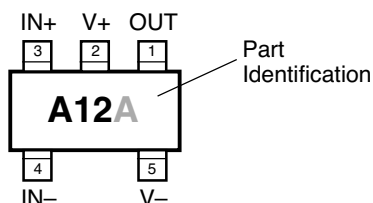
- Mobile communications, cellular phones, pagers
- Battery-powered instrumentation
- PCMCIA, USB
- Portable computers and PDAs

### Ordering Information

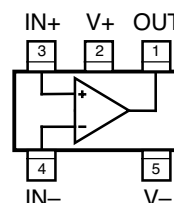
Standard		Pb-Free		Grade	Temp Range	Package
Part Number	Marking	Part Number	Marking*			
LMC7101AIM5	A12A	LMC7101AYM5	<u>A</u> 12A	Prime	-40°C to +85°C	SOT-23-5
LMC7101BIM5	A12	LMC7101BYM5	<u>A</u> 12	Standard	-40°C to +85°C	SOT-23-5

\*Under bar symbol (  ) may not be to scale.

### Pin Configuration



### Functional Configuration



SOT-23-5 (M5)

### Pin Description

Pin Number	Pin Name	Pin Function
1	OUT	Amplifier Output
2	V+	Positive Supply
3	IN+	Noninverting Input
4	IN-	Inverting Input
5	V-	Negative Supply: Negative supply for split supply application or ground for single supply application.

**Absolute Maximum Ratings (Note 1)**

Supply Voltage ( $V_{V+} - V_{V-}$ )	15V
Differential Input Voltage ( $V_{IN+} - V_{IN-}$ )	$\pm(V_{V+} - V_{V-})$
I/O Pin Voltage ( $V_{IN}, V_{OUT}$ ), <b>Note 2</b>	$V_{V+} + 0.3V$ to $V_{V-} - 0.3V$
Junction Temperature ( $T_J$ )	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (soldering, 10 sec.)	260°C
ESD, <b>Note 5</b>	2kV

**Operating Ratings (Note 1)**

Supply Voltage ( $V_{V+} - V_{V-}$ )	2.7V to 12V
Ambient Temperature ( $T_A$ )	-40°C to +85°C
Junction Temperature ( $T_J$ )	-40°C to +125°C
Max. Junction Temperature ( $T_{J(max)}$ ), <b>Note 3</b>	+125°C
Package Thermal Resistance ( $\theta_{JA}$ ), <b>Note 4</b>	325°C/W
Max. Power Dissipation	<b>Note 3</b>

**Electrical Characteristics (2.7V)**

$V_+ = +2.7V$ ,  $V_- = 0V$ ,  $V_{CM} = V_{OUT} = V_+/2$ ;  $R_L = 1M\Omega$ ;  $T_J = 25^\circ C$ , **bold** values indicate  $-40^\circ C \leq T_J \leq +85^\circ C$ ; unless noted

				LMC7101A		LMC7101B		
Symbol	Parameter	Condition	Typ	Min	Max	Min	Max	Units
$V_{OS}$	Input Offset Voltage		0.11		6		9	mV
$TCV_{OS}$	Input Offset Voltage Average Drift		1.0					$\mu V/^\circ C$
$I_B$	Input Bias Current		1.0		<b>64</b>		<b>64</b>	pA
$I_{OS}$	Input Offset Current		0.5		<b>32</b>		<b>32</b>	pA
$R_{IN}$	Input Resistance		>1					$T\Omega$
CMRR	Common-Mode Rejection Ratio	$0V \leq V_{CM} \leq 2.7V$ , <b>Note 6</b>	70	50		50		dB
$V_{CM}$	Input Common-Mode Voltage	input low, CMRR $\geq 50$ dB	-0.3		0.0		0.0	V
		input high, CMRR $\geq 50$ dB	3.0	2.7		2.7		V
PSRR	Power Supply Rejection Ratio	$V_+ = 1.35V$ to $1.65V$ , $V_- = -1.35V$ to $-1.65V$ , $V_{CM} = 0$	60	50		45		dB
$C_{IN}$	Common-Mode Input Capacitance		3					pF
$V_O$	Output Swing	output high, $R_L = 10k$	2.699	2.64		2.64		V
		output low, $R_L = 10k$	0.001		0.06		0.06	V
		output high, $R_L = 2k$	2.692	2.6		2.6		V
		output low, $R_L = 2k$	0.008		0.1		0.1	V
$I_S$	Supply Current	$V_{OUT} = V_+/2$	0.5		0.81		0.81	mA
					<b>0.95</b>		<b>0.95</b>	
SR	Slew Rate		0.4					V/ $\mu s$
GBW	Gain-Bandwidth Product		0.5					MHz

**Electrical Characteristics (3.0V)**

$V_+ = +3.0V$ ,  $V_- = 0V$ ,  $V_{CM} = V_{OUT} = V_+/2$ ;  $R_L = 1M\Omega$ ;  $T_J = 25^\circ C$ , **bold** values indicate  $-40^\circ C \leq T_J \leq +85^\circ C$ ; unless noted

				LMC7101A		LMC7101B		
Symbol	Parameter	Condition	Typ	Min	Max	Min	Max	Units
$V_{OS}$	Input Offset Voltage		0.11		4		7	mV
					<b>6</b>		<b>9</b>	
$TCV_{OS}$	Input Offset Voltage Average Drift		1.0					$\mu V/^\circ C$
$I_B$	Input Bias Current		1.0		<b>64</b>		<b>64</b>	pA
$I_{OS}$	Input Offset Current		0.5		<b>32</b>		<b>32</b>	pA
$R_{IN}$	Input Resistance		>1					$T\Omega$

Symbol	Parameter	Condition	Typ	LMC7101A		LMC7101B		Units
				Min	Max	Min	Max	
CMRR	Common-Mode Rejection Ratio	$0V \leq V_{CM} \leq 3.0V$ , <b>Note 6</b>	74	60		60		dB
$V_{CM}$	Input Common-Mode Voltage	input low, CMRR $\geq 50$ dB	-0.3		0		0	V
		input high, CMRR $\geq 50$ dB	3.3	3.0		3.0		V
PSRR	Power Supply Rejection Ratio	$V_+ = 1.5V$ to $6.0V$ , $V_- = -1.5V$ to $-6.0V$ , $V_{CM} = 0$	80	68		60		dB
$C_{IN}$	Common-Mode Input Capacitance		3					pF
$V_{OUT}$	Output Swing	output high, $R_L = 2k$	2.992	2.9		2.9		V
		output low, $R_L = 2k$	0.008		0.1		0.1	V
		output high, $R_L = 600\Omega$	2.973	2.85		2.85		V
		output low, $R_L = 600\Omega$	0.027		0.15		0.15	V
$I_S$	Supply Current		0.5		0.81 <b>0.95</b>		0.81 <b>0.95</b>	mA mA

## Electrical Characteristics—DC (5V)

$V_+ = +5.0V$ ,  $V_- = 0V$ ,  $V_{CM} = 1.5V$ ,  $V_{OUT} = V_+/2$ ;  $R_L = 1M\Omega$ ;  $T_J = 25^\circ C$ , **bold** values indicate  $-40^\circ C \leq T_J \leq +85^\circ C$ ; unless noted

Symbol	Parameter	Condition	Typ	LMC7101A		LMC7101B		Units
				Min	Max	Min	Max	
$V_{OS}$	Input Offset Voltage		0.11		3 <b>5</b>		7 <b>9</b>	mV mV
$TCV_{OS}$	Input Offset Voltage Average Drift		1.0					$\mu V/^\circ C$
$I_B$	Input Bias Current		1.0		<b>64</b>		<b>64</b>	pA
$I_{OS}$	Input Offset Current		0.5		<b>32</b>		<b>32</b>	pA
$R_{IN}$	Input Resistance		>1					$T\Omega$
CMRR	Common-Mode Rejection Ratio	$0V \leq V_{CM} \leq 5V$ , <b>Note 6</b>	82	60 <b>55</b>		60 <b>55</b>		dB dB
$V_{CM}$	Input Common-Mode Voltage	input low, CMRR $\geq 50$ dB	-0.3		-0.20 <b>0.00</b>		-0.20 <b>0.00</b>	V V
		input high, CMRR $\geq 50$ dB	5.3	5.20 <b>5.00</b>		5.20 <b>5.00</b>		V V
+PSRR	Positive Power Supply Rejection Ratio	$V_+ = 5V$ to $12V$ , $V_- = 0V$ , $V_{OUT} = 1.5V$	82	70 <b>65</b>		65 <b>62</b>		dB dB
-PSRR	Negative Power Supply Rejection Ratio	$V_+ = 0V$ , $V_- = -5V$ to $-12V$ , $V_{OUT} = -1.5V$	82	70 <b>65</b>		65 <b>62</b>		dB dB
$C_{IN}$	Common-Mode Input Capacitance		3					pF
$V_{OUT}$	Output Swing	output high, $R_L = 2k$	4.989	4.9 <b>4.85</b>		4.9 <b>4.85</b>		V V
		output low, $R_L = 2k$	0.011		0.1 <b>0.15</b>		0.1 <b>0.15</b>	V V
		output high, $R_L = 600\Omega$	4.963	4.9 <b>4.8</b>		4.9 <b>4.8</b>		V V
		output low, $R_L = 600\Omega$	0.037		0.1 <b>0.2</b>		0.1 <b>0.2</b>	V V
$I_{SC}$	Output Short Circuit Current <b>Note 7</b>	sourcing ( $V_{OUT} = 0V$ ) or sinking ( $V_{OUT} = 5V$ )	200	120 <b>80</b>		120 <b>80</b>		mA mA
$I_S$	Supply Current	$V_{OUT} = V_+/2$	0.5		0.85 <b>1.0</b>		0.85 <b>1.0</b>	mA mA

**Electrical Characteristics—DC (12V)**

$V_+ = +12V$ ,  $V_- = 0V$ ,  $V_{CM} = 1.5V$ ,  $V_{OUT} = V_+/2$ ;  $R_L = 1M\Omega$ ;  $T_J = 25^\circ C$ , **bold** values indicate  $-40^\circ C \leq T_J \leq +85^\circ C$ ; unless noted

Symbol	Parameter	Condition	Typ	LMC7101A		LMC7101B		Units
				Min	Max	Min	Max	
$V_{OS}$	Input Offset Voltage		0.11		6		9	mV
$TCV_{OS}$	Input Offset Voltage Average Drift		1.0					$\mu V/^\circ C$
$I_B$	Input Bias Current		1.0		<b>64</b>		<b>64</b>	pA
$I_{OS}$	Input Offset Current		0.5		<b>32</b>		<b>32</b>	pA
$R_{IN}$	Input Resistance		>1					$T\Omega$
CMRR	Common-Mode Rejection Ratio	$0V \leq V_{CM} \leq 12V$ , <b>Note 6</b>	82	65 <b>60</b>		65 <b>60</b>		dB dB
$V_{CM}$	Input Common-Mode Voltage	input low, $V_+ = 12V$ , CMRR $\geq 50dB$	-0.3		-0.20 <b>0.00</b>		-0.20 <b>0.00</b>	V V
		input high, $V_+ = 12V$ , CMRR $\geq 50dB$	12.3	12.2 <b>12.0</b>		12.2 <b>12.0</b>		V V
+PSRR	Positive Power Supply Rejection Ratio	$V_+ = 5V$ to $12V$ , $V_- = 0V$ , $V_{OUT} = 1.5V$	82	70 <b>65</b>		65 <b>62</b>		dB dB
-PSRR	Negative Power Supply Rejection Ratio	$V_+ = 0V$ , $V_- = -5V$ to $-12V$ , $V_{OUT} = -1.5V$	82	70 <b>65</b>		65 <b>62</b>		dB dB
$A_V$	Large Signal Voltage Gain	sourcing or sinking, $R_L = 2k$ , <b>Note 9</b>	340	80 <b>40</b>		80 <b>40</b>		V/mV V/mV
		sourcing or sinking, $R_L = 600\Omega$ , <b>Note 9</b>	300	15 <b>10</b>		15 <b>10</b>		V/mV V/mV
$C_{IN}$	Common-Mode Input Capacitance		3					pF
$V_{OUT}$	Output Swing	output high, $V_+ = 12V$ , $R_L = 2k$	11.98	11.9 <b>11.87</b>		11.9 <b>11.87</b>		V V
		output low, $V_+ = 12V$ , $R_L = 2k$ ,	0.02		0.10 <b>0.13</b>		0.10 <b>0.13</b>	V V
		output high, $V_+ = 12V$ , $R_L = 600\Omega$	11.93	11.73 <b>11.65</b>		11.73 <b>11.65</b>		V V
		output low, $V_+ = 12V$ , $R_L = 600\Omega$	0.07		0.27 <b>0.35</b>		0.27 <b>0.35</b>	V V
$I_{SC}$	Output Short Circuit Current	sourcing ( $V_{OUT} = 0V$ ) or sinking ( $V_{OUT} = 12V$ ), <b>Notes 7, 8</b>	300	200 <b>120</b>		200 <b>120</b>		mA mA
$I_S$	Supply Current	$V_{OUT} = V_+/2$	0.8		1.5 <b>1.71</b>		1.5 <b>1.71</b>	mA mA

## Electrical Characteristics—AC (5V)

$V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 1.5V$ ,  $V_{OUT} = V_+/2$ ;  $R_L = 1M\Omega$ ;  $T_J = 25^\circ C$ , **bold** values indicate  $-40^\circ C \leq T_J \leq +85^\circ C$ ; unless noted

Symbol	Parameter	Condition	Typ	LMC7101A		LMC7101B		Units
				Min	Max	Min	Max	
THD	Total Harmonic Distortion	$f = 10kHz$ , $A_V = -2$ , $R_L = 2k\Omega$ , $V_{OUT} = 4.0 V_{PP}$	0.01					%
SR	Slew Rate		0.3					V/ $\mu s$
GBW	Gain-Bandwidth Product		0.5					MHz

## Electrical Characteristics—AC (12V)

$V_+ = 12V$ ,  $V_- = 0V$ ,  $V_{CM} = 1.5V$ ,  $V_{OUT} = V_+/2$ ;  $R_L = 1M\Omega$ ;  $T_J = 25^\circ C$ , **bold** values indicate  $-40^\circ C \leq T_J \leq +85^\circ C$ ; unless noted

Symbol	Parameter	Condition	Typ	LMC7101A		LMC7101B		Units
				Min	Max	Min	Max	
THD	Total Harmonic Distortion	$f = 10kHz$ , $A_V = -2$ , $R_L = 2k$ , $V_{OUT} = 8.5 V_{PP}$	0.01					%
SR	Slew Rate	$V_+ = 12V$ , <b>Note 10</b>	0.3	0.19 <b>0.15</b>		0.19 <b>0.15</b>		V/ $\mu s$ V/ $\mu s$
GBW	Gain-Bandwidth Product		0.5					MHz
$\phi_m$	Phase Margin		45					$^\circ$
$G_m$	Gain Margin		10					dB
$e_n$	Input-Referred Voltage Noise	$f = 1kHz$ , $V_{CM} = 1V$	37					nV/ $\sqrt{Hz}$
$i_n$	Input-Referred Current Noise	$f = 1kHz$	1.5					fA/ $\sqrt{Hz}$

**General Notes:** Devices are ESD protected; however, handling precautions are recommended. All limits guaranteed by testing on statistical analysis.

**Note 1.** Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside its recommended operating ratings.

**Note 2.** I/O Pin Voltage is any external voltage to which an input or output is referenced.

**Note 3.** The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_{J(max)}$ ; the junction-to-ambient thermal resistance,  $\theta_{JA}$ ; and the ambient temperature,  $T_A$ . The maximum allowable power dissipation at any ambient temperature is calculated using:  $P_D = (T_{J(max)} - T_A) \div \theta_{JA}$ . Exceeding the maximum allowable power dissipation will result in excessive die temperature.

**Note 4.** Thermal resistance,  $\theta_{JA}$ , applies to a part soldered on a printed-circuit board.

**Note 5.** Human body model, 1.5k in series with 100pF.

**Note 6.** Common-mode performance tends to follow the typical value. Minimum value limits reflect performance only near the supply rails.

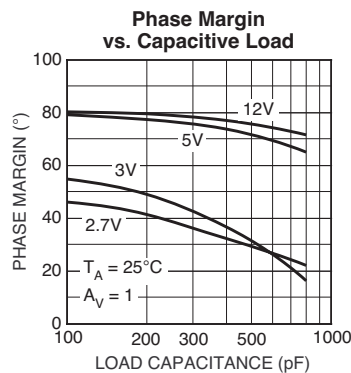
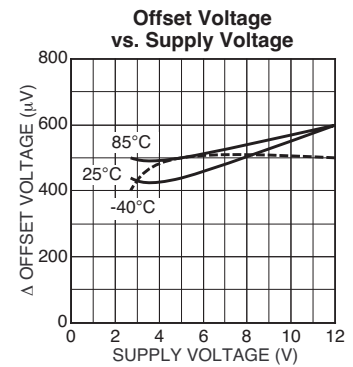
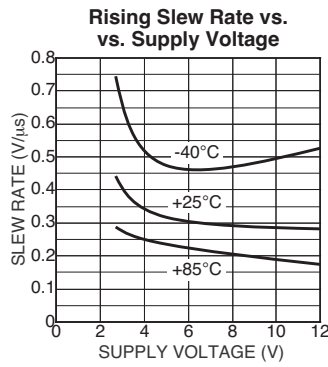
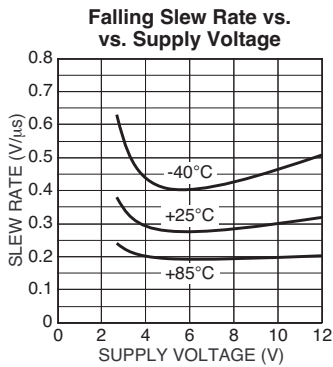
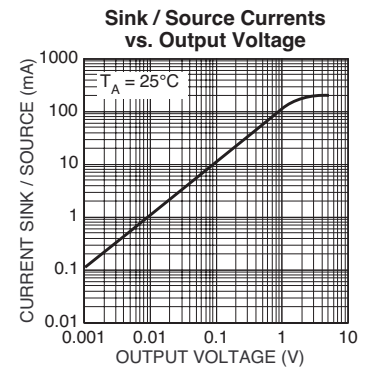
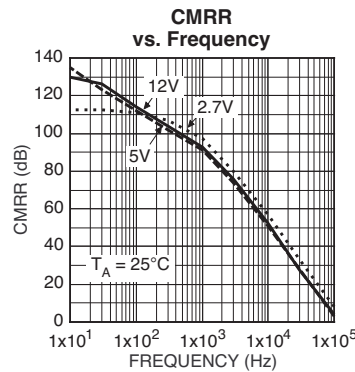
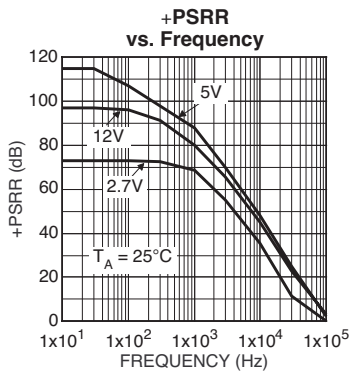
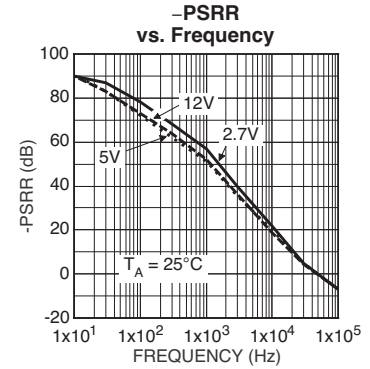
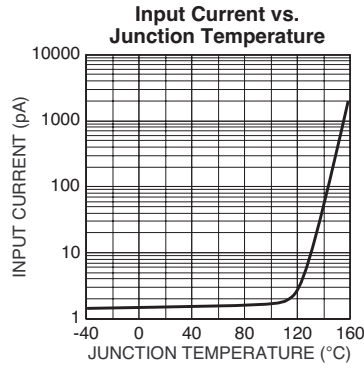
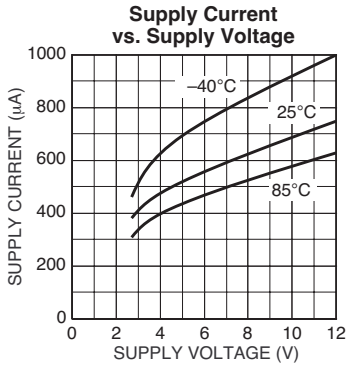
**Note 7.** Continuous short circuit may exceed absolute maximum  $T_J$  under some conditions.

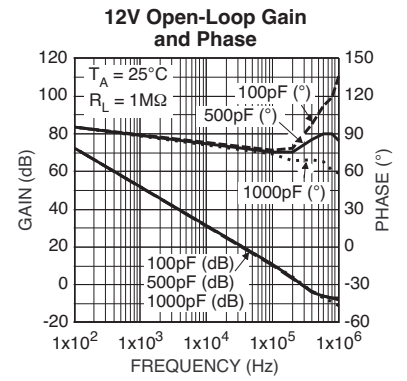
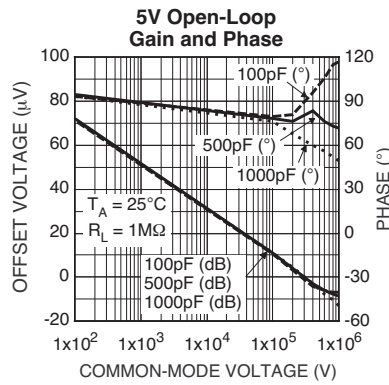
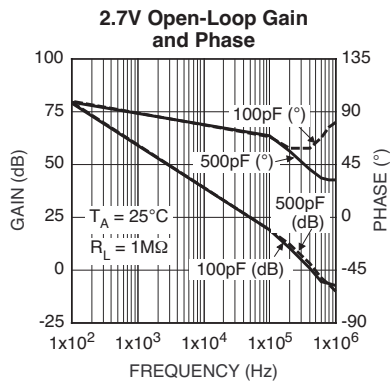
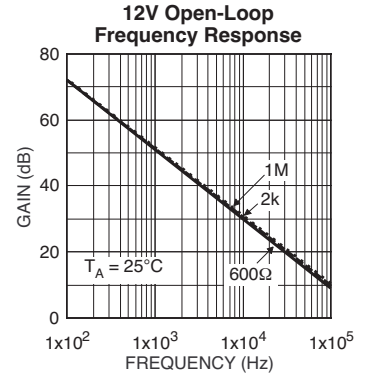
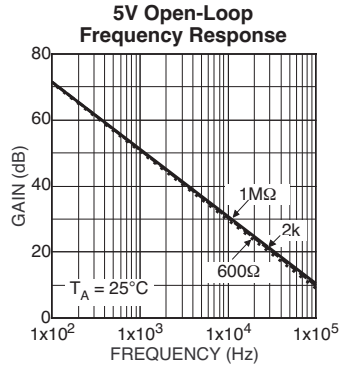
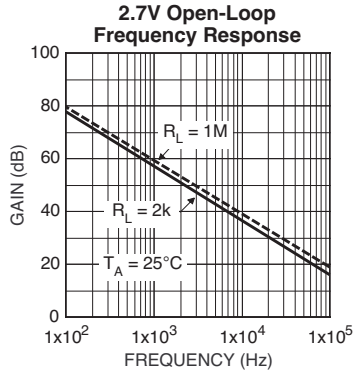
**Note 8.** Shorting OUT to  $V_+$  when  $V_+ > 12V$  may damage the device.

**Note 9.**  $R_L$  connected to 5.0V. Sourcing:  $5V \leq V_{OUT} \leq 12V$ . Sinking:  $2.5V \leq V_{OUT} \leq 5V$ .

**Note 10.** Device connected as a voltage follower with a 12V step input. The value is the positive or negative slew rate, whichever is slower.

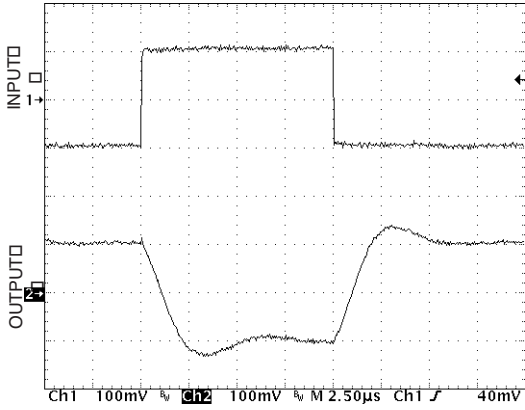
# Typical Characteristics



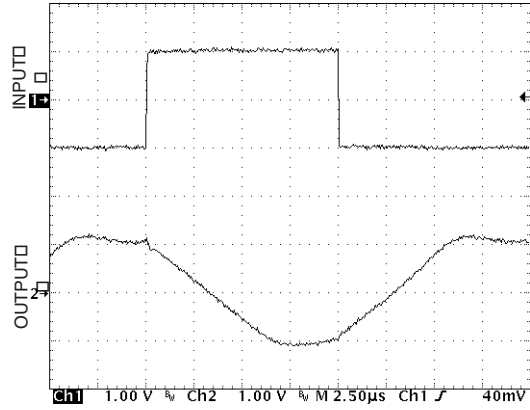


# Functional Characteristics

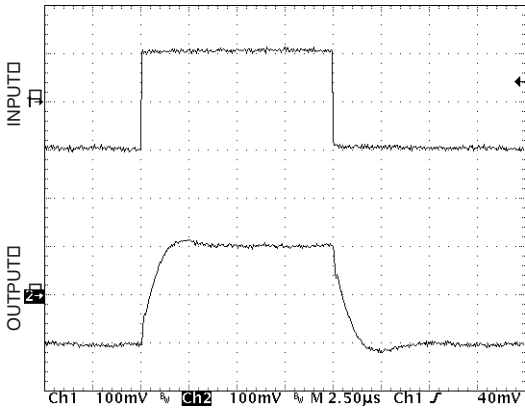
### Inverting Small-Signal Pulse Response



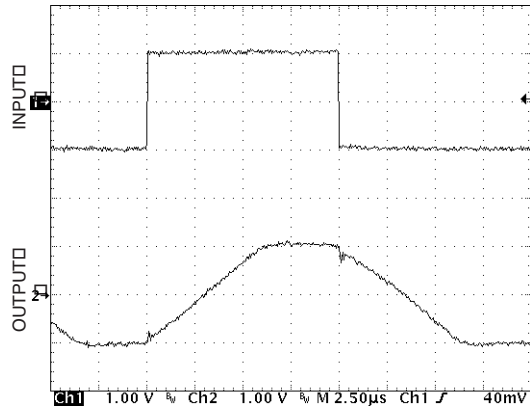
### Inverting Large-Signal Pulse Response



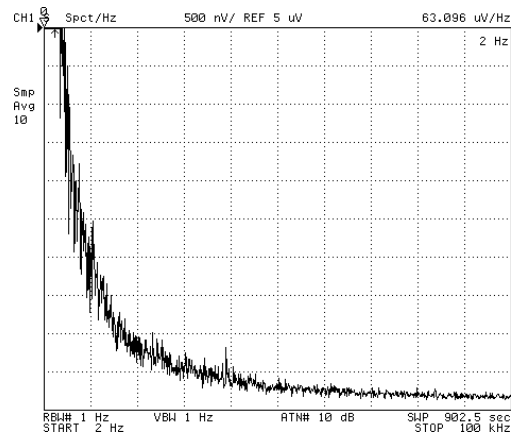
### Noninverting Small-Signal Pulse Response



### Noninverting Large-Signal Pulse Response



### Input Voltage Noise vs. Frequency



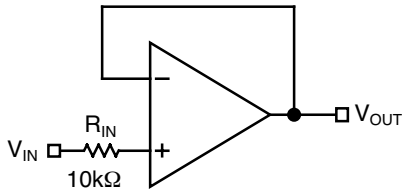


## Application Information

### Input Common-Mode Voltage

Some amplifiers exhibit undesirable or unpredictable performance when the inputs are driven beyond the common-mode voltage range, for example, phase inversion of the output signal. The LMC7101 tolerates input overdrive by at least 200mV beyond either rail without producing phase inversion.

If the absolute maximum input voltage (700mV beyond either rail) is exceeded, the input current should be limited to  $\pm 5\text{mA}$  maximum to prevent reducing reliability. A  $10\text{k}\Omega$  series input resistor, used as a current limiter, will protect the input structure from voltages as large as 50V above the supply or below ground. See Figure 1.



**Figure 1. Input Current-Limit Protection**

### Output Voltage Swing

Sink and source output resistances of the LMC7101 are equal. Maximum output voltage swing is determined by the load and the approximate output resistance. The output resistance is:

$$R_{\text{OUT}} = \frac{V_{\text{DROP}}}{I_{\text{LOAD}}}$$

$V_{\text{DROP}}$  is the voltage dropped within the amplifier output stage.  $V_{\text{DROP}}$  and  $I_{\text{LOAD}}$  can be determined from the  $V_{\text{O}}$  (output swing) portion of the appropriate Electrical Characteristics table.  $I_{\text{LOAD}}$  is equal to the typical output high voltage minus  $V_{+}/2$  and divided by  $R_{\text{LOAD}}$ . For example, using the Electrical Characteristics DC (5V) table, the typical output high voltage using a  $2\text{k}\Omega$  load (connected to  $V_{+}/2$ ) is 4.989V, which produces an  $I_{\text{LOAD}}$  of

$$1.245\text{mA} \left( \frac{4.989\text{V} - 2.5\text{V}}{2\text{k}\Omega} \right) = 1.245\text{mA}$$

Voltage drop in the amplifier output stage is:

$$V_{\text{DROP}} = 5.0\text{V} - 4.989\text{V}$$

$$V_{\text{DROP}} = 0.011\text{V}$$

Because of output stage symmetry, the corresponding typical output low voltage (0.011V) also equals  $V_{\text{DROP}}$ . Then:

$$R_{\text{OUT}} = \frac{0.011\text{V}}{0.001245\text{A}} = 8.8 \approx 9\Omega$$

### Driving Capacitive Loads

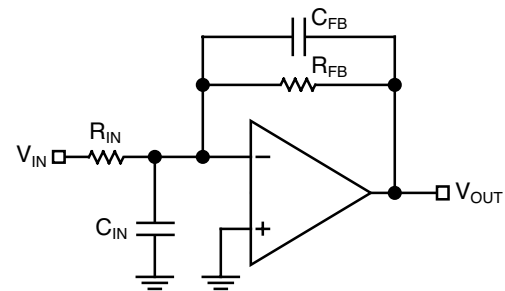
Driving a capacitive load introduces phase-lag into the output signal, and this in turn reduces op-amp system phase margin. The application that is least forgiving of reduced phase margin is a unity gain amplifier. The LMC7101 can typically drive a 100pF capacitive load connected directly to the output when configured as a unity-gain amplifier.

### Using Large-Value Feedback Resistors

A large-value feedback resistor ( $> 500\text{k}\Omega$ ) can reduce the phase margin of a system. This occurs when the feedback resistor acts in conjunction with input capacitance to create phase lag in the feedback signal. Input capacitance is usually a combination of input circuit components and other parasitic capacitance, such as amplifier input capacitance and stray printed circuit board capacitance.

Figure 2 illustrates a method of compensating phase lag caused by using a large-value feedback resistor. Feedback capacitor  $C_{\text{FB}}$  introduces sufficient phase lead to overcome the phase lag caused by feedback resistor  $R_{\text{FB}}$  and input capacitance  $C_{\text{IN}}$ . The value of  $C_{\text{FB}}$  is determined by first estimating  $C_{\text{IN}}$  and then applying the following formula:

$$R_{\text{IN}} \times C_{\text{IN}} \leq R_{\text{FB}} \times C_{\text{FB}}$$

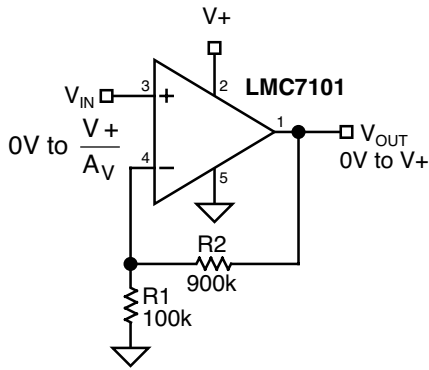


**Figure 2. Cancelling Feedback Phase Lag**

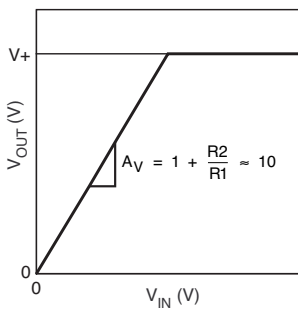
Since a significant percentage of  $C_{\text{IN}}$  may be caused by board layout, it is important to note that the correct value of  $C_{\text{FB}}$  may change when changing from a breadboard to the final circuit layout.

**Typical Circuits**

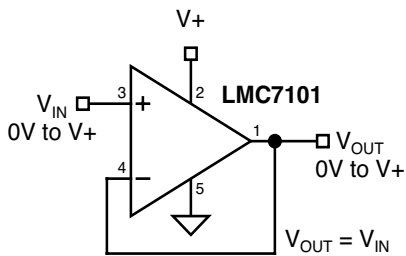
Some single-supply, rail-to-rail applications for which the LMC7101 is well suited are shown in the circuit diagrams of Figures 3 through 7.



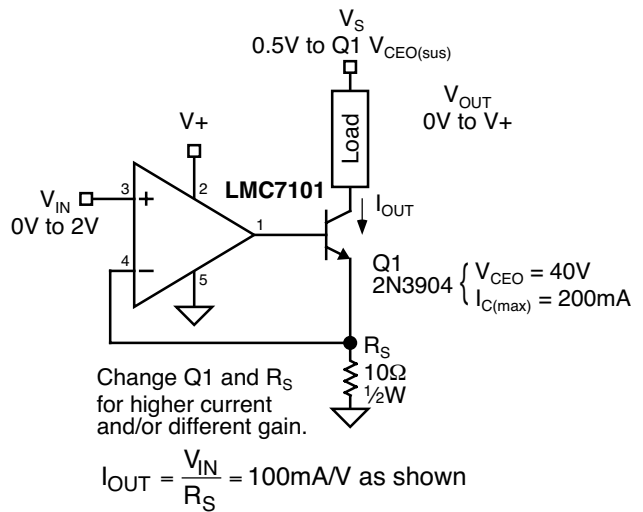
**Figure 3a. Noninverting Amplifier**



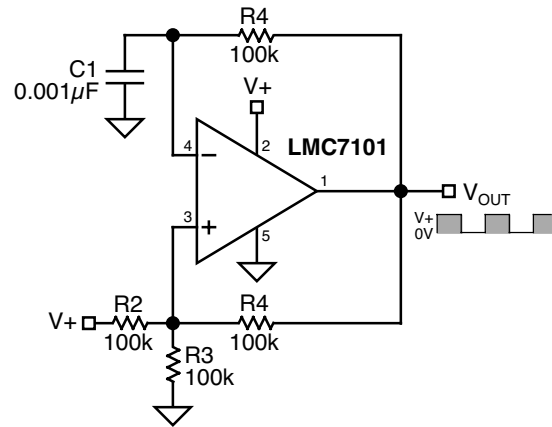
**Figure 3b. Noninverting Amplifier Behavior**



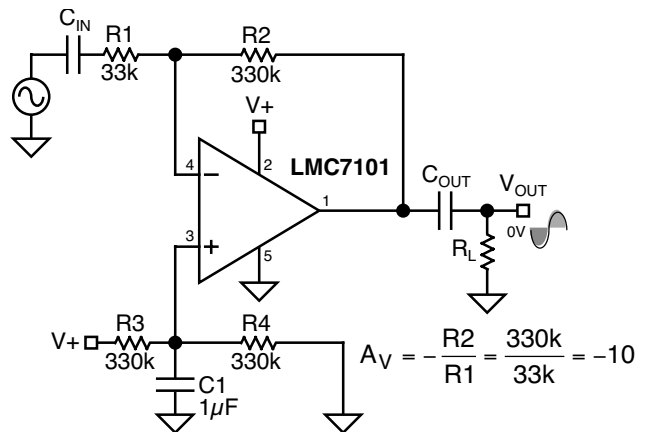
**Figure 4. Voltage Follower**



**Figure 5. Voltage-Controlled Current Sink**

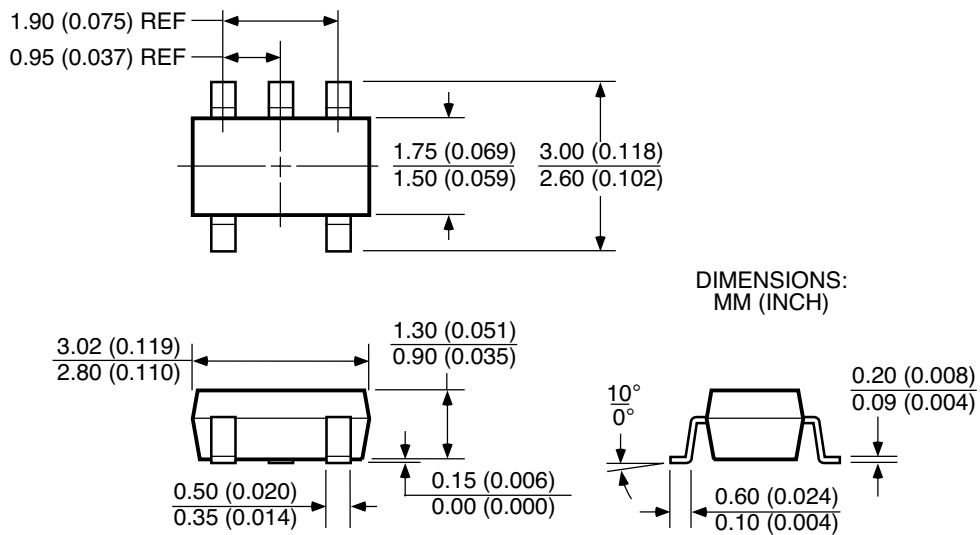


**Figure 6. Square Wave Oscillator**



**Figure 7. AC-Coupled Inverting Amplifier**

Package Information



SOT-23-5 (M5)

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