LPC2131/32/34/36/38

Single-chip 16/32-bit microcontrollers; 32/64/128/256/512 kB ISP/IAP flash with 10-bit ADC and DAC

Rev. 04 — 16 October 2007 Product data sheet

1. General description

The LPC2131/32/34/36/38 microcontrollers are based on a 16/32-bit ARM7TDMI-S CPU with real-time emulation and embedded trace support, that combine the microcontroller with 32 kB, 64 kB, 128 kB, 256 kB and 512 kB of embedded high-speed flash memory. A 128-bit wide memory interface and a unique accelerator architecture enable 32-bit code execution at maximum clock rate. For critical code size applications, the alternative 16-bit Thumb mode reduces code by more than 30 % with minimal performance penalty.

Due to their tiny size and low power consumption, these microcontrollers are ideal for applications where miniaturization is a key requirement, such as access control and point-of-sale. With a wide range of serial communications interfaces and on-chip SRAM options of 8 kB, 16 kB, and 32 kB, they are very well suited for communication gateways and protocol converters, soft modems, voice recognition and low-end imaging, providing both large buffer size and high processing power. Various 32-bit timers, single or dual 10-bit 8-channel ADC(s), 10-bit DAC, PWM channels and 47 GPIO lines with up to nine edge or level sensitive external interrupt pins make these microcontrollers particularly suitable for industrial control and medical systems.

2. Features

2.1 Enhancements brought by LPC213x/01 devices

- Fast GPIO ports enable port pin toggling up to 3.5 times faster than the original LPC213x. They also allow for a port pin to be read at any time regardless of its function.
- Dedicated result registers for ADC(s) reduce interrupt overhead.
- UART0/1 include fractional baud rate generator, auto-bauding capabilities and handshake flow-control fully implemented in hardware.
- Additional BOD control enables further reduction of power consumption.

2.2 Key features common for LPC213x and LPC213x/01

- 16/32-bit ARM7TDMI-S microcontroller in a tiny LQFP64 or HVQFN package.
- 8/16/32 kB of on-chip static RAM and 32/64/128/256/512 kB of on-chip flash program memory. 128-bit wide interface/accelerator enables high-speed 60 MHz operation.
- In-System Programming/In-Application Programming (ISP/IAP) via on-chip bootloader software. Single flash sector or full chip erase in 400 ms and programming of 256 B in 1 ms.
- EmbeddedICE RT and Embedded Trace interfaces offer real-time debugging with the on-chip RealMonitor software and high-speed tracing of instruction execution.

- One (LPC2131/32) or two (LPC2134/36/38) 8-channel 10-bit ADCs provide a total of up to 16 analog inputs, with conversion times as low as 2.44 µs per channel.
- Single 10-bit DAC provides variable analog output (LPC2132/34/36/38).
- Two 32-bit timers/external event counters (with four capture and four compare channels each), PWM unit (six outputs) and watchdog.
- Low power Real-time clock with independent power and dedicated 32 kHz clock input.
- Multiple serial interfaces including two UARTs (16C550), two Fast I^2C-bus (400 kbit/s), SPI and SSP with buffering and variable data length capabilities.
- Vectored interrupt controller with configurable priorities and vector addresses.
- Up to forty-seven 5 V tolerant general purpose I/O pins in tiny LQFP64 or HVQFN package.
- Up to nine edge or level sensitive external interrupt pins available.
- 60 MHz maximum CPU clock available from programmable on-chip PLL with settling time of 100 µs.
- On-chip integrated oscillator operates with external crystal in range of 1 MHz to 30 MHz and with external oscillator up to 50 MHz.
- Power saving modes include Idle and Power-down.
- Individual enable/disable of peripheral functions as well as peripheral clock scaling down for additional power optimization.
- Processor wake-up from Power-down mode via external interrupt or BOD.
- Single power supply chip with POR and BOD circuits:
  - CPU operating voltage range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2131FBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2131FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2132FBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2132FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2132FHN64	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-2
LPC2132FHN64/01	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-2
LPC2134FBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2134FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

Table 1. Ordering information *...continued*

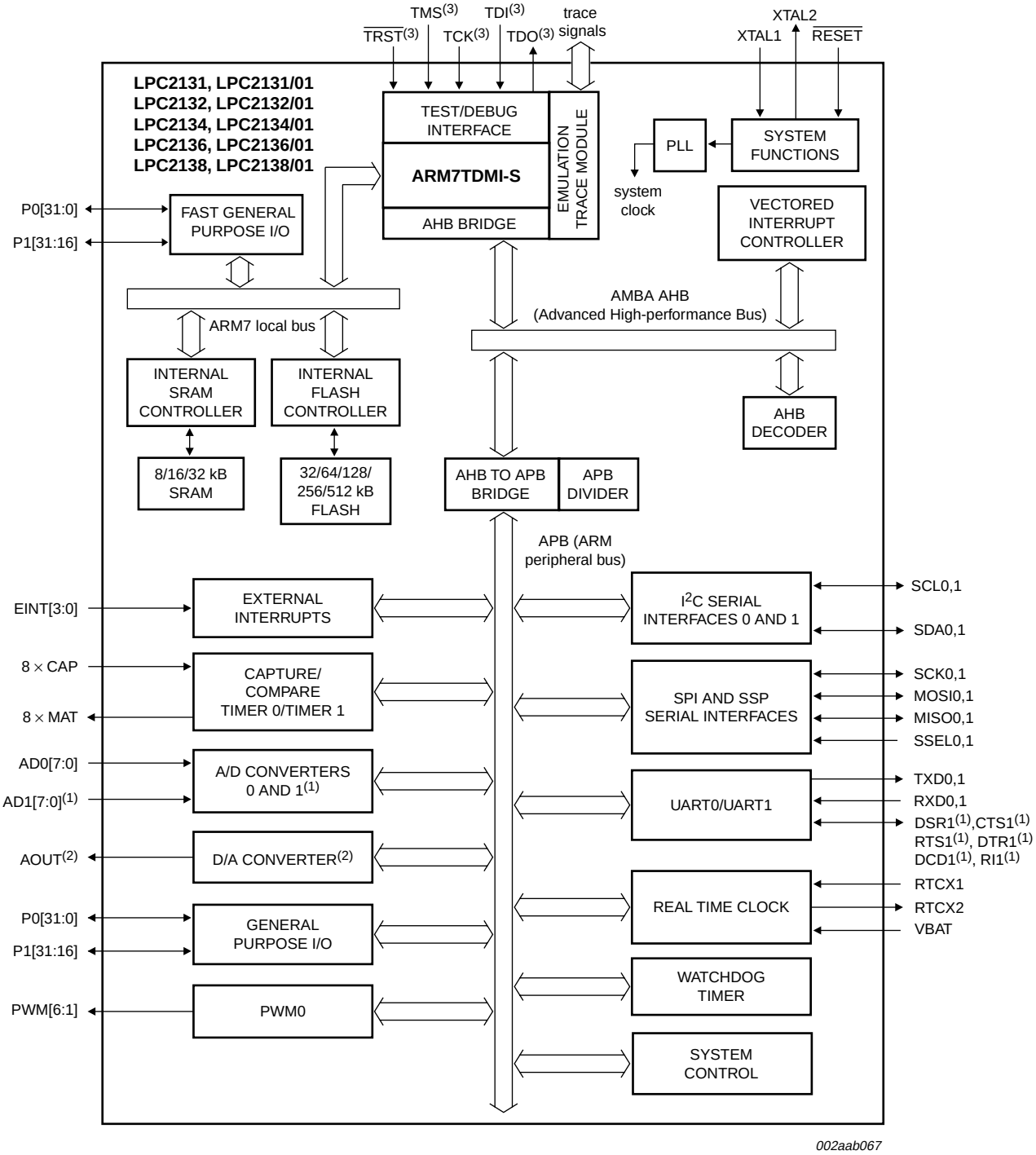
Type number	Package		
	Name	Description	Version
LPC2136FBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2136FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2138FBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2138FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2138FHN64	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-2
LPC2138FHN64/01	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-2

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	RAM	ADC	DAC	Enhanced UARTs, ADC, Fast I/Os, and BOD	Temperature range
LPC2131FBD64	32 kB	8 kB	1	-	no	–40 °C to +85 °C
LPC2131FBD64/01	32 kB	8 kB	1	-	yes	–40 °C to +85 °C
LPC2132FBD64	64 kB	16 kB	1	1	no	–40 °C to +85 °C
LPC2132FBD64/01	64 kB	16 kB	1	1	yes	–40 °C to +85 °C
LPC2132FHN64	64 kB	16 kB	1	1	no	–40 °C to +85 °C
LPC2132FHN64/01	64 kB	16 kB	1	1	yes	–40 °C to +85 °C
LPC2134FBD64	128 kB	16 kB	2	1	no	–40 °C to +85 °C
LPC2134FBD64/01	128 kB	16 kB	2	1	yes	–40 °C to +85 °C
LPC2136FBD64	256 kB	32 kB	2	1	no	–40 °C to +85 °C
LPC2136FBD64/01	256 kB	32 kB	2	1	yes	–40 °C to +85 °C
LPC2138FBD64	512 kB	32 kB	2	1	no	–40 °C to +85 °C
LPC2138FBD64/01	512 kB	32 kB	2	1	yes	–40 °C to +85 °C
LPC2138FHN64	512 kB	32 kB	2	1	no	–40 °C to +85 °C
LPC2138FHN64/01	512 kB	32 kB	2	1	yes	–40 °C to +85 °C

4. Block diagram



(1) LPC2134/36/38 only.

(2) LPC2132/34/36/38 only.

(3) Pins shared with GPIO.

Fig 1. Block diagram

5. Pinning information

5.1 Pinning

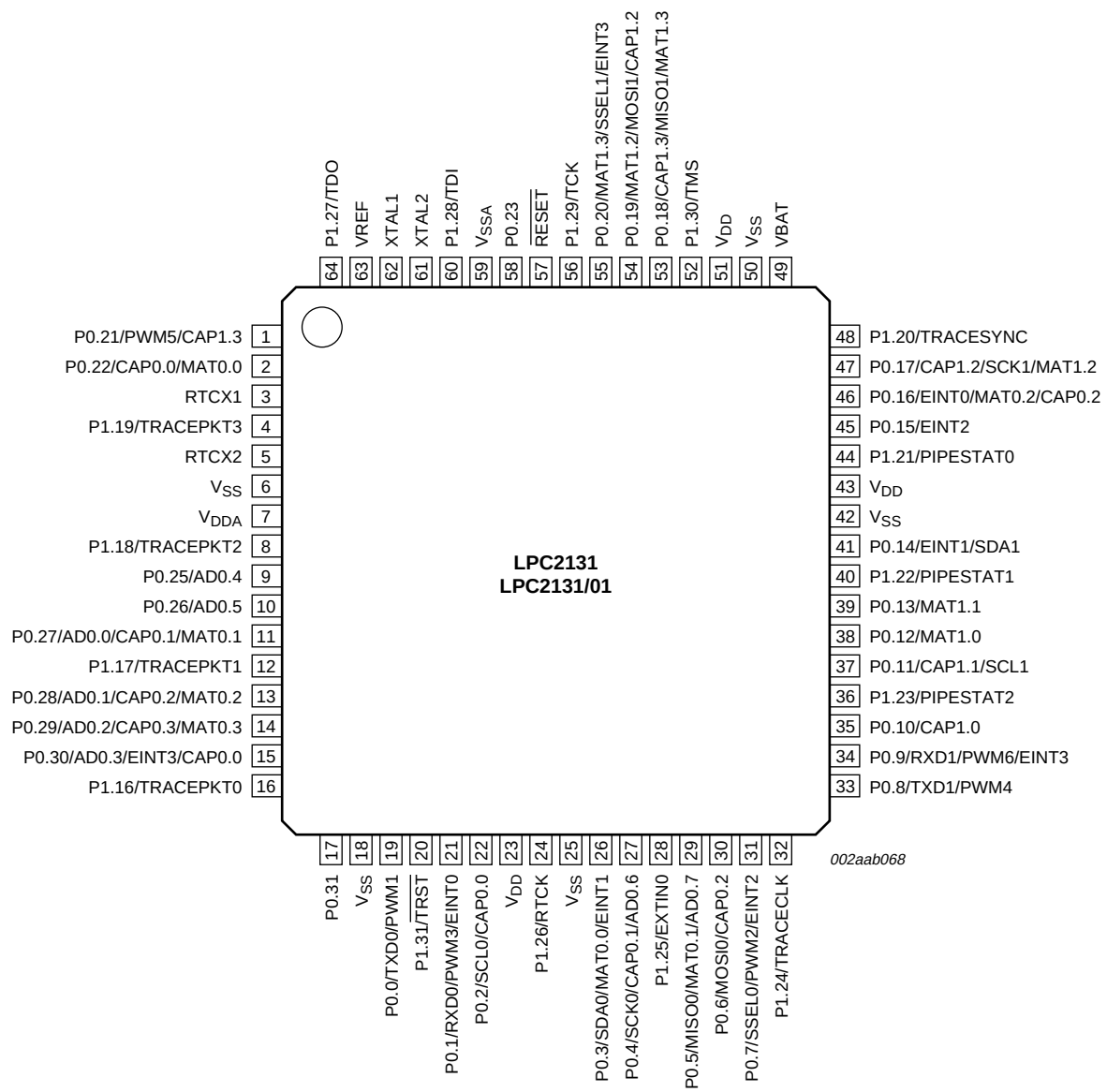


Fig 2. LPC2131 LQFP64 pinning

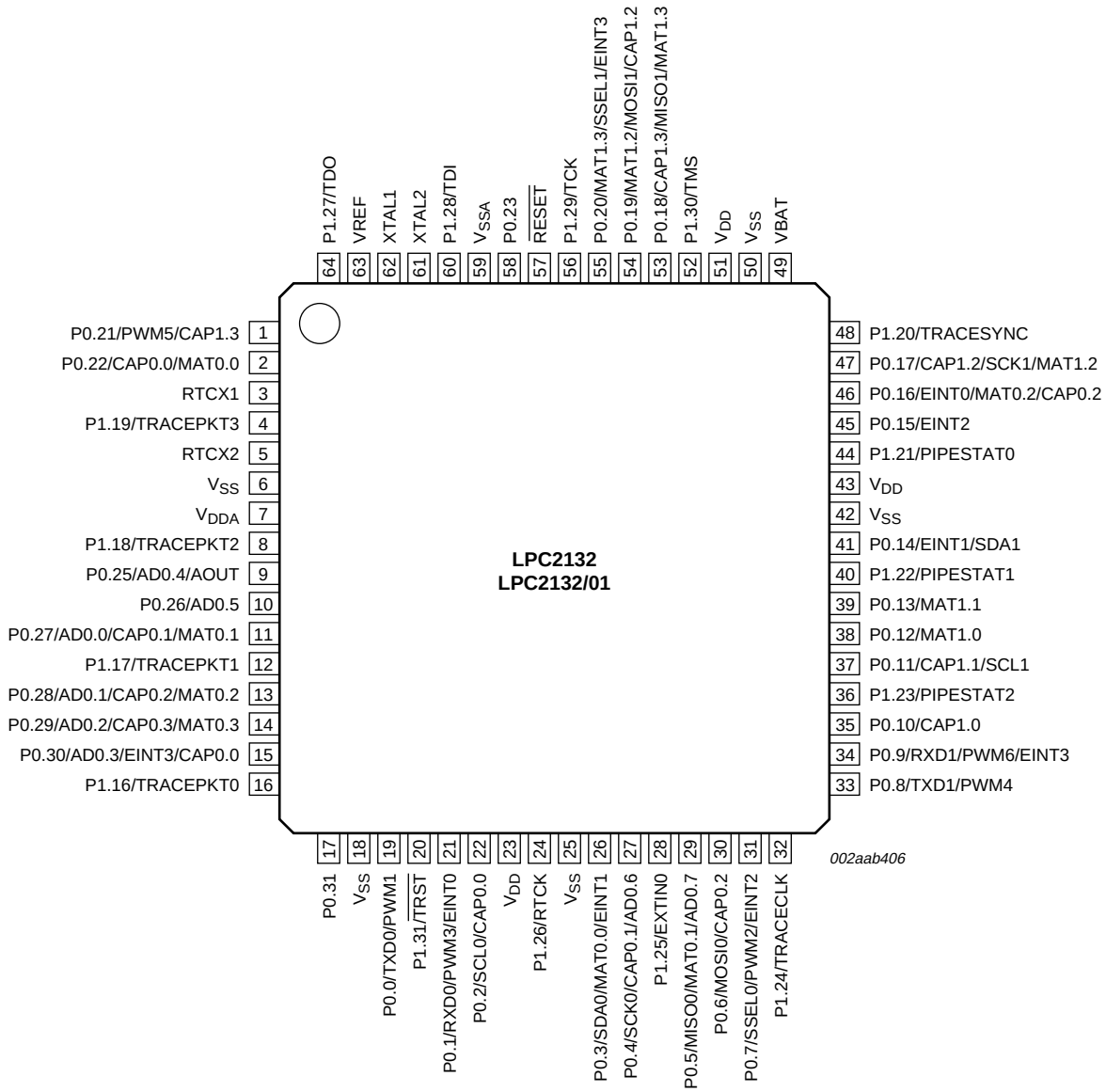


Fig 3. LPC2132 LQFP64 pin configuration

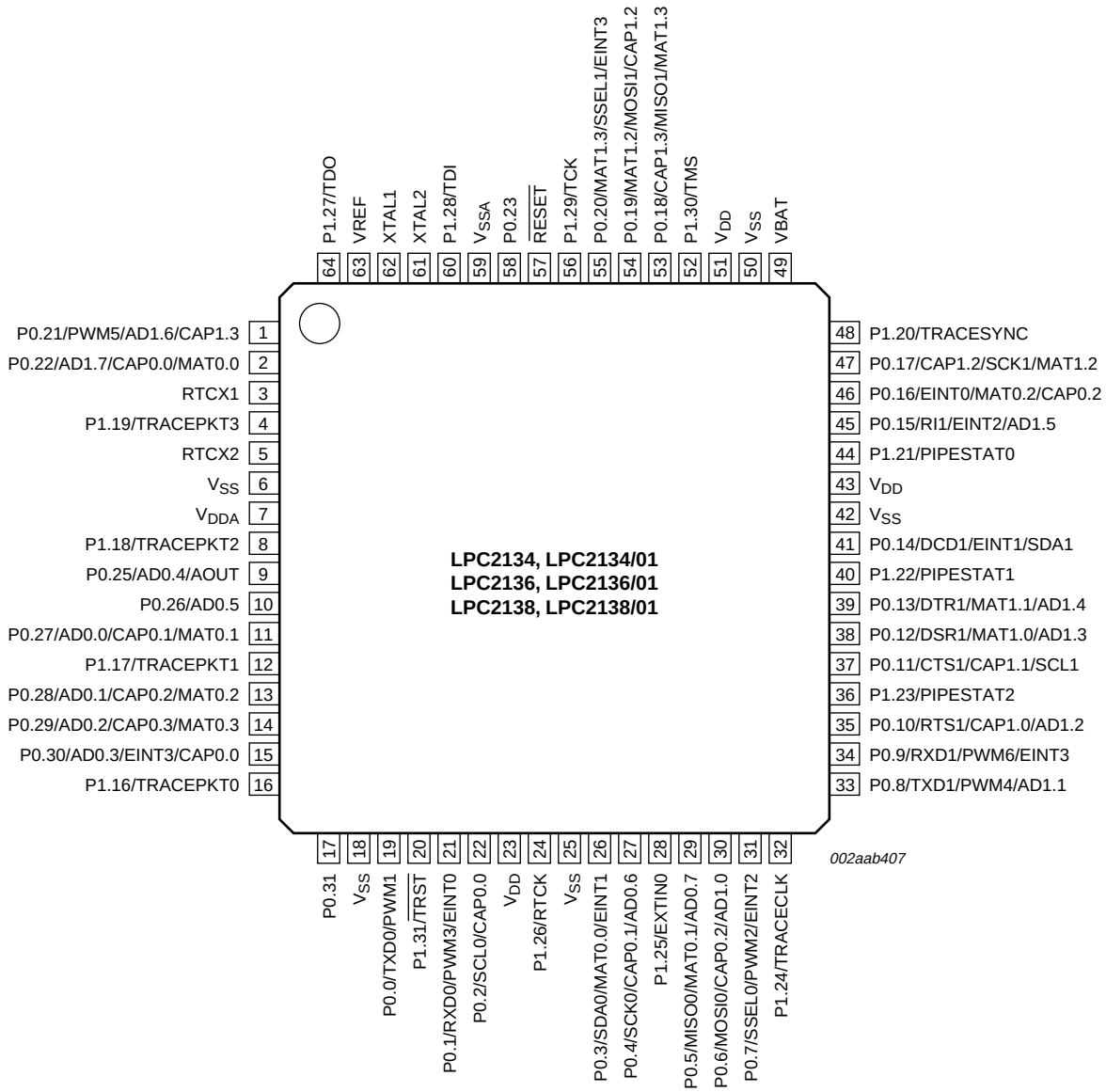
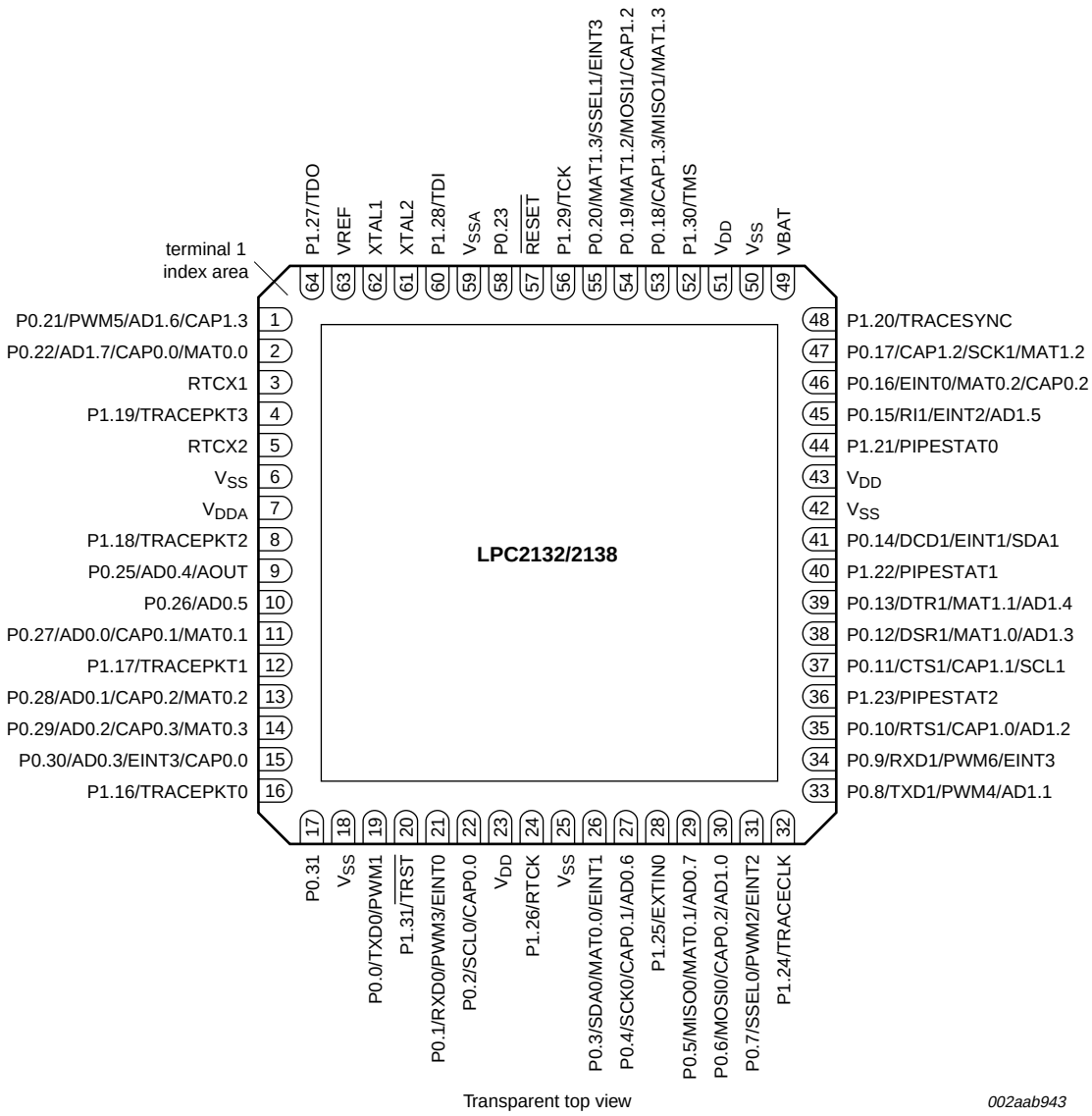


Fig 4. LPC2134/36/38 LQFP64 pin configuration



AD1.7 to AD1.0 only available on LPC2134/36/38.

Fig 5. LPC2132/38 HVQFN64 pin configuration

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0.0 to P0.31		I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. Total of 31 pins of the Port 0 can be used as a general purpose bidirectional digital I/Os while P0.31 is output only pin. The operation of port 0 pins depends upon the pin function selected via the pin connect block. Pin P0.24 is not available.
P0.0/TXD0/ PWM1	19[1]	O	**TXD0 —** Transmitter output for UART0.
		O	**PWM1 —** Pulse Width Modulator output 1.
P0.1/RXD0/ PWM3/EINT0	21[2]	I	**RXD0 —** Receiver input for UART0.
		O	**PWM3 —** Pulse Width Modulator output 3.
		I	**EINT0 —** External interrupt 0 input.
P0.2/SCL0/ CAP0.0	22[3]	I/O	**SCL0 —** I^2C0 clock input/output. Open drain output (for I^2C-bus compliance).
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.3/SDA0/ MAT0.0/EINT1	26[3]	I/O	**SDA0 —** I^2C0 data input/output. Open drain output (for I^2C-bus compliance).
		O	**MAT0.0 —** Match output for Timer 0, channel 0.
		I	**EINT1 —** External interrupt 1 input.
P0.4/SCK0/ CAP0.1/AD0.6	27[4]	I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
		I	**CAP0.1 —** Capture input for Timer 0, channel 1.
		I	**AD0.6 —** ADC 0, input 6. This analog input is always connected to its pin.
P0.5/MISO0/ MAT0.1/AD0.7	29[4]	I/O	**MISO0 —** Master In Slave V_{DD} = 3.6 V for SPI0. Data input to SPI master or data output from SPI slave.
		O	**MAT0.1 —** Match output for Timer 0, channel 1.
		I	**AD0.7 —** ADC 0, input 7. This analog input is always connected to its pin.
P0.6/MOSI0/ CAP0.2/AD1.0	30[4]	I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
		I	**AD1.0 —** ADC 1, input 0. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
P0.7/SSEL0/ PWM2/EINT2	31[2]	I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
		O	**PWM2 —** Pulse Width Modulator output 2.
		I	**EINT2 —** External interrupt 2 input.
P0.8/TXD1/ PWM4/AD1.1	33[4]	O	**TXD1 —** Transmitter output for UART1.
		O	**PWM4 —** Pulse Width Modulator output 4.
		I	**AD1.1 —** ADC 1, input 1. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
P0.9/RXD1/ PWM6/EINT3	34[2]	I	**RXD1 —** Receiver input for UART1.
		O	**PWM6 —** Pulse Width Modulator output 6.
		I	**EINT3 —** External interrupt 3 input.
P0.10/RTS1/ CAP1.0/AD1.2	35[4]	O	**RTS1 —** Request to Send output for UART1. Available in LPC2134/36/38.
		I	**CAP1.0 —** Capture input for Timer 1, channel 0.
		I	**AD1.2 —** ADC 1, input 2. This analog input is always connected to its pin. Available in LPC2134/36/38 only.

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
P0.11/CTS1/ CAP1.1/SCL1	37[3]	I	**CTS1 —** Clear to Send input for UART1. Available in LPC2134/36/38.
		I	**CAP1.1 —** Capture input for Timer 1, channel 1.
		I/O	**SCL1 —** I^2C1 clock input/output. Open drain output (for I^2C-bus compliance)
P0.12/DSR1/ MAT1.0/AD1.3	38[4]	I	**DSR1 —** Data Set Ready input for UART1. Available in LPC2134/36/38.
		O	**MAT1.0 —** Match output for Timer 1, channel 0.
		I	**AD1.3 —** ADC 1, input 3. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
P0.13/DTR1/ MAT1.1/AD1.4	39[4]	O	**DTR1 —** Data Terminal Ready output for UART1. Available in LPC2134/36/38.
		O	**MAT1.1 —** Match output for Timer 1, channel 1.
		I	**AD1.4 —** ADC 1, input 4. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
P0.14/DCD1/ EINT1/SDA1	41[3]	I	**DCD1 —** Data Carrier Detect input for UART1. Available in LPC2134/36/38.
		I	**EINT1 —** External interrupt 1 input.
		I/O	**SDA1 —** I^2C1 data input/output. Open drain output (for I^2C-bus compliance).
P0.15/RI1/ EINT2/AD1.5	45[4]	I	**RI1 —** Ring Indicator input for UART1. Available in LPC2134/36/38.
		I	**EINT2 —** External interrupt 2 input.
		I	**AD1.5 —** ADC 1, input 5. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
P0.16/EINT0/ MAT0.2/CAP0.2	46[2]	I	**EINT0 —** External interrupt 0 input.
		O	**MAT0.2 —** Match output for Timer 0, channel 2.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
P0.17/CAP1.2/ SCK1/MAT1.2	47[1]	I	**CAP1.2 —** Capture input for Timer 1, channel 2.
		I/O	**SCK1 —** Serial Clock for SSP. Clock output from master or input to slave.
		O	**MAT1.2 —** Match output for Timer 1, channel 2.
P0.18/CAP1.3/ MISO1/MAT1.3	53[1]	I	**CAP1.3 —** Capture input for Timer 1, channel 3.
		I/O	**MISO1 —** Master In Slave Out for SSP. Data input to SPI master or data output from SSP slave.
		O	**MAT1.3 —** Match output for Timer 1, channel 3.
P0.19/MAT1.2/ MOSI1/CAP1.2	54[1]	O	**MAT1.2 —** Match output for Timer 1, channel 2.
		I/O	**MOSI1 —** Master Out Slave In for SSP. Data output from SSP master or data input to SSP slave.
		I	**CAP1.2 —** Capture input for Timer 1, channel 2.
P0.20/MAT1.3/ SSEL1/EINT3	55[2]	O	**MAT1.3 —** Match output for Timer 1, channel 3.
		I	**SSEL1 —** Slave Select for SSP. Selects the SSP interface as a slave.
		I	**EINT3 —** External interrupt 3 input.
P0.21/PWM5/ AD1.6/CAP1.3	1[4]	O	**PWM5 —** Pulse Width Modulator output 5.
		I	**AD1.6 —** ADC 1, input 6. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
		I	**CAP1.3 —** Capture input for Timer 1, channel 3.

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
P0.22/AD1.7/ CAP0.0/MAT0.0	2[4]	I	**AD1.7 —** ADC 1, input 7. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
		O	**MAT0.0 —** Match output for Timer 0, channel 0.
P0.23	58[1]	I/O	General purpose digital input/output pin.
P0.25/AD0.4/ AOUT	9[5]	I	**AD0.4 —** ADC 0, input 4. This analog input is always connected to its pin.
		O	**AOUT —** DAC output. Not available in LPC2131.
P0.26/AD0.5	10[4]	I	**AD0.5 —** ADC 0, input 5. This analog input is always connected to its pin.
P0.27/AD0.0/ CAP0.1/MAT0.1	11[4]	I	**AD0.0 —** ADC 0, input 0. This analog input is always connected to its pin.
		I	**CAP0.1 —** Capture input for Timer 0, channel 1.
		O	**MAT0.1 —** Match output for Timer 0, channel 1.
P0.28/AD0.1/ CAP0.2/MAT0.2	13[4]	I	**AD0.1 —** ADC 0, input 1. This analog input is always connected to its pin.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
		O	**MAT0.2 —** Match output for Timer 0, channel 2.
P0.29/AD0.2/ CAP0.3/MAT0.3	14[4]	I	**AD0.2 —** ADC 0, input 2. This analog input is always connected to its pin.
		I	**CAP0.3 —** Capture input for Timer 0, channel 3.
		O	**MAT0.3 —** Match output for Timer 0, channel 3.
P0.30/AD0.3/ EINT3/CAP0.0	15[4]	I	**AD0.3 —** ADC 0, input 3. This analog input is always connected to its pin.
		I	**EINT3 —** External interrupt 3 input.
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.31	17[6]	O	General purpose digital output only pin. **Important:** This pin MUST NOT be externally pulled LOW when $\overline{\text{RESET}}$ pin is LOW or the JTAG port will be disabled.
P1.0 to P1.31		I/O	**Port 1:** Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block. Pins 0 through 15 of port 1 are not available.
P1.16/ TRACEPKT0	16[6]	O	**TRACEPKT0 —** Trace Packet, bit 0. Standard I/O port with internal pull-up.
P1.17/ TRACEPKT1	12[6]	O	**TRACEPKT1 —** Trace Packet, bit 1. Standard I/O port with internal pull-up.
P1.18/ TRACEPKT2	8[6]	O	**TRACEPKT2 —** Trace Packet, bit 2. Standard I/O port with internal pull-up.
P1.19/ TRACEPKT3	4[6]	O	**TRACEPKT3 —** Trace Packet, bit 3. Standard I/O port with internal pull-up.
P1.20/ TRACESYNC	48[6]	O	**TRACESYNC —** Trace Synchronization. Standard I/O port with internal pull-up. LOW on TRACESYNC while $\overline{\text{RESET}}$ is LOW enables pins P1.25:16 to operate as Trace port after reset.
P1.21/ PIPESTAT0	44[6]	O	**PIPESTAT0 —** Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P1.22/ PIPESTAT1	40[6]	O	**PIPESTAT1 —** Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P1.23/ PIPESTAT2	36[6]	O	**PIPESTAT2 —** Pipeline Status, bit 2. Standard I/O port with internal pull-up.

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
P1.24/ TRACECLK	32[6]	O	**TRACECLK —** Trace Clock. Standard I/O port with internal pull-up.
P1.25/EXTIN0	28[6]	I	**EXTIN0 —** External Trigger Input. Standard I/O with internal pull-up.
P1.26/RTCK	24[6]	I/O	**RTCK —** Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. LOW on RTCK while $\overline{\text{RESET}}$ is LOW enables pins P1.31:26 to operate as Debug port after reset.
P1.27/TDO	64[6]	O	**TDO —** Test Data out for JTAG interface.
P1.28/TDI	60[6]	I	**TDI —** Test Data in for JTAG interface.
P1.29/TCK	56[6]	I	**TCK —** Test Clock for JTAG interface.
P1.30/TMS	52[6]	I	**TMS —** Test Mode Select for JTAG interface.
P1.31/$\overline{\text{TRST}}$	20[6]	I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
$\overline{\text{RESET}}$	57[7]	I	**External reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	62[8]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	61[8]	O	Output from the oscillator amplifier.
RTCX1	3[8]	I	Input to the RTC oscillator circuit.
RTCX2	5[8]	O	Output from the RTC oscillator circuit.
V_{SS}	6, 18, 25, 42, 50	I	**Ground:** 0 V reference.
V_{SSA}	59	I	**Analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
V_{DD}	23, 43, 51	I	**3.3 V power supply:** This is the power supply voltage for the core and I/O ports.
V_{DDA}	7	I	**Analog 3.3 V power supply:** This should be nominally the same voltage as V_{DD} but should be isolated to minimize noise and error. This voltage is used to power the on-chip PLL.
VREF	63	I	**ADC reference:** This should be nominally the same voltage as V_{DD} but should be isolated to minimize noise and error. Level on this pin is used as a reference for A/D and D/A convertor(s).
VBAT	49	I	**RTC power supply:** 3.3 V on this pin supplies the power to the RTC.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control.

[2] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns.

[3] Open drain 5 V tolerant digital I/O I^2C-bus 400 kHz specification compatible pad. It requires external pull-up to provide an output functionality.

[4] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog input function. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns. When configured as an ADC input, digital section of the pad is disabled.

[5] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[6] 5 V tolerant pad with built-in pull-up resistor providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. The pull-up resistor's value ranges from 60 kΩ to 300 kΩ.

[7] 5 V tolerant pad providing digital input (with TTL levels and hysteresis) function only.

[8] Pad provides special analog functionality.

6. Functional description

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

6.2 On-chip flash program memory

The LPC2131/32/34/36/38 incorporate a 32 kB, 64 kB, 128 kB, 256 kB and 512 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. When the LPC2131/32/34/36/38 on-chip bootloader is used, 32/64/128/256/500 kB of flash memory is available for user code.

The LPC2131/32/34/36/38 flash memory provides a minimum of 100000 erase/write cycles and 20 years of data-retention.

6.3 On-chip static RAM

On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8-bit, 16-bit, and 32-bit. The LPC2131, LPC2132/34, and LPC2136/38 provide 8 kB, 16 kB and 32 kB of static RAM respectively.

6.4 Memory map

The LPC2131/32/34/36/38 memory map incorporates several distinct regions, as shown in Figure 6.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in Section 6.18 “System control”.

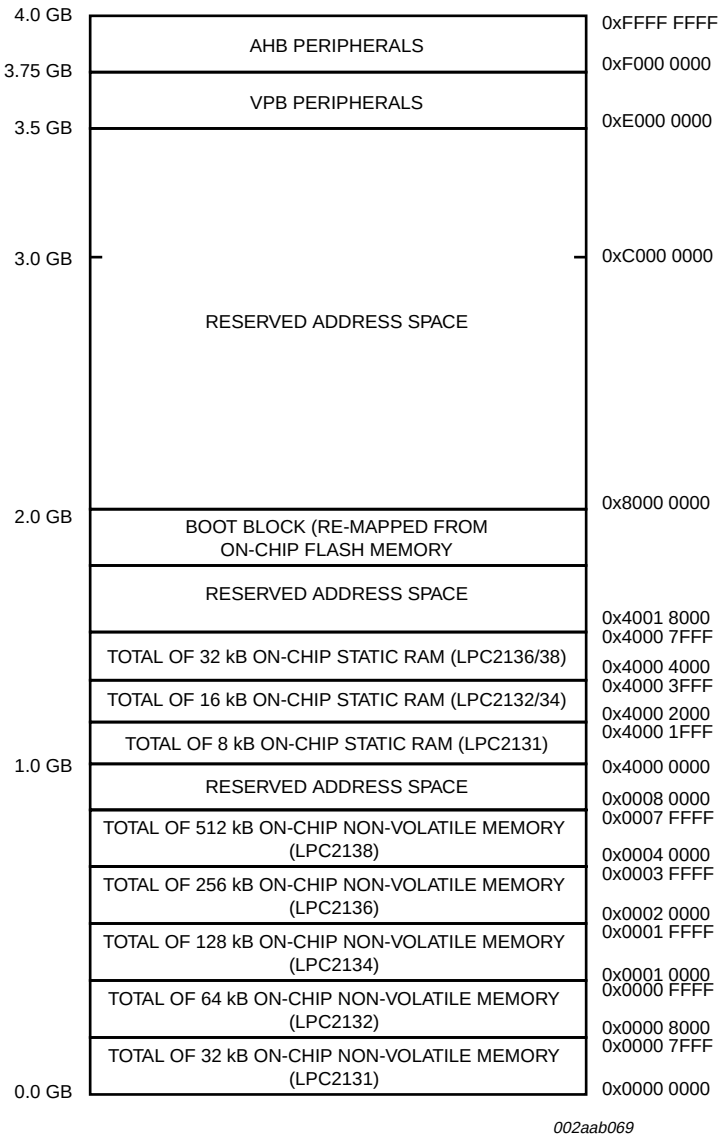


Fig 6. LPC2131/32/34/36/38 memory map

6.5 Interrupt controller

The Vectored Interrupt Controller (VIC) accepts all of the interrupt request inputs and categorizes them as Fast Interrupt Request (FIQ), vectored Interrupt Request (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are requesting, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.5.1 Interrupt sources

Table 4 lists the interrupt sources for each peripheral function. Each peripheral device has one interrupt line connected to the Vectored Interrupt Controller, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Table 4. Interrupt sources

Block	Flag(s)	VIC channel #
WDT	Watchdog Interrupt (WDINT)	0
-	Reserved for software interrupts only	1
ARM Core	EmbeddedICE, DbgCommRX	2
ARM Core	EmbeddedICE, DbgCommTX	3
TIMER0	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	4
TIMER1	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	5
UART0	RX Line Status (RLS) Transmit Holding Register empty (THRE) RX Data Available (RDA) Character Time-out Indicator (CTI)	6

Table 4. Interrupt sources *...continued*

Block	Flag(s)	VIC channel #
UART1	RX Line Status (RLS)	7
	Transmit Holding Register empty (THRE)	
	RX Data Available (RDA)	
	Character Time-out Indicator (CTI)	
	Modem Status Interrupt (MSI) (Available in LPC2134/36/38 only)	
PWM0	Match 0 to 6 (MR0, MR1, MR2, MR3, MR4, MR5, MR6)	8
	Capture 0 to 3 (CR0, CR1, CR2, CR3)	
I^2C0	SI (state change)	9
SPI0	SPIF, MODF	10
SSP	TX FIFO at least half empty (TXRIS)	11
	RX FIFO at least half full (RXRIS)	
	Receive Timeout (RTRIS)	
	Receive Overrun (RORRIS)	
PLL	PLL Lock (PLOCK)	12
RTC	RTCCIF (Counter Increment), RTCALF (Alarm)	13
System Control	External Interrupt 0 (EINT0)	14
	External Interrupt 1 (EINT1)	15
	External Interrupt 2 (EINT2)	16
	External Interrupt 3 (EINT3)	17
AD0	ADC 0	18
I2C1	SI (state change)	19
BOD	Brown Out Detect	20
AD1	ADC 1 (Available in LPC2134/36/38 only)	21

6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

6.7 General purpose parallel I/O and Fast I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

6.7.1 Features

- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.7.2 Fast I/O features available in LPC213x/01 only

- Fast I/O registers are located on the ARM local bus for the fastest possible I/O timing.
- All GPIO registers are byte addressable.
- Entire port value can be written in one instruction.
- Mask registers allow single instruction to set or clear any number of bits in one port.

6.8 10-bit ADC

The LPC2131/32 contain one and the LPC2134/36/38 contain two ADCs. These converters are single 10-bit successive approximation ADCs with eight multiplexed channels.

6.8.1 Features

- Measurement range of 0 V to 3.3 V.
- Each converter capable of performing more than 400000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.
- Global Start command for both converters (LPC2134/36/38 only).

6.8.2 ADC features available in LPC213x/01 only

- Every analog input has a dedicated result register to reduce interrupt overhead.
- Every analog input can generate an interrupt once the conversion is completed.

6.9 10-bit DAC

This peripheral is available in the LPC2132/34/36/38 only. The DAC enables the LPC2132/34/36/38 to generate variable analog output.

6.9.1 Features

- 10-bit digital to analog converter.
- Buffered output.
- Power-down mode available.
- Selectable speed versus power.

6.10 UARTs

The LPC2131/32/34/36/38 each contain two UARTs. In addition to standard transmit and receive data lines, the LPC2134/36/38 UART1 also provides a full modem control handshake interface.

6.10.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B

- Built-in baud rate generator.
- Standard modem interface signals included on UART1. (LPC2134/36/38 only)
- The LPC2131/32/34/36/38 transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs and hardware (CTS/RTS) flow control on the LPC2134/36/38 UART1 only.

6.10.2 UART features available in LPC213x/01 only

- Fractional baud rate generator enables standard baud rates such as 115200 to be achieved with any crystal frequency above 2 MHz.
- Auto-bauding.
- Auto-CTS/RTS flow-control fully implemented in hardware (LPC2134/36/38 only).

6.11 I^2C-bus serial I/O controller

The LPC2131/32/34/36/38 each contain two I^2C-bus controllers.

The I^2C-bus is bidirectional, for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver or a transmitter with the capability to both receive and send information (such as memory)). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

This I^2C-bus implementation supports bit rates up to 400 kbit/s (Fast I^2C).

6.11.1 Features

- Standard I^2C compliant bus interface.
- Easy to configure as Master, Slave, or Master/Slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus may be used for test and diagnostic purposes.

6.12 SPI serial I/O controller

The LPC2131/32/34/36/38 each contain one SPI controller. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

6.12.1 Features

- Compliant with Serial Peripheral Interface (SPI) specification.
- Synchronous, Serial, Full Duplex, Communication.
- Combined SPI master and slave.
- Maximum data bit rate of one eighth of the input clock rate.

6.13 SSP serial I/O controller

The LPC2131/32/34/36/38 each contain one Serial Synchronous Port controller (SSP). The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. However, only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. Often only one of these data flows carries meaningful data.

6.13.1 Features

- Compatible with Motorola SPI, 4-wire TI SSI and National Semiconductor Microwire buses.
- Synchronous Serial Communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- Four bits to 16 bits per frame.

6.14 General purpose timers/external event counters

The Timer/Counter is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock, and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with ‘or’ and ‘and’, as well as ‘broadcast’ functions among them.

At any given time only one of peripheral’s capture inputs can be selected as an external event signal source, i.e., timer’s clock. The rate of external events that can be successfully counted is limited to PCLK/2. In this configuration, unused capture lines can be selected as regular timer capture inputs.

6.14.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.
- External Event Counter or timer operation.
- Four 32-bit capture channels per timer/counter that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.

- Stop timer on match with optional interrupt generation.
- Reset timer on match with optional interrupt generation.

- Four external outputs per timer/counter corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

6.15 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

6.15.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.16 Real-time clock

The Real-Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.16.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Can use either the RTC dedicated 32 kHz oscillator input or clock derived from the external crystal/oscillator input at XTAL1. Programmable Reference Clock Divider allows fine adjustment of the RTC.
- Dedicated power supply pin can be connected to a battery or the main 3.3 V.

6.17 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2131/32/34/36/38. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.17.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.

- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.

6.18 System control

6.18.1 Crystal oscillator

On-chip integrated oscillator operates with external crystal in range of 1 MHz to 30 MHz and with external oscillator up to 50 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.18.2 “PLL” for additional information.

6.18.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle.The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μs.

6.18.3 Reset and wake-up timer

Reset has two sources on the LPC2131/32/34/36/38: the $\overline{\text{RESET}}$ pin and watchdog reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the wake-up timer (see wake-up timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The wake-up timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up timer.

The wake-up timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

6.18.4 Brownout detector

The LPC2131/32/34/36/38 include 2-stage monitoring of the voltage on the V_{DD} pins. If this voltage falls below 2.9 V, the BOD asserts an interrupt signal to the Vectored Interrupt Controller. This signal can be enabled for interrupt; if not, software can monitor the signal by reading dedicated register.

The second stage of low-voltage detection asserts reset to inactivate the LPC2131/32/34/36/38 when the voltage on the V_{DD} pins falls below 2.6 V. This reset prevents alteration of the flash as operation of the various elements of the chip would otherwise become unreliable due to low voltage. The BOD circuit maintains this reset down below 1 V, at which point the POR circuitry maintains the overall reset.

Both the 2.9 V and 2.6 V thresholds include some hysteresis. In normal operation, this hysteresis allows the 2.9 V detection to reliably interrupt, or a regularly-executed event loop to sense the condition.

Features available only in LPC213x/01 parts include ability to put the BOD in power-down mode, turn it on or off and to control when the BOD will reset the LPC213x/01 microcontroller. This can be used to further reduce power consumption when a low power mode (such as Power Down) is invoked.

6.18.5 Code security

This feature of the LPC2131/32/34/36/38 allow an application to control whether it can be debugged or protected from observation.

If after reset on-chip bootloader detects a valid checksum in flash and reads 0x8765 4321 from address 0x1FC in flash, debugging will be disabled and thus the code in flash will be protected from observation. Once debugging is disabled, it can be enabled only by performing a full chip erase using the ISP.

6.18.6 External interrupt inputs

The LPC2131/32/34/36/38 include up to nine edge or level sensitive External Interrupt Inputs as selectable pin functions. When the pins are combined, external events can be processed as four independent interrupt signals. The External Interrupt Inputs can optionally be used to wake up the processor from Power-down mode.

6.18.7 Memory Mapping Control

The Memory Mapping Control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

6.18.8 Power Control

The LPC2131/32/34/36/38 support two reduced power modes: Idle mode and Power-down mode.

In Idle mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

Selecting an external 32 kHz clock instead of the PCLK as a clock-source for the on-chip RTC will enable the microcontroller to have the RTC active during Power-down mode. Power-down current is increased with RTC active. However, it is significantly lower than in Idle mode.

A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

6.18.9 VPB bus

The VPB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The VPB divider serves two purposes. The first is to provide peripherals with the desired PCLK via VPB bus so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the VPB bus may be slowed down to $\frac{1}{2}$ to $\frac{1}{4}$ of the processor clock rate. Because the VPB bus must work properly at power-up (and its timing cannot be altered if it does not work since the VPB divider control registers reside on the VPB bus), the default condition at reset is for the VPB bus to run at $\frac{1}{4}$ of the processor clock rate. The second purpose of the VPB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the VPB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.19 Emulation and debugging

The LPC2131/32/34/36/38 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on Port 1. This means that all communication, timer and interface peripherals residing on Port 0 are available during the development and debugging phase as they are when the application is run in the embedded system itself.

6.19.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. EmbeddedICE protocol convertor converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

6.19.2 Embedded trace

Since the LPC2131/32/34/36/38 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

6.19.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC, which is present in the EmbeddedICE logic. The LPC2131/32/34/36/38 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)			–0.5	+3.6	V
V_{DDA}	analog 3.3 V pad supply voltage			–0.5	+4.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT	for the RTC		–0.5	+4.6	V
$V_{i(VREF)}$	input voltage on pin VREF			–0.5	+4.6	V
V_{IA}	analog input voltage	on ADC related pins		–0.5	+5.1	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the V_{DD} supply voltage is present	[2]	–0.5	+6.0	V
		other I/O pins	[2]	–0.5	V_{DD} + 0.5[3]	V
I_{DD}	supply current	per supply pin		-	100[4]	mA
I_{SS}	ground current	per ground pin		-	100[4]	mA
T_{stg}	storage temperature		[5]	–40	+125	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model	[6]			
		all pins		–4000	+4000	V

[1] The following applies to the Limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] Not to exceed 4.6 V.

[4] The peak current is limited to 25 times the corresponding maximum current.

[5] Dependent on package type.

[6] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

8. Static characteristics

Table 6. Static characteristics

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)			3.0	3.3	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage			2.5	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT			2.0[2]	3.3	3.6	V
$V_{i(VREF)}$	input voltage on pin VREF			3.0	3.3	3.6	V
Standard port pins, $\overline{\text{RESET}}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	µA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; no-pull-down		-	-	3	µA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; no pull-up/down		-	-	3	µA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; T_j < 125 °C		-	-	100	mA
V_I	input voltage	pin configured to provide a digital function	[3][4][5]	0	-	5.5	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[6]	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −4 mA	[6]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD}$ − 0.4 V	[6]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[6]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit current	V_{OH} = 0 V	[7]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit current	$V_{OL} = V_{DDA}$	[7]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[8]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V	[9]	−15	−50	−85	µA
		$V_{DD} < V_I$ < 5 V	[8]	0	0	0	µA
$I_{DD(act)}$	active mode supply current	V_{DD} = 3.3 V; T_{amb} = 25 °C; code `while(1){}` executed from flash, no active peripherals					
		CCLK = 10 MHz		-	10	-	mA
		CCLK = 60 MHz		-	40	-	mA
$I_{DD(pd)}$	Power-down mode supply current	V_{DD} = 3.3 V; T_{amb} = 25 °C		-	60	-	µA
		V_{DD} = 3.3 V; T_{amb} = 85 °C		-	200	500	µA

Table 6. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{BATpd}	Power-down mode battery supply current[10]	RTC clock = 32 kHz (from RTCX pins); T_{amb} = 25 °C					
		V_{DD} = 3.0 V; $V_{i(VBAT)}$ = 2.5 V		-	14	-	µA
		V_{DD} = 3.0 V; $V_{i(VBAT)}$ = 3.0 V		-	16	-	µA
		V_{DD} = 3.3 V; $V_{i(VBAT)}$ = 3.3 V		-	18	-	µA
		V_{DD} = 3.6 V; $V_{i(VBAT)}$ = 3.6 V		-	20	-	µA
I_{BATact}	active mode battery supply current[10]	CCLK = 60 MHz; PCLK = 15 MHz; PCLK enabled to RTCK; RTC clock = 32 kHz (from RTCX pins); T_{amb} = 25 °C					
		V_{DD} = 3.0 V; $V_{i(VBAT)}$ = 3.0 V		-	78	-	µA
		V_{DD} = 3.3 V; $V_{i(VBAT)}$ = 3.3 V		-	80	-	µA
		V_{DD} = 3.6 V; $V_{i(VBAT)}$ = 3.6 V		-	82	-	µA
$I_{BATact(opt)}$	optimized active mode battery supply current[10][11]	PCLK disabled to RTCK in the PCONP register; RTC clock = 32 kHz (from RTCX pins); T_{amb} = 25 °C; $V_{i(VBAT)}$ = 3.3 V					
		CCLK = 6 MHz		-	21	-	µA
		CCLK = 25 MHz		-	23	-	µA
		CCLK = 50 MHz		-	27	-	µA
		CCLK = 60 MHz		-	30	-	µA
I^2C-bus pins							
V_{IH}	HIGH-level input voltage		[12]	$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		[12]	-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.5V_{DD}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA	[6]	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD}$	[13]	-	2	4	µA
		V_I = 5 V	[13]	-	10	22	µA
Oscillator pins							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			0	-	1.8	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			0	-	1.8	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1			0	-	1.8	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2			0	-	1.8	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[3] Including voltage on outputs in 3-state mode.

[4] V_{DD} supply voltages must be present.

[5] 3-state outputs go into 3-state mode when V_{DD} is grounded.

[6] Accounts for 100 mV voltage drop in all supply lines.

[7] Only allowed for a short time period.

[8] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

[9] Applies to P1.16 to P1.25.

[10] On pin VBAT.

[11] Optimized for low battery consumption.

[12] The input threshold voltage of I^2C-bus pins meets the I^2C-bus specification, so an input voltage below 1.5 V will be recognized as a logic 0 while an input voltage above 3.0 V will be recognized as a logic 1.

[13] To V_{SS}.

Table 7. ADC static characteristics

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +85 °C, unless otherwise specified; ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[1][2]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[3]	-	-	±2	LSB
E_O	offset error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[4]	-	-	±3	LSB
E_G	gain error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[5]	-	-	±0.5	%
E_T	absolute error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[6]	-	-	±4	LSB

[1] The ADC is monotonic, there are no missing codes.

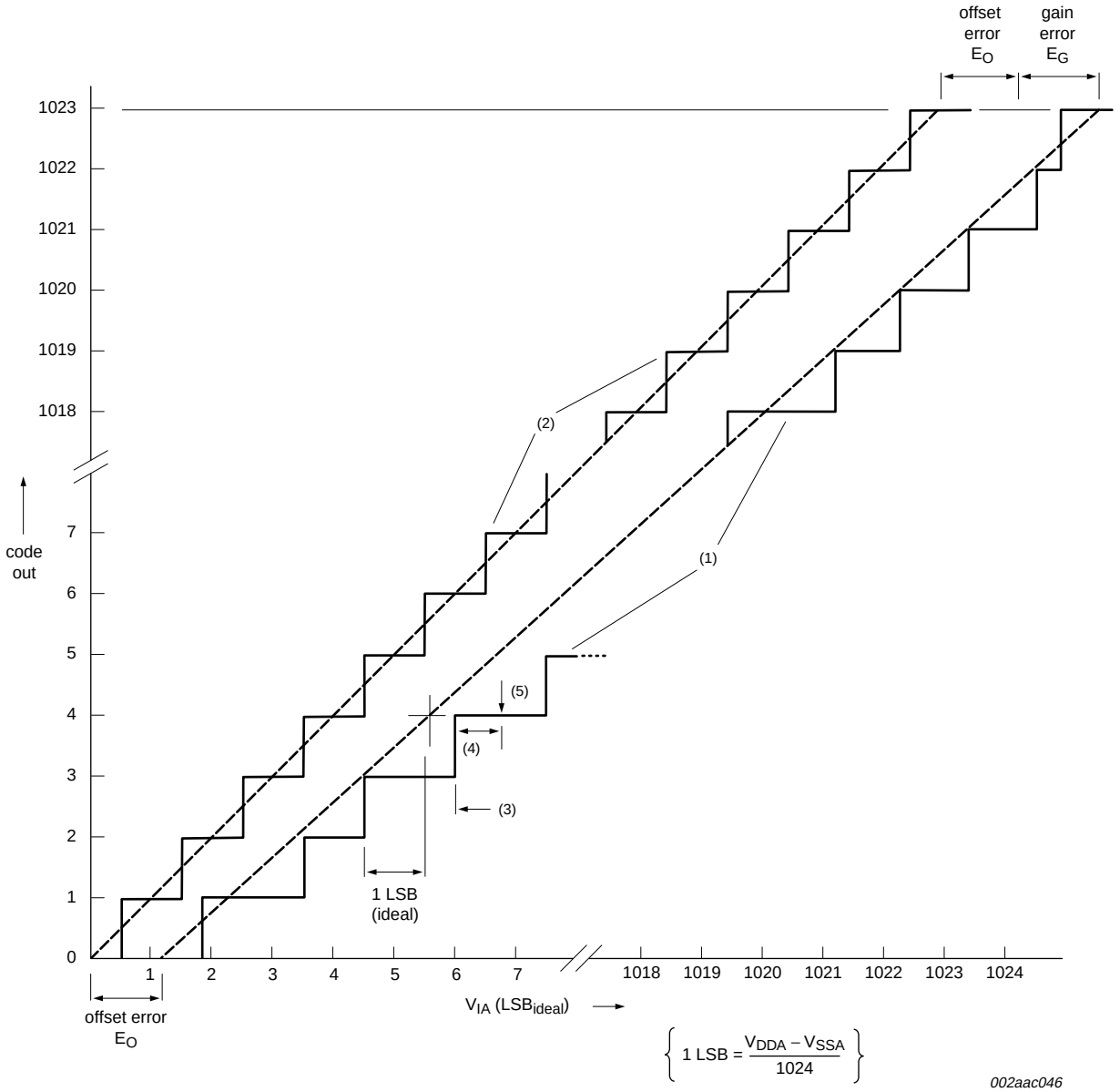
[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 7.

[3] The integral no-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 7.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 7.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 7.

[6] The absolute voltage error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated A/D and the ideal transfer curve. See Figure 7.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 7. ADC characteristics

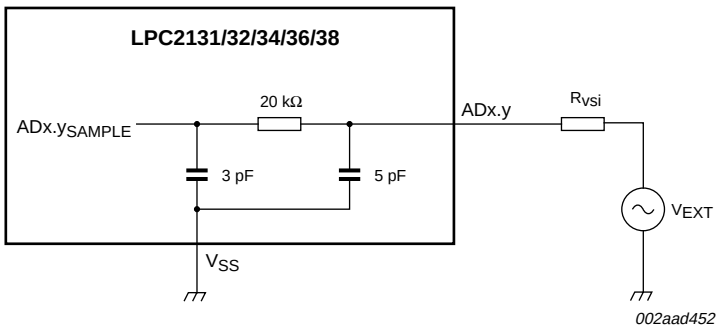


Fig 8. Suggested ADC interface - LPC2131/32/34/36/38 ADx.y pin

9. Dynamic characteristics

Table 8. Dynamic characteristics

T_{amb} = −40 °C to +85 °C for commercial applications, V_{DD} over specified ranges.[1]

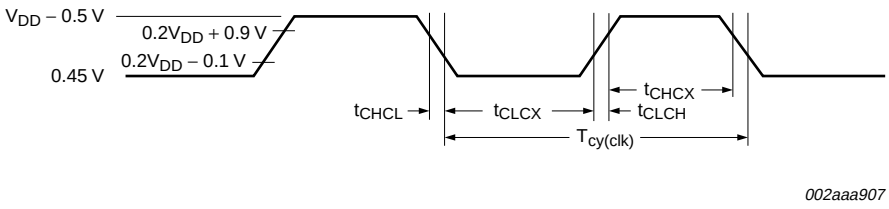
Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
External clock						
f_{osc}	oscillator frequency		10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	100	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0.2 and P0.3)						
$t_{r(o)}$	output rise time		-	10	-	ns
$t_{f(o)}$	output fall time		-	10	-	ns
I^2C-bus pins (P0.2 and P0.3)						
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$[3]	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

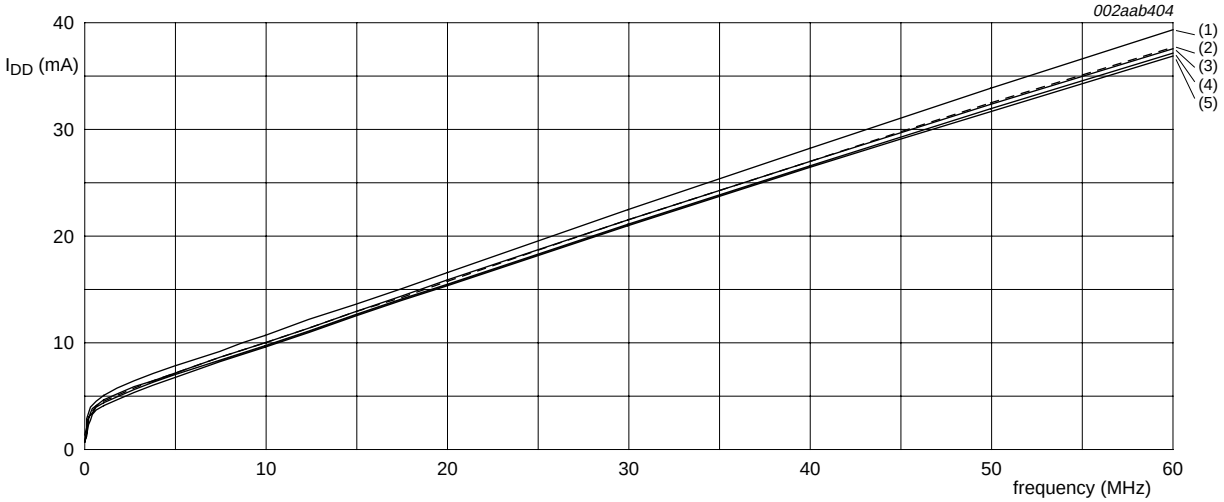
9.1 Timing



V_{DD} = 1.8 V.

Fig 9. External clock timing

9.2 LPC2138 power consumption measurements



Test conditions: code executed from flash; all peripherals are enabled in PCONP register; PCLK = CCLK/4.

(1) V_{DD} = 3.6 V at −60 °C (max)

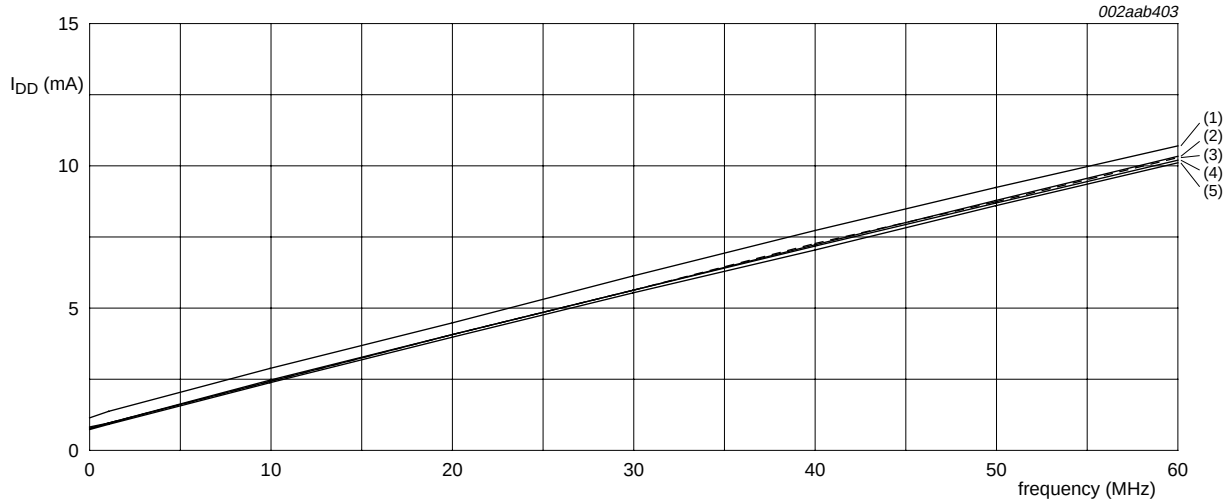
(2) V_{DD} = 3.6 V at 140 °C

(3) V_{DD} = 3.6 V at 25 °C

(4) V_{DD} = 3.3 V at 25 °C (typical)

(5) V_{DD} = 3.3 V at 95 °C (typical)

Fig 10. $I_{DD(act)}$ measured at different frequencies (CCLK) and temperatures



Test conditions: Idle mode entered executing code from flash; all peripherals are enabled in PCONP register; PCLK = CCLK/4.

(1) V_{DD} = 3.6 V at 140 °C (max)

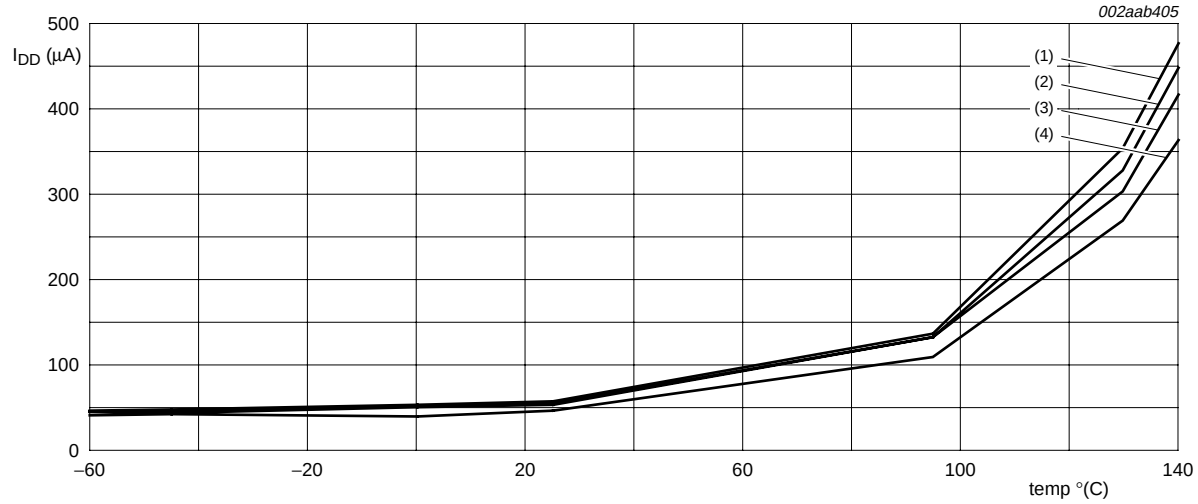
(2) V_{DD} = 3.6 V at −60 °C

(3) V_{DD} = 3.6 V at 25 °C

(4) V_{DD} = 3.3 V at 25 °C (typical)

(5) V_{DD} = 3.3 V at 95 °C (typical)

Fig 11. I_{DD} idle measured at different frequencies (CCLK) and temperatures



Test conditions: Power-down mode entered executing code from flash; all peripherals are enabled in PCONP register.

(1) V_{DD} = 3.6 V

(2) V_{DD} = 3.3 V (max)

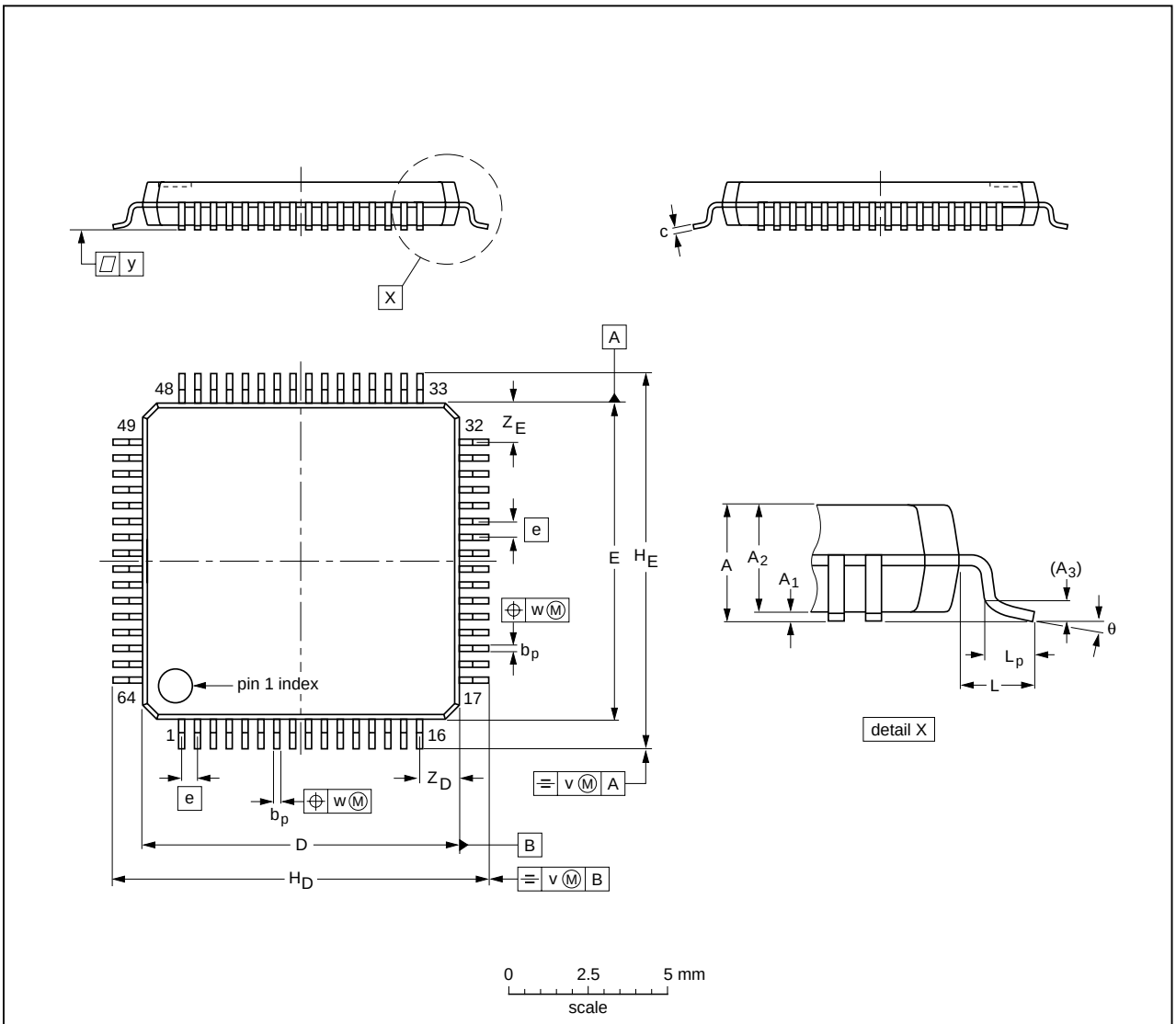
(3) V_{DD} = 3.0 V

(4) V_{DD} = 3.3 V (typical)

Fig 12. $I_{DD(pd)}$ measured at different temperatures

10. Package outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

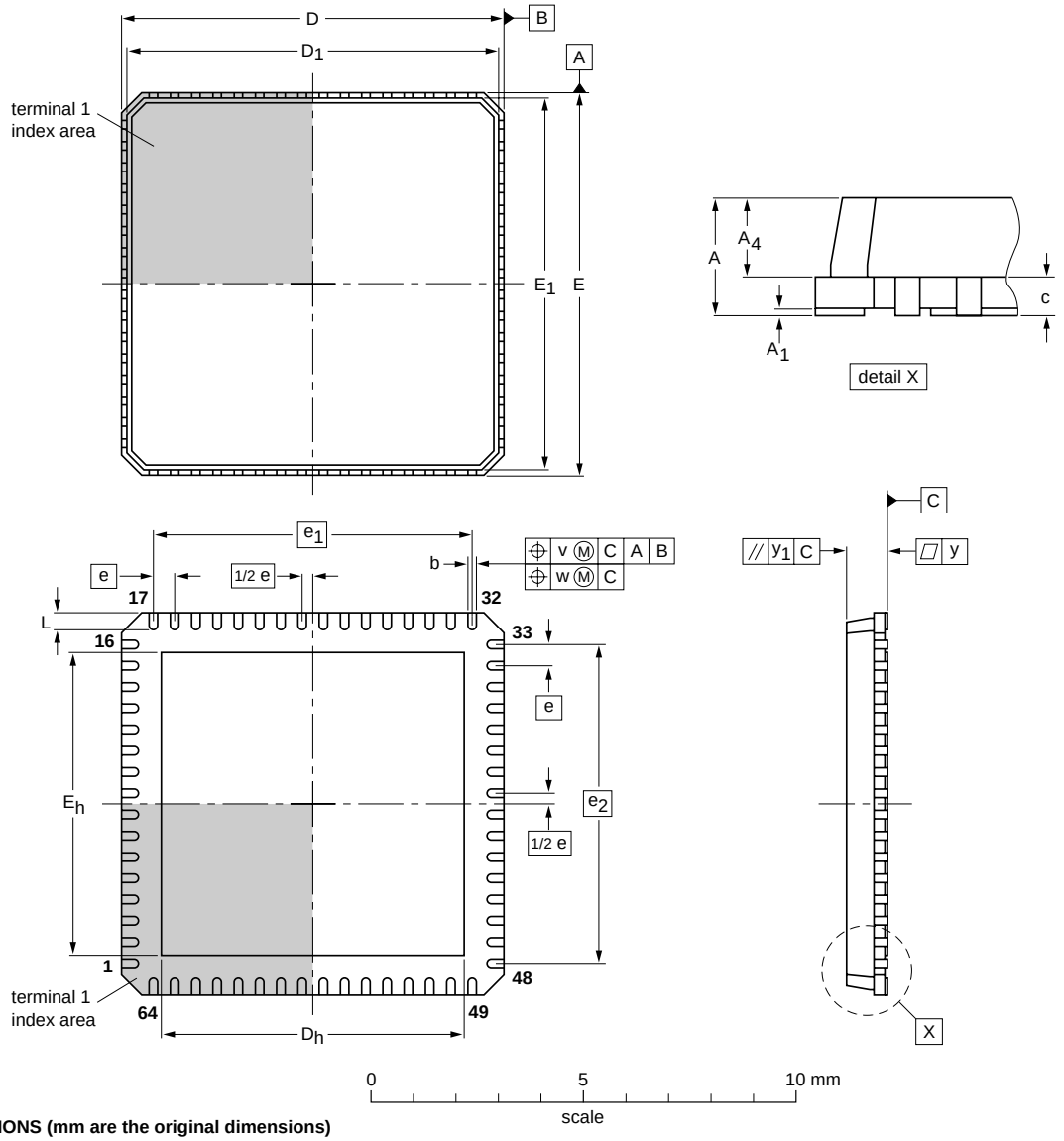
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 13. Package outline SOT314-2 (LQFP64)

HVQFN64: plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 x 9 x 0.85 mm **SOT804-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_4	b	c	D	D_1	D_h	E	E_1	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.80 0.65	0.30 0.18	0.2	9.05 8.95	8.95 8.55	7.25 6.95	9.05 8.95	8.95 8.55	7.25 6.95	0.5	7.5	7.5	0.5 0.3	0.1	0.05	0.05	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT804-2	- - -	MO-220	- - -			04-03-25

Fig 14. Package outline SOT804-2 (HVQFN64)

11. Abbreviations

Table 9. Acronym list

Acronym	Description
ADC	Analog-to-Digital Converter
BOD	BrownOut Detection
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DCC	Debug Communications Channel
FIFO	First In, First Out
GPIO	General Purpose Input/Output
JTAG	Joint Test Action Group
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulator
RAM	Random Access Memory
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSP	Synchronous Serial Port
UART	Universal Asynchronous Receiver/Transmitter
VPB	VLSI Peripheral Bus

12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2131_32_34_36_38_4	20071016	Product data sheet	-	LPC2131_32_34_36_38_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Figure 1: changed incorrect character font • Figure 5: added figure note • Table 3: description for function AD1.3, pin 38, changed LPC2138 into LPC2134/36/38 • Figure 7: added • Figure 9: added figure note			
LPC2131_32_34_36_38_3	20060921	Product data sheet	-	LPC2131_32_34_36_38_2
LPC2131_32_34_36_38_2	20050318	Preliminary data sheet	-	LPC2131_2132_2138_1
LPC2131_2132_2138_1	20041118	Preliminary data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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15. Contents

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Document identifier: LPC2131_32_34_36_38_4

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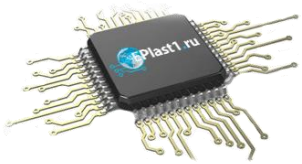

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