EMI/EMC-Compliant, ±15 kV, ESD-Protected RS-232 Line Drivers/Receivers

ADM202E/ADM1181A

FEATURES

Complies with 89/336/EEC EMC directive
ESD protection to IEC1000-4-2 (801.2)
±8 kV: contact discharge
±15 kV: air-gap discharge
±15 kV: human body model
EFT fast transient/burst immunity (IEC1000-4-4)
Low EMI emissions (EN55022)
230 kbits/s data rate guaranteed
TSSOP package option
Upgrade for MAX202E, 232E, LT1181A

APPLICATIONS

General-purpose RS-232 data link
Portable instruments
PDAs

GENERAL DESCRIPTION

The ADM202E and ADM1181A are robust, high speed, 2-channel RS-232/V.28 interface devices that operate from a single 5 V power supply. Both products are suitable for operation in harsh electrical environments and are compliant with the EU directive on EMC (89/336/EEC). Both the level of electromagnetic emissions and immunity are in compliance. EM immunity includes ESD protection in excess of ±15 kV on all I/O lines, fast transient/burst protection (1000-4-4), and radiated immunity (1000-4-3). EM emissions include radiated and conducted emissions as required by Information Technology Equipment EN55022, CISPR22.

The ADM202E and ADM1181A conform to the EIA-232E and CCITT V.28 specifications and operate at data rates up to 230 kbps.

Four external 0.1 μF charge-pump capacitors are used for the voltage doubler/inverter, permitting operation from a single 5 V supply.

FUNCTIONAL BLOCK DIAGRAMS

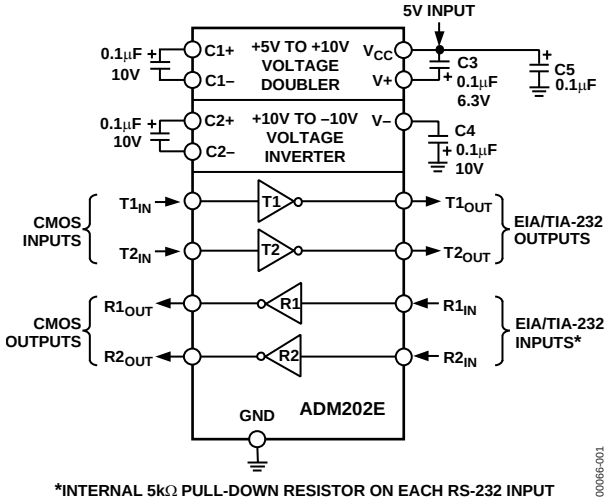

Figure 1.

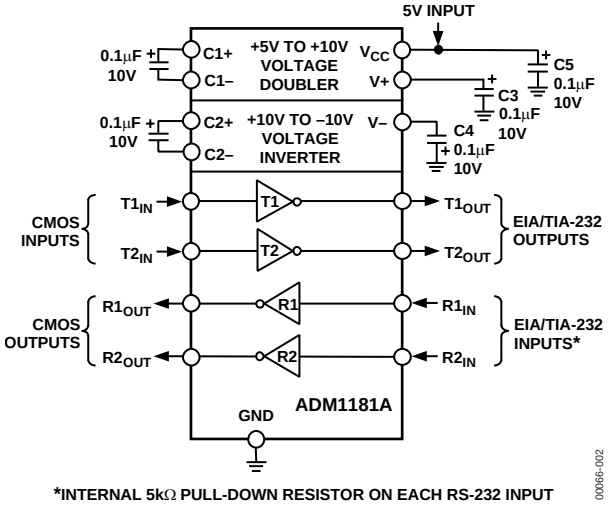

Figure 2.

The ADM202E provides a robust pin-compatible upgrade for existing ADM202, ADM232L, or MAX202E/MAX232E sockets. It is available in a 16-lead PDIP, a wide SOIC, a narrow SOIC, and a space-saving TSSOP package that is 44% smaller than the SOIC package.

The ADM1181A provides a robust pin-compatible upgrade for the LTC1181A, and it is available in a 16-lead PDIP package and a wide 16-lead SOIC package.

Rev. C
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REVISION HISTORY

2/05—Rev. B to Rev. C.

Updated Format ... Universal
Changed Hysteresis Level ... Universal
Change to Specifications ... 3
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2/01—Rev. A to Rev. B.

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SPECIFICATIONS

V_{CC} = 5.0 V ± 10%, C1 to C4 = 0.1 µF. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC CHARACTERISTICS					
Operating Voltage Range	4.5	5.0	5.5	V	
V_{CC} Power Supply Current		2.5	6.0	mA	No load
		13	18	mA	R_L = 3 kΩ to GND
LOGIC					
Input Logic Threshold Low, V_{INL}			0.8	V	T_{IN}
Input Logic Threshold High, V_{INH}	2.4			V	T_{IN}
CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = 3.2 mA
CMOS Output Voltage High, V_{OH}	3.5			V	I_{OUT} = −1 mA
Logic Pull-Up Current		+12	±25	µA	T_{IN} = 0 V
RS-232 RECEIVER					
EIA-232 Input Voltage Range	−30		+30	V	
EIA-232 Input Threshold Low	0.4	1.2		V	
EIA-232 Input Threshold High		1.6	2.4	V	
EIA-232 Input Hysteresis		0.65		V	
EIA-232 Input Resistance	3	5	7	kΩ	T_A = 0°C to 85°C
RS-232 TRANSMITTER					
Output Voltage Swing	±5.0	±9.0		V	All transmitter outputs loaded with 3 kΩ to ground
Transmitter Output Resistance	300			Ω	V_{CC} = 0 V, V_{OUT} = ±2 V
RS-232 Output Short-Circuit Current		±10	±60	mA	
TIMING CHARACTERISTICS					
Maximum Data Rate	230			kbps	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF to 1000 pF
Receiver Propagation Delay					
T_{PHL}		0.1	1	µs	
T_{PLH}		0.3	1	µs	
Transmitter Propagation Delay		1.0	1.5	µs	R_L = 3 kΩ, C_L = 1000 pF
Transition Region Slew Rate	3	8	30	V/µs	R_L = 3 kΩ, C_L = 1000 pF
					Measured from +3 V to −3 V, or −3 V to +3 V
EM IMMUNITY					
ESD Protection (I/O Pins)		±15		kV	Human body model
		±15		kV	IEC1000-4-2 air discharge
		±8 kV		kV	IEC1000-4-2 contact discharge
EFT Protection (I/O Pins)		±2		kV	IEC1000-4-4
EMI Immunity		10		V/m	IEC1000-4-3

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Values
V_{CC}	−0.3 V to +6 V
V+	(V_{CC} − 0.3 V) to +14 V
V−	+0.3 V to −14 V
Input Voltages	
T_{IN}	0.3 V to (V+, +0.3 V)
R_{IN}	±30 V
Output Voltages	
T_{OUT}	±15 V
R_{OUT}	−0.3 V to (V_{CC} + 0.3 V)
Short-Circuit Duration	
T_{OUT}	Continuous
Power Dissipation N-16	450 mW
(Derate 6 mW/°C Above 50°C)	
θ_{JA}, Thermal Impedance	117°C/W
Power Dissipation R-16	450 mW
(Derate 6 mW/°C Above 50°C)	
θ_{JA}, Thermal Impedance	158°C/W
Power Dissipation RU-16	500 mW
(Derate 6 mW/°C Above 50°C)	
θ_{JA}, Thermal Impedance	158°C/W
Operating Temperature Range	
Industrial (A Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
ESD Rating (MIL-STD-883B) (I/O Pins)	±15 kV
ESD Rating (IEC1000-4-2 Air) (I/O Pins)	±15 kV
ESD Rating (IEC1000-4-2 Contact) (I/O Pins)	±8 kV
EFT Rating (IEC1000-4-4) (I/O Pins)	±2 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

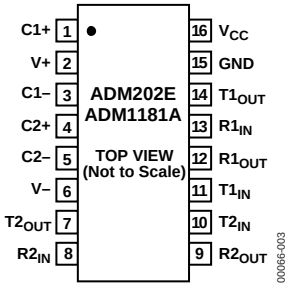


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
16	V_{CC}	Power Supply Input: 5 V ± 10%.
2	V+	Internally Generated Positive Supply (+9 V nominal).
6	V–	Internally Generated Negative Supply (–9 V nominal).
15	GND	Ground Pin. Must be connected to 0 V.
1, 3	C1+, C1–	External Capacitor 1 is connected between these pins. A 0.1 µF capacitor is recommended, but larger capacitors of up to 47 µF can be used.
4, 5	C2+, C2–	External Capacitor 2 is connected between these pins. A 0.1 µF capacitor is recommended, but larger capacitors of up to 47 µF can be used.
10, 11	T_{IN}	Transmitter (Driver) Inputs. These inputs accept TTL/CMOS levels.
7, 14	T_{OUT}	Transmitter (Driver) Outputs. These are RS-232 signal levels (typically ±9 V).
8, 13	R_{IN}	Receiver Inputs. These inputs accept RS-232 signal levels. An internal 5 kΩ pull-down resistor to GND is connected on each input.
9, 12	R_{OUT}	Receiver Outputs. These are CMOS output logic levels.

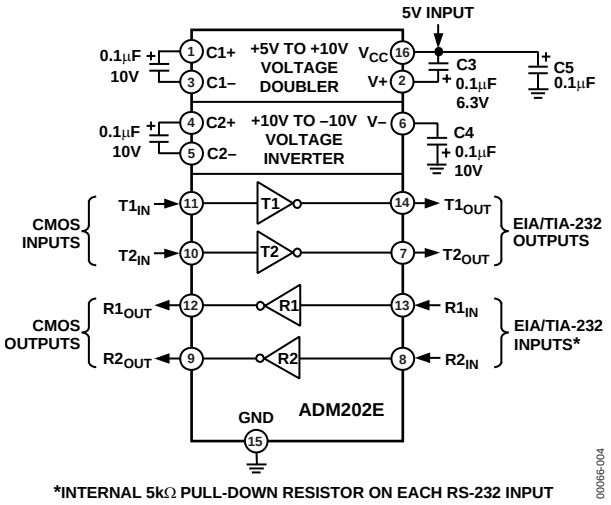


Figure 4. ADM202E Typical Operating Circuit

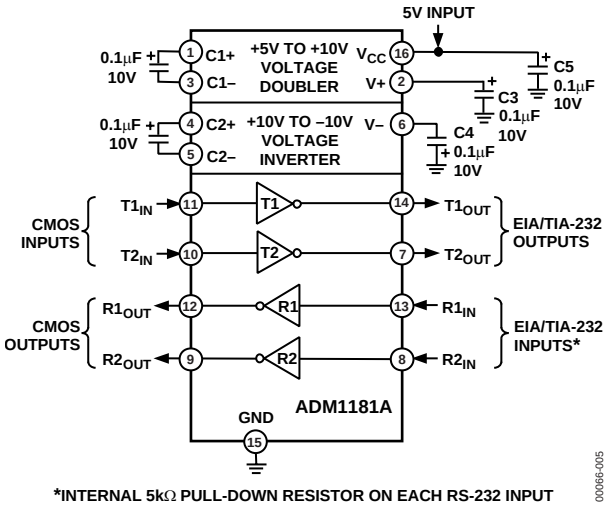


Figure 5. ADM1181A Typical Operating Circuit

GENERAL DESCRIPTION

The ADM202E/ADM1181E are rugged RS-232 line drivers/receivers. Step-up voltage converters coupled with level-shifting transmitters and receivers allow RS-232 levels to be developed while operating from a single 5 V supply.

Features include low power consumption, high transmission rates, and compliance with the EU directive on electromagnetic compatibility. EM compatibility includes protection against radiated and conducted interference, including high levels of electrostatic discharge.

All inputs and outputs contain protection against electrostatic discharges of up to ±15 kV and electrical fast transients of up to ±2 kV. This ensures compliance to IEC1000-4-2 and IEC1000-4-4 requirements.

The devices are ideally suited for operation in electrically harsh environments or where RS-232 cables are frequently being plugged/unplugged. They are also immune to high RF field strengths without special shielding precautions.

CMOS technology is used to minimize the power dissipation, allowing maximum battery life in portable applications.

The ADM202E/ADM1181A serve as a modification, enhancement, and improvement to the ADM230–ADM241 family and its derivatives. It is essentially plug-in compatible and do not have materially different applications.

CIRCUIT DESCRIPTION

The internal circuitry consists of four main sections:

- A charge-pump voltage converter
- 5 V logic to EIA-232 transmitters
- EIA-232 to 5 V logic receivers.
- Transient protection circuit on all I/O lines

Charge-Pump DC-to-DC Voltage Converter

The charge-pump voltage converter consists of a 200 kHz oscillator and a switching matrix. The converter generates a ±10 V supply from the input 5 V level. This is done in two stages, using a switched capacitor technique, as illustrated in Figure 6 and Figure 7. First, the 5 V input supply is doubled to 10 V, using Capacitor C1 as the charge storage element. The 10 V level is then inverted to generate −10 V, using C2 as the storage element.

Capacitor C3 and Capacitor C4 are used to reduce the output ripple. Their values are not critical and can be increased if desired. On the ADM202E, Capacitor C3 is shown connected between V+ and V_{CC}, whereas it is connected between V+ and GND on the ADM1181A. It is acceptable to use either configuration with both the ADM202E and ADM1181A. If desired, larger capacitors (up to 47 μF) can be used for Capacitor C1 to Capacitor C4. This facilitates direct substitution with older generation charge-pump RS-232 transceivers.

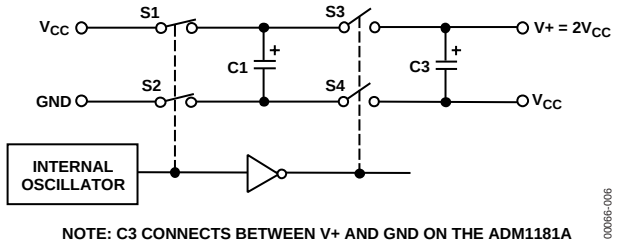


Figure 6. Charge-Pump Voltage Doubler

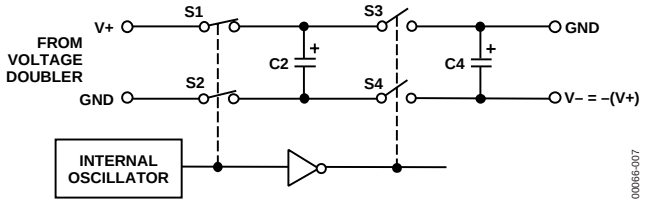


Figure 7. Charge-Pump Voltage Inverter

Transmitter (Driver) Section

The drivers convert 5 V logic input levels into RS-232 output levels. When driving an RS-232 load with V_{CC} = 5 V, the output voltage swing is typically ±9 V.

Receiver Section

The receivers are inverting level shifters that accept RS-232 input levels and translate them into 5 V logic output levels. The inputs have internal 5 kΩ pull-down resistors to ground and are also protected against overvoltages of up to ±30 V. Unconnected inputs are pulled to 0 V by the internal 5 kΩ pull-down resistor. Therefore, unconnected inputs and those connected to GND have a Logic 1 output level.

The receivers have Schmitt-trigger inputs with a hysteresis level of 0.65 V. This ensures error-free reception for both noisy inputs and inputs with slow transition times.

HIGH BAUD RATE

The ADM202E/ADM1181A feature high slew rates, permitting data transmission at rates well in excess of the EIA/RS-232-E specifications. RS-232 voltage levels are maintained at data rates of up to 230 kbps, even under worst case loading conditions. This allows for high speed data links between two terminals and is also suitable for the new generation ISDN modem standards, which require data rates of 230 kbps. The slew rate is internally controlled to less than 30 V/μs to minimize EMI interference.

ESD/EFT TRANSIENT PROTECTION SCHEME

The ADM202E/ADM1181A use protective clamping structures on all inputs and outputs to clamp the voltage to a safe level and dissipate the energy present in electrostatic (ESD) and electrical fast transients (EFT) discharges. A simplified schematic of the protection structure is shown in Figure 8 and Figure 9. Each input and output contains two back-to-back high speed clamping diodes. During normal operation with maximum RS-232 signal levels, the diodes have no effect because one or the other is reverse biased depending on the polarity of the signal. However, if the voltage exceeds about 50 V in either direction, reverse breakdown occurs and the voltage is clamped at this level. The diodes are large p-n junctions that are designed to handle instantaneous current surges that exceed several amperes.

The transmitter outputs and receiver inputs have a similar protection structure. The receiver inputs can dissipate some of the energy through the internal 5 kΩ resistor to GND, as well as through the protection diodes.

The protection structure achieves ESD protection up to ±15 kV and EFT protection up to ±2 kV on all RS-232 I/O lines. The methods used to test the protection scheme are discussed in the ESD Testing (IEC1000-4-2) and Fast Transient/Burst Testing (IEC1000-4-4) sections.

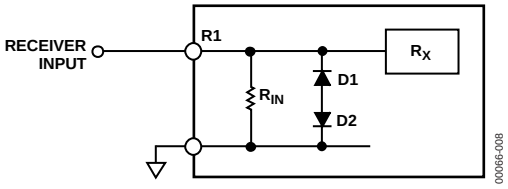


Figure 8. Receiver Input Protection Scheme

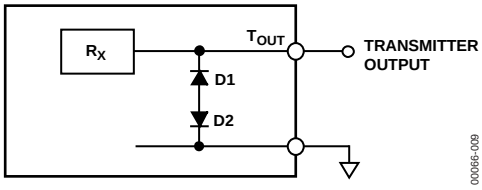


Figure 9. Transmitter Output Protection Scheme

TYPICAL PERFORMANCE CHARACTERISTICS

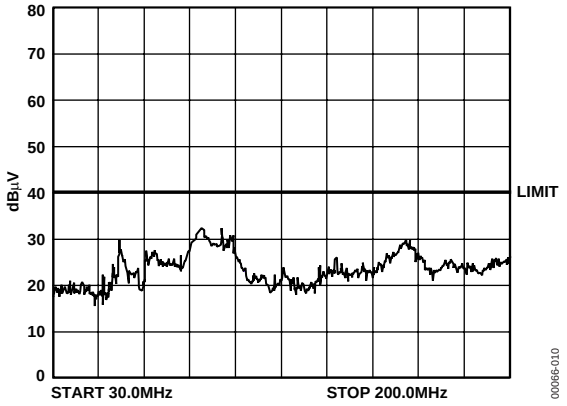


Figure 10. EMC Radiated Emissions

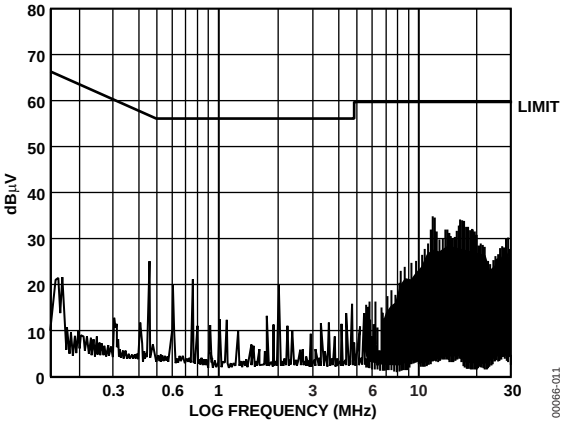


Figure 11. EMC Conducted Emissions

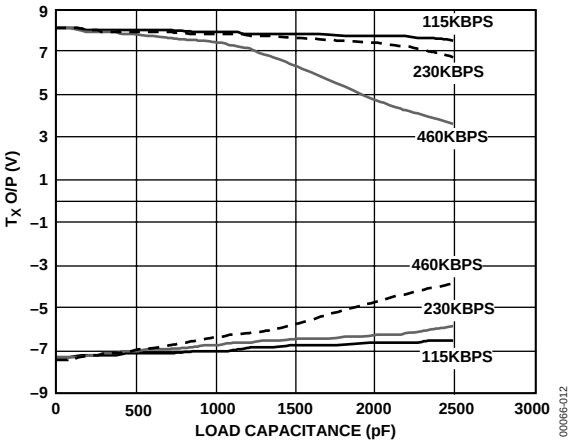


Figure 12. Transmitter Output Voltage High/Low vs. Load Capacitance @ 115 kbps, 230 kbps, and 460 kbps

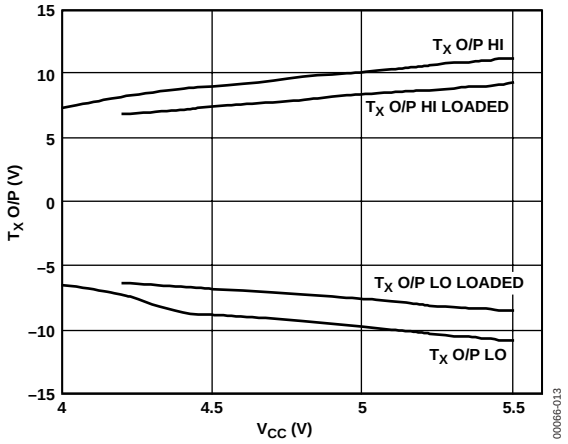


Figure 13. Transmitter Output Voltage High/Low vs. V_{CC}

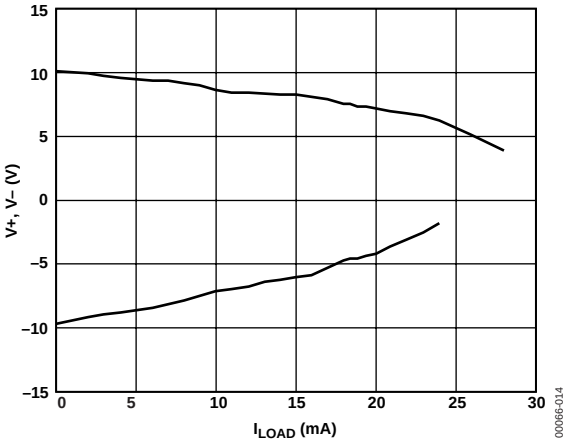


Figure 14. Charge Pump V+ and V– vs. Current

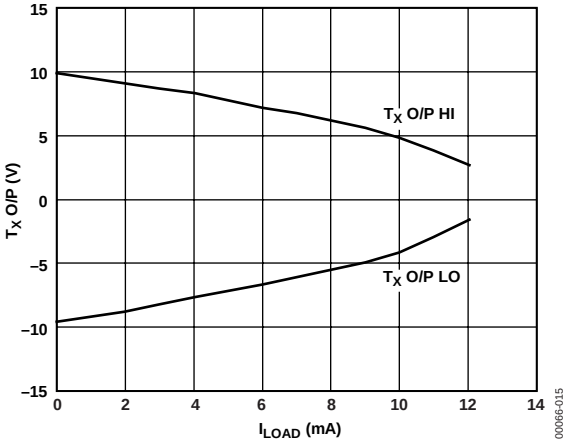


Figure 15. Transmitter Output Voltage Low/High vs. Load Current

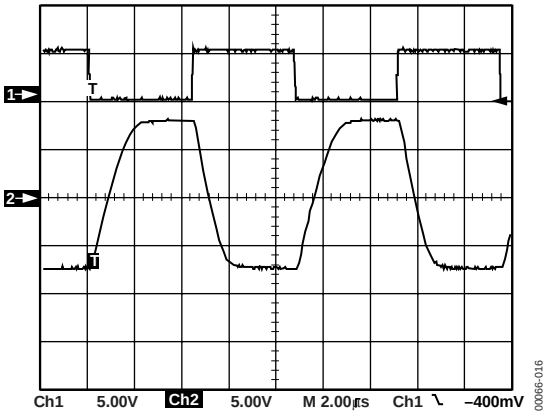


Figure 16. 230 kbps Data Transmission

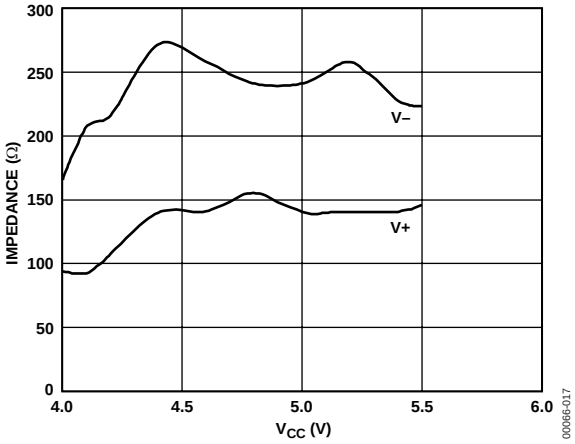


Figure 17. Charge-Pump Impedance vs. V_{CC}

ESD TESTING (IEC1000-4-2)

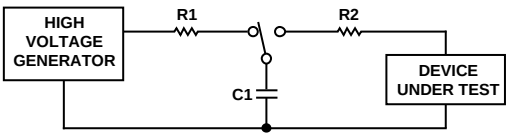
IEC1000-4-2 (previously 801-2) specifies compliance testing using two coupling methods, contact discharge and air-gap discharge. Contact discharge calls for a direct connection to the unit being tested. Air-gap discharge uses a higher test voltage, but does not make direct contact with the unit being tested. With air-gap discharge, the discharge gun is moved toward the unit being tested, developing an arc across the air gap. This method is influenced by humidity, temperature, barometric pressure, distance, and rate of closure of the discharge gun. Although less realistic, the contact-discharge method is more repeatable and is gaining preference to the air-gap method.

Although very little energy is contained within an ESD pulse, the extremely fast rise time coupled with high voltages can cause failures in unprotected semiconductors. Catastrophic destruction can occur immediately as a result of arcing or heating. Even if catastrophic failure does not occur immediately, the device might suffer from parametric degradation, which can result in degraded performance. The cumulative effects of continuous exposure can eventually lead to complete failure.

I/O lines are particularly vulnerable to ESD damage. Simply touching or plugging in an I/O cable can result in a static discharge, which can damage or completely destroy the interface product connected to the I/O port. Traditional ESD test methods, such as the MIL-STD-883B method 3015.7, do not fully test a product's susceptibility to this type of discharge. This test was intended to test a product's susceptibility to ESD damage during handling. Each pin is tested with respect to all other pins. There are some important differences between the traditional test and the IEC test:

- The IEC test is much more stringent in terms of discharge energy. The injected peak current is over four times greater.
- The current rise time is significantly faster in the IEC test.
- The IEC test is carried out while power is applied to the device.

It is possible that the ESD discharge could induce latch-up in the device being tested. Therefore, this test is more representative of a real-world I/O discharge where the equipment is operating normally with power applied. For peace of mind, however, both tests should be performed to ensure maximum protection during both handling and field service.



ESD TEST METHOD	R2	C1
H. BODY MIL-STD883B	1.5kΩ	100pF
IEC1000-4-2	330Ω	150pF

Figure 18. ESD Test Standards

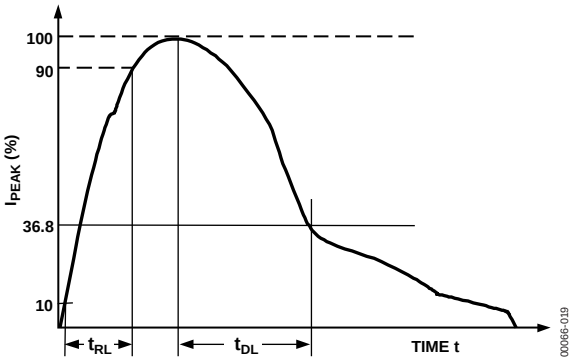


Figure 19. Human Body Model ESD Current Waveform

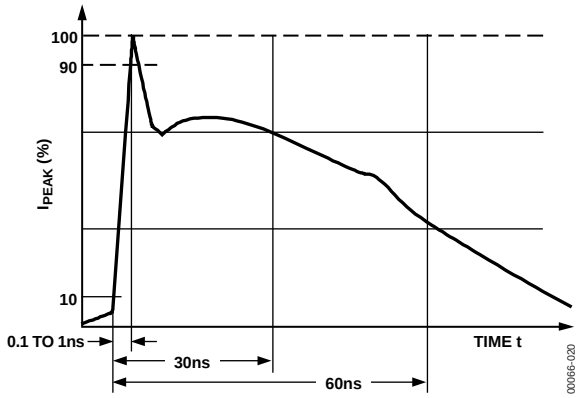


Figure 20. IEC1000-4-2 ESD Current Waveform

The ADM202E/ADM1181E products are tested using both of the previously mentioned test methods. Pins are tested with respect to all other pins as per the MIL-STD-883B specification. In addition, I/O pins are tested as per the IEC test specification. The products were tested under the following conditions:

- Power-On
- Power-Off

There are four levels of compliance defined by IEC1000-4-2. The ADM202E/ADM1181A products meet the most stringent level of compliance both for contact and for air-gap discharge. This means that the products are able to withstand contact discharges in excess of 8 kV and air-gap discharges in excess of 15 kV.

Table 4. IEC1000-4-2 Compliance Levels

Level	Contact Discharge	Air Discharge
1	2 kV	2 kV
2	4 kV	4 kV
3	6 kV	8 kV
4	8 kV	15 kV

Table 5. ADM202E/ADM1181A ESD Test Results

ESD Test Method	I/O Pins
MIL-STD-883B	±15 kV
IEC1000-4-2	
Contact	±8 kV
Air	±15 kV

FAST TRANSIENT/BURST TESTING (IEC1000-4-4)

IEC1000-4-4 (previously 801-4) covers electrical fast transient (EFT)/burst immunity. Electrical fast transients occur as a result of arcing contacts in switches and relays. The tests simulate the interference generated when, for example, a power relay disconnects an inductive load. A spark is generated due to the well-known back EMF effect. In fact, the spark consists of a burst of sparks as the relay contacts separate. The voltage appearing on the line, therefore, consists of a burst of extremely fast transient impulses. A similar effect occurs when switching on fluorescent lights.

The fast transient/burst test defined in IEC1000-4-4 simulates this arcing, and its waveform is illustrated in Figure 17. It consists of a burst of 2.5 kHz to 5 kHz transients repeating at 300 ms intervals. It is specified for both power and data lines.

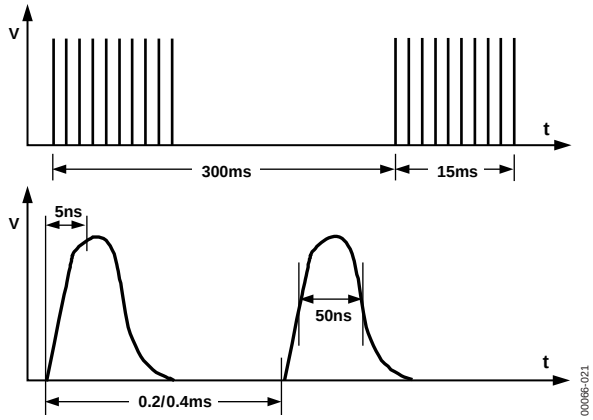


Figure 21. IEC1000-4-4 Fast Transient Waveform

A simplified circuit diagram of the actual EFT generator is illustrated in Figure 22.

The transients are coupled onto the signal lines using an EFT coupling clamp. The clamp, which is 1 m long, completely surrounds the cable, providing maximum coupling capacitance (50 pF to 200 pF typ) between the clamp and the cable. High energy transients are capacitively coupled to the signal lines. Fast rise times (5 ns), as specified by the standard, result in very effective coupling. This test is very strenuous because high voltages are coupled onto the signal lines. The repetitive transients often cause problems where single pulses do not. Destructive latch-up can be induced due to the high energy content of the transients. Note that this stress is applied while the interface products are powered up and transmitting data. The EFT test applies hundreds of pulses with higher energy than ESD. Worst-case transient current on an I/O line can be as high as 40 A.

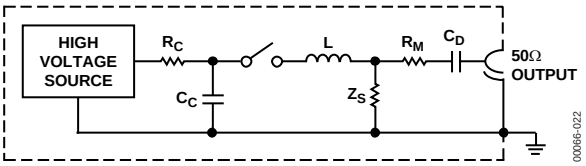


Figure 22. IEC1000-4-4 Fast Transient Generator

Test results are classified according to the following:

- Classification 1: Normal performance within specification limits
- Classification 2: Temporary degradation or loss of performance that is self-recoverable
- Classification 3: Temporary degradation or loss of function or performance that requires operator intervention or system reset
- Classification 4: Degradation or loss of function that is not recoverable due to damage

The ADM202E/ADM1181A meet Classification 2 and have been tested under worst-case conditions using unshielded cables. Data transmission during the transient condition is corrupted, but can resume immediately following the EFT event without user intervention.

IEC1000-4-3 RADIATED IMMUNITY

IEC1000-4-3 (previously IEC801-3) describes the measurement method and defines the levels of immunity to radiated electromagnetic fields. It was originally intended to simulate the electromagnetic fields generated by portable radio transceivers and other devices that generate continuous wave-radiated electromagnetic energy. Its scope has since been broadened to include spurious EM energy, which can be radiated from fluorescent lights, thyristor drives, inductive loads, and other sources.

Testing for immunity involves irradiating the device with an EM field. There are various methods of achieving this, including use of anechoic chamber, stripline cell, TEM cell, and GTEM cell. A stripline cell consists of two parallel plates with an electric field developed between them. The device being tested is placed within the cell and exposed to the electric field. There are three severity levels that have field strengths ranging from 1 V to 10 V/m. Results are classified in a similar fashion to those for IEC1000-4-2.

- Classification 1: Normal operation
- Classification 2: Temporary degradation or loss of function that is self-recoverable when the interfering signal is removed
- Classification 3: Temporary degradation or loss of function that requires operator intervention or system reset when the interfering signal is removed
- Classification 4: Degradation or loss of function that is not recoverable due to damage

The ADM202E/ADM1181A products easily meet Classification 1 at the most stringent (Level 3) requirement. In fact, field strengths of up to 30 V/m showed no performance degradation, and error-free data transmission continued even during irradiation.

Table 6. Test Severity Levels (IEC1000-4-3)

Level	Field Strength V/m
1	1
2	3
3	10

EMISSIONS/INTERFERENCE

EN55 022 and CISPR22 define the permitted limits of radiated and conducted interference from information technology (IT) equipment. The objective of the standard is to minimize the level of emissions, both conducted and radiated. For ease of measurement and analysis, conducted emissions are assumed to predominate below 30 MHz, and radiated emissions are assumed to predominate above 30 MHz.

CONDUCTED EMISSIONS

Conducted emissions is a measure of noise conducted onto the mains power supply. Switching transients from the charge pump that are 20 V in magnitude and that contain significant energy can lead to conducted emissions. Another source of conducted emissions is the overlap in switch-on times in the charge-pump voltage converter. In the voltage doubler shown in Figure 23, if S2 is not fully turned off before S4 turns on, a transient current glitch occurs between V_{CC} and GND that results in conducted emissions. Therefore, it is important that the switches in the charge pump guarantee break-before-make switching under all conditions to prevent instantaneous short-circuit conditions.

The ADM202E is designed to minimize the switching transients and ensure break-before-make switching, thereby minimizing conducted emissions. This results in emission levels well below the specified limits. No additional filtering or decoupling, other than the recommended 0.1 µF capacitor, is required.

Conducted emissions are measured by monitoring the mains line. The equipment used consists of a spectrum analyzer and a LISN (line impedance stabilizing network) that essentially presents a fixed impedance at RF. The spectrum analyzer scans for emissions of up to 30 MHz; a plot for the ADM202E is shown in Figure 25.

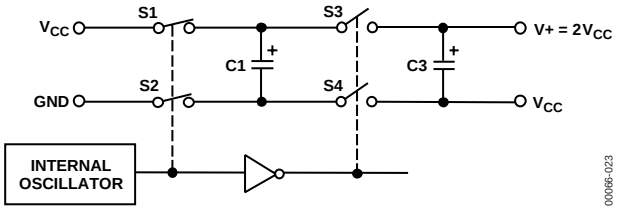


Figure 23. Charge-Pump Voltage Doubler

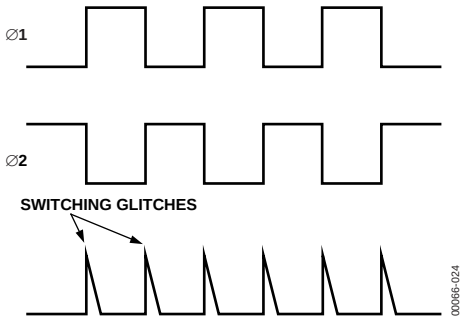


Figure 24. Switching Glitches

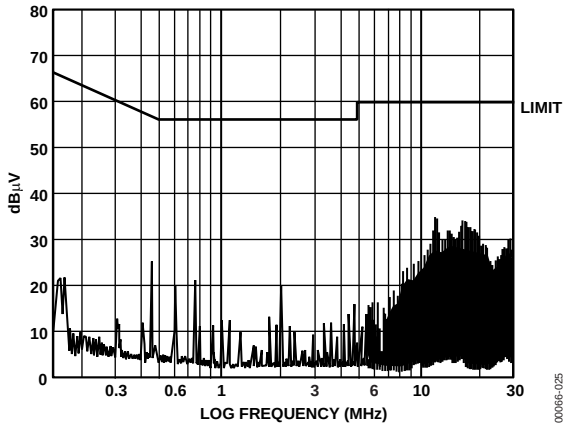


Figure 25. ADM202E Conducted Emissions

RADIATED EMISSIONS

Radiated emissions are measured at frequencies in excess of 30 MHz. RS-232 outputs are designed for operation at high baud rates, while driving cables can radiate high frequency EM energy. The previously described causes of conducted emissions can also cause radiated emissions. Fast RS-232 output transitions can radiate interference, especially when lightly loaded and driving unshielded cables. Charge-pump devices are also prone to radiating noise due to the high frequency oscillator and the high voltages being switched by the charge pump. The move toward smaller capacitors to conserve board space has resulted in higher frequency oscillators in the charge-pump design, causing higher levels of conducted and radiated emissions.

The RS-232 outputs on the ADM202E feature a controlled slew rate to minimize the level of radiated emissions, yet they are fast enough to support data rates of up to 230 kBaud.

Figure 27 shows radiated emissions vs. frequency. The levels of emissions are well within specifications without the need for additional shielding or filtering components. The ADM202E was operated at maximum baud rates and configured like a typical RS-232 interface. Testing for radiated emissions was carried out in a shielded anechoic chamber.

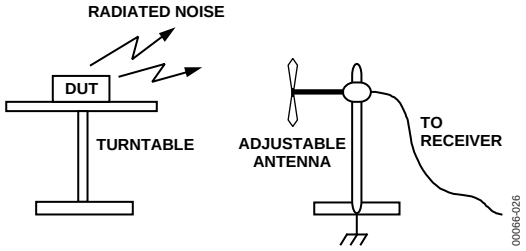


Figure 26. Radiated Emissions Test Setup

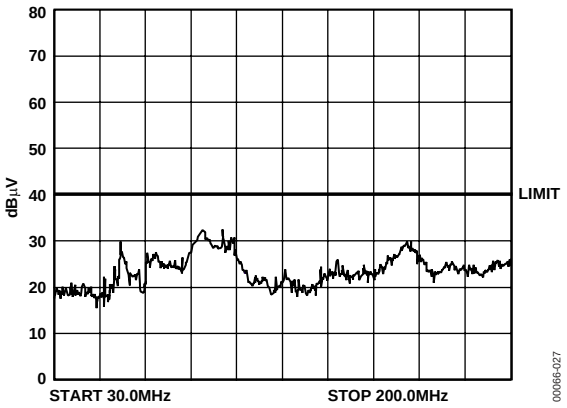
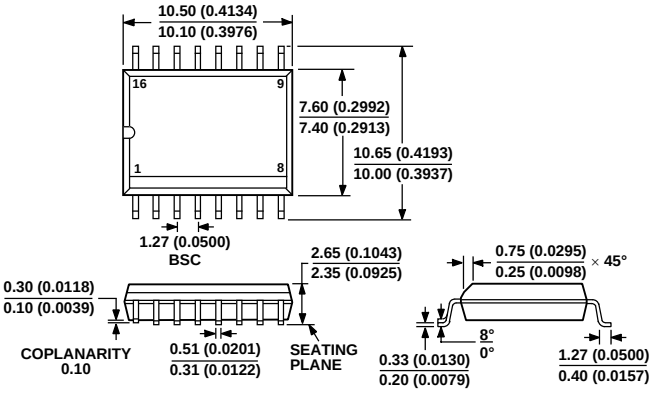


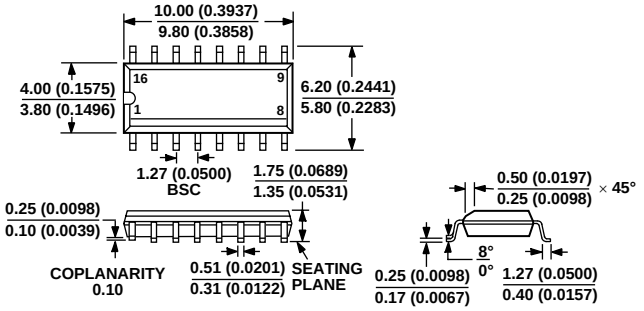
Figure 27. ADM202E Radiated Emissions vs. Frequency

OUTLINE DIMENSIONS



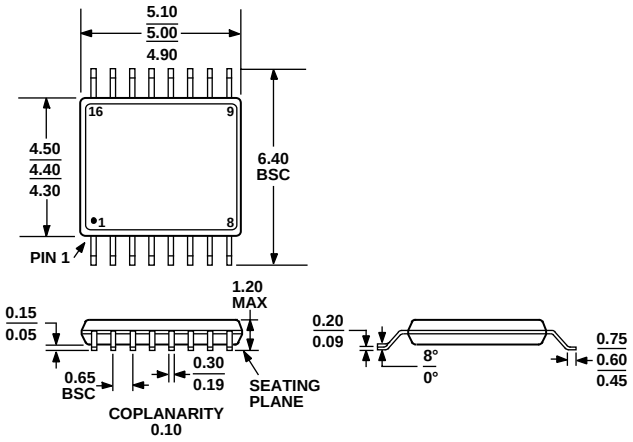
COMPLIANT TO JEDEC STANDARDS MS-013AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 28. 16-Lead Standard Small Outline Package [SOIC] Wide Body (RW-16) Dimensions shown in millimeters and (inches)



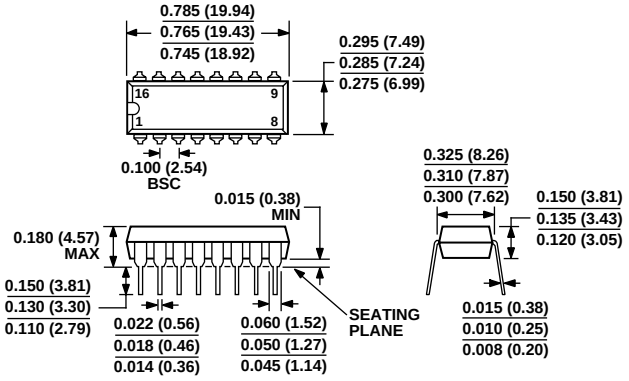
COMPLIANT TO JEDEC STANDARDS MS-012AC
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 29. 16-Lead Standard Small Outline Package [SOIC] Narrow Body (R-16) Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153AB

Figure 30. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16) Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-095AC
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 31. 16-Lead Plastic Dual In-Line Package [PDIP] (N-16) Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM202EAN	−40°C to +85°C	Plastic DIP	N-16
ADM202EANZ[1]	−40°C to +85°C	Plastic DIP	N-16
ADM202EARW	−40°C to +85°C	Wide SOIC	R-16W
ADM202EARW-REEL	−40°C to +85°C	Wide SOIC	R-16W
ADM202EARWZ[1]	−40°C to +85°C	Wide SOIC	R-16W
ADM202EARWZ-REEL[1]	−40°C to +85°C	Wide SOIC	R-16W
ADM202EARN	−40°C to +85°C	Narrow SOIC	R-16N
ADM202EARN-REEL	−40°C to +85°C	Narrow SOIC	R-16N
ADM202EARN-REEL7	−40°C to +85°C	Narrow SOIC	R-16N
ADM202EARNZ[1]	−40°C to +85°C	Narrow SOIC	R-16N
ADM202EARNZ-REEL[1]	−40°C to +85°C	Narrow SOIC	R-16N
ADM202EARNZ-REEL7[1]	−40°C to +85°C	Narrow SOIC	R-16N
ADM202EARU	−40°C to +85°C	TSSOP	RU-16
ADM202EARU-REEL	−40°C to +85°C	TSSOP	RU-16
ADM202EARU-REEL7	−40°C to +85°C	TSSOP	RU-16
ADM202EARUZ[1]	−40°C to +85°C	TSSOP	RU-16
ADM202EARUZ-REEL[1]	−40°C to +85°C	TSSOP	RU-16
ADM202EARUZ-REEL7[1]	−40°C to +85°C	TSSOP	RU-16
ADM1181AAN	−40°C to +85°C	Plastic DIP	N-16
ADM1181AARW	−40°C to +85°C	Wide SOIC	R-16W
ADM1181AARW-REEL	−40°C to +85°C	Wide SOIC	R-16W
ADM1181AARWZ[1]	−40°C to +85°C	Wide SOIC	R-16W
ADM1181AARWZ-REEL[1]	−40°C to +85°C	Wide SOIC	R-16W

[1] Z = Pb-free part.

NOTES

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C00066-0-2/05(C)

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