

Features

- 25 dB Small Signal Gain
- 43 dBm Third Order Intercept Point (OIP3)
- >2 W Output P1dB
- 34.5 dBm Saturated Output Power
- Integrated Power Detector
- Bias 1330 mA @ 6 V
- Lead-Free 7 mm Cavity Package
- RoHS* Compliant and 260°C Reflow Compatible

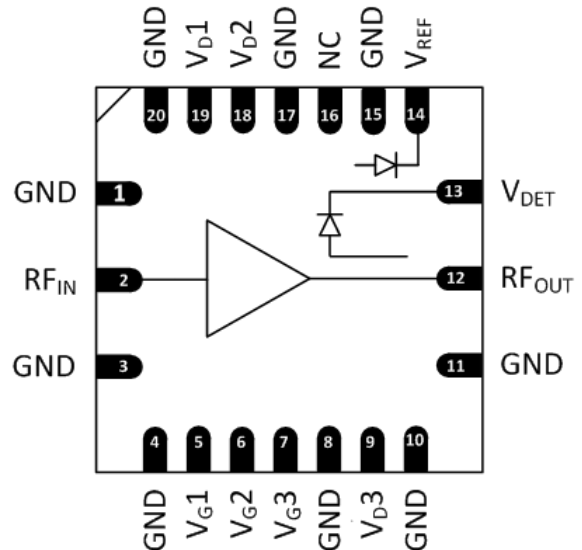
Description

The MAAP-011145-STD is a power amplifier assembled in a 7 mm surface mount package with a temperature compensated integrated power detector operating from 17.65 to 19.75 GHz. The circuit provides 25 dB gain, 43 dBm OIP3, 2 W P1dB and 34.5 dBm saturated output power.

The device includes ESD protection and by-pass capacitors to ease the implementation and volume assembly of the packaged part.

This power amplifier is specifically designed for use in point-to-point radios for cellular backhaul applications in the 18 GHz band.

Functional Schematic



Pin Configuration²

Pin No.	Function	Pin No.	Function
1	Ground	11	Ground
2	RF Input	12	RF Output
3	Ground	13	Power Detector
4	Ground	14	Reference
5	Gate 1 Bias	15	Ground
6	Gate 2 Bias	16	No Connection
7	Gate 3 Bias	17	Ground
8	Ground	18	Drain 2 Bias
9	Drain 3 Bias	19	Drain 1 Bias
10	Ground	20	Ground
		21 ³	Paddle

Ordering Information¹

Part Number	Package
MAAP-011145-STD	Bulk Quantity
MAAP-011145-STR500	500 Piece Reel
MAAP-011145-001SMB	Sample Board

1. Reference Application Note M513 for reel size information.

2. All "No Connection" pins should be grounded.
3. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

Power Amplifier, 2 W
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Electrical Specifications: $V_{DD} = 6\text{ V}$, $I_{DQ}^4 = 1330\text{ mA}$, $T_A = +25^\circ\text{C}$

Parameter	Units	Min.	Typ.	Max.
Small Signal Gain	dB	22.7	26	28.3
P_{SAT}	dBm	33.2	34.5	—
Output IP3, +20 dBm SCL	dBm	40.5	44	—
Output IP3, +24 dBm SCL	dBm	37.5	42	—
P1dB	dBm	—	34	—
Input Return Loss	dB	—	15	—
Output Return Loss	dB	—	10	—
Detector V_{diff} , $P_{out} = +20\text{dBm}$	V	0.5	1.1	1.7
Noise Figure	dB	—	7	—
Gain Ripple over frequency	dB	—	2	—
Gate Voltage	V	—	—	-0.60

4. Adjust V_{G1} , V_{G2} and V_{G3} between -1.2 and -0.6 V to achieve specified I_{DQ} ($I_{DQ} = I_{D1} + I_{D2} + I_{D3}$). V_{G1} , V_{G2} and V_{G3} are nominally the same voltage.

Absolute Maximum Ratings^{5,6,7}

Parameter	Rating
Input Power	+18 dBm
Drain Voltage (V_D 1,2,3)	+7 V
Gate Voltage (V_G 1,2,3)	-3 V
Drain to Gate Voltage (V_D-V_G)	+10 V
Current ($I_{DQ} = I_{D1}+I_{D2}+I_{D3}$)	2000 mA
Detector Pin	+6 V
Detector Reference Pin	+6 V
Junction Temperature	+175°C
Storage Temperature	-65°C to +150°C

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.
7. Operating at nominal conditions with $T_J \leq +150^\circ\text{C}$ will ensure $\text{MTTF} > 1 \times 10^6$ hours.

Maximum Operating Ratings^{8,9}

Parameter	Rating
P_{DISS}	11.2 W
Junction Temperature	+150°C
Operating Temperature	-40°C to +85°C

8. Channel temperature directly affects device MTTF. Channel temperature should be kept as low as possible to maximize lifetime. Thermal resistance, Θ_{jc} , is 5.8 °C/W.
9. For saturated performance, it is recommended that the sum of $(2V_{DD} + \text{abs}(V_{GG})) < 15 \text{ V}$.

Handling Procedures

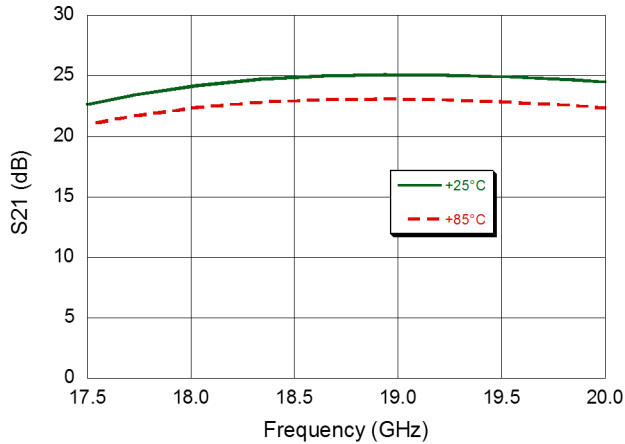
Please observe the following precautions to avoid damage:

Static Sensitivity

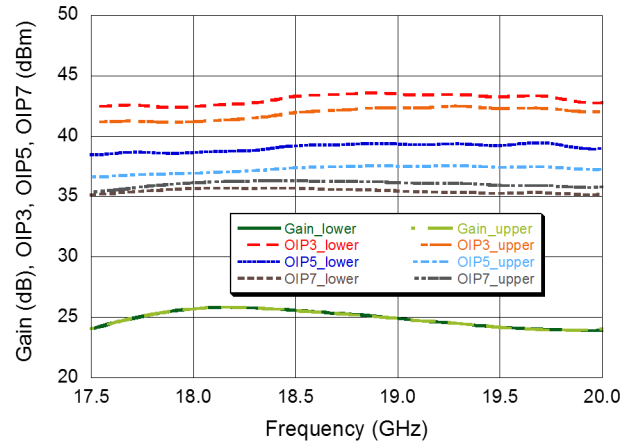
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these CDM class 2, HBM class 1B devices.

Typical Performance Curves: 8 W Quiescent Bias, $V_D = 6 V$

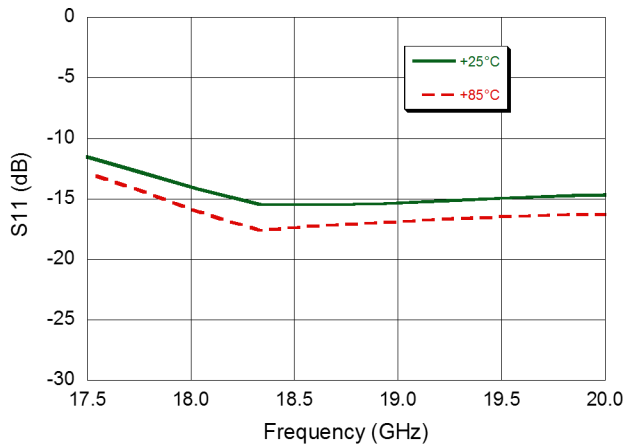
Gain



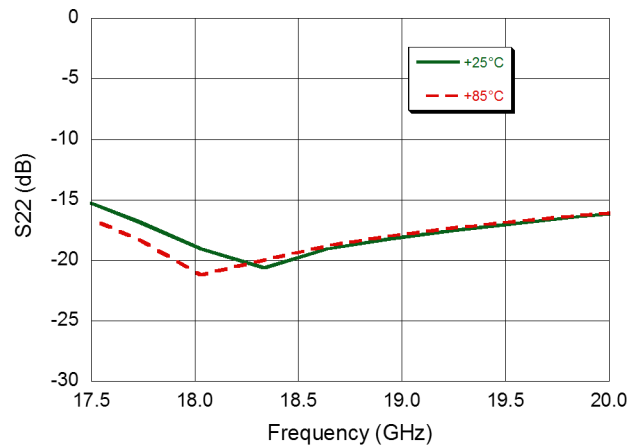
Gain, OIP3, OIP5, OIP7 @ $P_{IN} = -2 dBm$ per tone



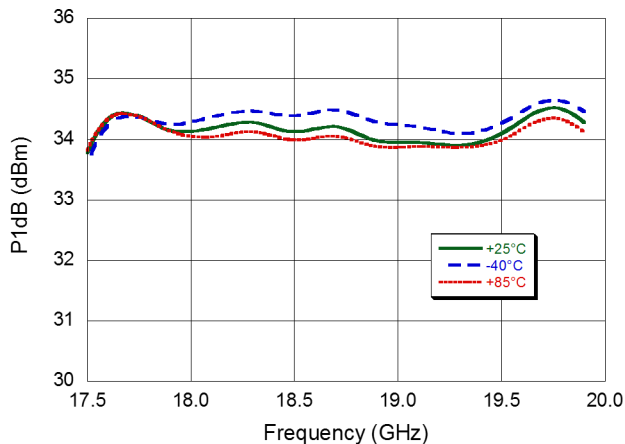
Input Return Loss



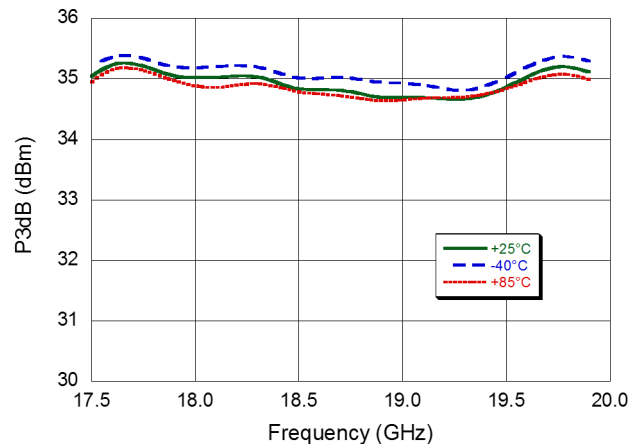
Output Return Loss



P1dB

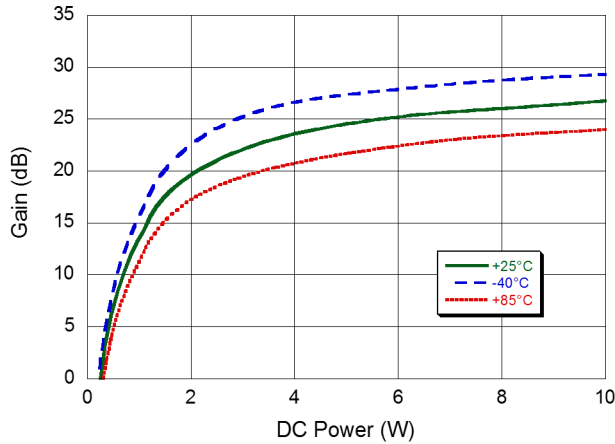


P3dB

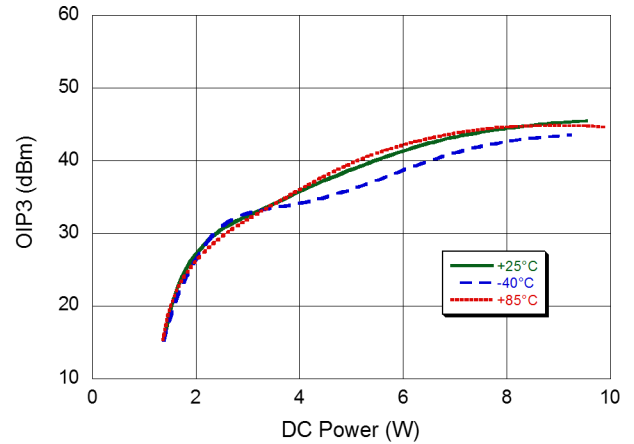


Typical Performance Curves: $V_D = 6\text{ V}$

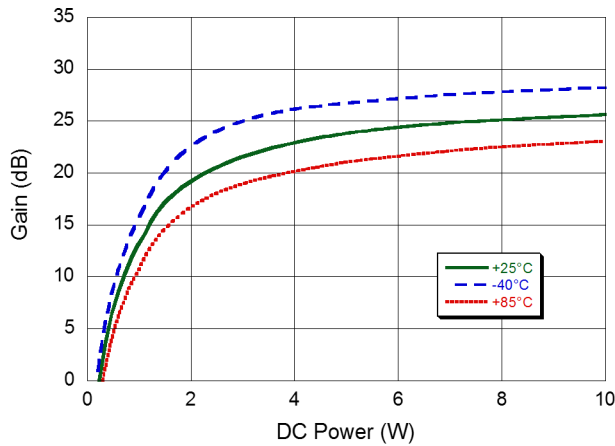
Gain @ 17.7 GHz



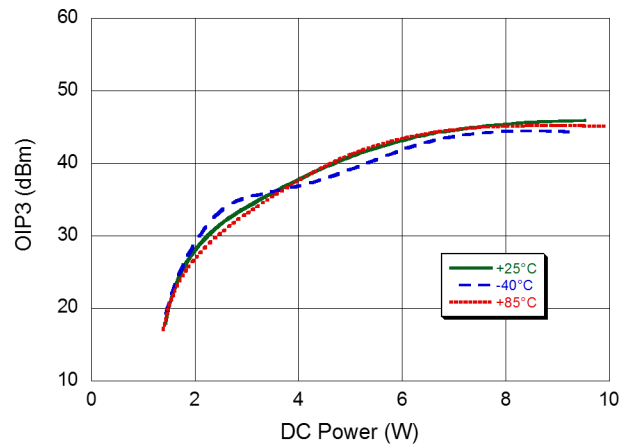
OIP3 @ 17.7 GHz



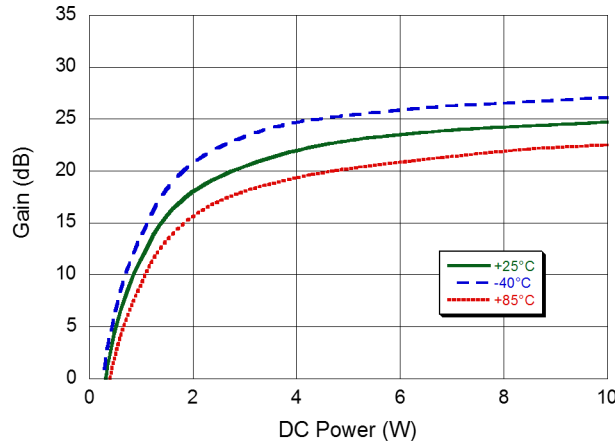
Gain @ 18.7 GHz



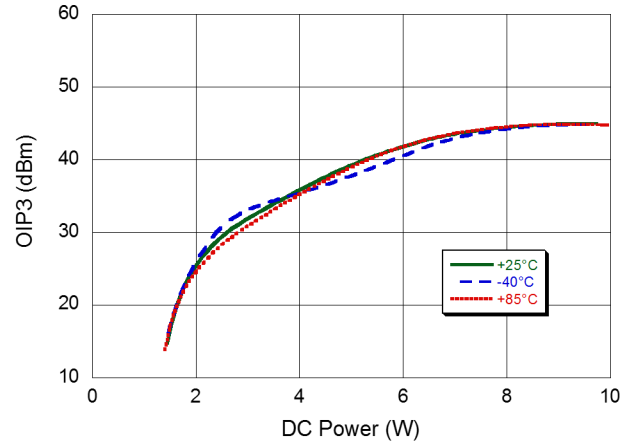
OIP3 @ 18.7 GHz



Gain @ 19.7 GHz

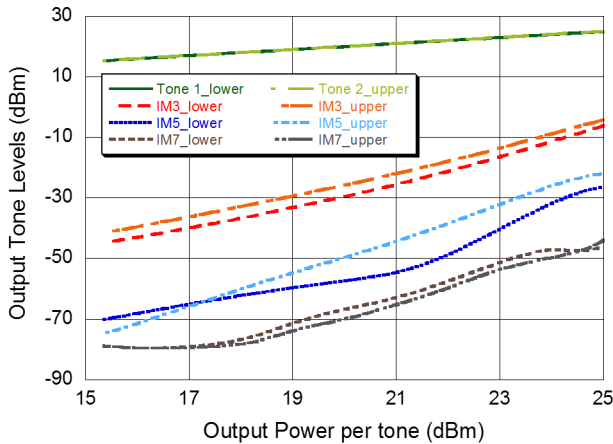


OIP3 @ 19.7 GHz

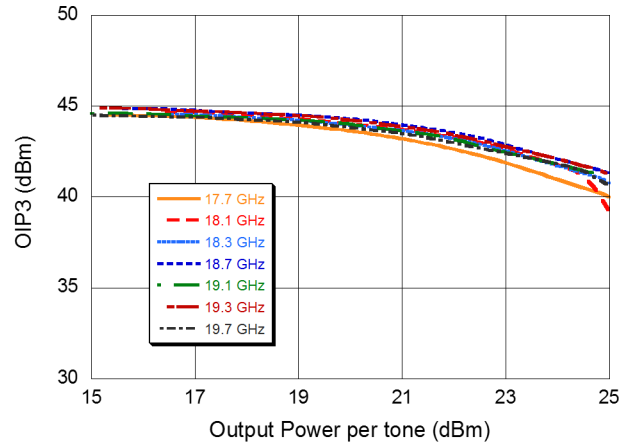


Typical Performance Curves: 8 W Quiescent Bias, $V_D = 6 V$

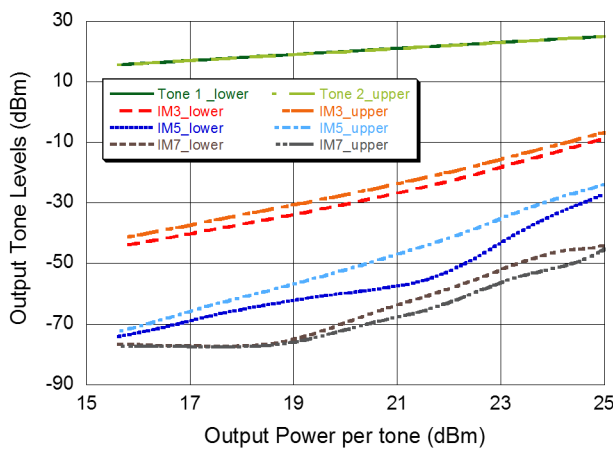
Lower and Upper Intermodulation Tones @ 17.7 GHz



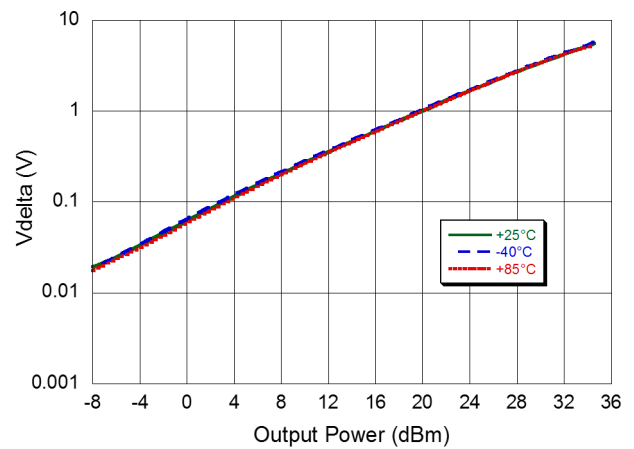
OIP3 vs. Output Power



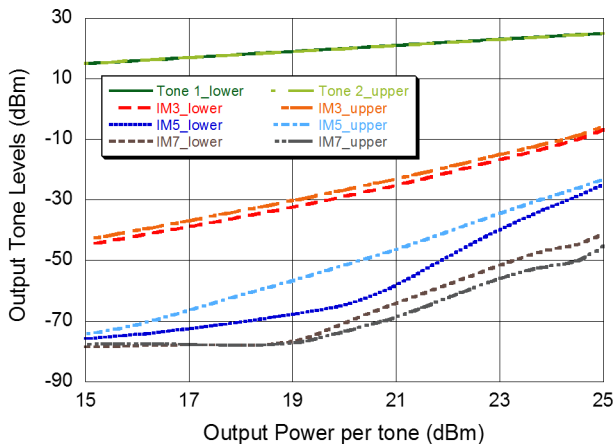
Lower and Upper Intermodulation Tones @ 18.7 GHz



Detector Delta Voltage vs. Output Power



Lower and Upper Intermodulation Tones @ 19.7 GHz



Biasing -

All gates should be pinched-off ($V_G < -2$ V) before applying drain voltage ($V_D = 6$ V). Then the gate voltages can be increased until the desired quiescent drain current is reached in each stage. The recommended quiescent bias is $V_D = 6$ V, $I_{D1} = 190$ mA, $I_{D2} = 380$ mA and $I_{D3} = 762$ mA. The performance in this datasheet has been measured with fixed gate voltage and no drain current regulation under large signal operation. It is also possible to regulate the drain current dynamically, to limit the DC power dissipation under RF drive. To turn off the device, the turn on bias sequence should be followed in reverse.

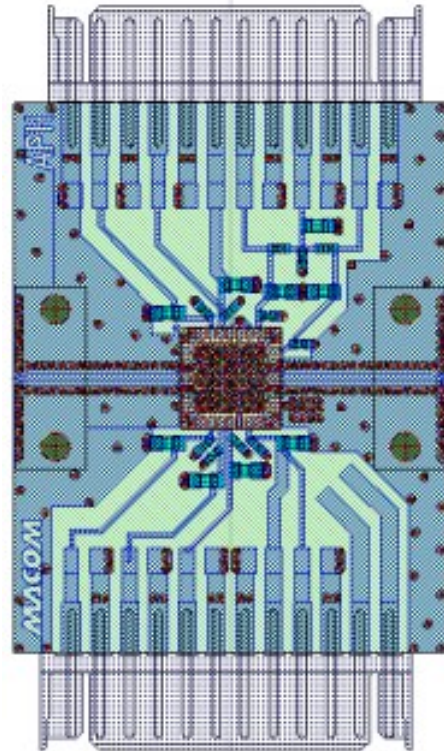
Bias Arrangement -

Each DC pin ($V_{D1,2,3}$ and $V_{G1,2,3}$) needs to have bypass capacitance (120 pF and 10 nF) mounted as close to the MMIC as possible.

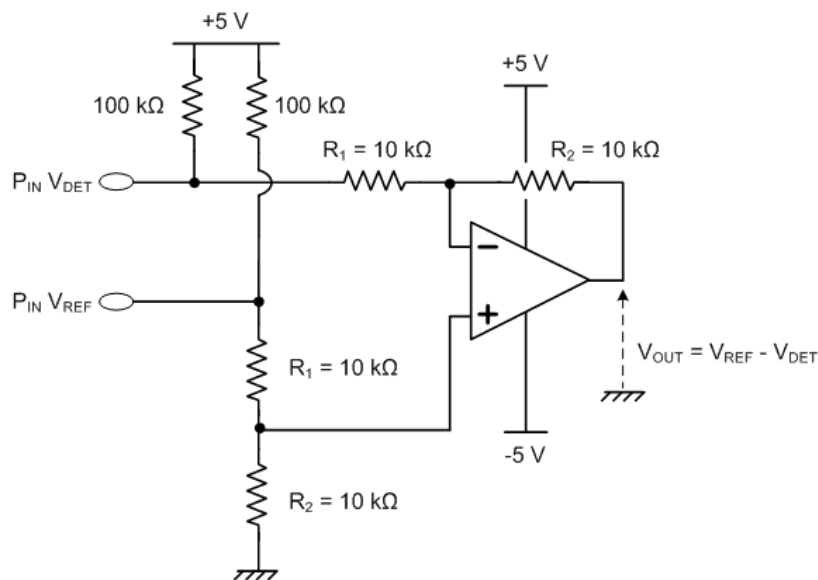
Power Detector -

As shown in the schematic below, the power detector is implemented by providing +5 V bias and measuring the difference in output voltage with standard op-amp in a differential mode configuration.

Evaluation Board Layout



Application Schematic



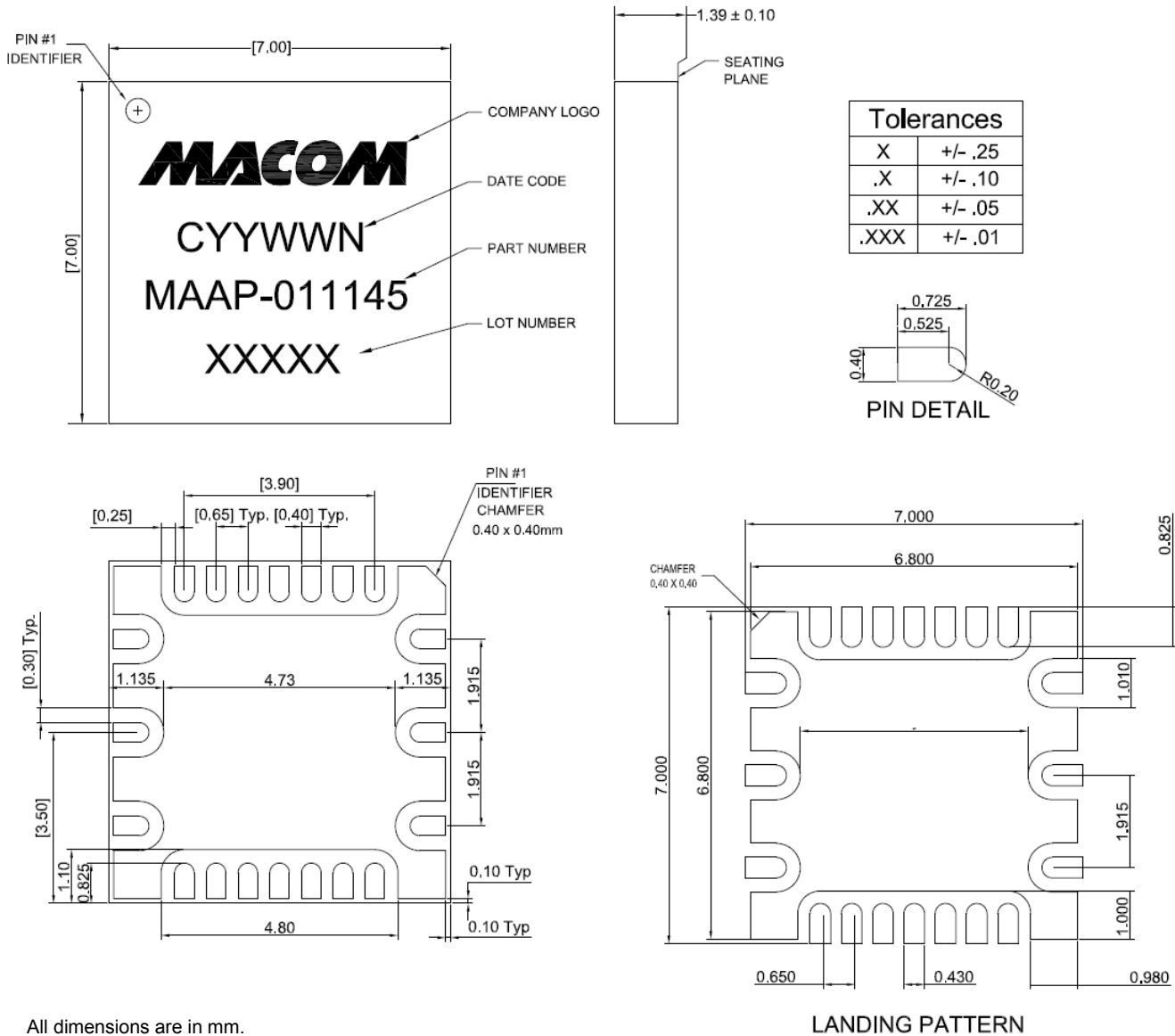
MAAP-011145-STD



Power Amplifier, 2 W
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Rev. V2

Package Outline Drawing and Recommended Land Pattern†



All dimensions are in mm.

† Meets JEDEC moisture sensitivity level 3 requirements.



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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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