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Panasonic Global Part Number AN44067A-VF

Vendor Issue Number 1203030

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# Product Standards

Part No.	AN44067A
Package Code No.	HSOP034-P-0300A

Semiconductor Company  
Matsushita Electric Industrial Co., Ltd.

Established by	Applied by	Checked by	Prepared by
K.Kemichi	M.Hiramatsu	H.Nobekawa	T.Nagano

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# AN44067A

## Driver IC for Stepping Motor

### ■ Overview

AN44067A is a two channel H-bridge driver IC. Bipolar stepping motor can be controlled by a single driver IC. 2 phase excitation, half-step, 1-2 phase excitation, W1-2 phase excitation and 2W1-2 phase excitation can be selected.

### ■ Features

- Built-in decoder for micro steps  
(2 phase excitation, half-step, 1-2 phase excitation, W1-2 phase excitation and 2W1-2 phase excitation)  
Stepping motor can be driven by only external clock signal.
- PMW can be driven by built-in CR (3-value can be selected during PWM OFF period.)  
Selection during PWM OFF period enables the best PWM drive.
- Mix Decay compatible (4-value for Fast Decay ratio can be selected.)  
Mix Decay control can improve accuracy of motor current wave form.
- Built-in low voltage detection  
If supply voltage lowers less than the range of operating supply voltage, low voltage detection operates and all phases of motor drive output are turned OFF.
- Built-in thermal protection  
If chip junction temperature rises and reaches setup temperature, all phases of motor drive output are turned OFF.
- 1 power supply with built-in 5 V power supply (accuracy  $\pm 5\%$ )  
Motor can be driven by only 1 power supply because of built-in 5 V power supply.
- Built-in standby function  
Operation of standby function can lower current consumption of IC.
- Built-in Home Position function  
Home Position function can detect the position of a motor.

### ■ Applications

- IC for stepping motor drives

### ■ Package

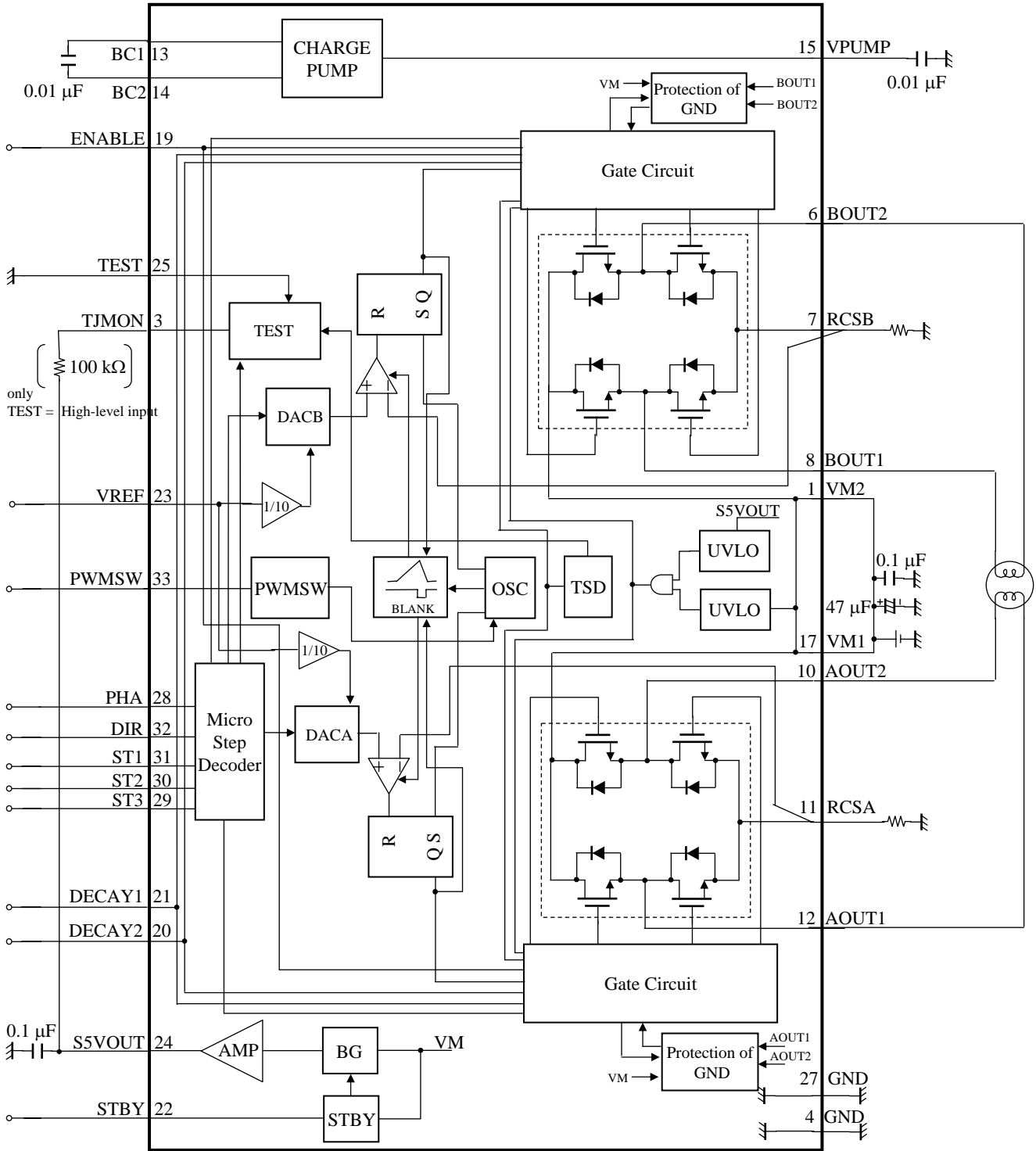
- 34 pin Plastic Small Outline Package With Heat Sink (SOP Type)

### ■ Type

- Bi-CDMOS IC

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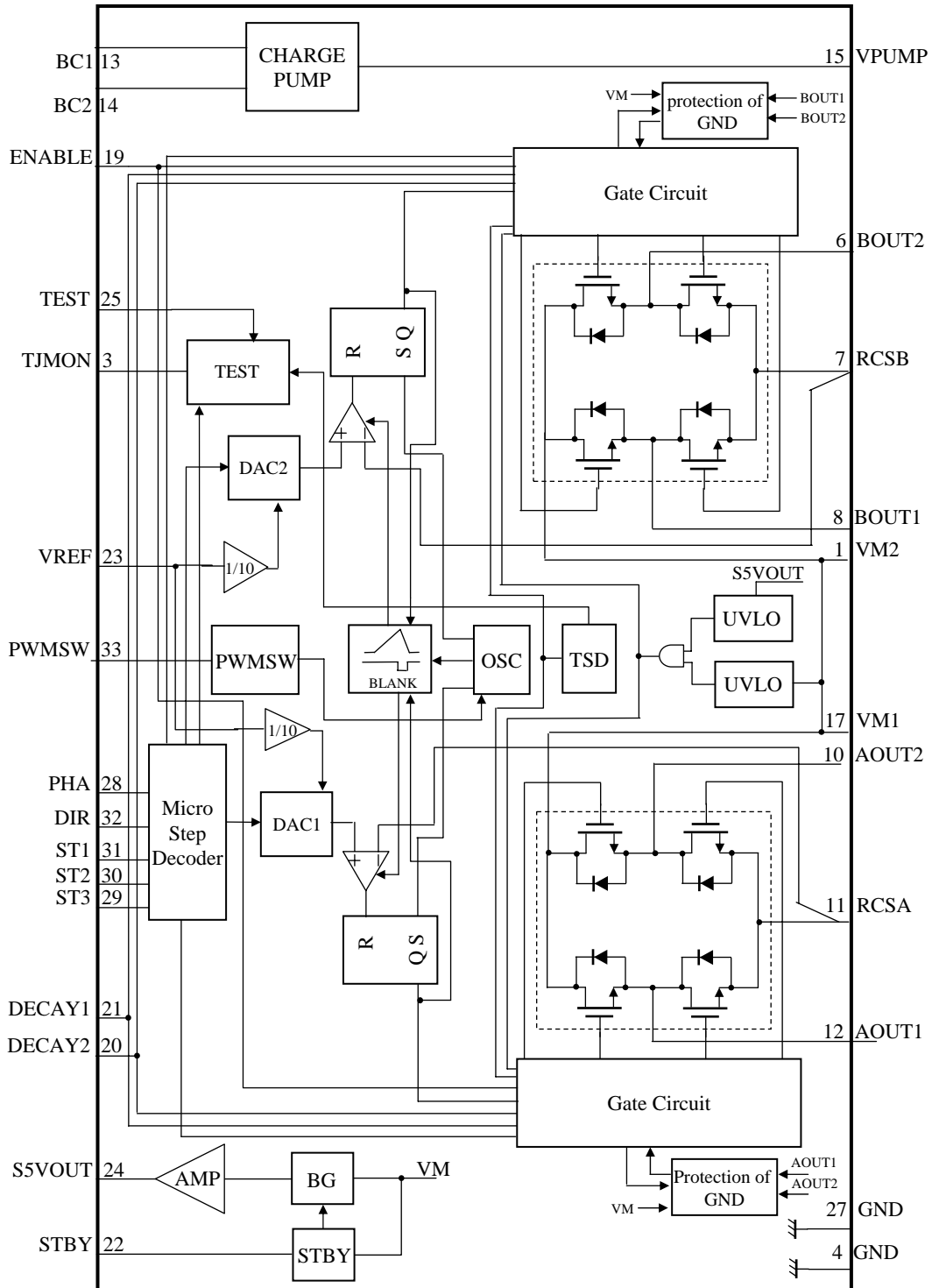
■ Application Circuit Example



Notes) • This application circuit is shown as an example but does not guarantee the design for mass production set.

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■ Block Diagram



Note) This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.

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### ■ Pin Descriptions

Pin No.	Pin name	Type	Description
1	VM2	Power supply	Motor power supply 2
2	N.C.	—	—
3	TJMON	Output	VBE monitor / Test output / Home Position output
4	GND	Ground	ground
5	N.C.	—	—
6	BOU2	Output	Phase B motor drive output 2
7	RCSB	Input / Output	Phase B current detection
8	BOU1	Output	Phase B motor drive output 1
9	GND	Ground	Die pad ground
10	AOU2	Output	Phase A motor drive output 2
11	RCSA	Input / Output	Phase A current detection
12	AOU1	Output	Phase A motor drive output 1
13	BC1	Output	Charge pump capacitor connection 1
14	BC2	Output	Charge pump capacitor connection 2
15	VPUMP	Output	Charge pump circuit output
16	N.C.	—	—
17	VM1	Power supply	Motor power supply 1
18	N.C.	—	—
19	ENABLE	Input	Enable / disable CTL
20	DECAY2	Input	Mix Decay setup 2
21	DECAY1	Input	Mix Decay setup 1
22	STBY	Input	Standby
23	VREF	Input	Torque reference voltage input
24	S5VOUT	Output	Internal reference voltage (output 5 V)
25	TEST	Input	Test mode
26	GND	Ground	Die pad ground
27	GND	Ground	Signal ground
28	PHA	Input	Clock input
29	ST3	Input	Step select 3
30	ST2	Input	Step select 2
31	ST1	Input	Step select 1
32	DIR	Input	Rotation direction
33	PWMSW	Input	PWM OFF period selection input
34	N.C.	—	—

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### ■ Absolute Maximum Ratings

Note) Absolute maximum ratings are limit values which are not destructed, and are not the values to which operation is guaranteed.

A No.	Parameter	Symbol	Rating	Unit	Notes
1	Supply voltage (Pin 1, 17)	$V_M$	37	V	*1
2	Power dissipation	$P_D$	0.466	W	*2
3	Operating ambient temperature	$T_{opr}$	-20 to +70	°C	*3
4	Storage temperature	$T_{stg}$	-55 to +150	°C	*3
5	Output pin voltage (Pin 6, 8, 10, 12)	$V_{OUT}$	37	V	*4
6	Motor drive current (Pin 6, 8, 10, 12)	$I_{OUT}$	±2.5	A	*5, *6
7	Flywheel diode current (Pin 6, 8, 10, 12)	$I_f$	2.5	A	*5, *6

Notes) \*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

\*2 : The power dissipation shown is the value at  $T_a = 70^\circ\text{C}$  for the independent (unmounted) IC package without a heat sink.

When using this IC, refer to the  $P_D$ - $T_a$  diagram of the package standard and design the heat radiation with sufficient margin so that the allowable value might not be exceeded based on the conditions of power supply voltage, load, and ambient temperature.

\*3 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for  $T_a = 25^\circ\text{C}$ .

\*4 : This is output voltage rating and do not apply input voltage from outside to these pins. Set not to exceed allowable range at any time.

\*5 : Do not apply external currents to any pin specially mentioned. For circuit currents, (+) denotes current flowing into the IC and (-) denotes current flowing out of the IC.

\*6 : Rating when cooling fin on the back side of the IC is connected to the GND pattern of the glass epoxy 4-layer board.

(GND area : 2nd-layer or 3rd-layer : more than 1 500 mm<sup>2</sup>)

In case of no cooling fin on the back side of the IC, rating current is 1.5 A on the glass epoxy 2-layer board.

### ■ Operating supply voltage range

Parameter	Symbol	Range	Unit	Notes
Supply voltage range	$V_M$	10.0 to 34.0	V	*

Notes) \* : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

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### ■ Allowable Current and Voltage Range

- Notes) • Voltage values, unless otherwise specified, are with respect to GND.  
• Do not apply external currents or voltages to any pin not specifically mentioned.  
• For the circuit currents, "+" denotes current flowing into the IC, and "-" denotes current flowing out of the IC.  
• Voltages and currents below show the limit value of nondestructive range which must not be exceeded in a moment.

Pin No.	Pin name	Rating	Unit	Notes
7	RCSB	2.5	V	—
11	RCSA	2.5	V	—
14	BC2	$(V_M - 1)$ to 43	V	*1
15	VPUMP	$(V_M - 2)$ to 43	V	*1
19	ENABLE	-0.3 to 6	V	—
20	DECAY2	-0.3 to 6	V	—
21	DECAY1	-0.3 to 6	V	—
22	STBY	-0.3 to 6	V	—
23	VREF	-0.3 to 6	V	—
25	TEST	-0.3 to 6	V	—
28	PHA	-0.3 to 6	V	—
29	ST3	-0.3 to 6	V	—
30	ST2	-0.3 to 6	V	—
31	ST1	-0.3 to 6	V	—
32	DIR	-0.3 to 6	V	—
33	PWMSW	-0.3 to 6	V	—

Pin No.	Pin name	Rating	Unit	Notes
3	TJMON	1	mA	*2
24	S5VOUT	-7 to 0	mA	—

注) \*1 : These are pins not applied voltage from outside. Set so that the rating must not be exceeded transiently.

\*2 : In case of TEST = High-level input, TJMON voltage is only Low-level. (Detail : refer to Electrical Characteristics No.52 described in Page 10).

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**■ Electrical Characteristics at  $V_M = 24.0\text{ V}$**

Note)  $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$  unless otherwise specified.

B No.	Parameter	Symbol	Test circuits	Conditions	Limits			Unit	Notes
					Min	Typ	Max		
<b>Output Drivers</b>									
1	High-level output saturation voltage	$V_{OH}$	2	$I = -1.2\text{ A}$	$V_M$ -0.75	$V_M$ -0.42	—	V	—
2	Low-level output saturation voltage	$V_{OL}$	2	$I = 1.2\text{ A}$	—	0.54	0.825	V	—
3	Flywheel diode forward voltage	$V_{DI}$	2	$I = 1.2\text{ A}$	0.5	1.0	1.5	V	—
4	Output leakage current	$I_{LEAK}$	2	$V_M = 37\text{ V}$ , $V_{RCS} = 0\text{ V}$	—	10	20	$\mu\text{A}$	—
5	Supply current (Active)	$I_M$	1	ENABLE = High, STBY = High	—	5.5	10	mA	—
6	Supply current (STBY)	$I_{MSTBY}$	1	STBY = Low	—	25	50	$\mu\text{A}$	—
<b>I/O Block</b>									
7	High-level STBY input voltage	$V_{STBYH}$	1	—	2.1	—	5.5	V	—
8	Low-level STBY input voltage	$V_{STBYL}$	1	—	0	—	0.6	V	—
9	High-level STBY input current	$I_{STBYH}$	1	STBY = 5 V	25	50	100	$\mu\text{A}$	—
10	Low-level STBY input current	$I_{STBYL}$	1	STBY = 0 V	-2	—	2	$\mu\text{A}$	—
11	High-level PHA input voltage	$V_{PHAH}$	1	—	2.1	—	5.5	V	—
12	Low-level PHA input voltage	$V_{PHAL}$	1	—	0	—	0.6	V	—
13	High-level PHA input current	$I_{PHAH}$	1	PHA = 5 V	25	50	100	$\mu\text{A}$	—
14	Low-level PHA input current	$I_{PHAL}$	1	PHA = 0 V	-2	—	2	$\mu\text{A}$	—
15	Highest-level PHA input frequency	$f_{PHA}$	1	—	—	—	100	kHz	—
16	High-level ENABLE input voltage	$V_{ENABLEH}$	1	—	2.1	—	5.5	V	—
17	Low-level ENABLE input voltage	$V_{ENABLEL}$	1	—	0	—	0.6	V	—
18	High-level ENABLE input current	$I_{ENABLEH}$	1	ENABLE = 5 V	25	50	100	$\mu\text{A}$	—
19	Low-level ENABLE input current	$I_{ENABLEL}$	1	ENABLE = 0 V	-2	—	2	$\mu\text{A}$	—
20	High-level PWMSW input voltage	$V_{PWMSWH}$	1	—	2.3	—	5.5	V	—
21	Middle-level PWMSW input voltage	$V_{PWMSWM}$	1	—	1.3	—	1.7	V	—
22	Low-level PWMSW input voltage	$V_{PWMSWL}$	1	—	0	—	0.6	V	—
23	High-level PWMSW input current	$I_{PWMSWH}$	1	PWMSW = 5 V	40	83	150	$\mu\text{A}$	—
24	Low-level PWMSW input current	$I_{PWMSWL}$	1	PWMSW = 0 V	-70	-36	-18	$\mu\text{A}$	—
25	PWMSW voltage at open	$V_{PWMSWO}$	1	—	1.3	1.5	1.7	V	—

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■ Electrical Characteristics (continued) at  $V_M = 24.0$  V

Note)  $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$  unless otherwise specified.

B No.	Parameter	Symbol	Test circuits	Conditions	Limits			Unit	Notes
					Min	Typ	Max		
26	High-level DECAF input voltage	$V_{\text{DECAFH}}$	1	—	2.1	—	5.5	V	—
27	Low-level DECAF input voltage	$V_{\text{DECAF L}}$	1	—	0	—	0.6	V	—
28	High-level DECAF input current	$I_{\text{DECAFH}}$	1	DECAF1 = DECAF2 = 5 V	25	50	100	$\mu\text{A}$	—
29	Low-level DECAF input current	$I_{\text{DECAF L}}$	1	DECAF1 = DECAF2 = 0 V	-2	—	2	$\mu\text{A}$	—
30	High-level DIR input voltage	$V_{\text{DIRH}}$	1	—	2.1	—	5.5	V	—
31	Low-level DIR input voltage	$V_{\text{DIR L}}$	1	—	0	—	0.6	V	—
32	High-level DIR input current	$I_{\text{DIRH}}$	1	DIR = 5 V	25	50	100	$\mu\text{A}$	—
33	Low-level DIR input current	$I_{\text{DIR L}}$	1	DIR = 0 V	-2	—	2	$\mu\text{A}$	—
34	High-level ST input voltage	$V_{\text{STH}}$	1	—	2.1	—	5.5	V	—
35	Low-level ST input voltage	$V_{\text{ST L}}$	1	—	0	—	0.6	V	—
36	High-level ST input current	$I_{\text{STH}}$	1	ST1 = ST2 = ST3 = 5 V	25	50	100	$\mu\text{A}$	—
37	Low-level ST input current	$I_{\text{ST L}}$	1	ST1 = ST2 = ST3 = 0 V	-2	—	2	$\mu\text{A}$	—
38	High-level TEST input voltage	$V_{\text{TESTH}}$	1	—	4.0	—	5.5	V	—
39	Middle-level TEST input voltage	$V_{\text{TESTM}}$	1	—	2.3	—	2.7	V	—
40	Low-level Test input voltage	$V_{\text{TEST L}}$	1	—	0	—	0.6	V	—
41	High-level TEST input current	$I_{\text{TESTH}}$	1	TEST = 5 V	25	50	100	$\mu\text{A}$	—
42	Low-level TEST input current	$I_{\text{TEST L}}$	1	TEST = 0 V	-2	—	2	$\mu\text{A}$	—
<b>Torque Control Block</b>									
43	Input bias current 1	$I_{\text{REFH}}$	1	$V_{\text{REF}} = 5$ V	-15	—	5	$\mu\text{A}$	—
44	Input bias current 2	$I_{\text{REF L}}$	1	$V_{\text{REF}} = 0$ V	-2	—	2	$\mu\text{A}$	—
45	PWM OFF time 1	$T_{\text{OFF1}}$	1	PWMSW = Low	16.8	28	39.2	$\mu\text{s}$	—
46	PWM OFF time 2	$T_{\text{OFF2}}$	1	PWMSW = Middle	9.1	15.2	21.3	$\mu\text{s}$	—
47	PWM OFF time 3	$T_{\text{OFF3}}$	1	PWMSW = High	4.9	8.1	11.3	$\mu\text{s}$	—
48	Pulse blanking time	$T_{\text{B}}$	1	$V_{\text{REF}} = 0$ V	0.4	0.7	1.0	$\mu\text{s}$	—
49	Comp threshold	$V_{\text{T}_{\text{CMP}}}$	1	$V_{\text{REF}} = 5$ V	475	500	525	mV	—
<b>Reference Voltage Block</b>									
50	Reference voltage	$V_{\text{SSVOUT}}$	1	$I_{\text{SSVOUT}} = 0$ mA	4.75	5.0	5.25	V	—
51	Output impedance	$Z_{\text{SSVOUT}}$	1	$I_{\text{SSVOUT}} = -7$ mA	—	—	10	$\Omega$	—
<b>Home Position Block</b>									
52	At TEST High-level input TJMON output Low-level voltage	$V_{\text{TJL}}$	1	Pull up TJMON pin to 5 V with 100 k $\Omega$ .	—	0.1	0.3	V	—
53	At TEST High-level input TJMON output leakage current	$I_{\text{TJ(leak)}}$	1	$V_{\text{TJMON}} = 5$ V	—	—	5	$\mu\text{A}$	—

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■ **Electrical Characteristics (Reference values for design) at  $V_M = 24\text{ V}$**

Notes)  $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$  unless otherwise specified.

The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.

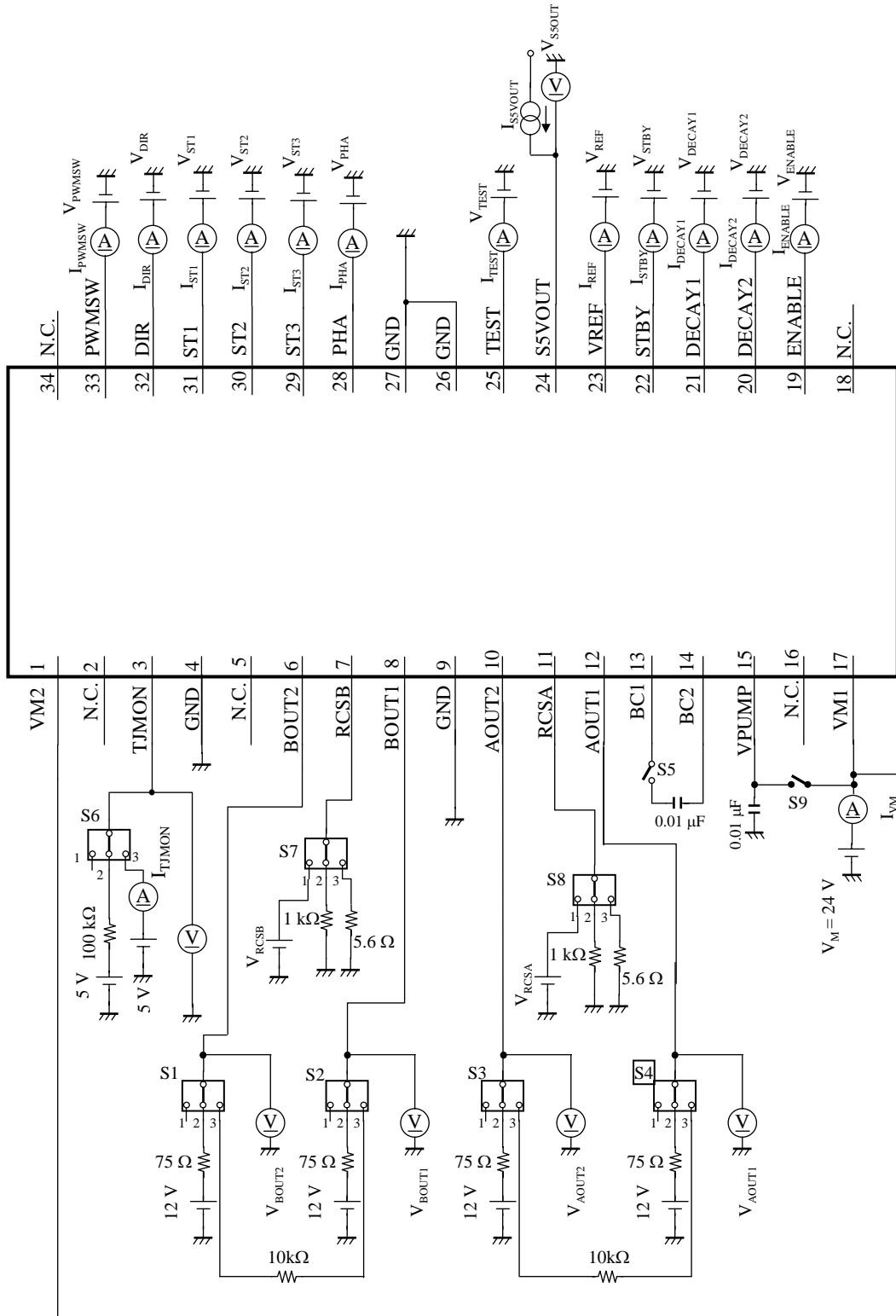
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Test circuits	Conditions	Reference values			Unit	Notes
					Min	Typ	Max		
<b>Output Drivers</b>									
54	Output slew rate 1	$VT_r$	—	Output voltage rise	—	220	—	V/ $\mu\text{s}$	—
55	Output slew rate 2	$VT_f$	—	Output voltage fall	—	200	—	V/ $\mu\text{s}$	—
56	Dead time	$T_D$	—	—	—	0.8	—	$\mu\text{s}$	—
<b>Thermal Protection</b>									
57	Thermal protection operating temperature	$TSD_{on}$	—	—	—	150	—	$^\circ\text{C}$	—
58	Thermal protection hysteresis width	$\Delta TSD$	—	—	—	40	—	$^\circ\text{C}$	—
<b>Low voltage Protection</b>									
59	Protection operating voltage	$V_{UVLO1}$	—	—	—	7.9	—	V	—
60	Protection releasing voltage	$V_{UVLO2}$	—	—	—	8.7	—	V	—

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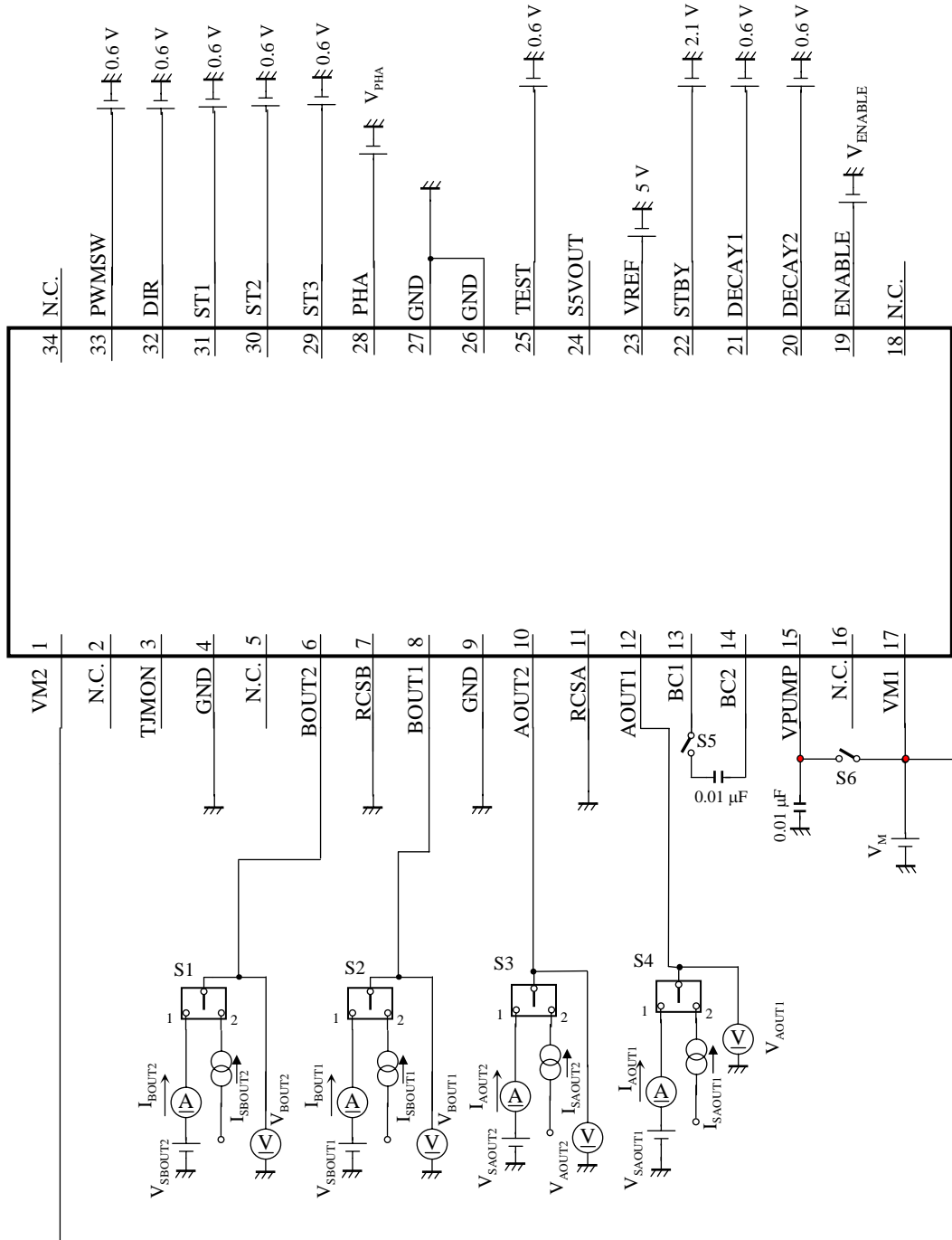
■ Test Circuit Diagram

1. Test Circuit 1



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■ Test Circuit Diagram  
2. Test Circuit 2



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## ■ Electrical Characteristics Test Procedures

### 1. Test Circuit 1

C No.	Measuring pin	S1 to S4	S5	S6	S7, S8	S9	V <sub>PHA</sub>	V <sub>DECAY1</sub> V <sub>DECAY2</sub>	V <sub>STBY</sub>	V <sub>ENABLE</sub>	V <sub>PWMSW</sub>	V <sub>RCSA</sub> V <sub>RCSB</sub>	V <sub>DIR</sub>	V <sub>ST1</sub> V <sub>ST2</sub> V <sub>ST3</sub>	V <sub>TEST</sub>	V <sub>REF</sub>	I <sub>S5VOUT</sub>
5, 7	1, 17, 22	1	ON	1	1	OFF	0 V	5.5 V	2.1 V	2.1 V	5.5 V	0 V	5.5 V	5.5 V	0.6 V	5 V	Hi-Z
6, 8	1, 17, 22	1	ON	1	1	OFF	0.6 V	0.6 V	0.6 V	2.1 V	0.6 V	0 V	0.6 V	0.6 V	0.6 V	5 V	Hi-Z
50	24	1	ON	1	1	OFF	0 V	5.5 V	2.1 V	0.6 V	5.5 V	0 V	5.5 V	5.5 V	0.6 V	5 V	Hi-Z
51	24	1	ON	1	1	OFF	0 V	5.5 V	2.1 V	0.6 V	5.5 V	0 V	5.5 V	5.5 V	0.6 V	5 V	-7 mA
9, 13, 18, 23, 28, 32, 36, 41	19 to 22, 25, 28 to 33	3	ON	1	1	OFF	5 V	5 V	5 V	5 V	5 V	0 V	5 V	5 V	5 V	5 V	Hi-Z
14, 19, 24, 29, 33, 37, 42	19 to 21, 25, 28 to 33	3	ON	1	1	OFF	0 V	0 V	5 V	0 V	0 V	0 V	0 V	0 V	0 V	5 V	Hi-Z
10	22	3	ON	1	1	OFF	0 V	0 V	0 V	0 V	0 V	0 V	0 V	0 V	0 V	5 V	Hi-Z
43	23	1	ON	1	1	OFF	0 V	0 V	2.1 V	0 V	0 V	0 V	0 V	0 V	0 V	5 V	Hi-Z
44	23	1	ON	1	1	OFF	0 V	0 V	2.1 V	0 V	0 V	0 V	0 V	0 V	0 V	0 V	Hi-Z
16	6, 8, 10, 12, 19	2	ON	1	1	OFF	0 V	0 V	2.1 V	2.1 V	0 V	0 V	0.6 V	0.6 V	0 V	5 V	Hi-Z
17	6, 8, 10, 12, 19	2	ON	1	1	OFF	0 V	0 V	2.1 V	0.6 V	0 V	0 V	0.6 V	0.6 V	0 V	5 V	Hi-Z
49	6, 7, 8, 10, 11, 12	3	OFF	1	2	ON	5 V	0 V	2.1 V	0.6 V	0 V	0.475 V, 0.525 V	0.6 V	0.6 V	0 V	5 V	Hi-Z
11, 12, 15	6, 8, 10, 12, 28	2	ON	1	1	OFF	0.6 V to 2.1 V 200 kHz pulse	0.6 V	2.1 V	0.6 V	5 V	0 V	0.6 V	0.6 V	0.6 V	5 V	Hi-Z
25	33	1	ON	1	1	OFF	0 V	0 V	2.1 V	0 V	Hi-Z	0 V	0 V	0 V	0 V	0 V	Hi-Z
38, 39, 40	3, 6, 8, 10, 12, 25	2	ON	1 or 2	1	OFF	2.1 V	V <sub>DECAY1</sub> = 0.6 V V <sub>DECAY2</sub> = 2.1 V	5 V	0.6 V	0.6 V	0 V	0.6 V	0.6 V	0.6 V, 2.3 V, 2.7 V, 4.0 V	5 V	Hi-Z

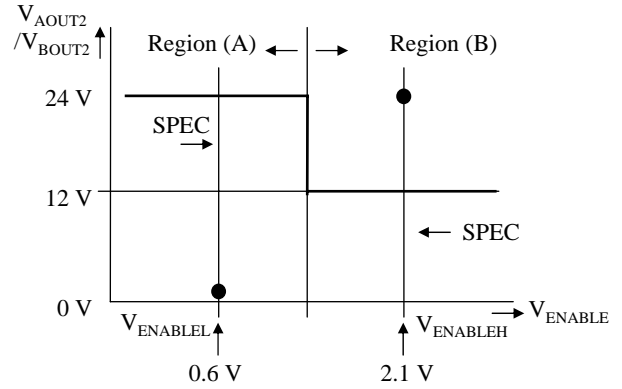
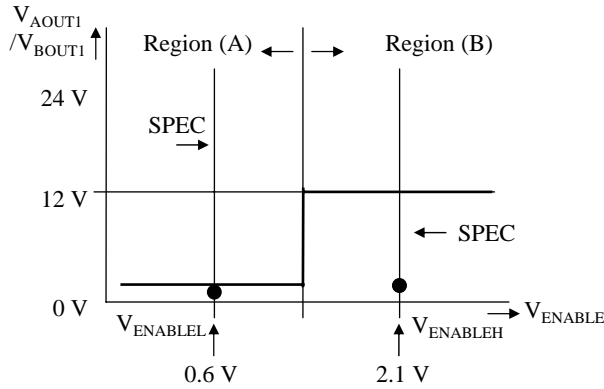
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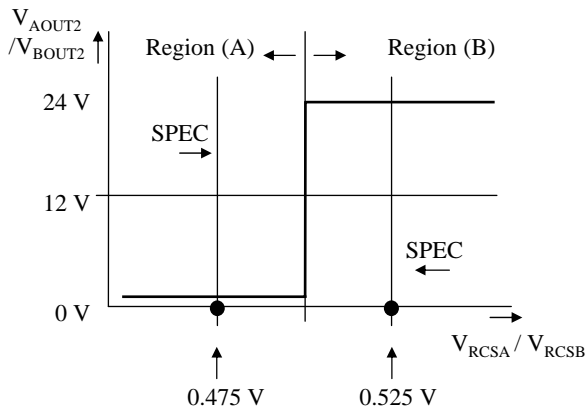
■ Electrical Characteristics Test Procedures (continued)

1. Test Circuit 1 (continued)

- 16) ENABLE High-level input voltage  $V_{ENABLEH}$
- 17) ENABLE Low-level input voltage  $V_{ENABLEL}$



49) Comp threshold  $V_{TCMP}$

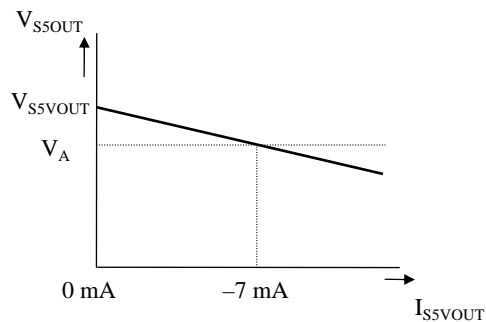


Check the conditions by measuring  $V_{AOUT2}$  and  $V_{BOUT2}$  voltage with the input voltage set to 0.475 V and 0.525 V respectively.

Region (A) : Always output Low-level  
 Region (B) : Output Low-level with minimum duty



51) Output impedance  $Z_{SSVOUT}$



$$Z_{SSVOUT} = \frac{V_{SSVOUT} - V_A}{7 \text{ mA}}$$

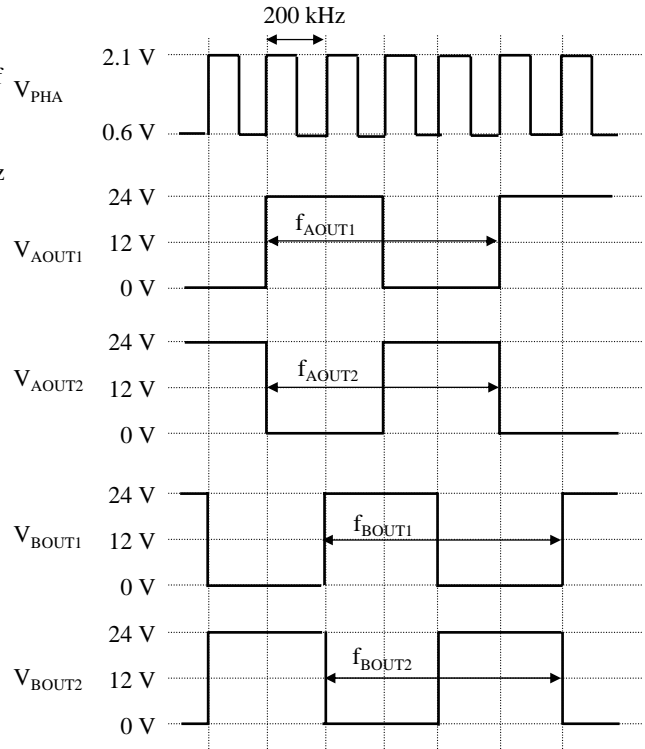
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■ Electrical Characteristics Test Procedures (continued)

1. Test Circuit 1 (continued)

- |                                  |            |
|----------------------------------|------------|
| 11) PHA High-level input voltage | $V_{PHAH}$ |
| 12) PHA Low-level input voltage  | $V_{PHAL}$ |
| 15) PHA Highest input frequency  | $f_{PHA}$  |

Check PHA High, Low and Highest input voltage in case of input of the pulse of 200 kHz (Low-level voltage = 0.6 V, High-level voltage = 2.1 V) to PHA and the frequency of  $V_{AOUT1}$ ,  $V_{AOUT2}$ ,  $V_{BOUT1}$ ,  $V_{BOUT2}$  = 50 kHz as the timing chart in the right figure.



- |                                     |             |
|-------------------------------------|-------------|
| 38) TEST High-level input voltage   | $V_{TESTH}$ |
| 39) TEST Middle-level input voltage | $V_{TESTM}$ |
| 40) TEST Low-level input voltage    | $V_{TESTL}$ |

Check that output status follows as the below chart when Low-level (0.6 V), Middle-level (2.3 V, 2.7 V) and High-level (4.0 V) are applied to TEST pin.

Chart Output status at input voltage of Low, Middle, High-level

Parameter	TEST pin voltage conditions	S6	Status
TEST Low-level input voltage	0.6 V	1	TJMON pin = VBE monitor
TEST Middle-level input voltage	2.3 V / 2.7 V	1	Output transistor : all OFF $V_{AOUT1}$ , $V_{AOUT2}$ , $V_{BOUT1}$ , $V_{BOUT2}$ = 12 V
TEST High-level input voltage	4.0 V	2	TJMON pin = Home Position output (For detail, refer to Page 36, 37)

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■ Electrical Characteristics Test Procedures (continued)

1. Test Circuit 1 (continued)

C No.	Measuring pin	S1 to S4	S5	S6	S7, S8	S9	V <sub>PHA</sub>	V <sub>DECAY1</sub> V <sub>DECAY2</sub>	V <sub>STBY</sub>	V <sub>ENABLE</sub>	V <sub>PWMSW</sub>	V <sub>RCSA</sub> V <sub>RCSB</sub>	V <sub>DIR</sub>	V <sub>ST1</sub> V <sub>ST2</sub> V <sub>ST3</sub>	V <sub>TEST</sub>	V <sub>RE F</sub>	I <sub>SSVOUT</sub>
30, 31, 34, 35	6, 8, 10, 12, 28 to 32	2	ON	1	1	OFF	Pulse input	V <sub>DECAY1</sub> = 2.1 V V <sub>DECAY2</sub> = 2.1 V	2.1 V	0.6 V	0.6 V	0 V	Refer to below chart	Refer to below chart	0.6 V	5 V	Hi-Z
20, 21, 22, 26, 27, 45, 46, 47, 48	6, 8, 10, 12, 20, 21, 28, 33	2	ON	1	3	OFF	Pulse input	Refer to the next page	2.1 V	0.6 V	Refer to the next page	—	0.6 V	0.6 V	0.6 V	0 V	Hi-Z
52, 53	3	1	ON	2 or 3	1	OFF	Pulse input	V <sub>DECAY1</sub> = 2.1 V V <sub>DECAY2</sub> = 2.1 V	2.1 V	0.6 V	0.6 V	0 V	0.6 V	V <sub>ST1</sub> = V <sub>ST2</sub> = 0.6 V V <sub>ST3</sub> = 2.1 V	4 V	5 V	Hi-Z

- 30) DIR High -level input voltage
- 31) DIR Low-level input voltage
- 34) ST High-level input voltage
- 35) ST Low-level input voltage

- V<sub>DIRH</sub>
- V<sub>DIRL</sub>
- V<sub>STH</sub>
- V<sub>STL</sub>

DIR	ST1	ST2	ST3	Exciting mode
0.6 V	0.6 V	0.6 V	0.6 V	2 phase excitation drive (4-step sequence) / Forward
0.6 V	0.6 V	2.1 V	0.6 V	Half-step drive (8-step sequence) / Forward
0.6 V	2.1 V	0.6 V	0.6 V	1-2 phase excitation drive (8-step sequence) / Forward
0.6 V	2.1 V	2.1 V	0.6 V	W1-2-phase drive (16-stepsequence) / Forward
0.6 V	0.6 V	2.1 V	2.1 V	2W1-2-phase drive (32-step sequence) / Forward
2.1 V	0.6 V	0.6 V	0.6 V	2 phase excitation drive (4-step sequence) / Reverse
2.1 V	0.6 V	2.1 V	0.6 V	Half-step drive (8-step sequence) / Reverse
2.1 V	2.1 V	0.6 V	0.6 V	1-2-phase excitation (8-step sequence) / Reverse
2.1 V	2.1 V	2.1 V	0.6 V	W1-2 phase drive (16-step sequence) / Reverse
2.1 V	0.6 V	2.1 V	2.1 V	2W1-2-phase driver (32-step sequence) / Reverse

Check the DIR Low/High input voltage and ST Low/High input voltage by setting the voltages of DIR, ST1, ST2, ST3 to voltages following to the above chart and checking the operation of each excitation mode (Page 31 to 34).

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■ Electrical Characteristics Test Procedures (continued)

1. Test Circuit 1 (continued)

20) PWMSW High-level input voltage	$V_{PWMSWH}$
21) PWMSW Middle-level input voltage	$V_{PWMSWM}$
22) PWMSW Low-level input voltage	$V_{PWMSWL}$
26) DECAY High-level input voltage	$V_{DECAYH}$
27) DECAY Low-level input voltage	$V_{DECAYL}$
45) PWM OFF time 1	$T_{OFF1}$
46) PWM OFF time 2	$T_{OFF2}$
47) PWM OFF time 3	$T_{OFF3}$
48) Pulse blanking time	$T_B$

Each value is obtained by the timing chart of  $V_{AOUT1}(V_{BOUT1})$  and  $V_{AOUT2}(V_{BOUT2})$  at  $V_{REF} = 0\text{ V}$

The timing chart of  $V_{AOUT1}(V_{BOUT1})/V_{AOUT2}(V_{BOUT2})$  is shown as below.

- For 20) to 22), 45) to 47), check  $T_{OFF1}/T_{OFF2}/T_{OFF3}$  on the input conditions of PWMSW pin in the below chart.
- For 26), 27), check  $T_{DECAY}/T_{OFF}$  on the conditions of DECAY1/DECAY2 in the below chart in case of PWMSW High, Middle, Low-level input voltage.
- For 48), check Low-level interval of  $V_{AOUT1}(V_{BOUT1}) : T_B$  in the below chart.

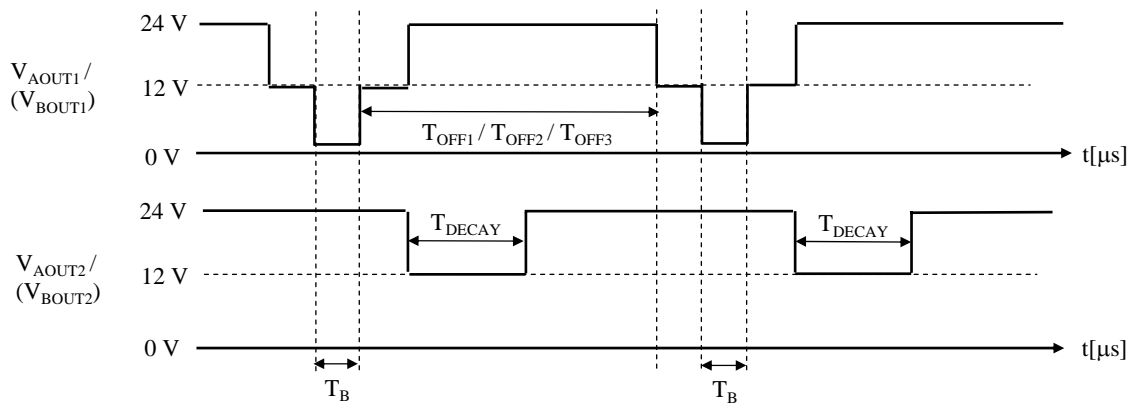


Chart  $T_{OFF}$  to PWMSW input voltage

Input pin	Voltage conditions	Status
	$V_{PWMSWH} / V_{PWMSWM} / V_{PWMSWL}$	
PWMSW	0.6 V	$T_{OFF1} = 28\ \mu\text{s}$
	1.3 V	$T_{OFF2} = 15.2\ \mu\text{s}$
	1.7 V	$T_{OFF2} = 15.2\ \mu\text{s}$
	2.3 V	$T_{OFF3} = 8.1\ \mu\text{s}$

Chart Decay control to DECAY1/2 input voltage

DECAY1	DECAY2	Decay control ( $T_{DECAY} / T_{OFF}$ )
0.6 V	0.6 V	0% mode (Slow Decay)
0.6 V	2.1 V	25% mode
2.1 V	0.6 V	50% mode
2.1 V	2.1 V	100% mode

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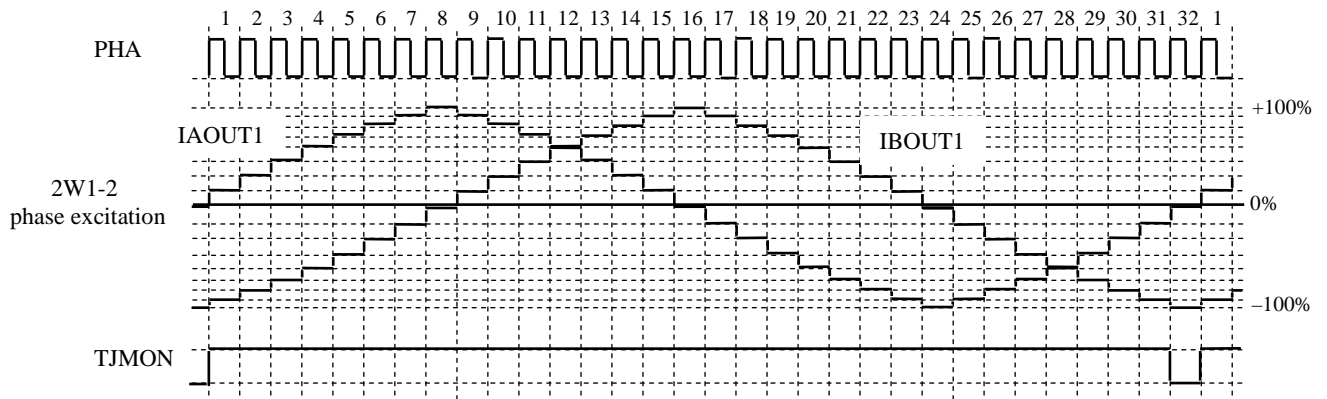
■ Electrical Characteristics Test Procedures (continued)

1. Test Circuit 1 (continued)

- 52) TJMON pin output Low-level voltage at TEST pin High-level input  $V_{TJL}$
- 53) TJMON pin output leakage current at TEST pin High-level input  $I_{TJ(leak)}$

Check when TJMON pin in Home Position output timing chart is Low and High-level.

- TJMON pin output Low-level voltage at TEST pin High-level input  $V_{TJL}$   
 → Check TJMON pin voltage by connection pull-up resistor 100 kΩ (to 5 V) to TJMON pin.
- TJMON pin output leakage current at TEST High-level input  $I_{TJ(leak)}$   
 → Check the leakage current after applying 5 V to TJMON pin.



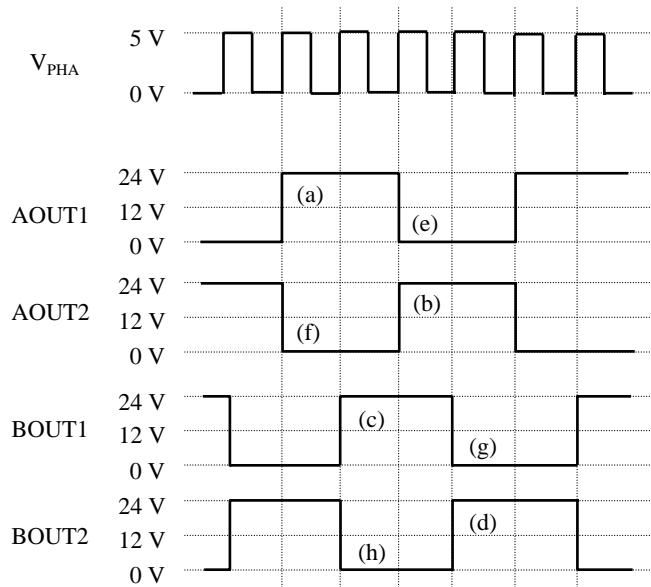
Home Position output timing chart (DIR = Low-level)

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■ Electrical Characteristics Test Procedures (continued)

2. Test Circuit 2

- 1) Output saturation voltage High-level  $V_{OH}$   
 2) Output saturation voltage Low-level  $V_{OL}$



Check output saturation voltage High and Low-level on the below conditions

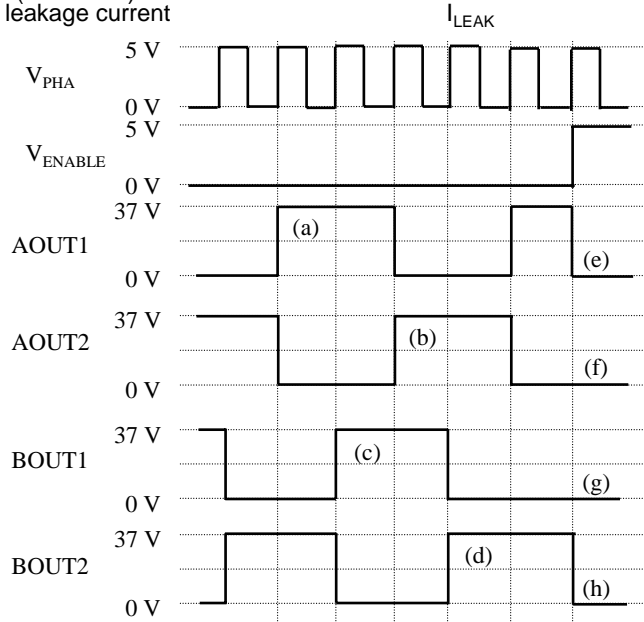
	(a)	(b)	(c)	(d)	(e)	(f)	(g)	(h)
Applying pin/ measuring voltage	AOUT1/ $V_{AOUT1}$	AOUT2/ $V_{AOUT2}$	BOUT1/ $V_{BOUT1}$	BOUT2/ $V_{BOUT2}$	AOUT1/ $V_{AOUT1}$	AOUT2/ $V_{AOUT2}$	BOUT1/ $V_{BOUT1}$	BOUT2/ $V_{BOUT2}$
Applying conditions	$I_{SAOUT1} = -1.2\text{ A}$	$I_{SAOUT2} = -1.2\text{ A}$	$I_{SBOUT1} = -1.2\text{ A}$	$I_{SBOUT2} = -1.2\text{ A}$	$I_{SAOUT1} = +1.2\text{ A}$	$I_{SAOUT2} = +1.2\text{ A}$	$I_{SBOUT1} = +1.2\text{ A}$	$I_{SBOUT2} = +1.2\text{ A}$
S1 to S4	2	2	2	2	2	2	2	2
S5	ON	ON	ON	ON	ON	ON	ON	ON
S6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
$V_M$	24 V	24 V	24 V	24 V	24 V	24 V	24 V	24 V
$V_{ENABLE}$	0.6 V	0.6 V	0.6 V	0.6 V	0.6 V	0.6 V	0.6 V	0.6 V

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■ Electrical Characteristics Test Procedures (continued)

2. Test Circuit 2 (continued)

4) Output leakage current



	(a)	(b)	(c)	(d)	(e), (f), (g), (h)
Applying pin/ measuring current	AOUT1 / $I_{AOUT1}$	AOUT2 / $I_{AOUT2}$	BOUT1 / $I_{BOUT1}$	BOUT2 / $I_{BOUT2}$	AOUT1, AOUT2, BOUT1, BOUT2 / $I_{AOUT1}, I_{AOUT2}, I_{BOUT1}, I_{BOUT2}$
Applying conditions	$V_{SAOUT1} = 37\text{ V}$	$V_{SAOUT2} = 37\text{ V}$	$V_{SBOUT1} = 37\text{ V}$	$V_{SBOUT2} = 37\text{ V}$	$V_{SAOUT1} = V_{SAOUT2} = V_{SBOUT1} = V_{SBOUT2} = 0\text{ V}$
S1 to S4	1	1	1	1	1
S5	OFF	OFF	OFF	OFF	ON
S6	ON	ON	ON	ON	OFF
$V_M$	37 V	37 V	37 V	37 V	37 V
$V_{ENABLE}$	0 V	0 V	0 V	0 V	5 V

Check output leakage current  $I_{LEAK}$  \*1 of each output pin on the above conditions

Note) \*1  $I_{LEAK}$ : Electrical characteristics No.4 shows absolute values.

3) Flywheel diode forward voltage

$V_{DI}$

Applying pin/ Measuring voltage	AOUT1 / $V_{AOUT1}$	AOUT2 / $V_{AOUT2}$	BOUT1 / $V_{BOUT1}$	BOUT2 / $V_{BOUT2}$
Applying conditions	$I_{SAOUT1} = 1.2\text{ A}$	$I_{SAOUT2} = 1.2\text{ A}$	$I_{SBOUT1} = 1.2\text{ A}$	$I_{SBOUT2} = 1.2\text{ A}$
S1 to S4	2	2	2	2
S5	ON	ON	ON	ON
S6	ON	ON	ON	ON
$V_M$	0 V	0 V	0 V	0 V
$V_{ENABLE}$	2.1 V	2.1 V	2.1 V	2.1 V

Check Flywheel diode forward voltage  $V_{DI}$  on the above conditions

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■ Technical Data

1. I/O block circuit diagrams and pin function descriptions

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
3	—	<p>Pin3 TJMON</p>	—	<p>Pin 3 : VBE monitor /TEST output /Home Position output</p>
6 7 8 10 11 12	—	<p>Pin 6 BOUT2 8 BOUT1 10 AOUT2 12 AOUT1</p> <p>Pin 7 RCSB 11 RCSA</p>	—	<p>Pin 6 : Phase B motor drive output 2 7 : Phase B current detection 8 : Phase B motor drive output 1 10 : Phase A motor drive output 2 11 : Phase A current detection 12 : Phase A motor drive output 1</p>

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■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
13	—		—	Pin 13 : Charge pump capacitor connection 1
14 15	—		—	Pin 14 : Charge pump capacitor connection 2 Pin 15 : Charge pump circuit output

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■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
19 20 21 28 29 30 31 32	—	<p>Pin19 ENABLE 20 DECAY2 21 DECAY1 28 PHA 29 ST3 30 ST2 31 ST1 32 DIR</p>	100 kΩ	<p>Pin 19 : Enable/disable CTL 20 : Mix Decay setup 2 21 : Mix Decay setup 1 28 : Clock input 29 : Step select 3 30 : Step select 2 31 : Step select 1 32 : Rotation direction</p>
22	—	<p>Pin22 STBY</p>	100 kΩ	<p>Pin 22 : Standby</p>

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■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
23	—	<p style="text-align: center;">Pin23 VREF</p>	—	Pin 23 : Torque reference voltage input
24	—	<p style="text-align: center;">Pin24 S5VOUT</p>	—	Pin 24 : Internal reference voltage (Output 5 V)

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■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
25	—	<p>Pin25 TEST</p>	100 kΩ	Pin 25 : TEST mode
33	—	<p>Pin33 PWMSW</p>	—	Pin 33 : PWM OFF period selection input

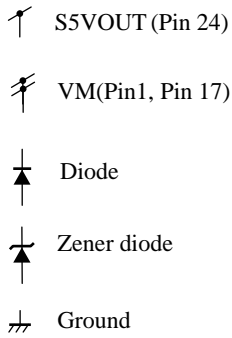





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■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
—	—	 <p>  S5VOUT (Pin 24)   VM (Pin 1, Pin 17)   Diode   Zener diode   Ground         </p>	—	—

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■ Technical Data (continued)

2. Control mode

1) Truth table (Step select)

ENABLE	DIR	ST1	ST2	ST3	Output excitation mode (Phase B 90° delay : to Phase A)
High	—	—	—	—	Output OFF
Low	Low	Low	Low	Low	2 phase excitation drive (4-step sequence)
Low	Low	Low	High	Low	Half-step drive (8-step sequence)
Low	Low	High	Low	Low	1-2 phase excitation drive (8-step sequence)
Low	Low	High	High	Low	W1-2 phase excitation drive (16-step sequence)
Low	Low	—	—	High	2W1-2 phase excitation drive (32-step sequence)

ENABLE	DIR	ST1	ST2	ST3	Output excitation mode (Phase B 90° advance : to Phase A)
High	—	—	—	—	Output OFF
Low	High	Low	Low	Low	2 phase excitation drive (4-step sequence)
Low	High	Low	High	Low	Half-step drive (8-step sequence)
Low	High	High	Low	Low	1-2 phase excitation drive (8-step sequence)
Low	High	High	High	Low	W1-2 phase drive (16-step sequence)
Low	High	—	—	High	2W1-2 phase drive (32-step sequence)

2) Truth table (Control/Charge pump circuit)

STBY	ENABLE	Control /Charge pump circuit	Output transistor
Low	—	OFF	OFF
High	High	ON	OFF
High	Low	ON	ON

3) Truth table (PWM OFF period selection)

PWMSW	PWM OFF period
Low	28.0 μs
Middle	15.2 μs
High	8.1 μs

4) Truth table (Decay selection)

DECAY1	DECAY2	Decay control
Low	Low	Slow Decay
Low	High	25%
High	Low	50%
High	High	100%

5) Truth table (Test mode)

TEST	TJMON
Low	VBE monitor
Middle	Test output (Output transistor : OFF)
High	Home Position output

Note) For each PWM OFF period, Fast Decay is applied according to the above table.

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■ Technical Data (continued)

3. Each phase current value

1) 1-2 phase, W1-2 phase, 2W1-2 phase DIR = Low

Note) The definition of Phase A and B current 「100%」 :  $(VREF \times 0.1) / \text{Current detection resistance}$

1-2 phase (8 Step)	W1-2 phase (16 Step)	2W1-2 phase (32 Step)	Phase A current (%)	Phase B current (%)
		1	19.5	-98.1
	1	2	38.3	-92.4
		3	55.6	-83.2
1	2	4	70.7	-70.7
		5	83.2	-55.6
	3	6	92.4	-38.3
		7	98.1	-19.5
2	4	8	100	0
		9	98.1	19.5
	5	10	92.4	38.3
		11	83.2	55.6
3	6	12	70.7	70.7
		13	55.6	83.2
	7	14	38.3	92.4
		15	19.5	98.1
4	8	16	0	100
		17	-19.5	98.1
	9	18	-38.3	92.4
		19	-55.6	83.2
5	10	20	-70.7	70.7
		21	-83.2	55.6
	11	22	-92.4	38.3
		23	-98.1	19.5
6	12	24	-100	0
		25	-98.1	-19.5
	13	26	-92.4	-38.3
		27	-83.2	-55.6
7	14	28	-70.7	-70.7
		29	-55.6	-83.2
	15	30	-38.3	-92.4
		31	-19.5	-98.1
8	16	32	0	-100

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■ Technical Data (continued)

3. Each phase current value (continued)

1) 1-2 phase, W1-2 phase, 2W1-2 phase DIR = High

Note) The definition of Phase A and B current 「100%」 :  $(VREF \times 0.1) / \text{Current detection resistance}$

1-2 phase (8 Step)	W1-2 phase (16 Step)	2W1-2 phase (32 Step)	Phase A current (%)	Phase B current (%)
		1	-19.5	-98.1
	1	2	-38.3	-92.4
		3	-55.6	-83.2
1	2	4	-70.7	-70.7
		5	-83.2	-55.6
	3	6	-92.4	-38.3
		7	-98.1	-19.5
2	4	8	-100	0
		9	-98.1	19.5
	5	10	-92.4	38.3
		11	-83.2	55.6
3	6	12	-70.7	70.7
		13	-55.6	83.2
	7	14	-38.3	92.4
		15	-19.5	98.1
4	8	16	0	100
		17	19.5	98.1
	9	18	38.3	92.4
		19	55.6	83.2
5	10	20	70.7	70.7
		21	83.2	55.6
	11	22	92.4	38.3
		23	98.1	19.5
6	12	24	100	0
		25	98.1	-19.5
	13	26	92.4	-38.3
		27	83.2	-55.6
7	14	28	70.7	-70.7
		29	55.6	-83.2
	15	30	38.3	-92.4
		31	19.5	-98.1
8	16	32	0	-100

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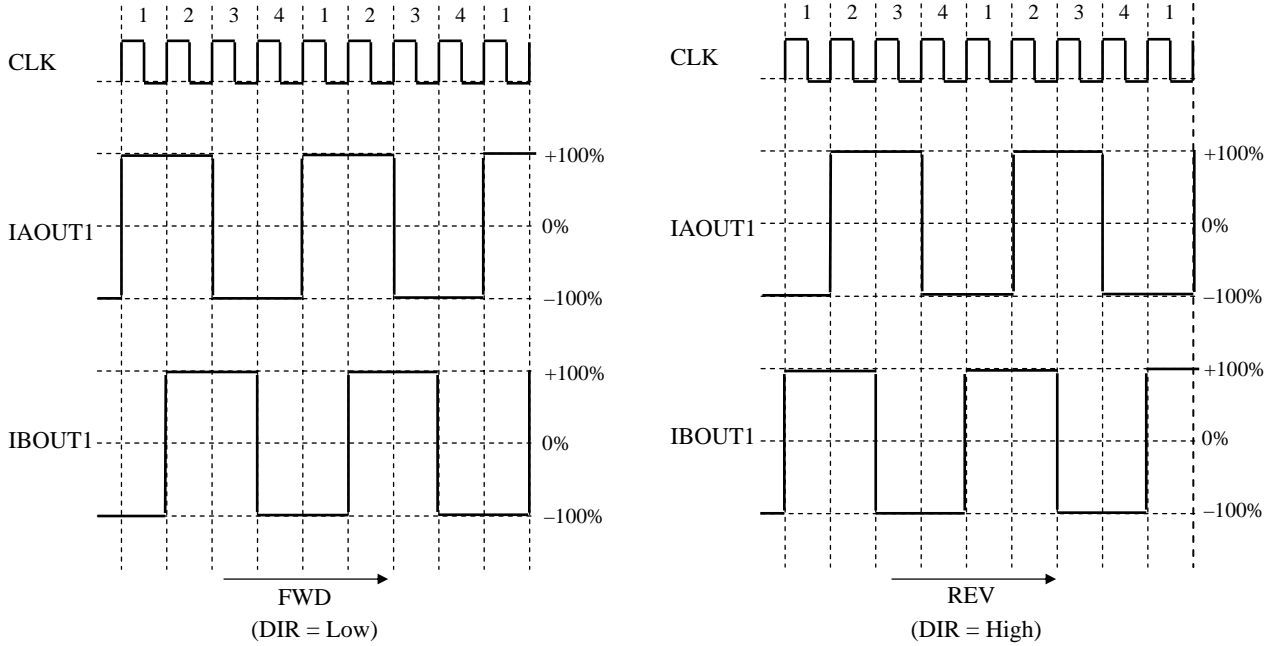


■ Technical Data (continued)

4. Each phase current (Timing chart)

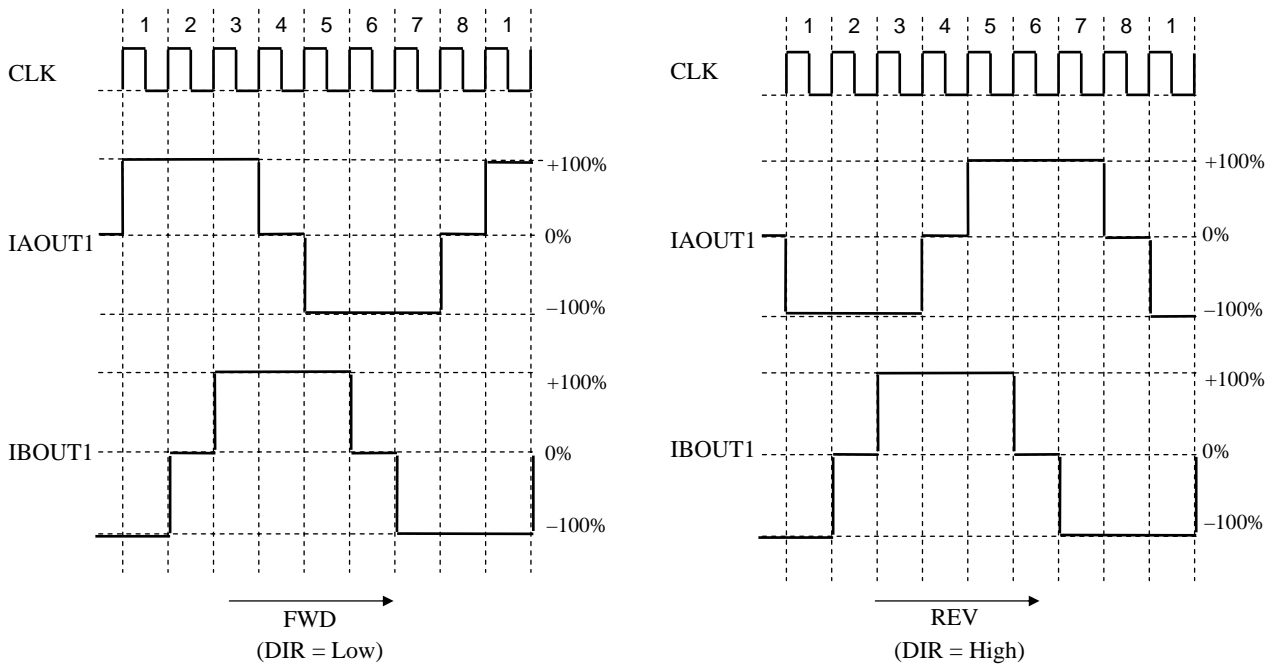
1) 2 phase excitation drive (4-step sequence)

(ST1 = Low, ST2 = Low, ST3 = Low)



2) Half-step drive (8-step sequence)

(ST1 = Low, ST2 = High, ST3 = Low)



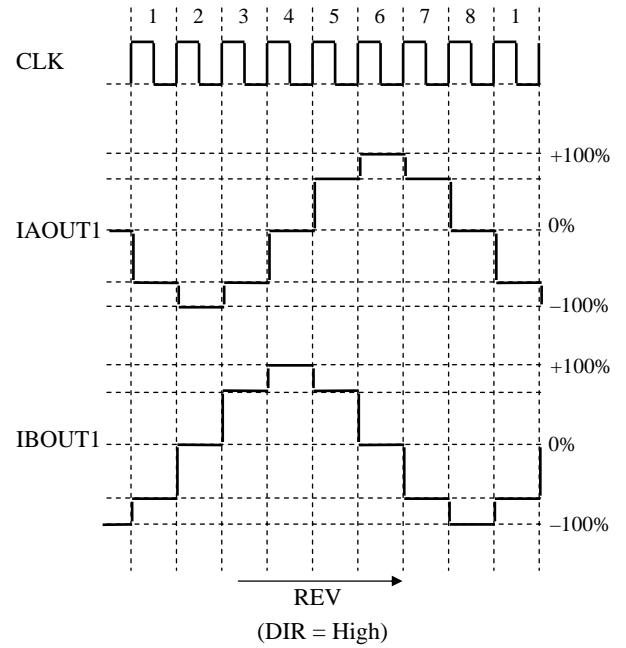
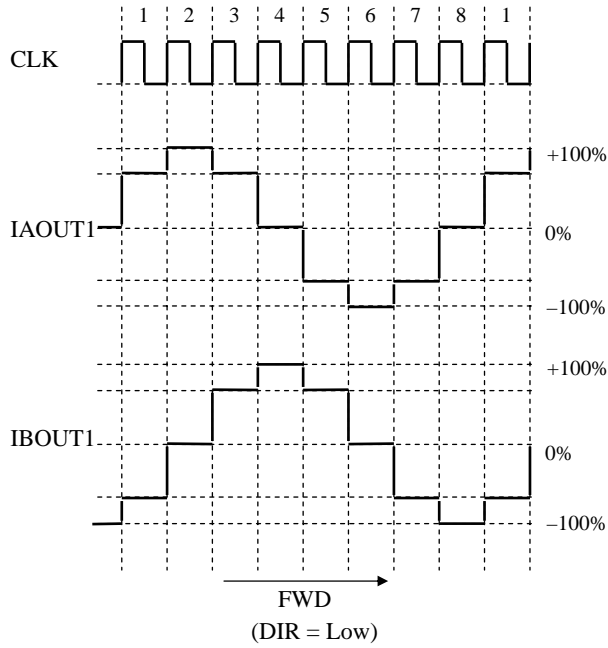
2008-02-20		
Established	Revised	

■ Technical Data (continued)

4. Each phase current (Timing chart) (continued)

3) 1-2 phase excitation (8-step sequence)

(ST1 = High, ST2 = Low, ST3 = Low)



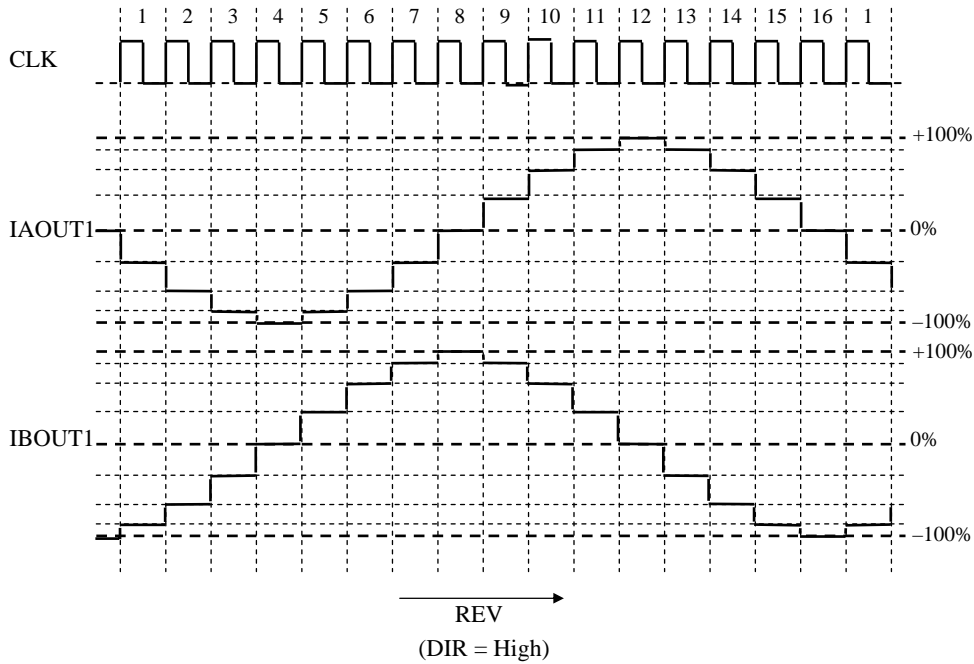
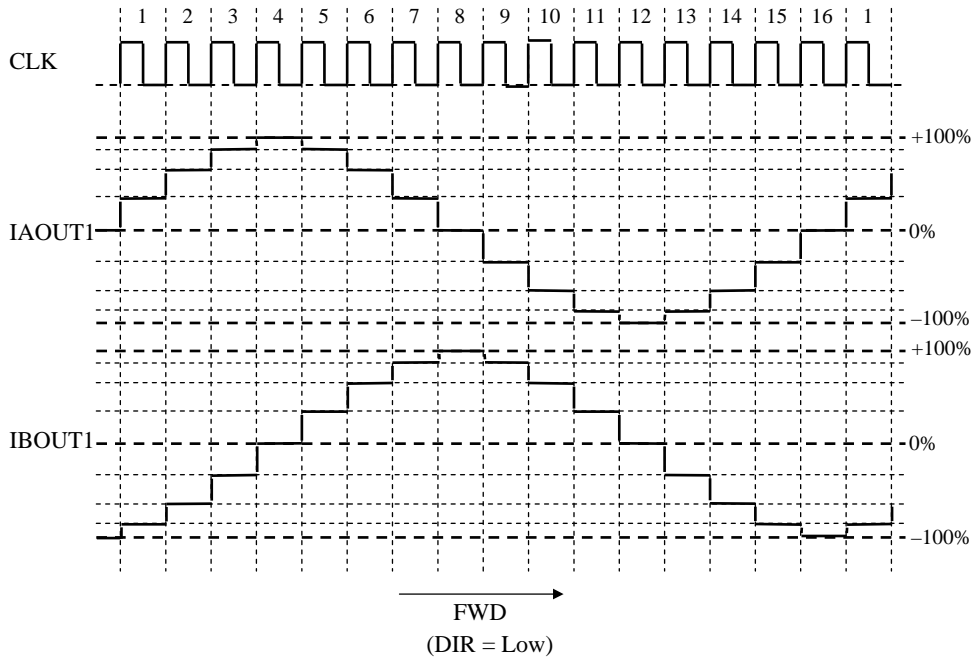
2008-02-20		
Established	Revised	

■ Technical Data (continued)

4. Each phase current (Timing chart) (continued)

4) W1-2 phase excitation (16-step sequence)

(ST1 = High, ST2 = High, ST3 = Low)

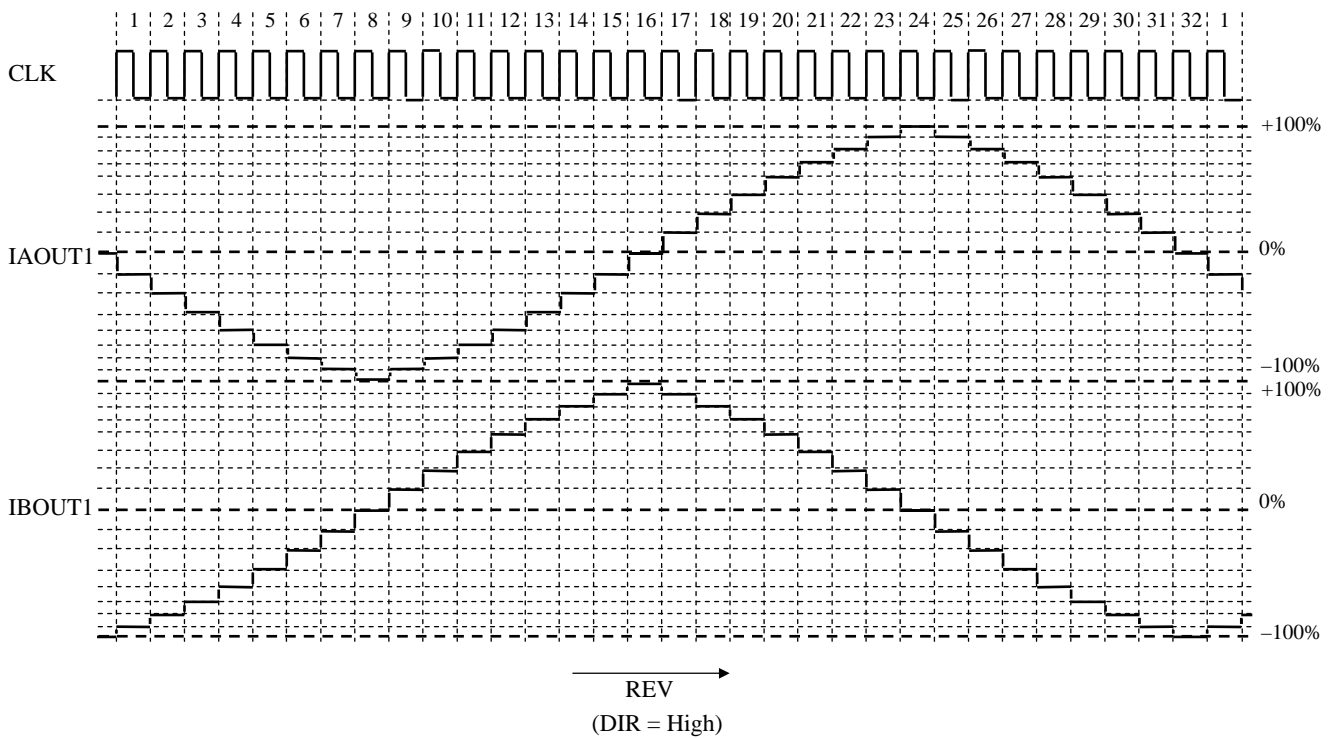
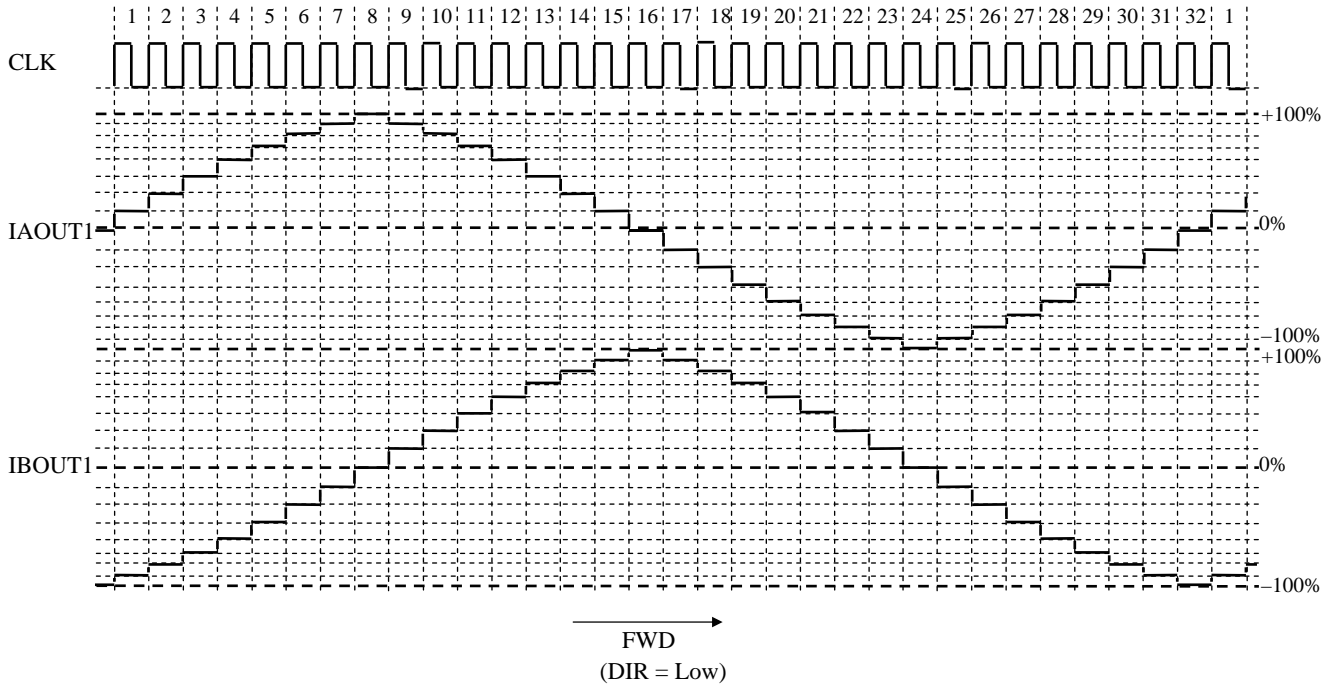


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■ Technical Data (continued)

4. Each phase current (Timing chart) (continued)

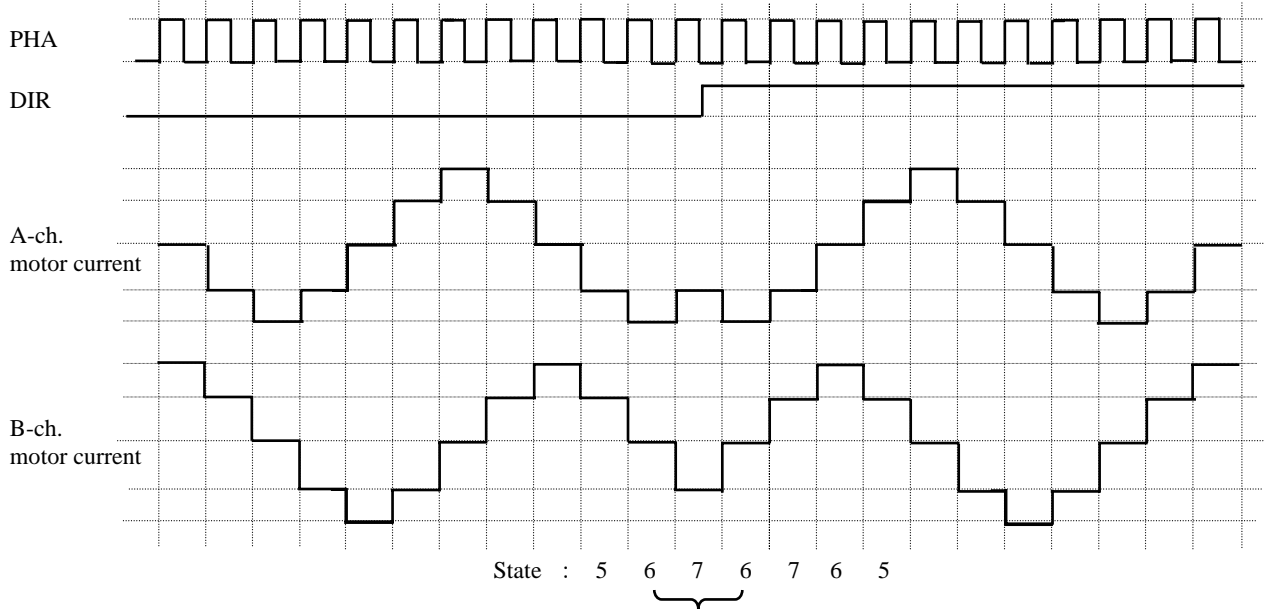
5) 2W1-2 phase excitation (32-step sequence)  
(ST3 = High)



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Established	Revised	

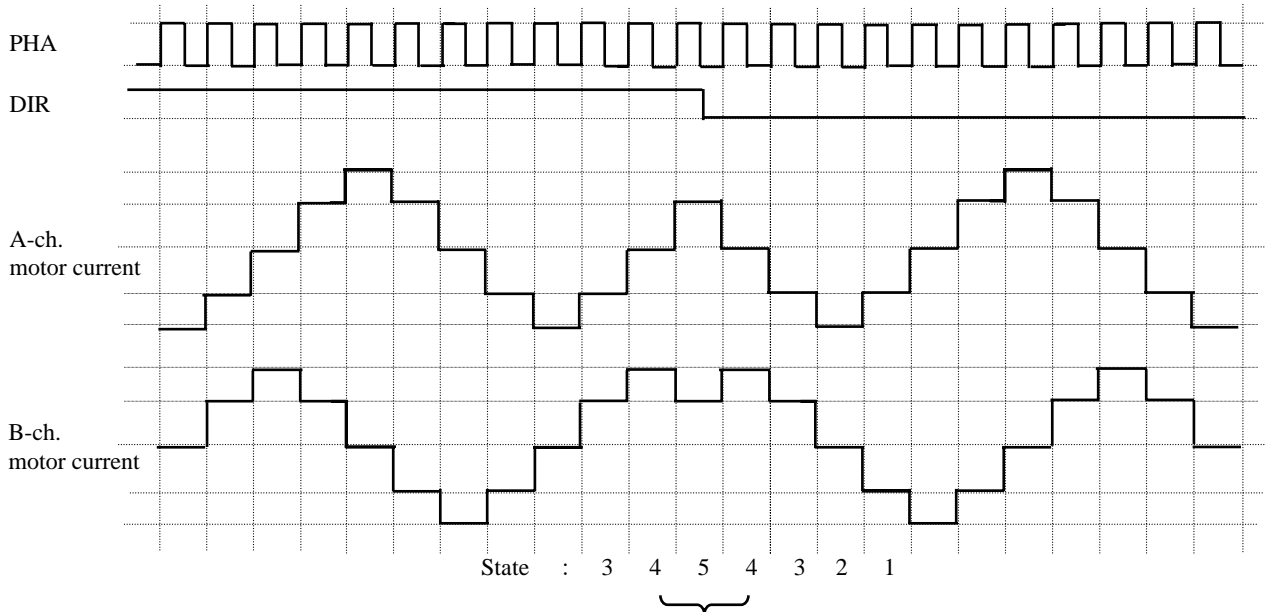
■ Technical Data (continued)  
 5. Timing chart at change of DIR

(Ex.1) Timing chart at 1-2 phase excitation (DIR : Low → High)



At change of DIR, the state before the change is held and the operation is continued.

(Ex.2) Timing chart at 1-2 phase excitation (DIR : High → Low)



At change of DIR, the state before the change is held and the operation is continued.

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■ Technical Data (continued)

6. Home Position function

This LSI has built-in Home Position function to reduce the displacement of motor current state at change of excitation mode while a motor is driving.

Home Position function, following as the below chart, outputs Low-level voltage to TJMON pin at the timing when the displacement of motor current state is minimum at change of excitation mode in case of TEST = High-level input.

At other timing, Home Position function outputs High-level voltage (in case the pull-up resistor (recommendation : 100 kΩ to 5 V) is connected because TJMON pin is made with open drain) at TJMON pin.

1) Home Position output timing chart (DIR = Low)

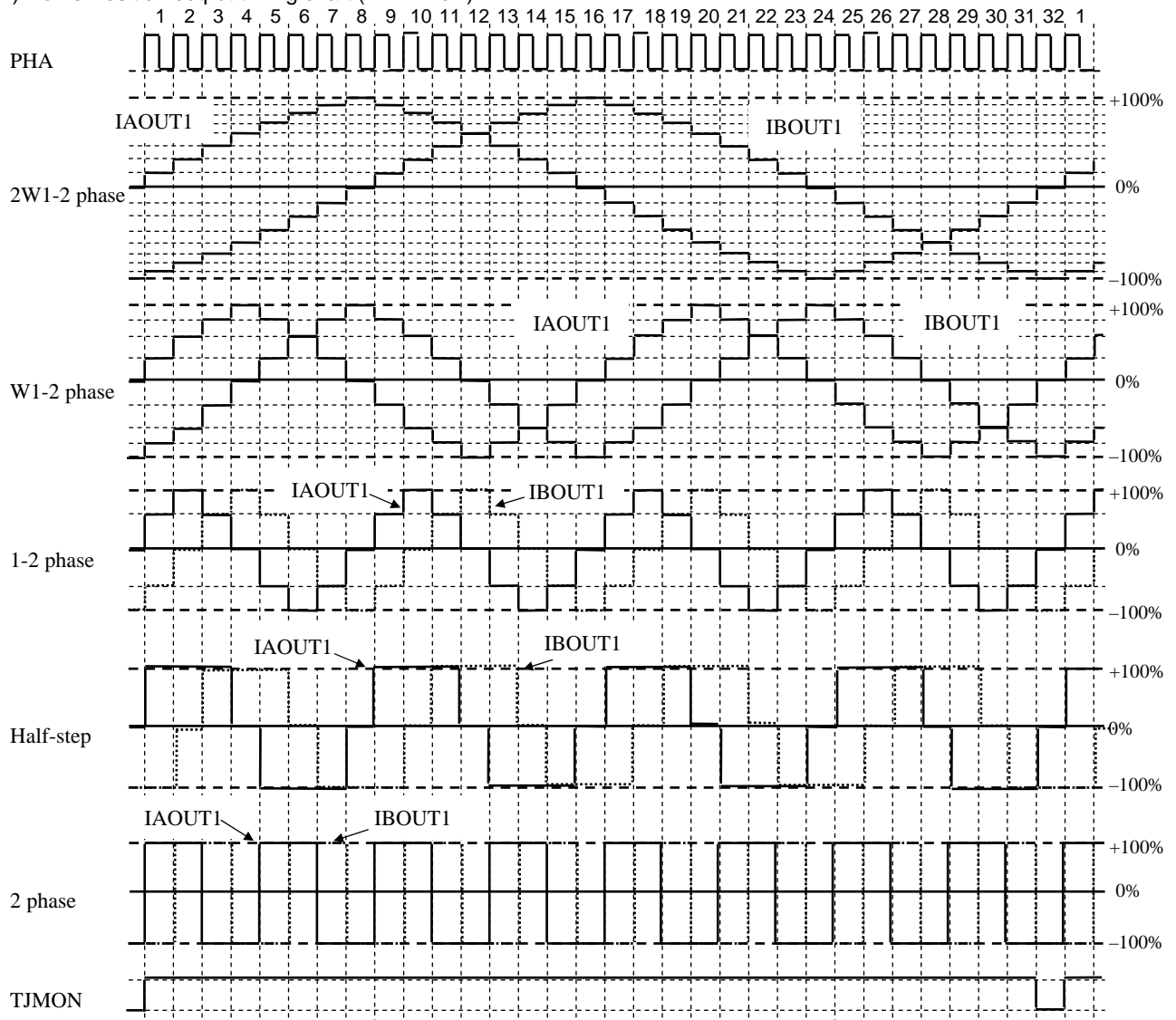


Table Output current of each excitation mode at Home Position = Low (DIR = Low)

	2 phase excitation	Half-step	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation
Phase A current	-100%	0%	0%	0%	0%
Phase B current	-100%	-100%	-100%	-100%	-100%

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■ Technical Data (continued)  
 6. Home Position function (continued)

2) Home Position output timing chart (DIR = High)

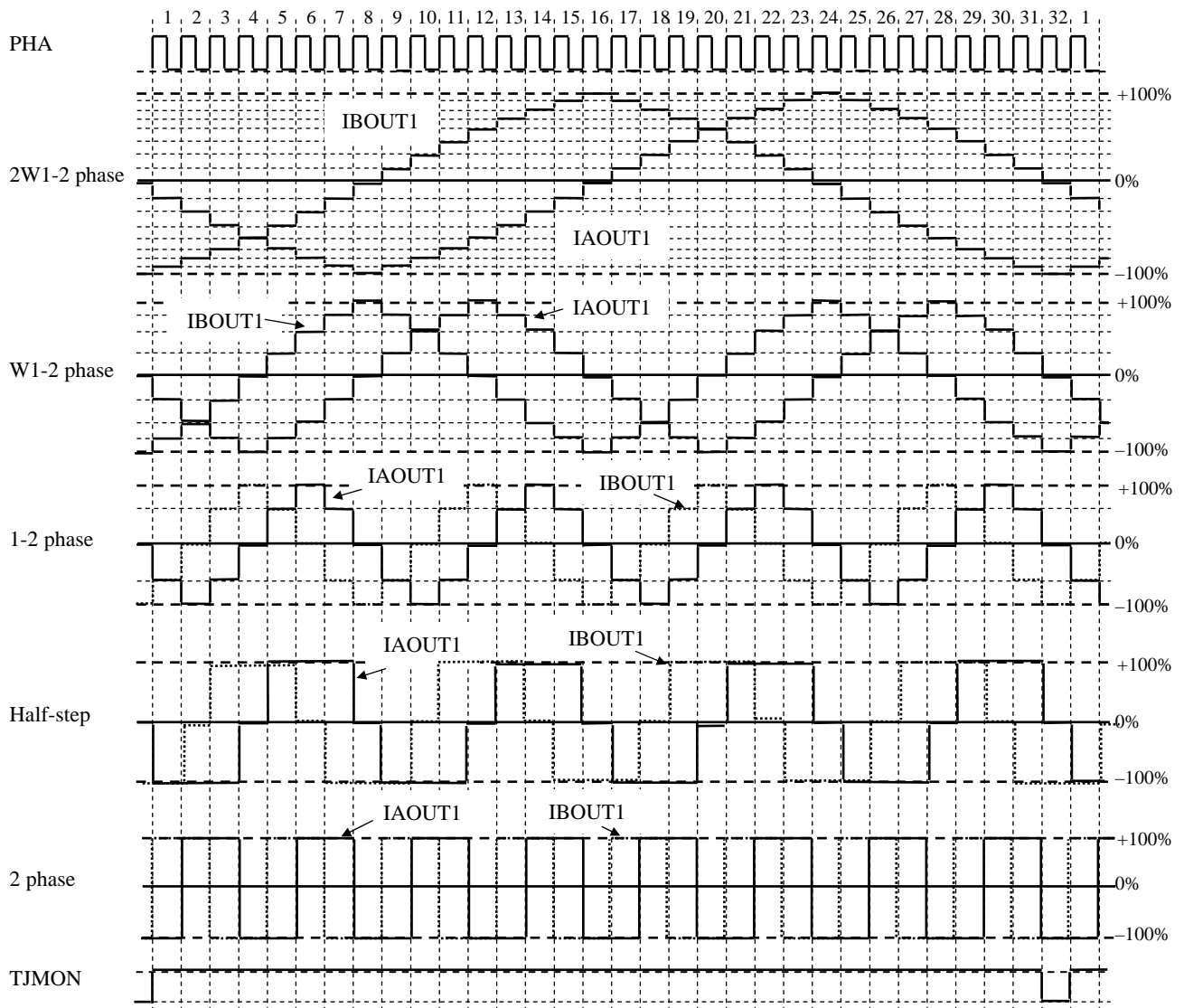


Table Output current of each excitation mode at Home Position = Low (DIR = High)

	2 phase excitation	Half-step	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation
Phase A current	-100%	0%	0%	0%	0%
Phase B current	-100%	-100%	-100%	-100%	-100%

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	<h1>Product Standards</h1>	<h2>AN44067A</h2>	
		Total Pages	Page
		45	38

### ■ Usage Notes

#### 1. Special attention and precaution in using

1. This IC is intended to be used for general electronic equipment [stepping motor].

Consult our sales staff in advance for information on the following applications:

- Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
- Any applications other than the standard applications intended.
  - (1) Space appliance (such as artificial satellite, and rocket)
  - (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
  - (3) Medical equipment for life support
  - (4) Submarine transponder
  - (5) Control equipment for power plant
  - (6) Disaster prevention and security device
  - (7) Weapon
  - (8) Others : Applications of which reliability equivalent to (1) to (7) is required

2. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.

3. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

4. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.

5. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin- $V_{CC}$  short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) . Especially, for the pins below, take notice Power supply fault, Ground fault, load short and short between the pin below and current detection pin.

(1) AOUT1(Pin 12), AOUT2(Pin 10), BOUT1(Pin 8), BOUT2(Pin 6)

(2) BC1(Pin 13), BC2(Pin 14), VPUMP(Pin 15)

(3) VM1(Pin 17), VM2(Pin 1), S5VOUT(Pin 24)

(4) RCSA(Pin 11), RCSB(Pin 7)

And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.

6. When using the LSI for new models, verify the safety including the long-term reliability for each product.

7. When the application system is designed by using this LSI, be sure to confirm notes in this book.

Be sure to read the notes to descriptions and the usage notes in the book.

8. Connect the metallic plate (fin) on the back side of the IC with the GND potential. The thermal resistance and the electrical characteristics are guaranteed only when the metallic plate (fin) is connected with the GND potential.

9. Confirm characteristics fully when using the LSI.

Secure adequate margin after considering variation of external part and this IC including not only static characteristics but transient characteristics. Especially, Pay attention that abnormal current or voltage must not be applied to external parts because the pins (Pin 6, 8, 10, 12, 13, 14, 15) output high current or voltage.

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■ Usage Notes (continued)

2. Notes of Power LSI.

1. Design the heat radiation with sufficient margin so that Power dissipation must not be exceeded base on the conditions of power supply voltage, load and ambient temperature.  
(It is recommended to design to set connective parts to 70% to 80% of maximum rating)
2. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.  
Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VM short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.
3. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
4. The product which has specified ASO (Area of Safe Operation) should be operated in ASO.
5. Verify the risks which might be caused by malfunctions of external parts.
6. Set capacitance value between VPUMP and GND so that VPUMP (Pin 15) must not exceed 43 V transiently at the time of motor standby to motor start.
7. This IC employs a PWM drive method that switches the high-current output of the output transistor. Therefore, the IC is apt to generate noise that may cause the IC to malfunction or have fatal damage. To prevent these problems, the power supply must be stable enough. Therefore, the capacitance between the S5VOUT and GND pins must be a minimum of 0.1  $\mu$ F and the one between the VM and GND pins must be a minimum of 47  $\mu$ F and as close as possible to the IC so that PWM noise will not cause the IC to malfunction or have fatal damage.

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■ Usage Notes (continued)

3. Notes

1) Pulse blanking time

This IC has pulse blanking time (0.7 μs/Typ.value) to prevent erroneous current detection caused by noise.

Therefore, the motor current value will not be less than current determined by pulse blanking time. Pay attention at the time of minimum current control.

The relation between pulse blanking time and minimum current value is shown as Chart 1.

In addition, increase-decrease of motor current value is determined by L value, wire wound resistance, induced voltage and PWM on Duty inside a motor.

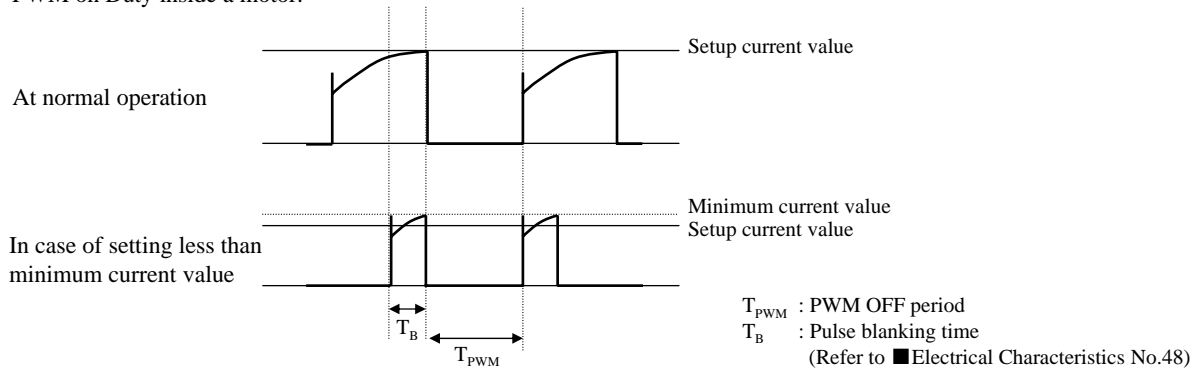


Chart 1. RCS current waveform

2) VREF voltage

When VREF voltage is set to Low-level, erroneous detection of current might be caused by noise because threshold of motor current detection comparator becomes low (= VREF/10 × motor current ratio [%]) (Refer to Page 29, 30). Use this IC after confirming no misdetection with setup REF voltage.

3) Notes on interface

Absolute maximum of Pin 19 to Pin 23 and Pin 28 to Pin 33 is -0.3 V to 6 V. When the setup current for a motor is large and lead line of GND is long, GND pin potential might rise. Take notice that interface pin potential is negative to difference in potential between GND pin reference and interface pin in spite of inputting 0 V to the interface pin. At that time, pay attention allowable voltage range must not be exceeded.

4) Notes on test mode

When inputting voltage of above 0.6 V and below 4.0 V to TEST (Pin 25), this LSI might become test mode.

When disturbance noise etc. makes this LSI test mode, motor output pin might be Hi-Z. Therefore, use this LSI on condition that TEST pin is shorted to GND or S5VOUT at normal motor operation.

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■ Usage Notes (continued)

3. Notes (continued)

5) Notes on Standby mode release / Low voltage protection release

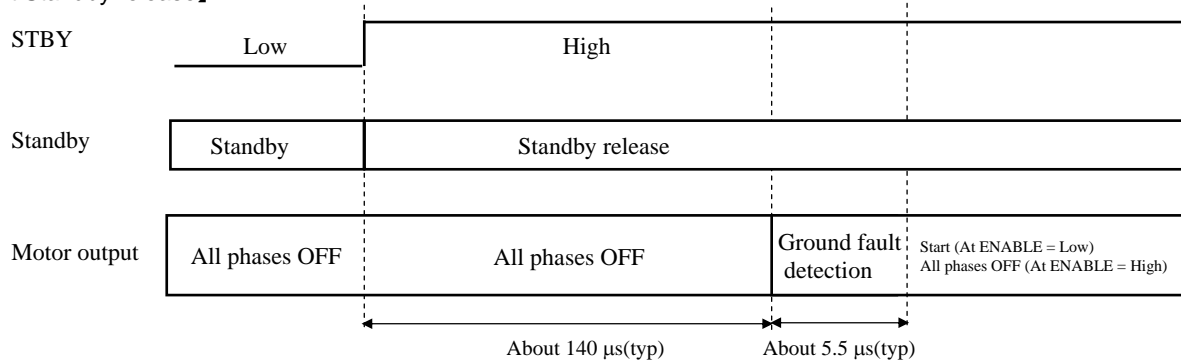
This LSI has all phases OFF period of about 140 μs (typ) owing to release of Standby and Low voltage protection (Refer to the below figure).

This is why restart from Standby and Low voltage protection is performed after booster voltage rises sufficiently because booster operation stops at Standby and Low voltage protection.

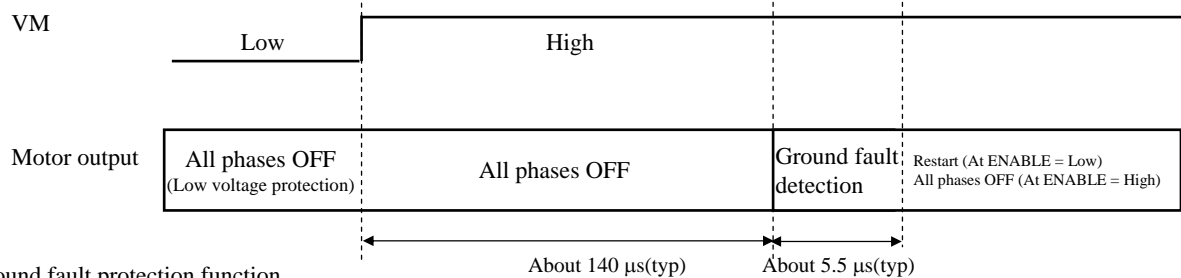
When the booster voltage does not rise sufficiently during all phases OFF period due to that capacitance voltage between VPUMP and GND becomes large etc., the IC might overheat. In this case, release Standby and Low voltage protection at ENABLE = High-level, and restart at ENABLE = Low-level after the booster voltage rises sufficiently.

Moreover, take notice that state of motor current becomes default position at Standby and Low voltage protection operation following as 3. Notes No.8.

【At Standby release】



【At Low voltage protection release】



6) Ground fault protection function

This IC has built-in ground fault protection function to detect ground fault of motor output pin at board mounting.

As the above figure, ground fault detection function will operate after release of Low voltage protection and Standby, and check ground fault of motor output pins.

If ground fault is detected, this function makes motor output all phases OFF and motor operation stop. If ground fault is not detected, this function makes motor start. However, take notice that IC might be destroyed before ground fault protection function operates in case that ASO ( Area of Safe Operation ) of device or maximum rating are exceeded in a moment.

In addition, this function might not detect ground fault when starting VM at STBY = High-level. It is recommended that VM is started at STBY = Low-level.

In case of release of ground fault detection, restart IC after inputting low voltage to STBY pin or making VM voltage OFF.

7) Notes on release of thermal protection

The release of thermal protection operation will restart after all phases OFF of about 140 μs and ground fault detection operation as 3. Notes No.5, 6.

Moreover, take notice that the state of motor current will become default position after release of thermal protection operation as 3. Notes No.8

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■ Usage Notes (continued)

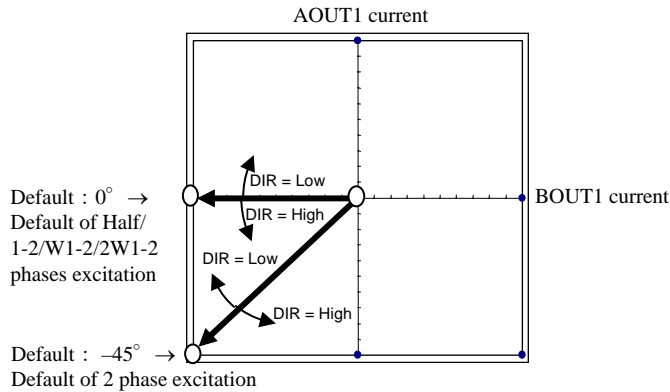
3. Notes (continued)

8) Default of motor current state

Default of motor current follows as the below figure after release of Low voltage protection, Standby and thermal protection on each excitation mode.

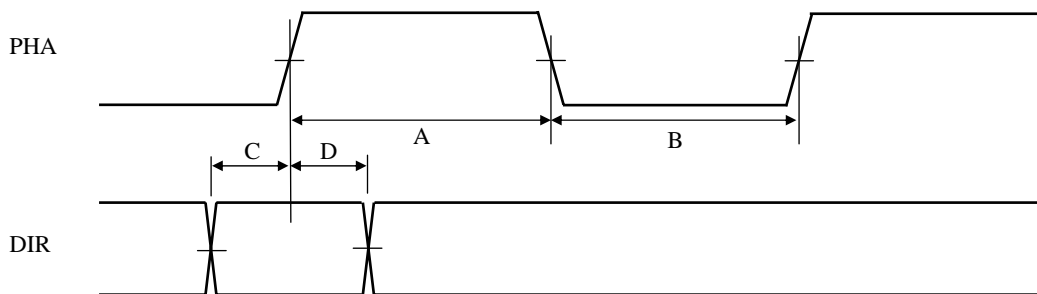
Table default position of each excitation mode

Excitation mode	Default electrical angle
2 phase excitation (4 step)	-45°
Half-step (8 step)	0°
1-2 phase excitation (8 step)	0°
W1-2 phase excitation (16 step)	0°
2W1-2 phase excitation (32 step)	0°



9) PHA input signal and DIR input signal

The set/hold time of PHA and DIR input signals, PHA input minimum pulse width (High/Low) are shown as the below figure. Input signals after securing set/hold time.



Period	Contents	Time
A	PHA input minimum pulse width (High)	5 μs or more
B	PHA input minimum pulse width (Low)	5 μs or more
C	DIR set time	2 μs or more
D	DIR hold time	2 μs or more

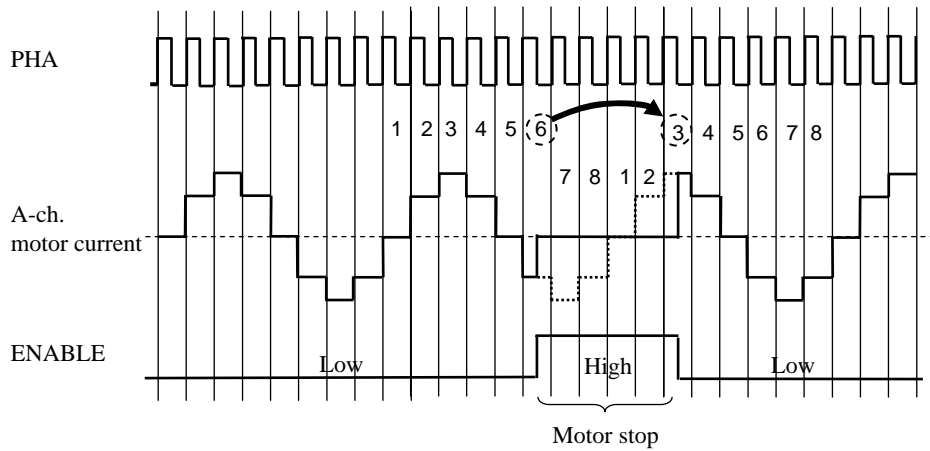
■ Usage Notes (continued)

3. Notes (continued)

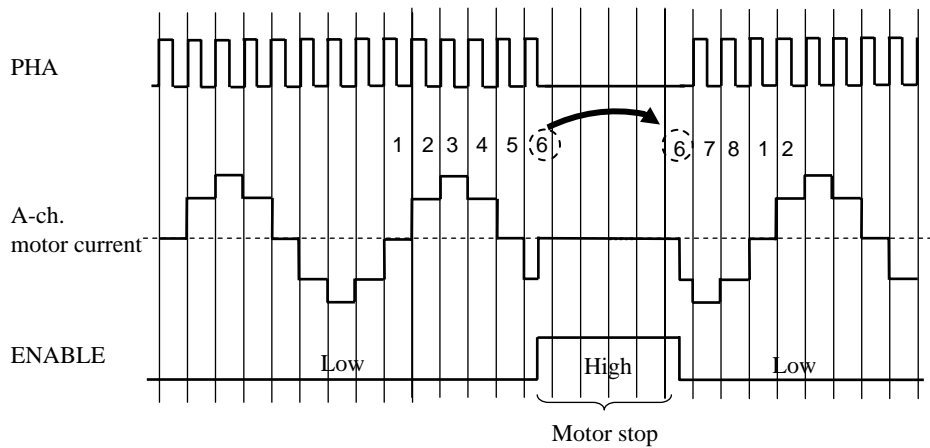
10) PHA input at ENABLE = High

As the below figure (Ex. 1-2 phase excitation), when inputting PHA at the time of motor stop and ENABLE = High (All phases are OFF → Motor current = 0 A), the setup value of motor current will proceed at PHA input. Therefore, in case of restart at ENABLE = Low, take notice that the position of restart is where the current state just before motor stop gains PHA input.

Ex.) 1-2 phase excitation



In spite of stop at state[6] , because PHA is input at ENABLE = High, the motor will restart after ENABLE = Low at state [3].



In spite of stop at state [6] , because PHA is not input at ENABLE = High, the motor will restart after ENABLE = Low at state [6] just before stop.

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Established	Revised	

■ Usage Notes (continued)

3. Notes (continued)

11) Notes on RCS line

Take consideration in the below figure and the points and design PCB pattern.

(1) Point 1

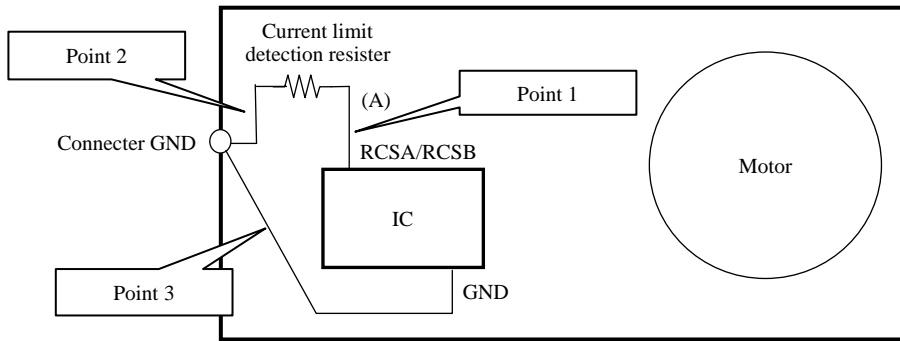
Design so that the wiring to the current detection pin (RCSA/RCSB pin) of this IC is thick and short to lower impedance. This is why current can not be detected correctly owing to wiring impedance and current might not be supplied to a motor sufficiently.

(2) Point 2

Design so that the wiring between current detection resistor and connector GND (the below figure Point 2) is thick and short to lower impedance. As the same as Point 1, sufficient current might not be supplied due to wiring impedance. In addition, if there is a common impedance on the side of GND of RASA and RCSB, peak detection might be erroneous detection. Therefore, install the wiring on the side of GND of RCSA and RCSB independently.

(3) Point 3

Connect GND pin of this IC to the connector on PCB independently. Separate the wiring removed current detection resistor of large current line (Point 2) from GND wiring and make these wirings one-point shorted at the connector as the below figure. That can make fluctuation of GND minimum.



12) A high current flows into the IC. Therefore, the common impedance of PCB can not be ignored. Take the following points into consideration and design the PCB pattern for a motor. Because the wiring connecting to VM1 (Pin 17) and VM2 (Pin 18) of this IC is high-current, it is easy to generate noise at time of switching by wiring L. That might cause malfunction and destruction (Figure 2). As Figure 3, the escape way of the noise is secured by connecting a capacitor to the connector close to the VM pin of the IC. This makes it possible to suppress the fluctuation of direct VM pin voltage of the IC. Make the setting as shown in Figure 3 as much as possible.

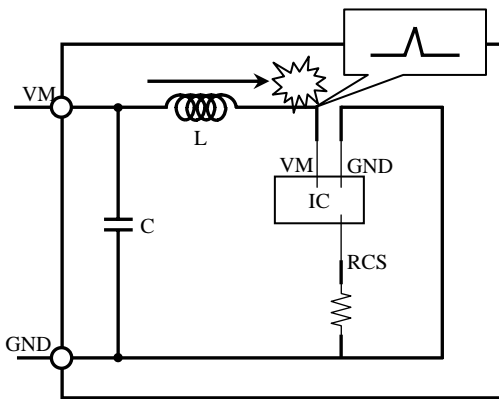


Figure 2. No recommended pattern

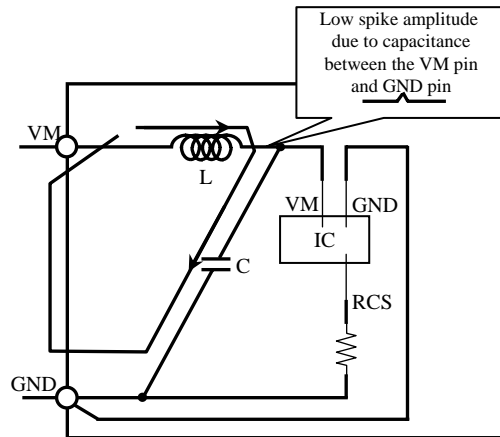


Figure 3. Recommended pattern

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	<h1>Product Standards</h1>	<h2>AN44067A</h2>	
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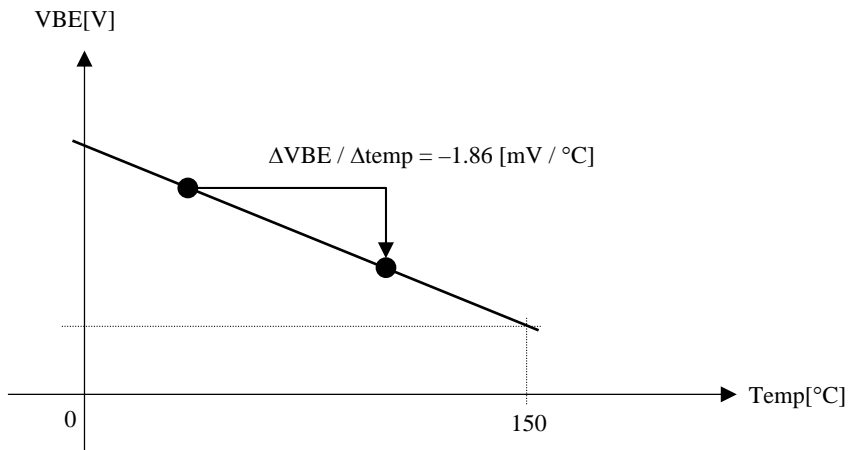
■ Usage Notes (continued)

3. Notes (continued)

13) IC junction temperature

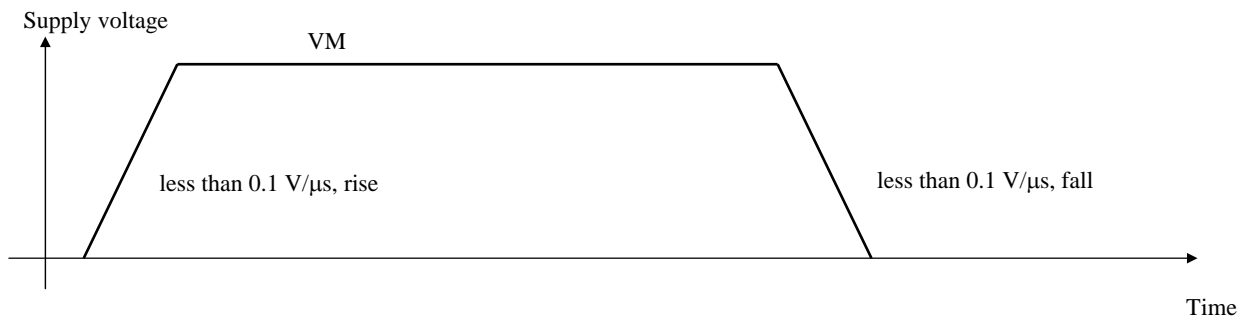
In case of measuring chip temperature of this IC, measure the voltage of TJMON pin (Pin 3) and estimate the chip temperature from the data below. However, because this data is technical reference data, conduct a sufficient reliability test of the IC and evaluate the product with the IC incorporated.

TJMON pin temperature characteristics



14) Speed of supply and cut of power

When supplying to VM pin (Pin 1, 17), set the rise speed of VM voltage to less than 0.1 V/μs and fall speed to less than 0.1 V/μs. If the speed of rise and fall of power supply is too rapid, that might cause malfunction and destruction of the IC. In this case, conduct a sufficient reliability test and also check a sufficient evaluation for a product.



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Established	Revised	

Regulations No.	SC3S0829	Total pages	Page
		6	1

# Package Standards

Package Code	HSOP034-P-0300A
--------------	-----------------

Semiconductor Company  
Panasonic Corporation

Established by	Applied by	Checked by	Prepared by
H.Shidooka	H.Yoshida	M.Okajima	M.Itoh

-	-
Established	Revised

Established: 2004-03-18  
Revised : 2009-06-26

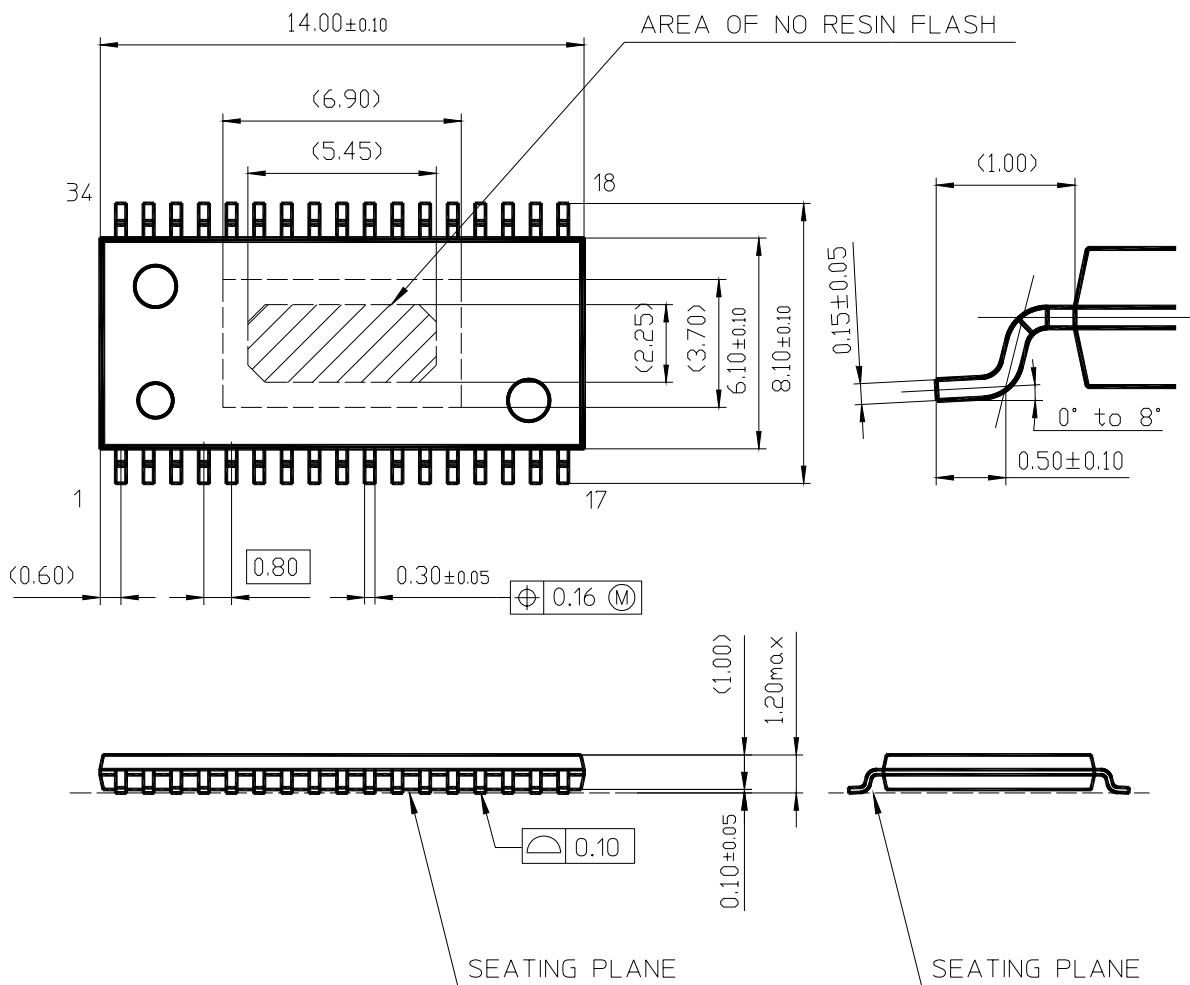


<h1>Package Standards</h1>		Total pages	Page
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## 1. Outline Drawing

Unit:mm

Package Code : HSOP034-P-0300A



Body Material	: Epoxy Resin
Lead Material	: Cu Alloy
Lead Finish Method	: Pd Plating

-	-	
Established	Revised	

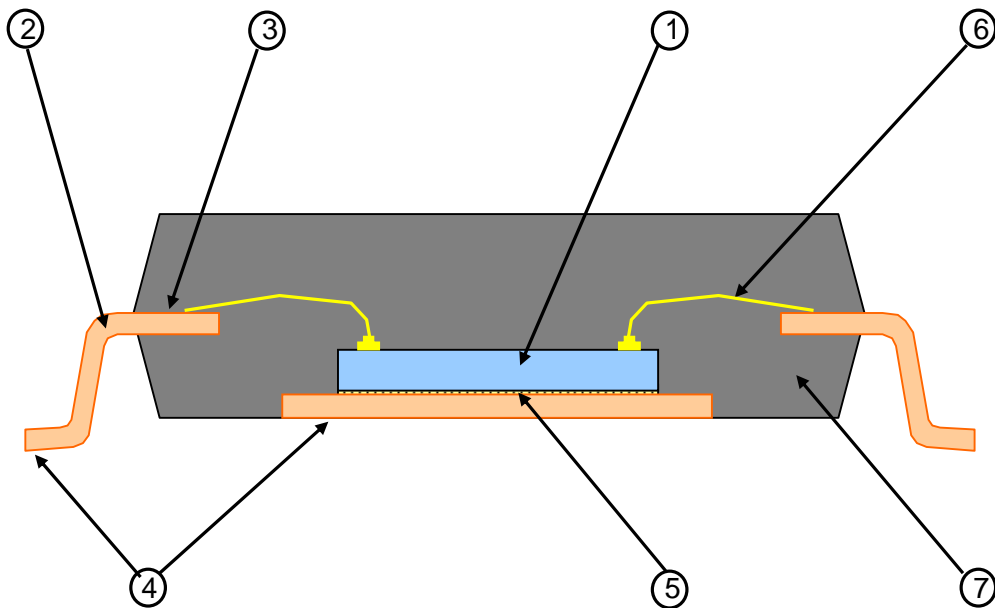
Semiconductor Company, Panasonic Corporation

	<h1>Package Standards</h1>		
		Total pages	Page
		6	3

## 2. Package Structure (Technical Report : Reference Value)

Package Code : HSOP034-P-0300A

Chip Material		Si	①
Leadframe material		Cu alloy	②
Inner lead surface		Pd plating	③
Outer lead surface		Pd plating	④
Chip mount	Method	Resin adhesive method	⑤
	Material	Adhesive material	
Wirebond	Method	Thermo-compression bonding	⑥
	Material	Au	
Molding	Method	Transfer molding	⑦
	Material	Epoxy resin	
Mass		250 mg	

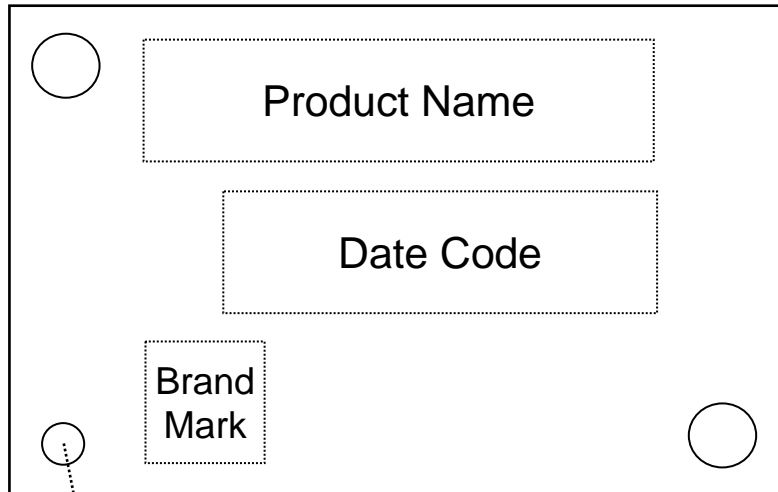


-	-	
Established	Revised	

	<h1>Package Standards</h1>		
		Total pages	Page
		6	4

### 3. Mark Layout

Package Code : HSOP034-P-0300A



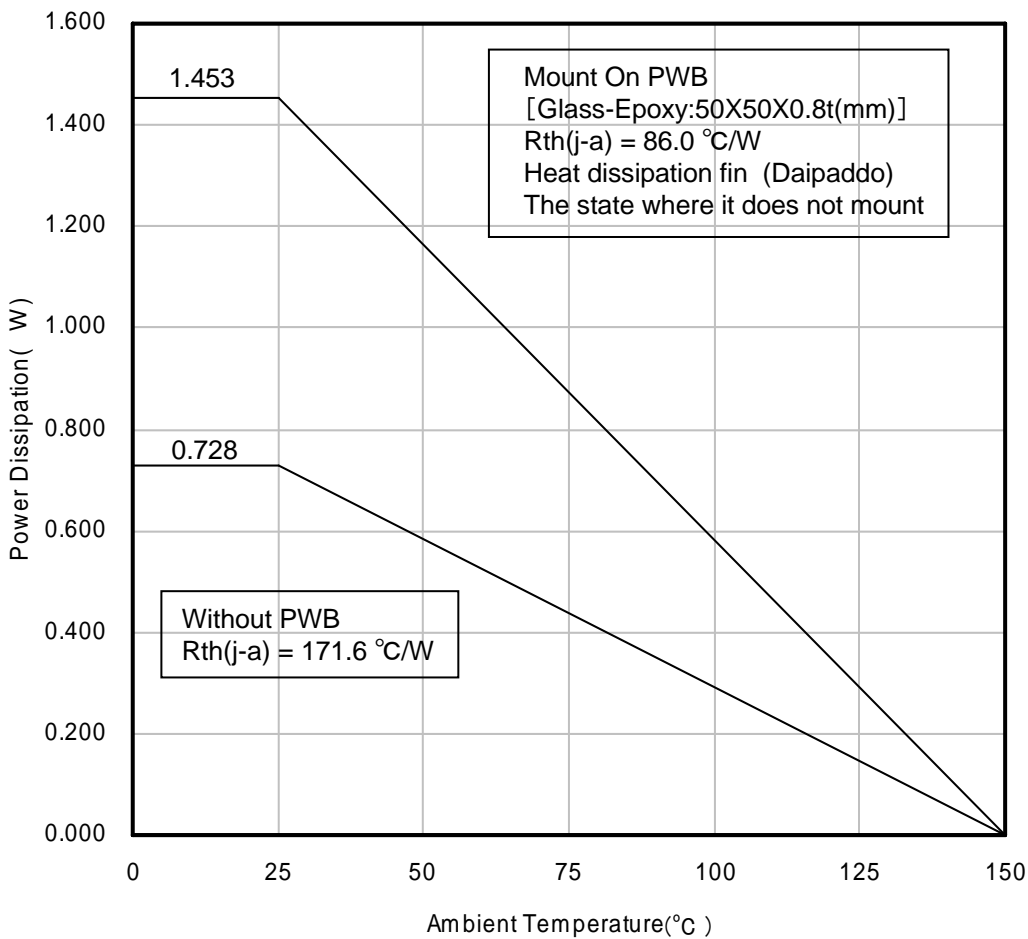
1-pin direction

-	-	
Established	Revised	

	<h1>Package Standards</h1>		
		Total pages	Page
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4. Power Dissipation (Technical Report)

Package Code : HSOP034-P-0300A



-	-	
Established	Revised	

<h1>Package Standards</h1>			
		Total pages	Page
		6	6

## 5. Power Dissipation (Supplementary Explanation)

### [Experiment environment]

Power Dissipation (Technical Report) is a result in the experiment environment of SEMI standard conformity. (Ambient air temperature (Ta) is 25 degrees C)

### [Supplementary information of PWB to be used for measurement]

The supplement of PWB information for Power Dissipation data (Technical Report) are shown below.

Indication	Total Layer	Resin Material
Glass-Epoxy	1-layer	FR-4
4-layer	4-layer	FR-4

### [Notes about Power Dissipation (Thermal Resistance) ]

Power Dissipation values (Thermal Resistance) depend on the conditions of the surroundings, such as specification of PWB and a mounting condition , and a ambient temperature. (Power Dissipation (Thermal Resistance) is not a fixed value.)

The Power Dissipation value (Technical Report) is the experiment result in specific conditions (evaluation environment of SEMI standard conformity) ,and keep in mind that Power Dissipation values (Thermal resistance) depend on circumference conditions and also change.

### [Definition of each temperature and thermal resistance]

Ta : Ambient air temperature

The temperature of the air is defined at the position where the convection, radiation, etc. don't affect the temperature value, and it's separated from the heating elements.

Tc : It's the temperature near the center of a package surface. The package surface is defined at the opposite side if the PWB.

Tj : Semiconductor element surface temperature (Junction temperature.)

Rth(j-c) : The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the package surface

Rth(c-a) : The thermal resistance (difference of temperature of per 1 Watts) between the package surface and the ambient air

Rth(j-a) : The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the ambient air

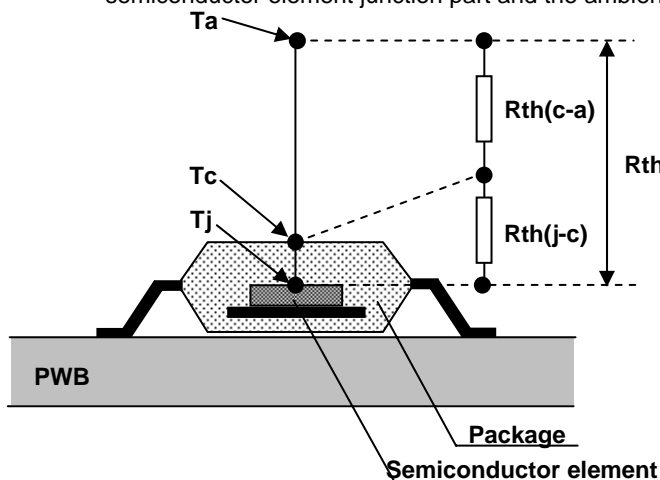


Fig1. Definition image

### [Definition formula]

$$T_j = \{R_{th}(j-c) + R_{th}(c-a)\} \times P + T_a$$

$$= R_{th}(j-a) \times P + T_a$$

$$R_{th}(j-c) = \frac{T_j - T_c}{P} \quad ( \text{ } / \text{W} )$$

$$R_{th}(c-a) = \frac{T_c - T_a}{P} \quad ( \text{ } / \text{W} )$$

$$R_{th}(j-a) = \frac{T_j - T_a}{P} \quad ( \text{ } / \text{W} )$$

$$= R_{th}(j-c) + R_{th}(c-a)$$

P:power(W)

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Established	Revised	

	Recommended Soldering Conditions		
		Total pages	page
		2	1

**Product name : AN44067A-VF**

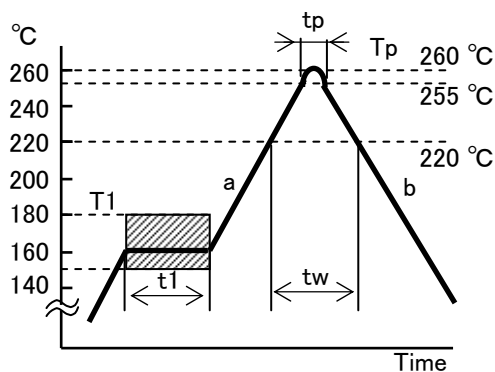
**Package : HSOP034-P-0300A**

## 1. Recommended Soldering Conditions

In case that the semiconductor packages are mounted on the PCB, the soldering should be performed under the following conditions.

### ① Reflow soldering

**Reflow peak temp. : max. 260 °C**



No.	mark	contents	value
1	T1	Pre-heating temp.	150 °C~180 °C
2	t1	Pre-heating temp. hold time	60 s~120 s
3	a	Rising rate	2 °C/s~5 °C/s
4	Tp	Peak temp.	255 °C+5 °C, -0 °C
5	tp	Peak temp. hold time	10 s±3 s
6	tw	High temp. region hold time	within 60 s (≥220 °C)
7	b	Down rate	2 °C/s~5 °C/s
8	-	Number of reflow	within 2 times

\* Peak temperature : less than 260 °C

\* Temperature is measured at package surface point

### ② Wave soldering (Flow soldering)

\* Temp. of solder : 260 °C or less

\* Soak time : within 5 s

\* Number of flow : only 1 time

### ③ Manual soldering

\* Iron Temperature : 350 °C or less (Device lead temperature : 270 °C、10 s max.)

\* Soldering time : within 3 s

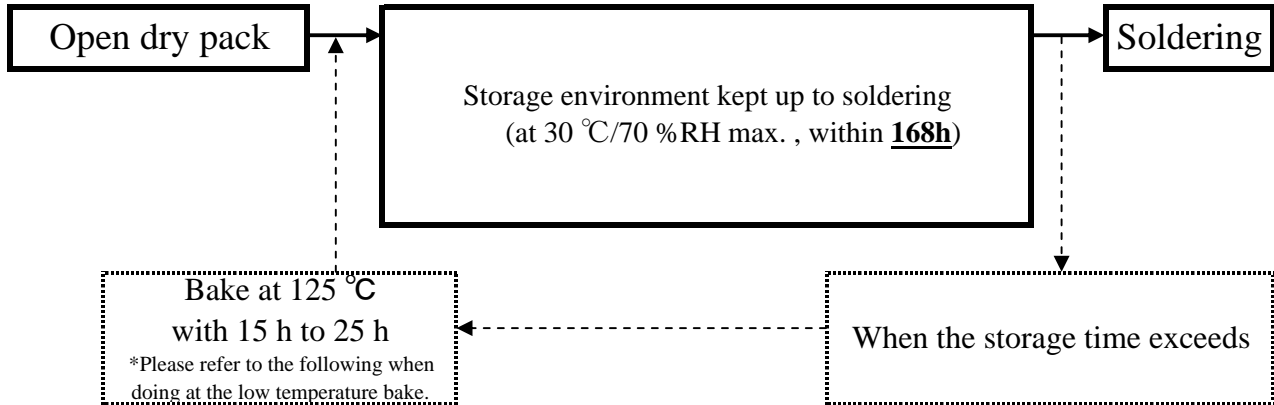
\* Number of manual soldering : only 1 time

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Prepared	Revised	

	<b>Recommended Soldering Conditions</b>		
		Total pages	page
		2	2

## 2. Storage environment after dry pack opening



- ※ Because the taping and the magazine materials are not the heat-resistant materials, the bake at 125°C cannot be done.  
Therefore, please solder everything or control everything in the rule time.  
Please keep them in an equal environment with the moisture-proof packaging or dry box.  
(Temperature: room temperature, relative humidity: 30% or less. )  
To control storage time, when bake in the taping and the magazine is necessary, it is necessary for each type to set a bake condition. Please inquire of our company.

☆ AN44067A-VF limitation, low temperature bake condition : 40 °C / 25 %RH or less / 192 h

## 3. Note

- ① Storage environment conditions: keep the following conditions Ta=5 °C~30 °C, RH=30 %~70 %.
- ② Storage period before opening dry pack shall be 1year from a shipping day under Ta=5 °C~30 °C, RH=30 %~70 %. When the storage exceeds, Bake at 125 °C with 15 h to 25 h.
- ③ Baking cycle should be only one time.  
Please be cautious of solderability at baking.
- ④ In case that use reflow two times, 2nd reflow must be finished within **168 hours**.
- ⑤ Remove flux sufficiently from product in the washing process.  
( Flux : Chlorineless rosin flux is recommended.)
- ⑥ In case that use ultrasonic for product washing,  
There is the possibility that the resonance may occur due to the frequency and shape of PCB.  
It may be affected to the strength of lead. Please be cautious of this matter.

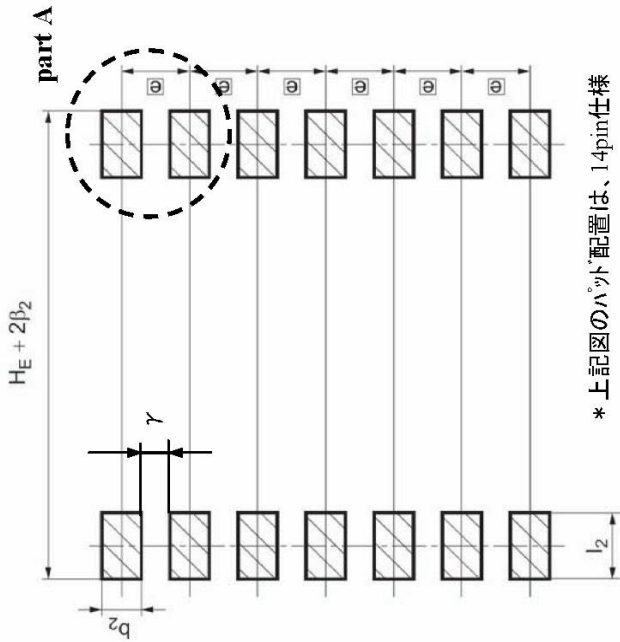
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# PCB & Mask spec. for HSOP034-P-0300A (Reflow)

Application Specific Standard Products Business Unit  
Semiconductor Business Group  
Industrial Devices Company  
Panasonic Corporation

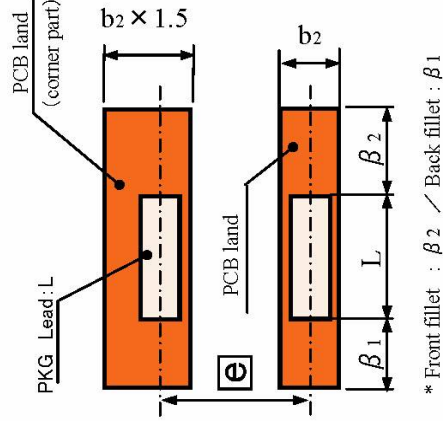
## 【Whole PCB land figure】



\* 上記図のハット配置は、14pin仕様

## 【Expansion of part A】

<Layout of PCB land and package land>



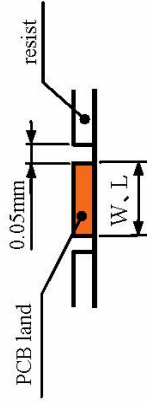
$$l_2 \geq L + \beta_1 + \beta_2$$

$$b \leq b_2 \leq e - \gamma$$

## Reference

\*4 land of the corner part (the both ends of each side) double land width 1.5 times to ensure the implementation strength.

## 【PCB land cross-sectional figure】



Resist specifications: Normal resist (NSMD)  
(PCB land size +0.10mm (One side +0.05mm))

\* Metal mask thickness : 0.13 ~ 0.15mm

Please check footprint length (L) and the terminal width: b in Package standards.

## ■ List of recommended dimensions

Terminal Pitch e	PCB land			Metal mask opening	
	Land Width: b <sub>2</sub> (Not corner land)	Front fillet β <sub>2</sub>	Back fillet β <sub>1</sub>	Width	Length
0.8mm	0.35~0.40	0.2~0.3	0.3~0.4	Same as the PCB land	L + β <sub>1</sub> + β <sub>2</sub>
			Distance between lands γ		
			0.3		

(Unit: mm)

\*The above size is calculated based on the experiment results by Matsushita Electric Industrial Co., Ltd., and is not intended as a guarantee of mounting reliability. Mounting reliability can vary depending on factors such as the equipment specifications and conditions, material specifications and properties, and environmental conditions. To ensure satisfactory results, your company should evaluate and confirm actual mounting performance.

**Panasonic ideas for life**

# Recommended Land Pattern

Total pages  
1

page  
1

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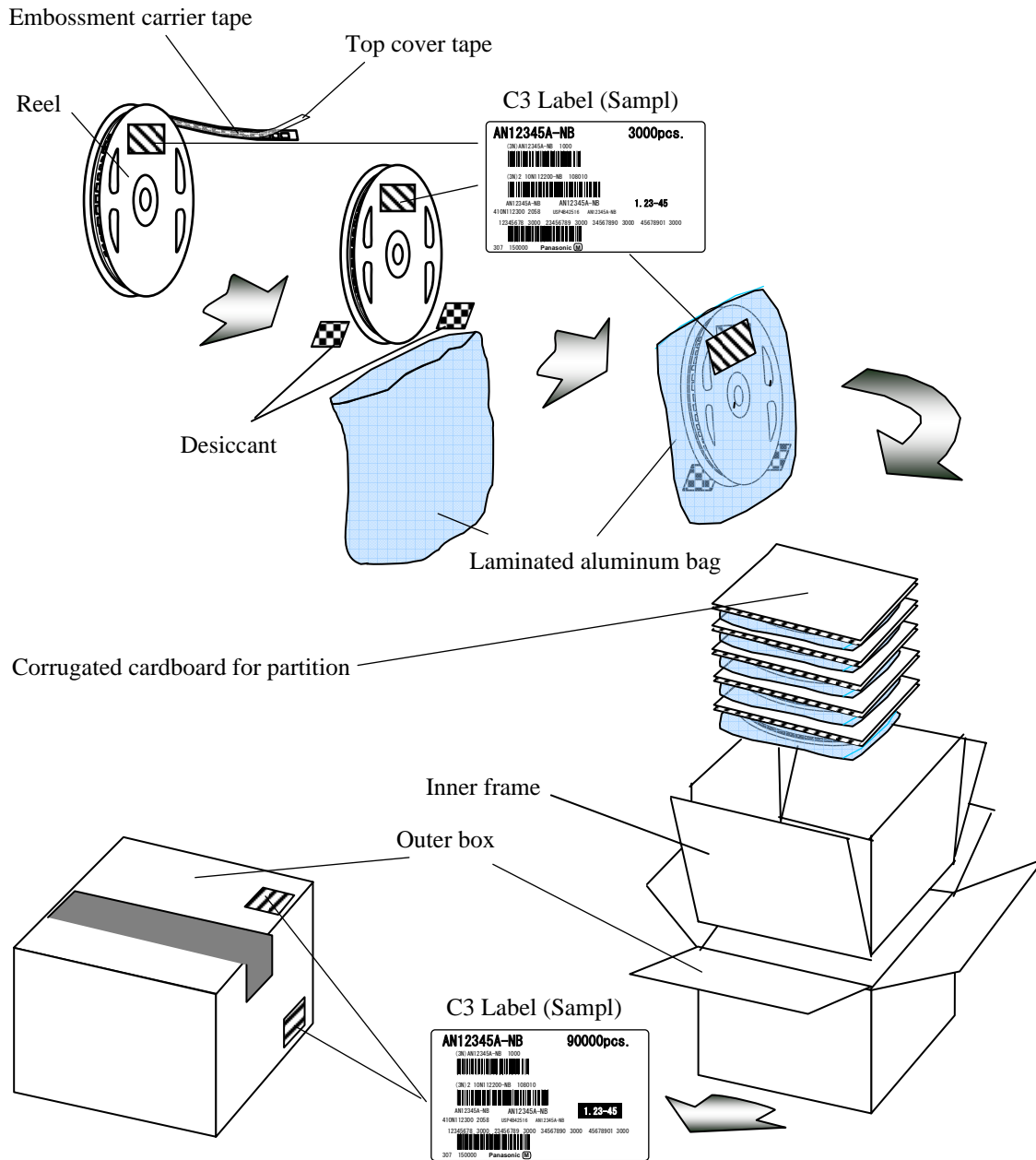
Prepared

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	<h1>Packing Specification</h1>	Total pages	page
		3	1

Specifications of packing by the embossment tape  
 ( Specifications for dampproof packing of the reel without the inner carton)



2009.03.09		
Prepared	Revised	

	<h1>Packing Specification</h1>		
		Total pages	page
			2

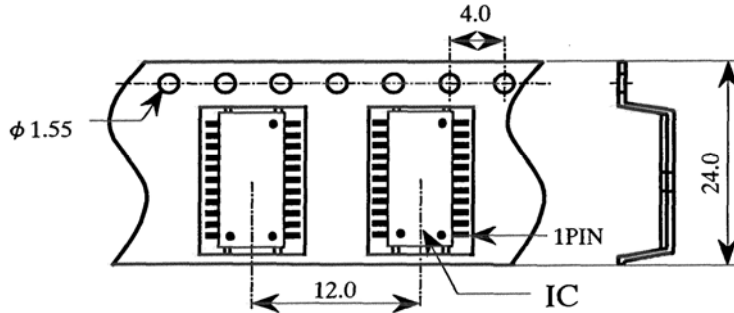
Package : HSOP034-P-0300A

Unit : mm

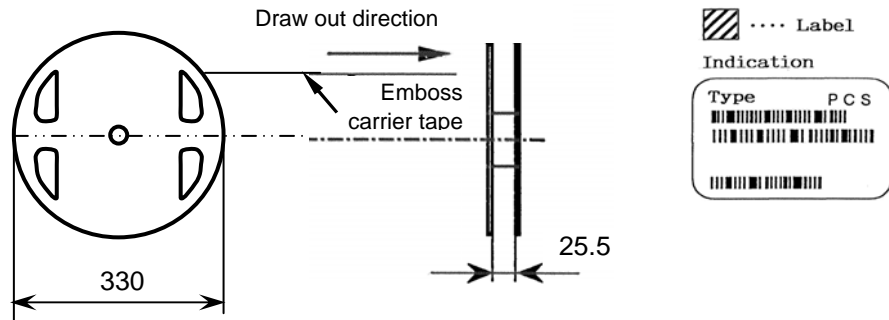
**1 Packing**

1) Tape

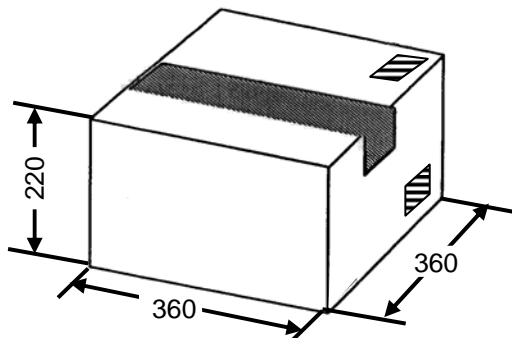
V F



2) Reel



3) Packing case



**2 Packing quantity**

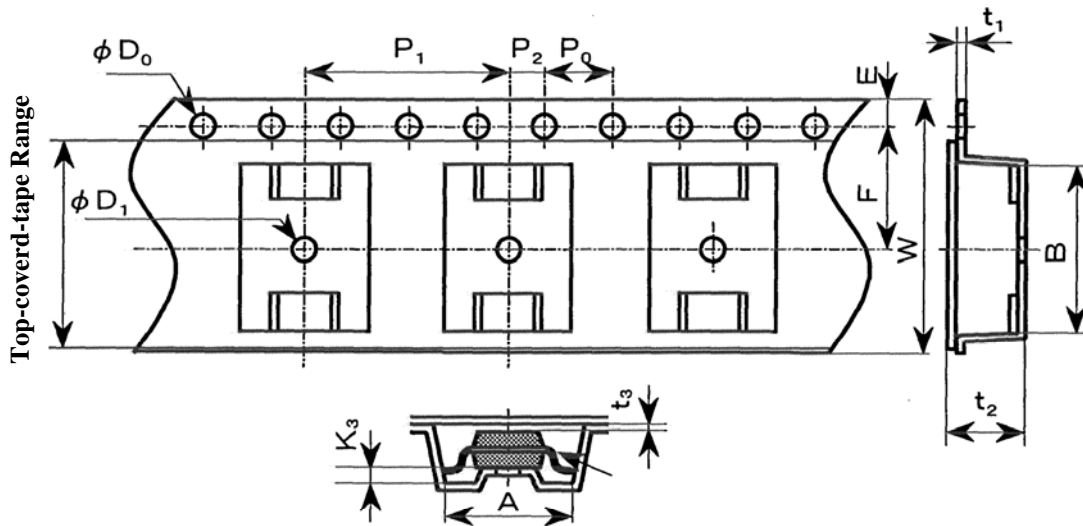
Form	IC quantity	Contents
Reel	3000 Pcs	Reel × 1Pcs
Packing case	15000 Pcs	Reel × 5Pcs

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	<h1>Packing Specification</h1>		
		Total pages	page
			3

Package : HSOP034-P-0300A

Unit : mm



Dimensions & Tolerance					
W	A	B	E	F	P <sub>1</sub>
24.0±0.3	8.7±0.1	14.5±0.1	1.75±0.1	11.5±0.1	12.0±0.1
P <sub>2</sub>	P <sub>0</sub>	$\phi D_1$	$\phi D_0$	t <sub>1</sub>	t <sub>2</sub>
2.0±0.1	4.0±0.1	2.05±0.05	1.55±0.05	0.3±0.05	1.9max
t <sub>3</sub>	K <sub>3</sub>				
(0.1)	(0.3)				

Prepared	Revised	
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# **Panasonic**

**Industrial Devices Company, Panasonic Corporation**

1 Kotari-yakemachi, Nagaokakyo City, Kyoto 617-8520, Japan  
Tel:075-951-8151



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.