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# FDMS8460

## N-Channel Power Trench<sup>®</sup> MOSFET

40V, 49A, 2.2mΩ

### Features

- Max  $r_{DS(on)}$  = 2.2mΩ at  $V_{GS} = 10V, I_D = 25A$
- Max  $r_{DS(on)}$  = 3.0mΩ at  $V_{GS} = 4.5V, I_D = 21.7A$
- Advanced Package and Silicon combination for low  $r_{DS(on)}$
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

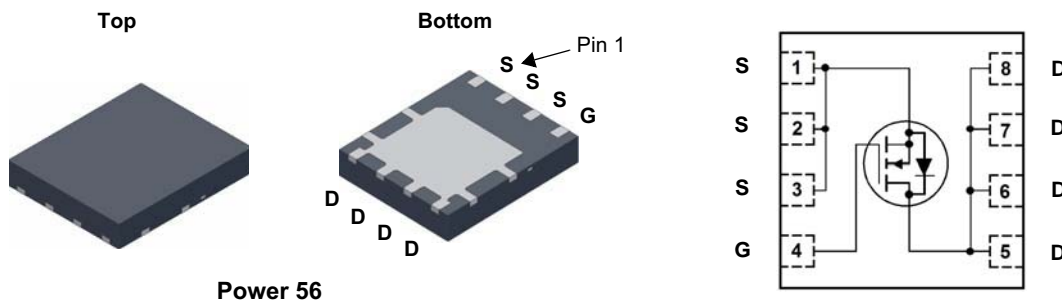


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench<sup>®</sup> process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Application

- DC - DC Conversion



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	40	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$	49	A
	-Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	167	
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	25	
	-Pulsed	160	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	864	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	104	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8460	FDMS8460	Power 56	13"	12 mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		32		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{V}, V_{DS} = 32\text{V}$ ,			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.0	1.9	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-7.5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 25\text{A}$		2.0	2.2	m $\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 21.7\text{A}$		2.6	3.0	
		$V_{GS} = 10\text{V}, I_D = 25\text{A}, T_J = 125^\circ\text{C}$		2.6	3.3	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\text{V}, I_D = 25\text{A}$		137		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$		5415	7205	pF
$C_{oss}$	Output Capacitance			1470	1955	pF
$C_{rss}$	Reverse Transfer Capacitance			170	250	pF
$R_g$	Gate Resistance	$f = 1\text{MHz}$	0.1	1.4	3.1	$\Omega$

### Switching Characteristics

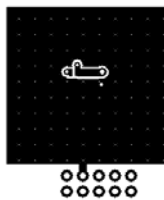
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\text{V}, I_D = 25\text{A}$ , $V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$		19	35	ns	
$t_r$	Rise Time			9	19	ns	
$t_{d(off)}$	Turn-Off Delay Time			48	78	ns	
$t_f$	Fall Time			7	14	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{V}$ to $10\text{V}$		78	110	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{V}$ to $4.5\text{V}$	$V_{DD} = 20\text{V}$ , $I_D = 25\text{A}$		36	51	nC
$Q_{gs}$	Gate to Source Charge				15		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				10		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 25\text{A}$ (Note 2)		0.8	1.3	V
		$V_{GS} = 0\text{V}, I_S = 2.1\text{A}$ (Note 2)		0.7	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 25\text{A}, di/dt = 100\text{A}/\mu\text{s}$		53	85	ns
$Q_{rr}$	Reverse Recovery Charge			40	64	nC

#### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a  $1\text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{in}$ . board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $50^\circ\text{C}/\text{W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper.

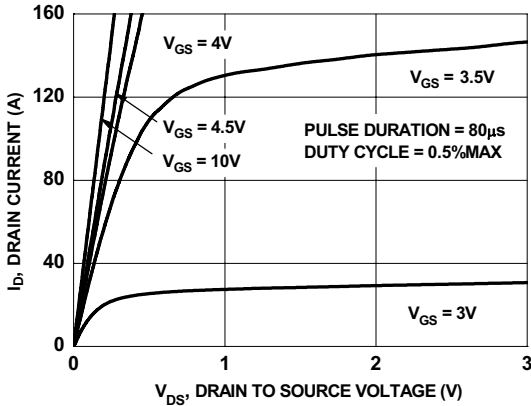


b.  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

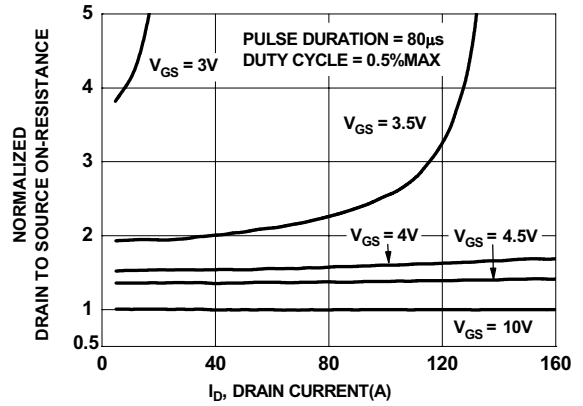
2. Pulse Test: Pulse Width  $< 300\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{mH}$ ,  $I_{AS} = 24\text{A}$ ,  $V_{DD} = 40\text{V}$ ,  $V_{GS} = 10\text{V}$

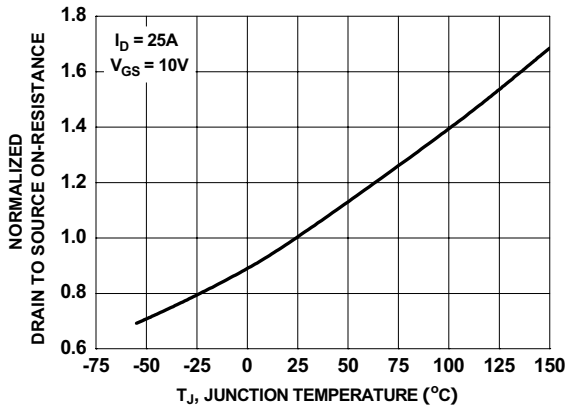
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



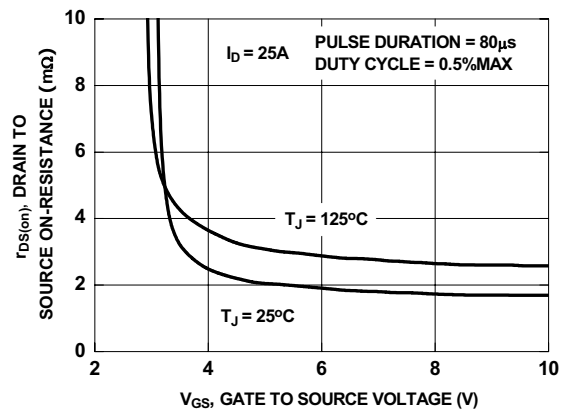
**Figure 1. On-Region Characteristics**



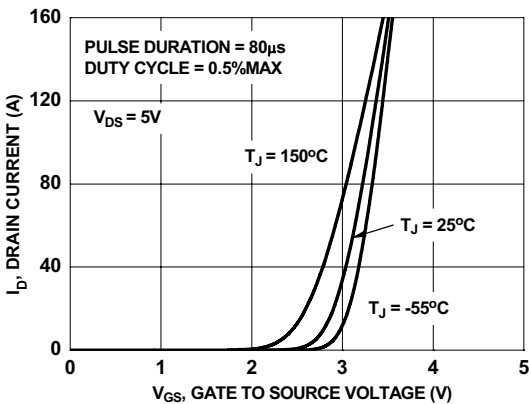
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



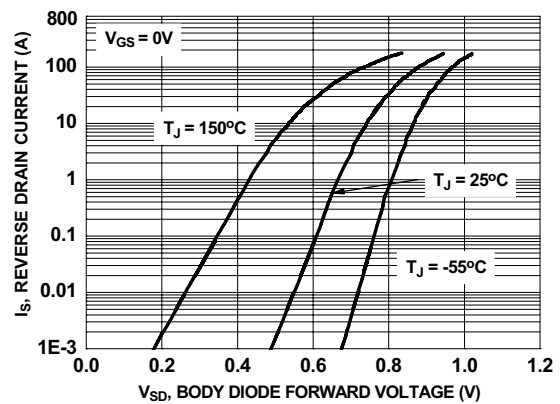
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

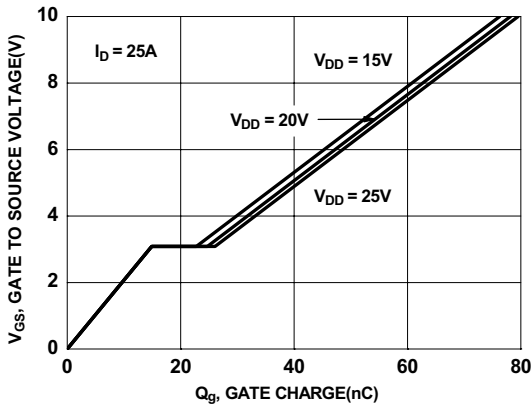


**Figure 5. Transfer Characteristics**

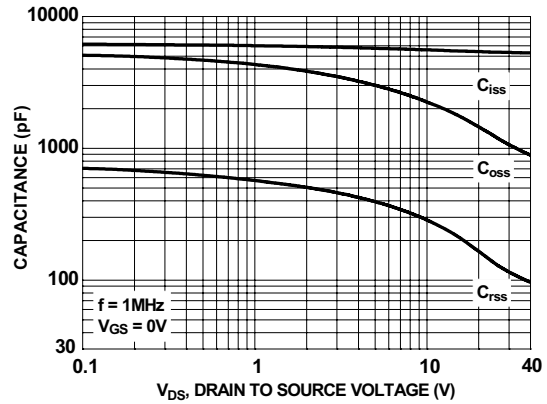


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

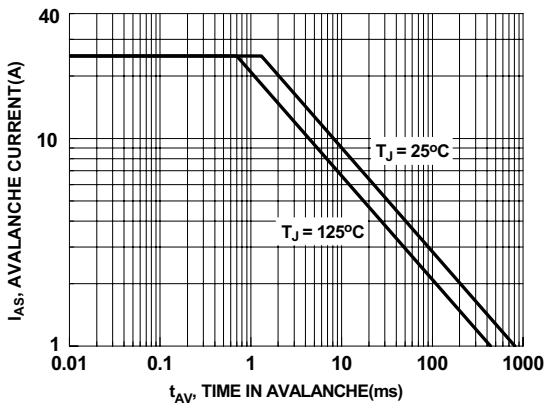
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



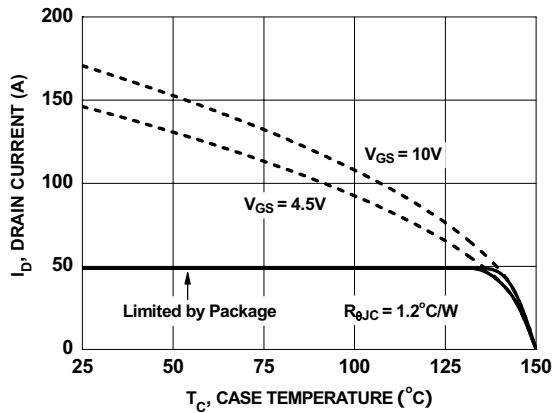
**Figure 7. Gate Charge Characteristics**



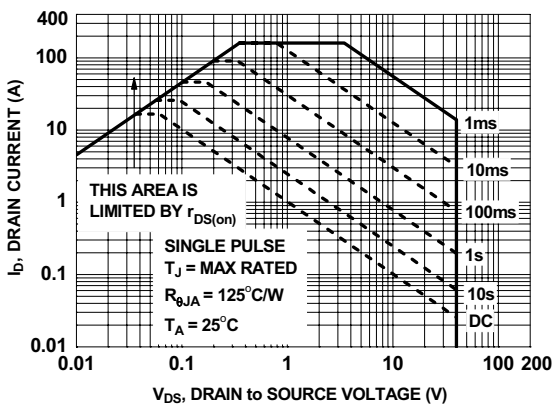
**Figure 8. Capacitance vs Drain to Source Voltage**



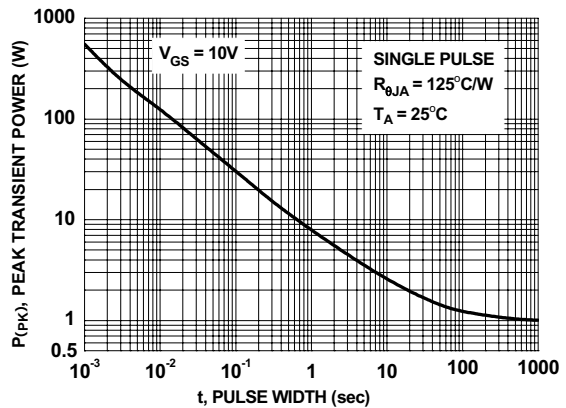
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

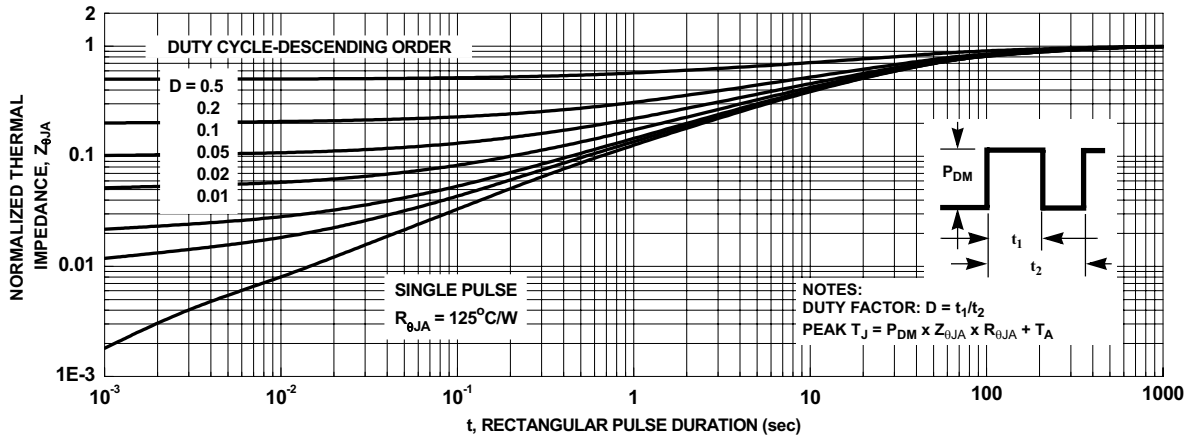


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 13. Transient Thermal Response Curve**

PQFN8 5X6, 1.27P  
CASE 483AE  
ISSUE A



TOP VIEW



LAND PATTERN RECOMMENDATION



SIDE VIEW

OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



DETAIL C  
SCALE: 2:1



DETAIL B  
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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