TPS7B4254-Q1 150-mA 40-V Voltage-Tracking LDO With 4-mV Tracking Tolerance

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 3A
  - Device CDM ESD Classification Level C6
- –40-V to 45-V Wide Input-Voltage Range (Maximum)
- Output-Voltage Adjust Range: 2 V to 40 V
- 150-mA Output Current Capability
- Very Low Output-Tracking Tolerance, ±4 mV
- 160-mV Low-Dropout Voltage When I_{OUT} = 100 mA
- Low Quiescent Current ($I_{(Q)}$):
  - < 4 µA When ADJ = LOW
  - 60 µA Typical at Light Load
- Extremely Wide ESR Range
  - 10-µF to 500-µF Ceramic Output Capacitor
  - ESR Range from 1 mΩ to 20 Ω
- Reverse Polarity Protection
- Current-Limit and Thermal-Shutdown Protection
- Output Short-Circuit-Proof to Ground and Supply
- Inductive Clamp at OUT Pin
- 8-Pin SO PowerPAD™ Package With Exposed Thermal Pad

2 Applications

- Off-Board Sensor Supply
- High-Precision Voltage Tracking
- Power Switch for Off-Board Load

3 Description

For automotive off-board sensors and low-current off-board modules, the power supply is through a long cable from the main board. In such cases, protection is required in the power devices for the off-board loads to prevent the onboard components from damage during a short to GND or short to battery caused by a broken cable. Off-board sensors require a power supply as consistent as that for onboard components to secure high accuracy of data acquisition.

The TPS7B4254-Q1 device is designed for automotive applications with a 45-V load dump. The device can either be used as one tracking low-dropout (LDO) regulator or as a voltage tracker to build one closed power loop for off-board sensors with an onboard main supply. The output of the device is accurately regulated by a reference voltage at the ADJ pin.

To provide an accurate power supply to the off-board modules, the device offers a 4-mV ultralow tracking tolerance between the ADJ and FB pins across temperature. The back-to-back PMOS topology eliminates the need for an external diode under a reverse-polarity condition. The TPS7B4254-Q1 device also includes thermal shutdown, inductive clamp, overload, and short-to-battery protection to prevent damage to onboard components during extreme conditions.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7B4254-Q1	SO PowerPAD (8)	4.89 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic

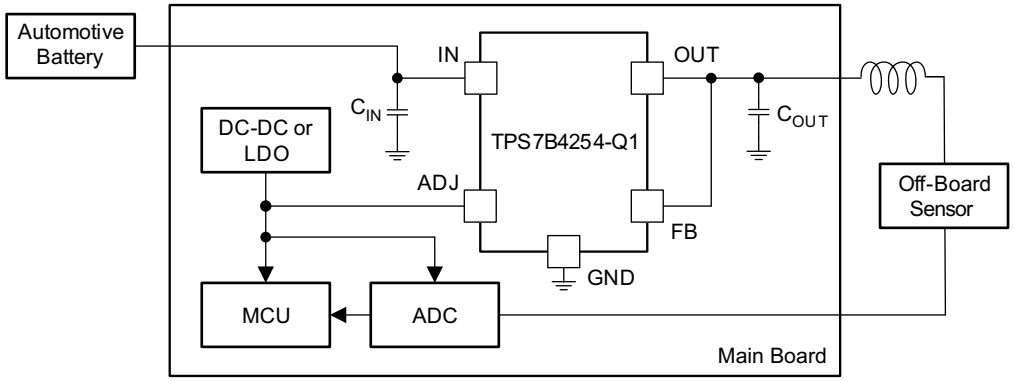


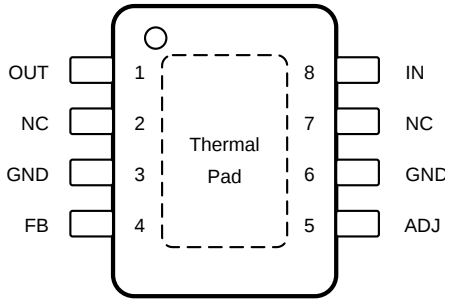
Table of Contents

4 Revision History

Changes from Original (April 2016) to Revision A	Page
• Changed data sheet from PRODUCT PREVIEW to PRODUCTION DATA	1

5 Pin Configuration and Functions

DDA Package
8-Pin HSOP With Exposed Thermal Pad
Top View



NC – No internal connection

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
ADJ	5	I	Connect the reference to this pin. A low signal disables the device and a high signal enables the device. The reference voltage can be connected directly or by a voltage divider for lower output voltages. To compensate for line influences, connect a capacitor close to the device pin.
FB	4	I	This pin is the feedback pin, which can connect to the external resistor divider to select the output voltage.
GND	3, 6	G	Ground reference
IN	8	I	This pin is the device supply. To compensate for line influences, connect a capacitor close to the device pin.
NC	2, 7	NC	Not internally connected.
OUT	1	O	Block to GND with a capacitor close to the device pins with respect to the capacitance and ESR requirements listed in the *Output Capacitor* section.
Exposed thermal pad		—	Connect the thermal pad to the GND pin or leave it floating.

(1) I = input, O = output, G = ground, NC = no internal connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Unregulated input voltage	IN(2)	–40	45	V
Regulated output voltage	OUT(2)(3)	–1	45	V
Voltage difference between the input and output	IN – OUT	–40	45	V
Reference voltage	ADJ(2)	–0.3	45	V
Feedback input voltage for the tracker	FB(2)	–1	45	V
Reference voltage minus the input voltage	ADJ – IN(4)		18	V
Operating junction temperature, T_J		–40	150	ºC
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND pin.
(3) An internal diode is connected between the OUT and GND pins with 600-mA dc current capability for inductive clamp protection.
(4) When the (ADJ – IN) voltage is higher than 18 V, the (ADJ – OUT) voltage should be maintained lower than 18 V, otherwise the device can be damaged.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	All pins except NC	±4000	V
			NC pins	±2000	
		Charged-device model (CDM), per AEC Q100-011		±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Unregulated input voltage(2)	4	40	V
V_{ADJ}	Reference input voltage	1.5	18	V
V_{FB}	Feedback input voltage for the tracker	1.5	18	V
V_{OUT}	Regulated output voltage	1.5	40	V
C_{OUT}	Output capacitor requirements(3)	10	500	µF
	Output ESR requirements(4)	0.001	20	Ω
T_J	Operating junction temperature	–40	150	ºC

(1) Within the functional range the device operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related *Electrical Characteristics* table.
(2) $V_{IN} > V_{ADJ} + V_{DROPOUT}$
(3) The minimum output capacitance requirement is applicable for a worst-case capacitance tolerance of 30%. When a resistor divider is connected between the OUT and FB pins (the output voltage is higher than reference voltage), a 47-nF feedforward capacitor is required to be connected between the OUT and FB pins for loop stability, and the ESR range of the output capacitor is required to be from 0.001 to 10 Ω.
(4) Relevant ESR value at f = 10 kHz

6.4 Thermal Information

THERMAL METRIC[1]		TPS7B4254-Q1 DDA (HSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{IN} = 13.5 V, V_{ADJ} ≥ 2 V, T_J = –40ºC to 150ºC, over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN(UVLO)}$	IN undervoltage detection	V_{IN} rising			3.65	V
		V_{IN} falling			2.8	V
ΔV_{OUT}	Output voltage tracking accuracy[1]	I_{OUT} = 100 µA to 150 mA, V_{IN} = 4 to 40 V $V_{ADJ} < V_{IN} – 1$ V 2 V < V_{ADJ} < 18 V	–4		4	mV
$\Delta V_{OUT(\Delta IO)}$	Load regulation, steady-state	I_{OUT} = 0.1 to 150 mA, V_{ADJ}= 5 V			4	mV
$\Delta V_{OUT(\Delta VI)}$	Line regulation, steady-state	I_{OUT} = 10 mA, V_{IN} = 6 to 40 V, V_{ADJ} = 5 V			4	mV
PSRR	Power-supply ripple rejection	f_{rip} = 100 Hz, V_{rip} = 0.5 VPP, C_{OUT} = 10 µF, I_{OUT} = 100 mA		70		dB
$V_{DROPOUT}$	Dropout voltage ($V_{DROPOUT} = V_{IN} – V_{OUT}$)	I_{OUT} = 100 mA, $V_{IN} = V_{ADJ}$ ≥ 4 V[2]		160	260	mV
$I_{OUT(LIM)}$	Output current limitation	V_{ADJ} = 5 V, OUT short to GND	151	450	520	mA
$I_{R(IN)}$	Reverse current at IN	V_{IN} = 0 V, V_{OUT} = 40 V, V_{ADJ} = 5 V	–2		0	µA
$I_{R(–IN)}$	Reverse current at negative IN	V_{IN} = –40 V, V_{OUT} = 0 V, V_{ADJ} = 5 V	–10			µA
T_{SD}	Thermal shutdown temperature			175		ºC
T_{SD_hys}	Thermal shutdown hysteresis			15		ºC
I_Q	Current consumption	4 V ≤ V_{IN} ≤ 40 V, V_{ADJ} = 0 V		2	4	µA
		4 V ≤ V_{IN} ≤ 40 V, V_{ADJ} = 5 V, I_{OUT} < 100 µA		60	100	µA
		4 V ≤ V_{IN} ≤ 40 V, V_{ADJ} = 5 V, I_{OUT} < 150 mA		210	260	µA
$I_{Q(DROPOUT)}$	Current consumption in dropout region	$V_{IN} = V_{ADJ}$ = 5 V, I_{OUT} = 100 µA		70	140	µA
I_{ADJ}	Reference input current	$V_{ADJ} = V_{FB}$ = 5 V			5.5	µA
$V_{ADJ(LOW)}$	Reference low signal valid	V_{OUT} = 0 V	0		0.7	V
$V_{ADJ(HIGH)}$	Reference high signal valid	$\lvert V_{OUT} – V_{ADJ} \rvert$ < 4 mV	2		18	V
I_{FB}	FB bias current	$V_{ADJ} = V_{FB}$ = 5 V			0.5	µA

(1) The tracking accuracy is specified when the FB pin is directly connected to the OUT pin which means $V_{ADJ} = V_{OUT}$, external resistor divider variance is not included.
(2) Measured when the output voltage, V_{OUT}, has dropped 10 mV from the nominal value.

6.6 Typical Characteristics

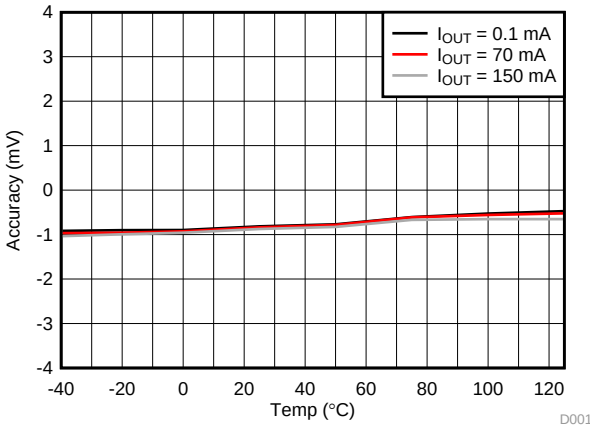


Figure 1. Tracking Accuracy vs Ambient Temperature

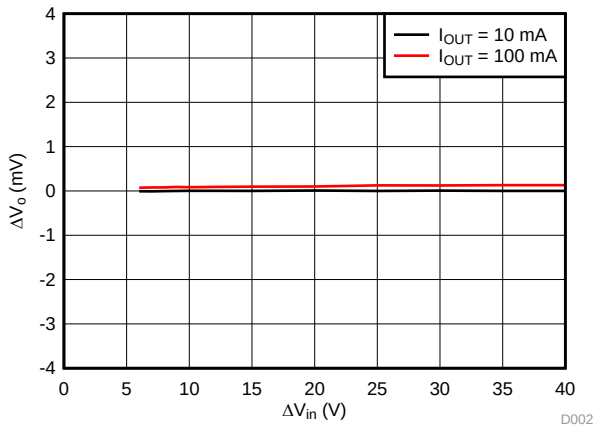


Figure 2. Line Regulation

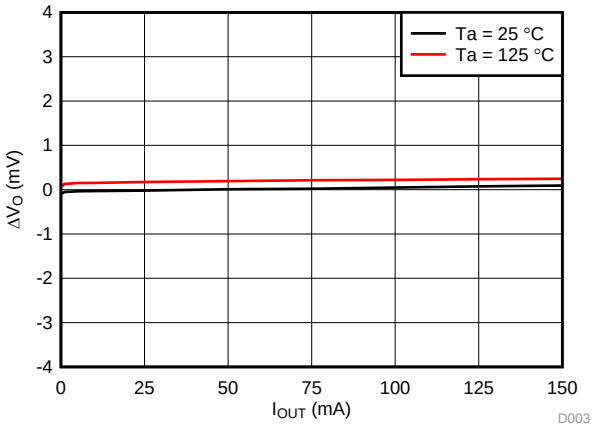
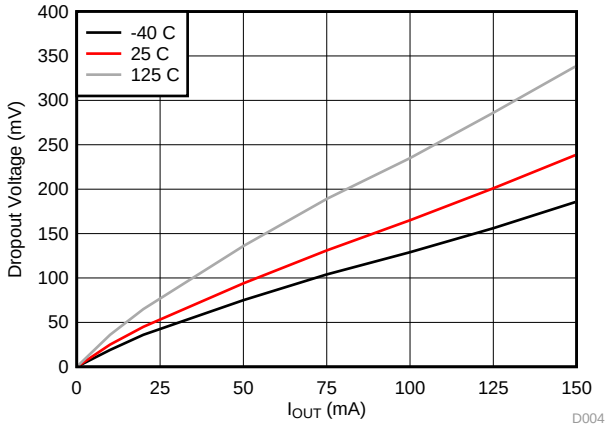
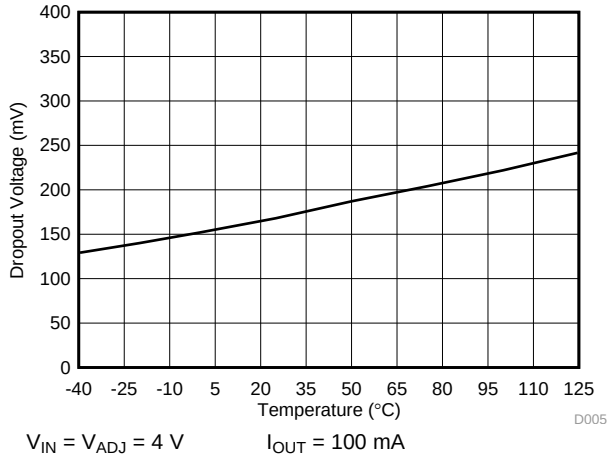


Figure 3. Load Regulation



V_{IN} = V_{ADJ} = 4 V

Figure 4. Dropout Voltage vs Output Current



V_{IN} = V_{ADJ} = 4 V I_{OUT} = 100 mA

Figure 5. Dropout Voltage vs Ambient Temperature

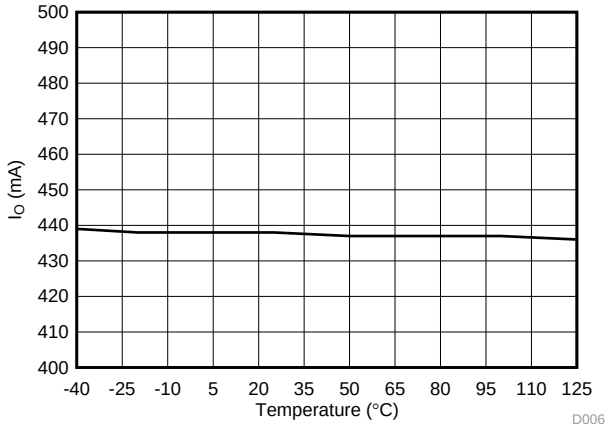


Figure 6. Current Limit ($I_{OUT(LIM)}$) vs Ambient Temperature

Typical Characteristics (continued)

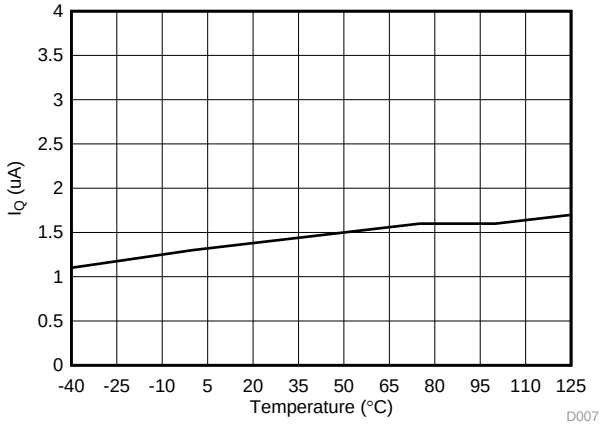


Figure 7. Shutdown Current vs Ambient Temperature

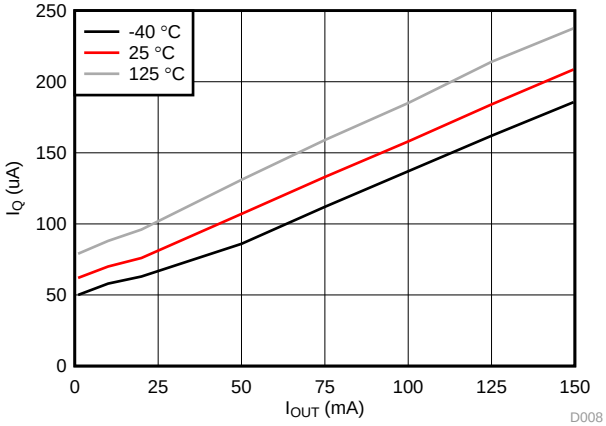


Figure 8. Quiescent Current vs Output Current

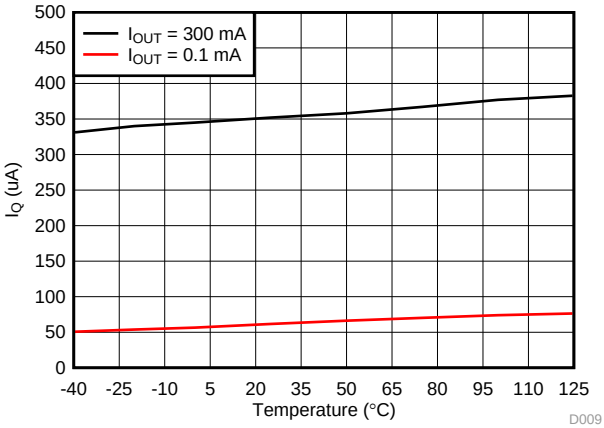
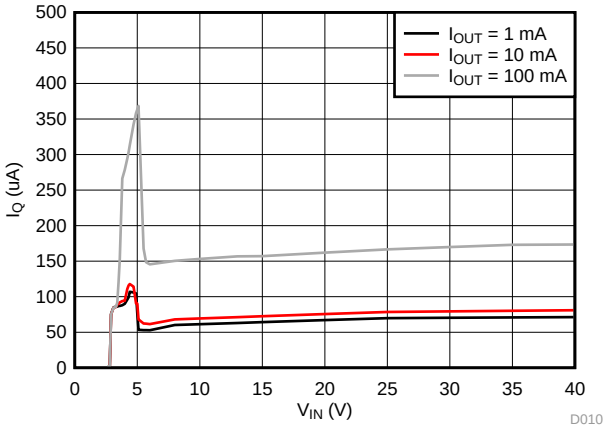
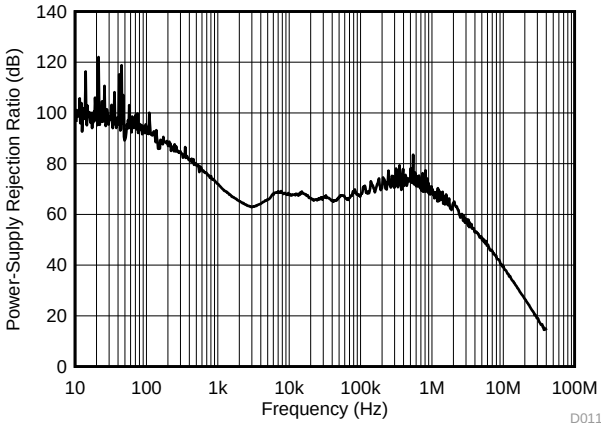


Figure 9. Quiescent Current vs Ambient Temperature



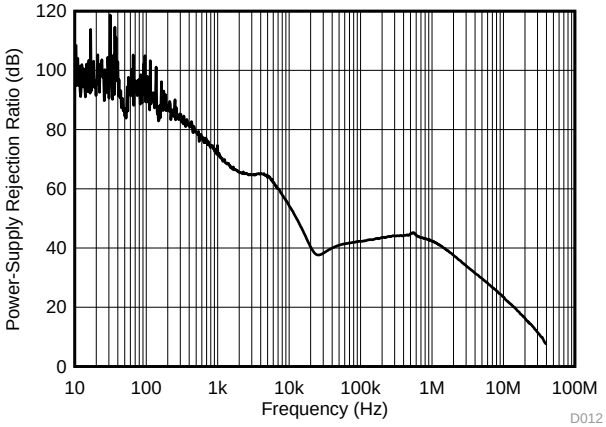
V_{ADJ} = 5 V

Figure 10. Quiescent Current vs Input Voltage



C_{OUT} = 10 µF I_{OUT} = 1 mA T_A = 25°C
V_{IN} = 14 V V_{ADJ} = 5 V

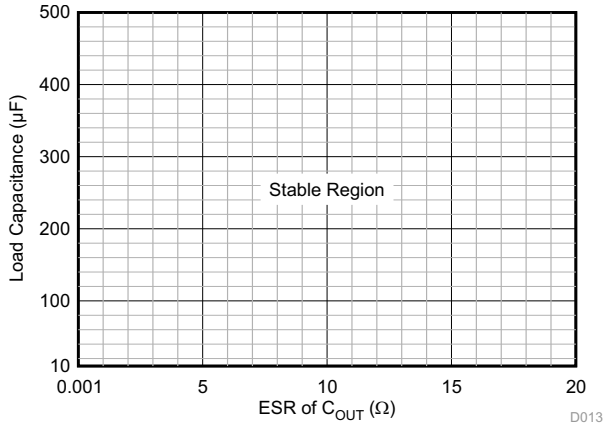
Figure 11. PSRR



C_{OUT} = 10 µF I_{OUT} = 100 mA T_A = 25°C
V_{IN} = 14 V V_{ADJ} = 5 V

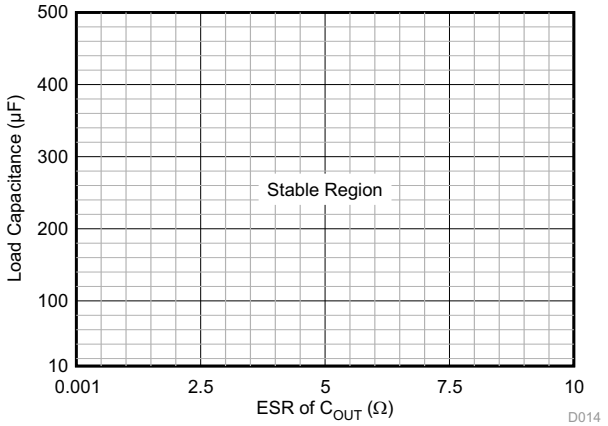
Figure 12. PSSR

Typical Characteristics (continued)



$V_{FB} = V_{OUT}$

Figure 13. ESR Stability vs Load Capacitance



$V_{FB} < V_{OUT}$

Figure 14. ESR Stability vs Load Capacitance

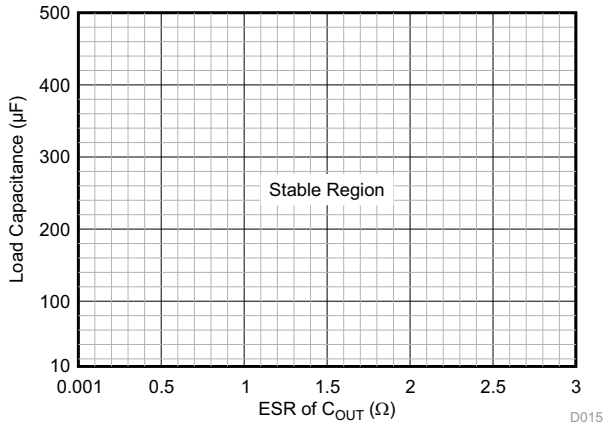
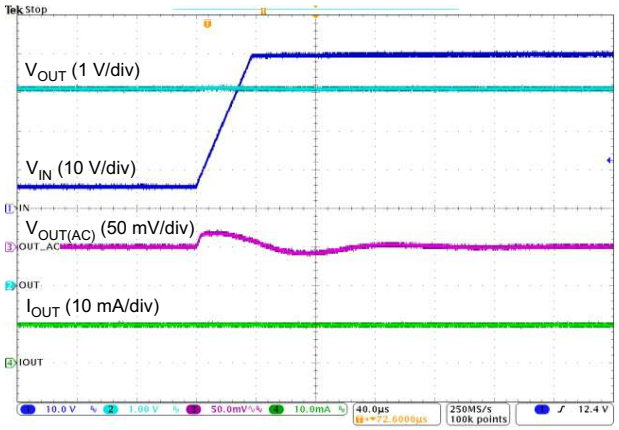
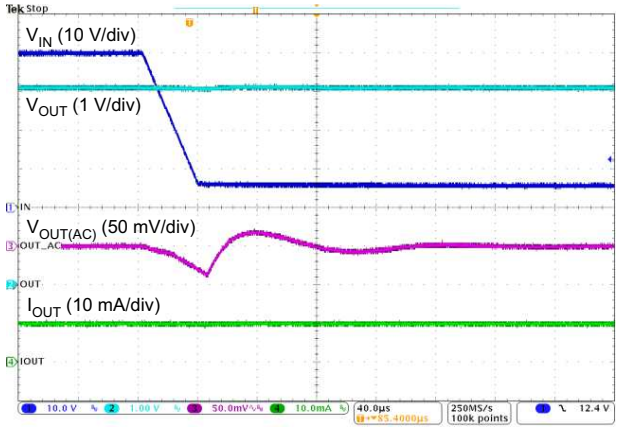


Figure 15. ESR Stability vs Load Capacitance (Multiple Output Capacitors in parallel)



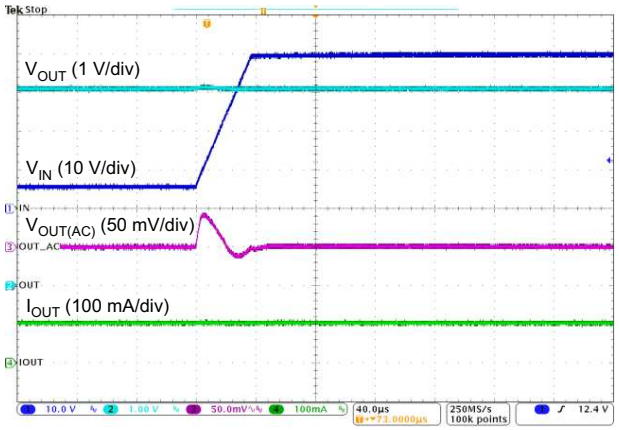
V_{IN} = 6 to 40 V V_{ADJ} = 5 V C_{OUT} = 10 µF
I_{OUT} = 10 mA 40 µs/div

Figure 16. 6-V to 40-V Line Transient



V_{IN} = 40 to 6 V V_{ADJ} = 5 V C_{OUT} = 10 µF
I_{OUT} = 10 mA 40 µs/div

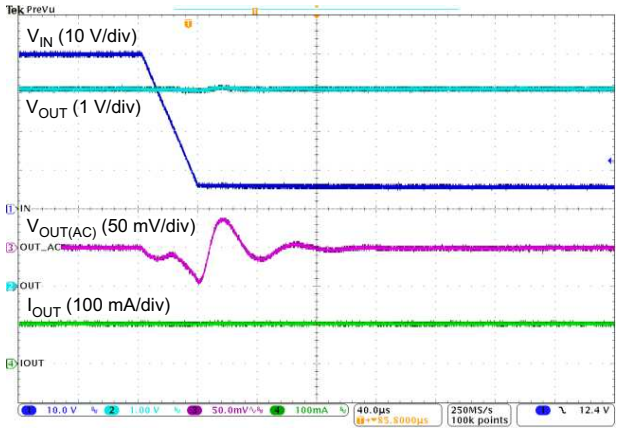
Figure 17. 40-V to 6-V Line Transient



V_{IN} = 6 to 40 V V_{ADJ} = 5 V C_{OUT} = 10 µF
I_{OUT} = 100 mA 40 µs/div

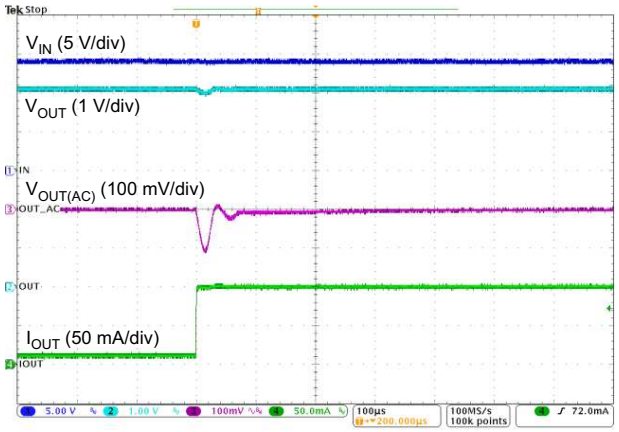
Figure 18. 6-V to 40-V Line Transient

Typical Characteristics (continued)



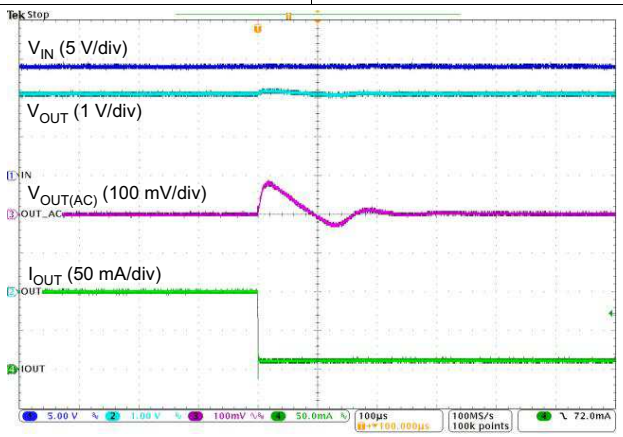
V_{IN} = 40 to 6 V V_{ADJ} = 5 V C_{OUT} = 10 µF
I_{OUT} = 100 mA 40 µs/div

Figure 19. 40-V to 6-V Line Transient



V_{IN} = 14 V V_{ADJ} = 5 V C_{OUT} = 10 µF
I_{OUT} = 10 mA to 100 mA 100 µs/div

Figure 20. 10-V to 100-mA Load Transient



V_{IN} = 14 V V_{ADJ} = 5 V C_{OUT} = 10 µF
I_{OUT} = 100 mA to 10 mA 100 µs/div

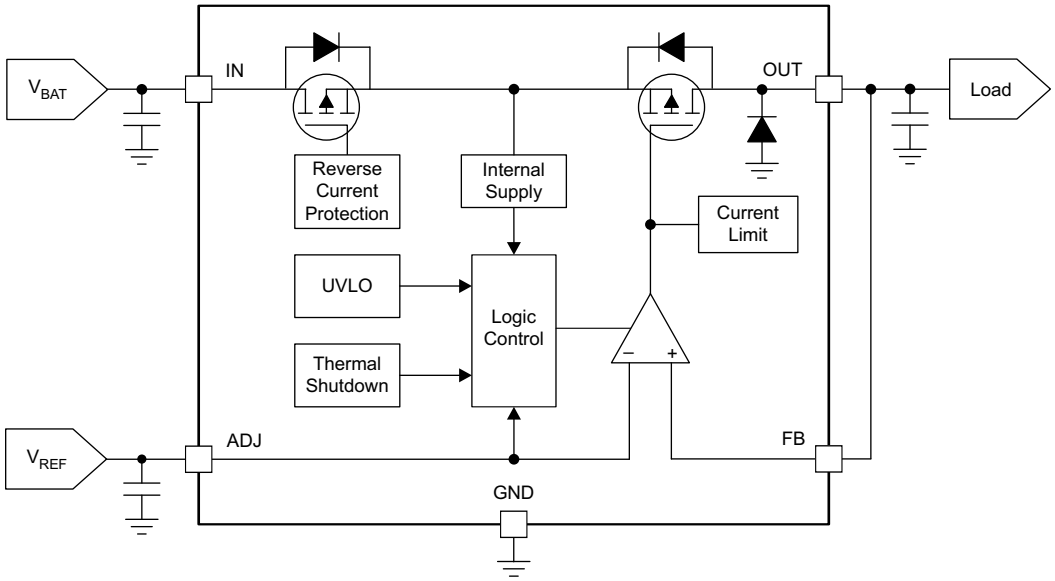
Figure 21. 100-mA to 10-mA Load Transient

7 Detailed Description

7.1 Overview

The TPS7B4254-Q1 device is a monolithic integrated low-dropout voltage tracker with an ultralow tracking tolerance. Key protection circuits are integrated in the device, including output current limitation, reverse polarity protection, inductive load clamp, output short-to-battery protection, and thermal shutdown in case of an overtemperature event.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Short-Circuit and Overcurrent Protection

The TPS7B4254-Q1 device features integrated fault protection, which makes the device ideal for automotive applications. To keep the device in a safe area of operation during certain fault conditions, internal current-limit protection is used to limit the maximum output current. This protection protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, the current through the pass element is limited to $I_{OUT(LIM)}$ to protect the device from excessive power dissipation.

7.3.2 Integrated Inductive Clamp Protection

During output turnoff, the cable inductance continues to source the current from the output of the device. The device integrates an inductive clamp at the OUT pin to help to dissipate the inductive energy stored in the cable. An internal diode is connected between the OUT and GND pins with a dc-current capability of 600 mA for inductive clamp protection.

7.3.3 OUT Short-to-Battery and Reverse-Polarity Protection

The TPS7B4254-Q1 device can withstand a short to battery on the output, as shown in Figure 22. Therefore, no damage to the device occurs.

Feature Description (continued)

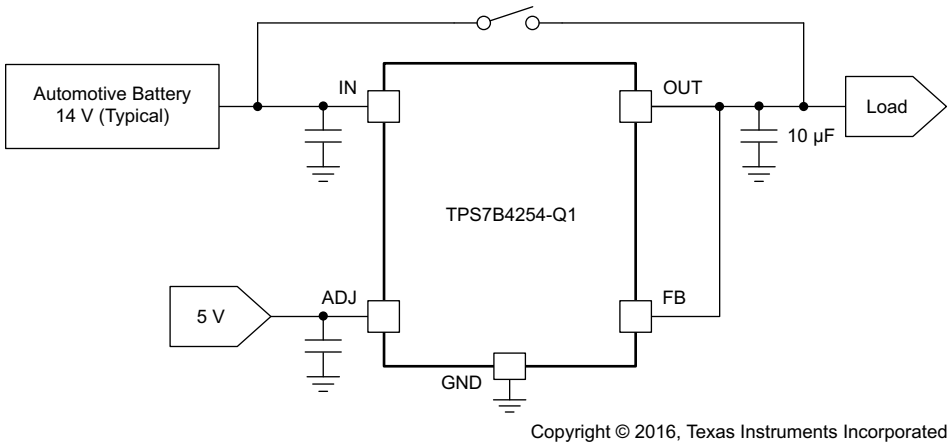


Figure 22. OUT Short to Battery, $V_{IN} = V_{BAT}$

A short to the battery can also occur when the device is powered by an isolated supply at lower voltage, as shown in Figure 23. In this case, the TPS7B4254-Q1 supply-input voltage is set to 7 V when a short to battery (14 V typical) occurs on the OUT pin, which operates at 5 V. The internal back-to-back PMOS remains on for 1 ms, during which the input voltage of the TPS7B4254-Q1 device charges up to the battery voltage. A diode connected between the output of the dc-dc converter and the input of the TPS7B4254-Q1 device is required in case the other loads connected behind the dc-dc converter cannot withstand the voltage of an automotive battery. To achieve a lower dropout voltage, TI recommends using a Schottky diode. This diode can be eliminated if the output of the dc-dc converter and the loads connected behind it withstand automotive battery voltage.

The internal back-to-back PMOS is switched to OFF when reverse polarity or a short to battery occurs for 1 ms. After that, the reverse current that flows out through the IN pin is less than 10 µA. Meanwhile, a special ESD structure implemented at the input ensures the device can withstand –40 V.

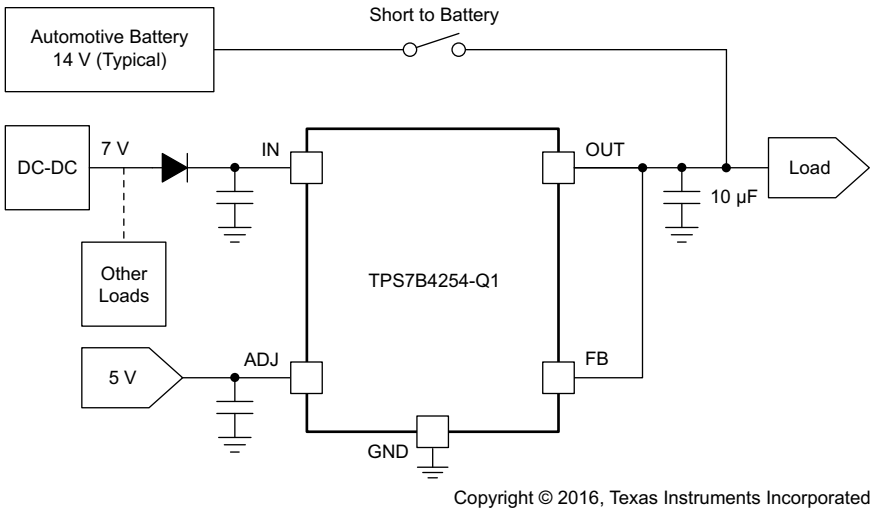


Figure 23. OUT Short to Battery, VIN < V_{BAT}

In most cases, the output of the TPS7B4254-Q1 device is shorted to the battery through an automotive cable. The parasitic inductance on the cable results in LC oscillation at the output of the TPS7B4254-Q1 device when the short to battery occurs. The peak voltage at the output of the TPS7B4254-Q1 device must be lower than the absolute-maximum voltage rating (45 V) during LC oscillation.

Feature Description (continued)

7.3.4 Undervoltage Shutdown

The device has an internally fixed undervoltage-shutdown threshold. Undervoltage shutdown activates when the input voltage on IN drops below UVLO. This activation ensures the regulator is not latched into an unknown state during a low input-supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and then recovers, the regulator shuts down and then powers up with a standard power-up sequence when the input voltage is above the required level.

7.3.5 Thermal Protection

The device incorporates a thermal shutdown (TSD) circuit as a protection from overheating. During continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature decreases to 15°C (typical) lower than the TSD trip point, the output turns on.

NOTE

The purpose of the internal protection circuitry of the TPS7B4254-Q1 device is to protect against overload conditions and is not intended as a replacement for proper heat-sinking. Continuously running the device into thermal shutdown degrades device reliability.

7.3.6 Regulated Output (OUT)

The OUT pin is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has an incorporated soft-start feature to control the initial current through the pass element.

7.3.7 Adjustable Output Voltage (FB and ADJ)

7.3.7.1 OUT Voltage Equal to the Reference Voltage

With the reference voltage applied directly at the ADJ pin and the FB pin connected to the OUT pin, the voltage at the OUT pin equals to the reference voltage at the ADJ pin, as shown in Figure 24.

$$V_{OUT} = V_{ADJ} \quad (1)$$

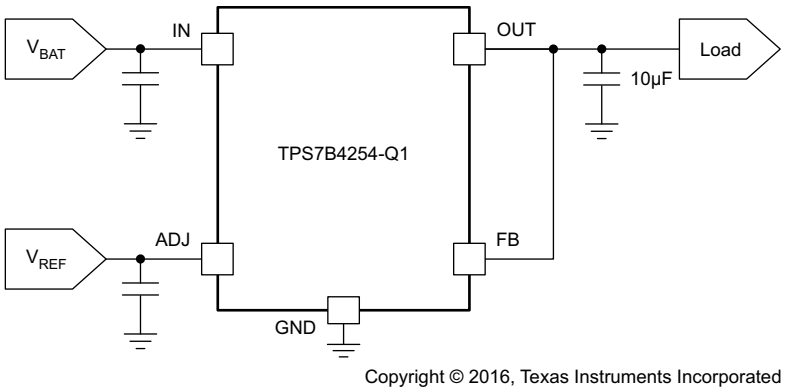


Figure 24. OUT Voltage Equal to the Reference Voltage

7.3.7.2 OUT Voltage Higher Than Reference Voltage

By using an external resistor divider connected between the OUT and FB pins, an output voltage higher than reference voltage can be generated as shown in Figure 25. Use Equation 2 to calculate the value of the output voltage. The recommended range for R1 and R2 is from 10 kΩ to 100 kΩ.

$$V_{OUT} = V_{ADJ} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

Feature Description (continued)

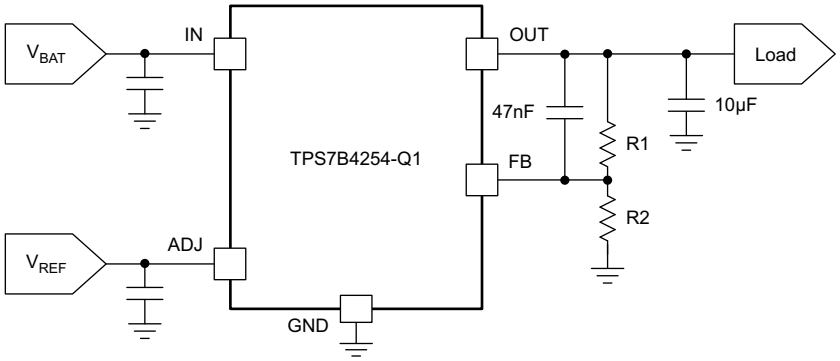


Figure 25. OUT Voltage Higher Than the Reference Voltage

7.3.7.3 Output Voltage Lower Than Reference Voltage

By using an external resistor divider connected at the ADJ pin, an output voltage lower than reference voltage can be generated as shown in Figure 26. Use Equation 3 to calculate the output voltage. The recommended value for both R1 and R2 is less than 100 kΩ.

$$V_{OUT} = V_{REF} \times \frac{R2}{R1 + R2} \quad (3)$$

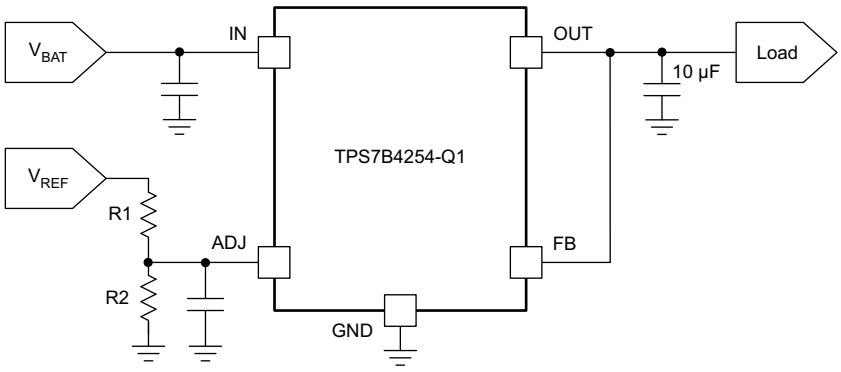


Figure 26. OUT Voltage Lower Than the Reference Voltage

7.4 Device Functional Modes

7.4.1 Operation With V_{IN} < 4 V

The maximum UVLO voltage is 3.65 V, and the device generally operates at an input voltage above 4 V. The device can also operate at a lower input voltage; no minimum UVLO voltage is specified. At an input voltage below the actual UVLO voltage, the device does not operate.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7B4254-Q1 device is a 150-mA low-dropout tracking regulator with ultralow tracking tolerance. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic function of the device.

8.2 Typical Applications

8.2.1 Application With Output Voltage Equal to the Reference Voltage

Figure 27 shows a typical application circuit for the TPS7B4254-Q1 device. Different values of external components can be used, depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. TI recommends using a low-ESR ceramic capacitor with a dielectric of type X5R or X7R.

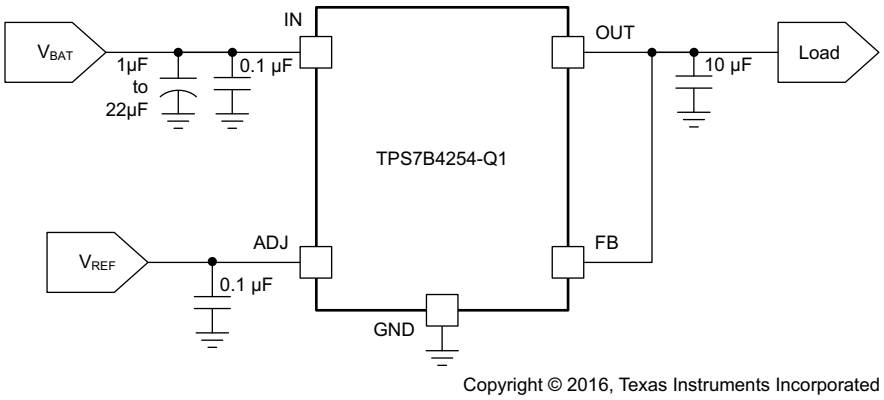


Figure 27. Output Voltage Equals the Reference Voltage

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the design parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	4 V to 40 V
Output voltage	2 V to 40 V
ADJ voltage	2 V to 18 V
Output capacitor	10 µF to 500 µF
Output capacitor ESR range	0.001 Ω to 20 Ω

8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Reference voltage
- Output current

- Current limit

8.2.1.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 10 µF with a 0.1 µF ceramic bypass capacitor in parallel. The voltage rating must be greater than the maximum input voltage.

8.2.1.2.2 Output Capacitor

To ensure the stability of the TPS7B4254-Q1 device, the device requires an output capacitor with a value in the range from 10 µF to 500 µF and with an ESR range from 0.001 Ω to 20 Ω when the FB pin is directly connected to the OUT pin. TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

To achieve an output voltage higher than the reference voltage, a resistor divider is connected between the OUT pin and the FB pin. In this case, a 47-nF feedforward capacitor must be connected between the OUT and FB pins for loop stability. The ESR of the output capacitor must be from 0.001 Ω to 10 Ω.

When multiple capacitors (two or more) are connected in parallel at the OUT pin, the ESR range of each output capacitor must be from 0.001 Ω to 3 Ω for loop stability.

In case the FB pin is shorted to ground, the TPS7B4254-Q1 device functions as a power switch with no need for the output capacitor.

8.2.1.3 Application Curve

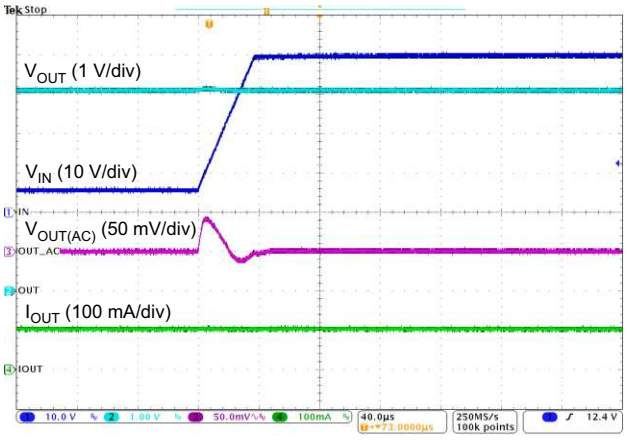


Figure 28. 6-V to 40-V Line Transient

8.2.2 High-Accuracy LDO

With an accurate voltage rail, the TPS7B4254-Q1 device can be used as an LDO with ultrahigh-accuracy output voltage by configuring the device as shown in Figure 29.

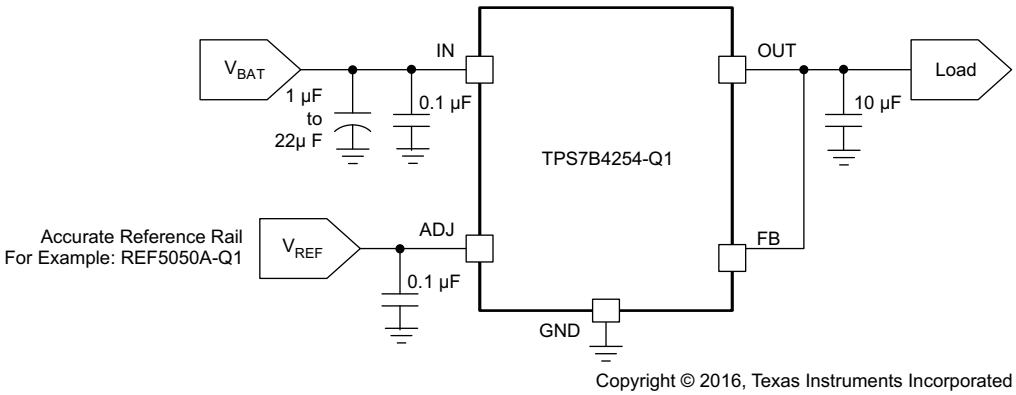


Figure 29. High-Accuracy LDO Application

For example, assume the reference voltage is a 5-V rail with 0.1% accuracy. Because the tracking accuracy between the ADJ and OUT pins is specified below 4 mV across temperature, the output accuracy of the TPS7B4254-Q1 device can be calculated with Equation 4.

$$\text{Accuracy of } V_{OUT} = \frac{V_{ADJ} \times 0.1\% + 4\ \text{mV}}{V_{OUT}} \times 100\ \% = \frac{5 \times 0.1\% + 0.004}{5} \times 100\ \% = 0.18\ \% \quad (4)$$

9 Power Supply Recommendations

The device is designed to operate with an input voltage supply from 4 V to 40 V. This input supply must be well regulated. If the input supply is more than a few inches away from the TPS7B4254-Q1 device, TI recommends adding an electrolytic capacitor with a value of 10 µF and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

For the layout of the TPS7B4254-Q1 device, place the input and output capacitors close to the devices as shown in the *Functional Block Diagram*. To enhance the thermal performance, TI recommends surrounding the device with some vias. Minimize equivalent series inductance (ESL) and ESR to maximize performance and ensure stability. Place every capacitor as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of vias and long traces for the path between the output capacitor and the OUT pins because vias can negatively impact system performance and even cause instability.

10.2 Layout Example

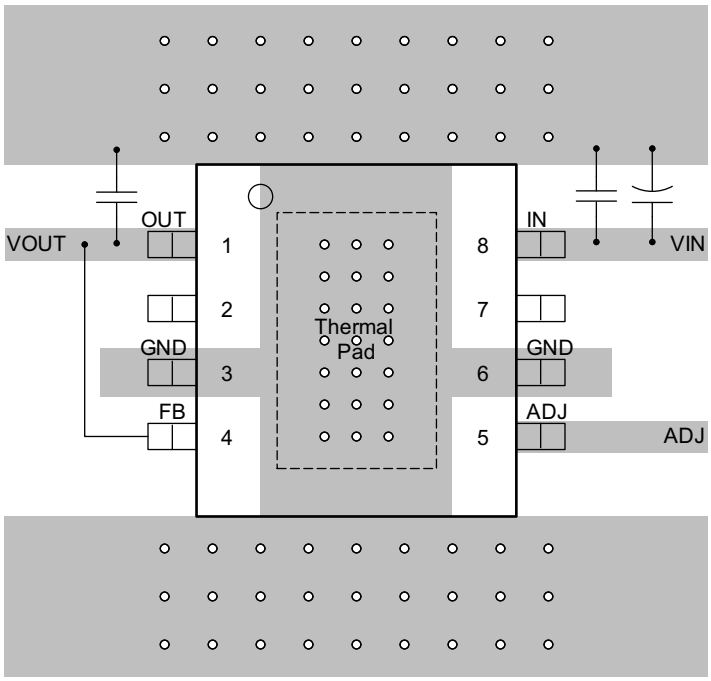


Figure 30. TPS7B4254-Q1 Layout Example

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B4254QDDARQ1	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	4254	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

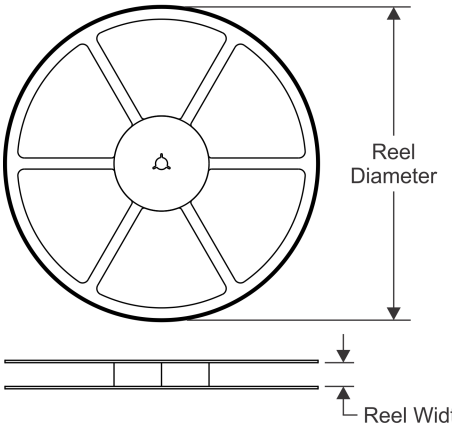
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

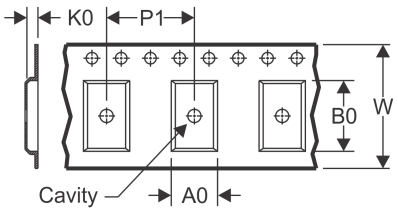
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

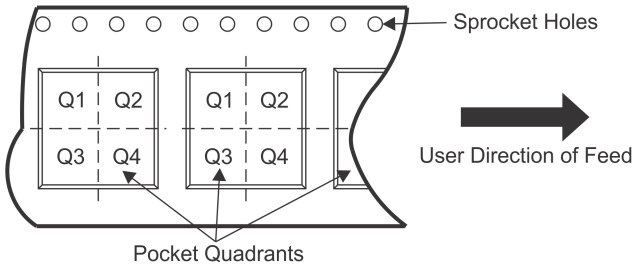


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

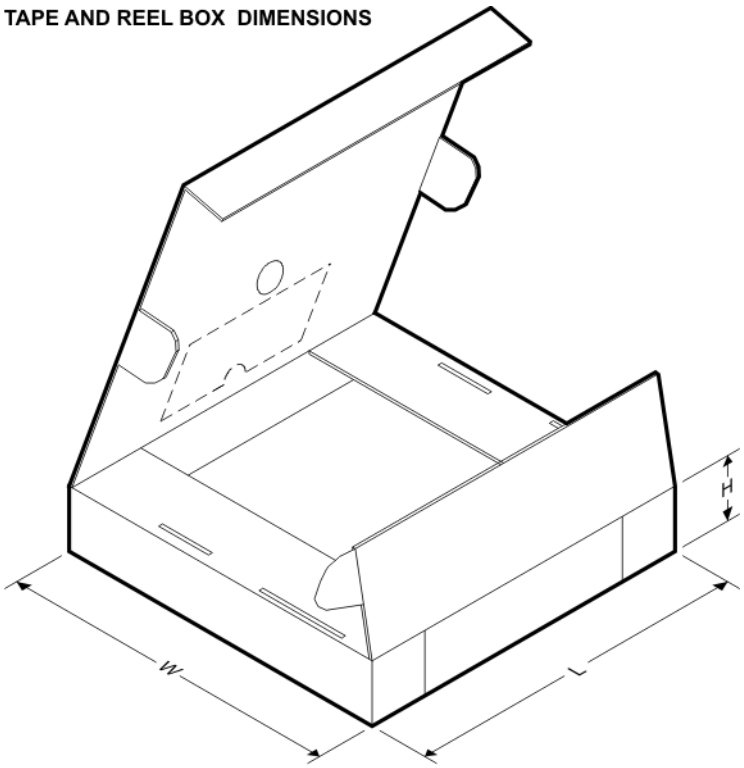
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B4254QDDARQ1	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

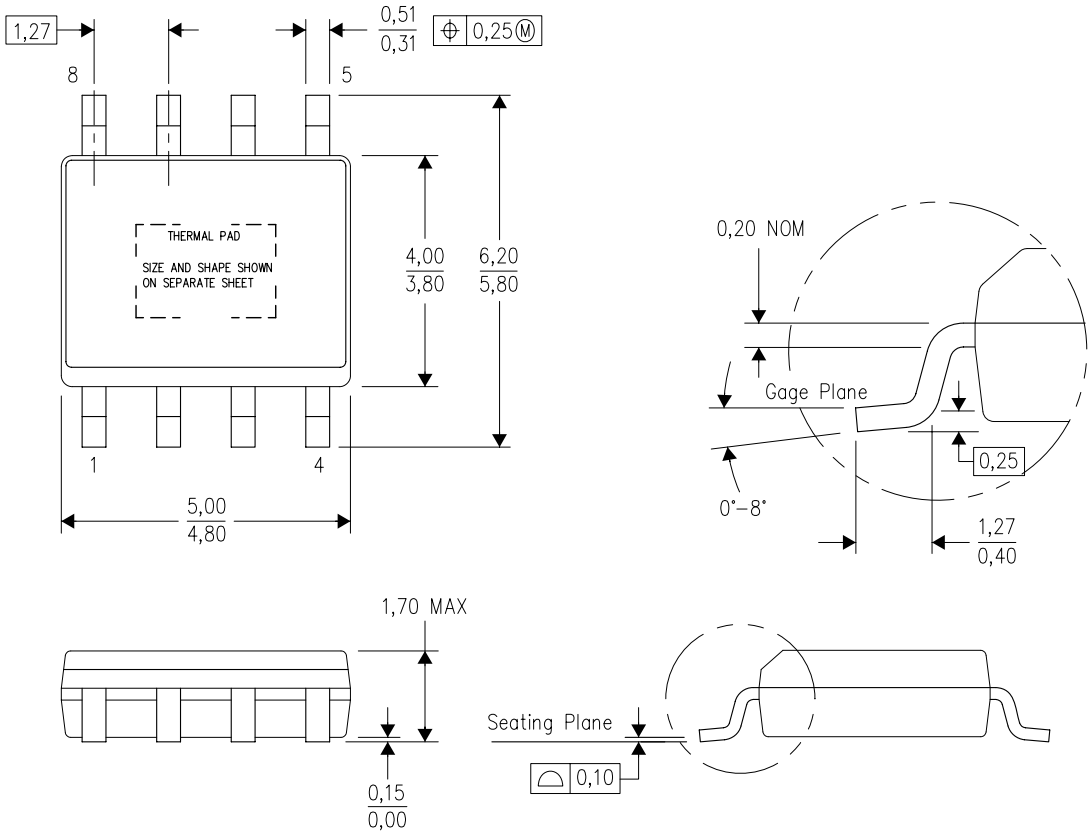
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B4254QDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

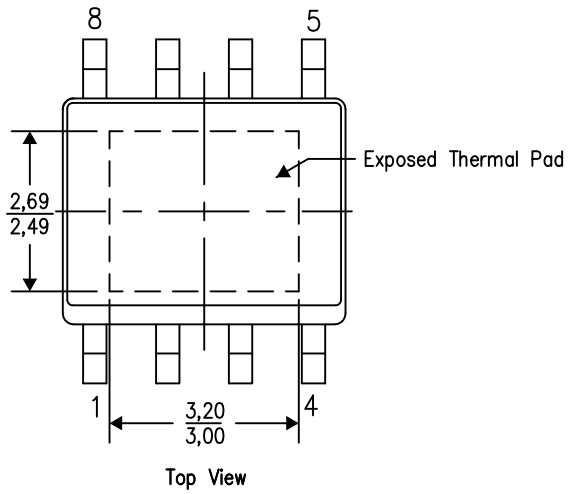
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206322–7/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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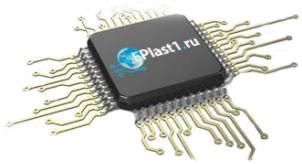

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