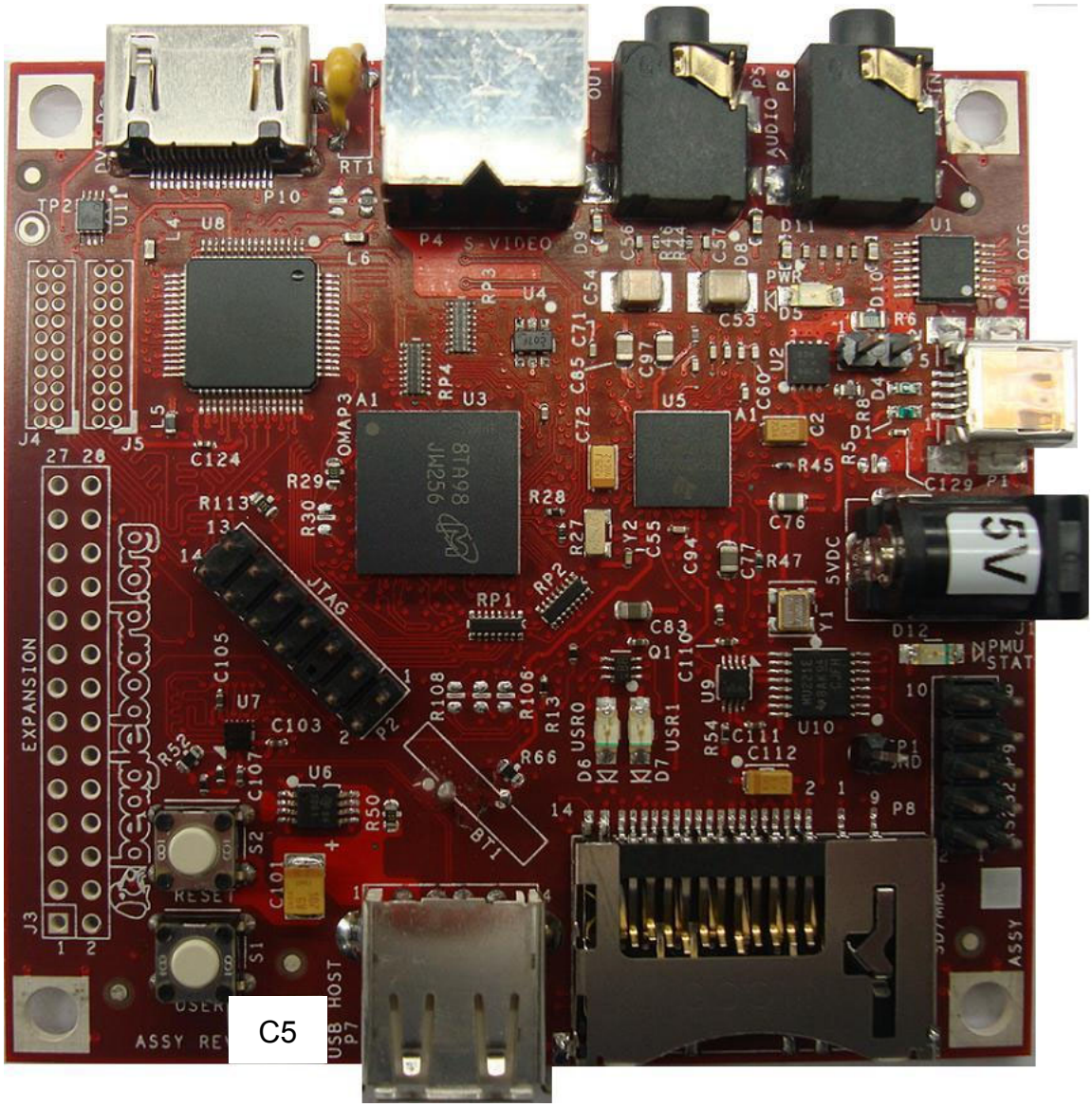

BeagleBoard
System Reference Manual
Rev C5

Revision 1.00
July 15, 2011

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1.0 Introduction

This document is the System Reference Manual for the BeagleBoard, a low cost OMAP3530 based board supported through BeagleBoard.org. This document provides detailed information on the overall design and usage of the BeagleBoard from the system level perspective. It is not intended to provide detailed documentation of the OMAP3530 processor or any other component used on the board. It is expected that the user will refer to the appropriate documents for these devices to access detailed information.

The key sections in this document are:

Section 2.0– Change History
Provides tracking for the changes made to the System Reference Manual.

Section 3.0– Definitions and References
This section provides definitions for commonly used terms and acronyms.

Section 4.0– Overview
This is a high level overview of the BeagleBoard.

Section 5.0– Specification
Provided here are the features and electrical specifications of the BeagleBoard.

Section 6.0-Product Contents
Describes what the BeagleBoard package looks like and what is included in the box.

Section 7.0– Hookup
Covered here is how to connect the various cables to the BeagleBoard.

Section 8.0– System Architecture and Design
This section provides information on the overall architecture and design of the BeagleBoard. This is a very detailed section that goes into the design of each circuit on the board.

Section 9.0– Connector Pinouts and Cables
The section describes each connector and cable used in the system. This will allow the user to create cables, purchase cables, or to perform debugging as needed.

Section 10.0– BeagleBoard Accessories
Covered in this section are a few of the accessories that may be used with BeagleBoard. This is not an exhaustive list, but does provide an idea of the types of cables and accessories that can be supported and how to find them. It also provides a definition of what they need to be. It does not guarantee that these devices will work on all OS implementations.

Section 11.0 – Mechanical
Information is provided here on the dimensions of the BeagleBoard.

Section 12.0 – Board Verification
A description is provided on how to setup the board and using the verification process and SW to verify that the board is functional.

Section 13.0 – Troubleshooting
Here is where you can find tips on troubleshooting the setup of the BeagleBoard.
Section 14.0- Known Issues
This section describes the known issues with the current revision of the BeagleBoard and any workarounds that may be possible.
Section 15.0- BeagleBoard Components
This section provides information on the top and bottom side silkscreen of the BeagleBoard showing the location of the components.
Section 16.0- BeagleBoard Schematics
These are the schematics for the BeagleBoard and information on where to get the PDF and OrCAD files..
Section 17.0- Bill Of Material
This section describes where to get the latest Bill of Material for the BeagleBoard.
Section 18.0- BeagleBoard PCB Information
This section describes where to get the PCB file information for the BeagleBoard.

2.0 Change History

2.1 Change History

Table 1 tracks the changes made for each revision of this document.

Table 1. Change History

Rev	Changes	Date	By
C4	Initial release.	12/15/2009	GC
C4.1	Typos and miscellaneous corrections.	7/29/2010	GC
C4.2	Updated resistor values in section 8.2.6 to reflect schematic and BOM values.	11/25/2010	GC
C5	1. Updated Tables 20 and 21 2. Updated to rev C5 to cover new Memory device used due to obsolescence of previous version.	7/15/2011	GC

2.2 Revision C3 vs. C4

There are three key changes on the Rev C4 board versus the Rev C3 version.

- Use of the OMAP3530DCBB72 device which is the 720MHZ version of the OMAP3530.
- An updated version of the UBoot software. The following changes will affect the user experience:

- The Beagle splash screen has been replaced with an orange only screen at boot up.
- Turning on VAUX2 for the EHCI fix

- A more advanced fix for the EHCI noise issue on Rev C3 board. This involves a change in the power circuitry for the 1.8V rail supplied to the EHCI PHY interface. The power is now derived from the VAUX2 on the TPS65950 through a filter circuit.

2.3 Revision C4 vs. C5

- The memory device is no longer offered by Micron. This required a move to upgrade to the replacement part. This resulted in a doubling of the NAND flash memory from 2Gb (256MB) to 4Gb (512MB). The LPDDR memory size remains the same.
- In order to support the new NAND size, a newer image is loaded onto the flash on the C5 version.

3.0 Definitions and References

3.1 Definitions

SD- Secure Digital
SDIO- Secure Digital Input Output
MMC- Multimedia Card
MDDR- Mobile Dual Data Rate
SDRAM- Synchronous Dual Access Memory
OMAP3530- The CortexA8 based System on a Chip from Texas Instruments.

4.0 BeagleBoard Overview

The BeagleBoard is an OMAP3530 platform designed specifically to address the Open Source Community. It has been equipped with a minimum set of features to allow the user to experience the power of the OMAP3530 and is not intended as a full development platform as many of the features and interfaces supplied by the OMAP3530 are not accessible from the BeagleBoard. By utilizing standard interfaces, the BeagleBoard is highly extensible to add many features and interfaces. It is not intended for use in end products. All of the design information is freely available and can be used as the basis for a product. BeagleBoards will not be sold for use in any product as this hampers the ability to get the boards to as many community members as possible and to grow the community.

4.1 BeagleBoard Usage Scenarios

The **Figure 1** provides an example of a few of the various usage scenarios for the BeagleBoard.

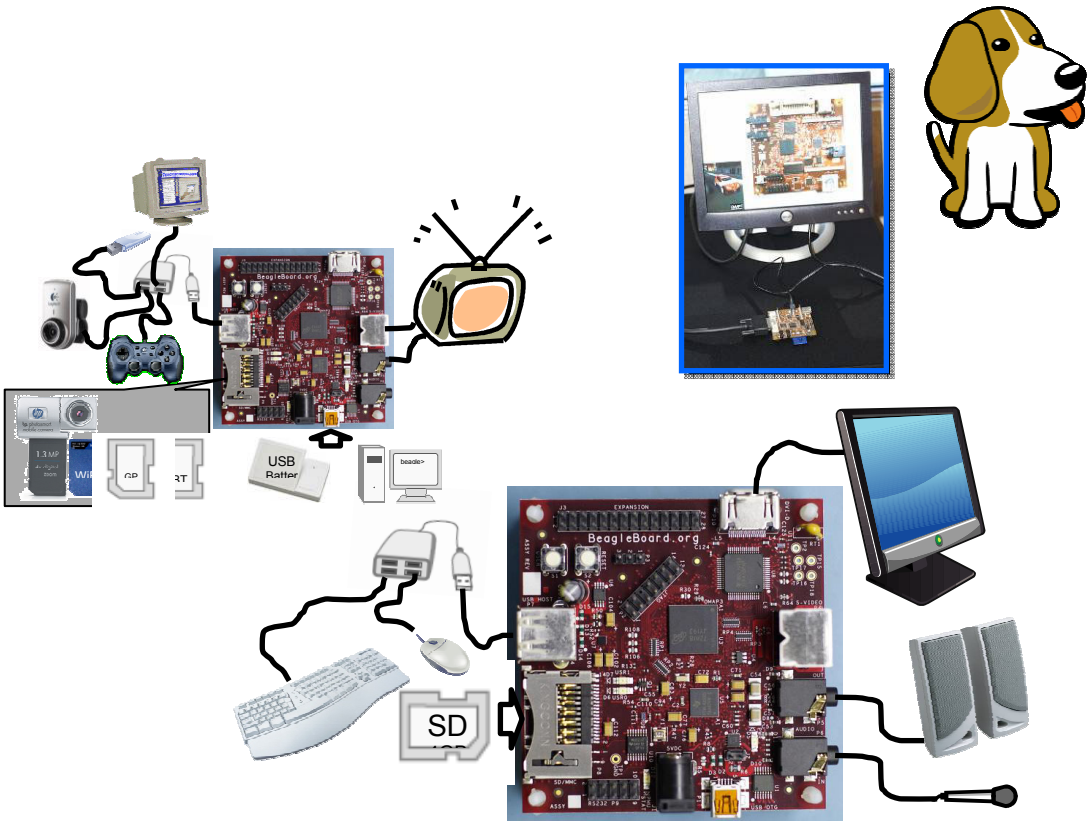

Figure 1. BeagleBoard Usage Scenarios

5.0 BeagleBoard Specification

This section covers the specifications of the BeagleBoard and provides a high level description of the major components and interfaces that make up the BeagleBoard.

5.1 BeagleBoard Features

Table 2 provides a list of the BeagleBoard's features.

Table 2. BeagleBoard Features

	Feature	
Processor	OMAP3530DCBB72 720MHz	
POP Memory	Micron	
	2Gb NAND (256MB) **4Gb C5**	2Gb MDDR SDRAM (256MB)
PMIC TPS65950	Power Regulators	
	Audio CODEC	
	Reset	
	USB OTG PHY	
Debug Support	14-pin JTAG	GPIO Pins
	UART	LEDs
PCB	3.1" x 3.0" (78.74 x 76.2mm)	6 layers
Indicators	Power	2-User Controllable
	PMU	
HS USB 2.0 OTG Port	Mini AB USB connector	
	TPS65950 I/F	
	MiniAB	
HS USB Host Port	Single USB HS Port	Up to 500ma Power
Audio Connectors	3.5mm	3.5mm
	L+R out	L+R Stereo In
SD/MMC Connector	6 in 1 SD/MMC/SDIO	4/8 bit support, Dual voltage
User Interface	1-User defined button	Reset Button
Video	DVI-D	S-Video
Power Connector	USB Power	DC Power
Expansion Connector (Not Populated)	Power (5V & 1.8V)	UART
	McBSP	McSPI
	I2C	GPIO
	MMC	PWM
2 LCD Connectors	Access to all of the LCD control signals plus I2C	3.3V, 5V, 1.8V

The following sections provide more detail on each feature and sections of the BeagleBoard.

5.2 OMAP Processor

The BeagleBoard uses the OMAP3530DCBB72 720MHZ version and comes in a .4mm pitch POP package. POP (Package on Package) is a technique where the memory, NAND and SDRAM, are mounted on top of the OMAP3530. For this reason, when looking at the BeagleBoard, you will not find an actual part labeled OMAP3530.

5.3 Memory

The Micron POP memory is used on the Rev C4 BeagleBoard and is mounted on top of the processor as mentioned. The key function of the POP memory is to provide:

- 2Gb NAND x 16 (256MB)
- 2Gb MDDR SDRAM x32 (256MB @ 166MHz)

No other memory devices are on the BeagleBoard. It is possible however, that additional memory can be added to BeagleBoard by:

- Installing a SD or MMC in the SD/MMC slot
- Use the USB OTG port and a powered USB hub to drive a USB Thumb drive or hard drive.
- Install a thumbdrive into the EHCI USB port

Support for this is dependent upon driver support in the OS.

5.4 Power Management

The TPS65950 is used on the Rev C4 to provide power to the BeagleBoard with the exception of the 3.3V regulator which is used to provide power to the DVI-D encoder and RS232 driver. In addition to the power the TPS65950 also provides:

- Stereo Audio Out
- Stereo Audio in
- Power on reset
- USB OTG PHY
- Status LED

5.5 HS USB 2.0 OTG Port

The USB OTG port can be used as the primary power source and communication link for the BeagleBoard and derives power from the PC over the USB cable. The client port is limited in most cases to 500mA by the PC. A single PC USB port is sufficient to power the BeagleBoard. If additional devices are connected to the expansion bus and the 5V rail is used to power them or if a high powered USB device is connected to the EHCI port, then the power required could exceed that supplied by a USB port or Hub.

It is possible to take this to 1A by using a Y cable if additional power is needed for either the USB host port or an expansion card. **Figure 2** shows and example of the Y-Cable for the USB.

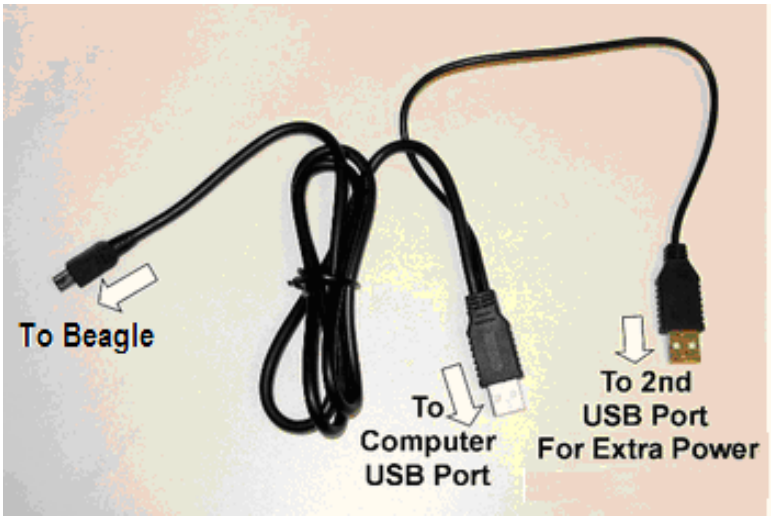

Figure 2. USB Y-Cable

The BeagleBoard requires a single minAB to USB A cable or as mentioned a Y-Cable can be used if needed.

There is an option to provide external power to the BeagleBoard using a 5V DC supply and is discussed later in this section.

5.6 HS USB 2.0 Host Port

On the Rev C4 board a single USB HS only Host port is provided via a USB Type A connector. It provides power on/off control and up to 500mA of current at 5V.

The HS USB Port is HS only. In order to support a FS/LS device, a HUB must be used.

5.7 Stereo Audio Output Connector

A 3.5mm standard stereo output audio jack is provided to access the stereo output of the onboard audio CODEC. The Audio CODEC is provided by the TPS65950.

5.8 Stereo Audio In Connector

A 3.5mm standard stereo audio input jack is provided to access the stereo output of the onboard audio CODEC.

5.9 S-Video Connector

A 4 pin DIN connector is provided to access the S-Video output of the BeagleBoard. This is a separate output from the OMAP processor and can contain different video output data from what is found on the DVI-D output if the software is configured to do it.

It will support NTSC or PAL format output to a standard TV. The default is NTSC, but can be changed via the Software.

5.10 DVI-D Connector

The BeagleBoard can drive a LCD panel equipped with a DVI-D digital input. This is the standard LCD panel interface of the OMAP3530 and will support 24b color output. DDC2B (Display Data Channel) or EDID (Enhanced Display ID) support over I2C is provided in order to allow for the identification of the LCD monitor type and the required settings.

The BeagleBoard is equipped with a DVI-D interface that uses an HDMI connector that was selected for its small size. It does not support the full HDMI interface and is used to provide the DVI-D interface portion only. The user must use a HDMI to DVI-D cable or adapter to connect to a LCD monitor. This cable or adapter is not provided with the BeagleBoard. A standard HDMI cable can be used when connecting to a monitor with an HDMI connector.

DO NOT PLUG IN THE DVI-D CONNECTOR TO A DISPLAY WITH THE BEAGLEBAORD POWERED ON. PLUG IN THE CABLE TO THE DISPLAY AND THEN POWER ON THE BEAGLEBOARD.

5.11 LCD Header

A pair of 1.27mm pitch 2x10 headers are provided to gain access to the LCD signals. This allows for the creation of LCD boards that will allow adapters to be made to provide the level translation to support different LCD panels.

5.12 SD/MMC 6 in 1 Connector

A 6 in 1 SD/MMC connector is provided as a means for expansion and can support such devices as:

- WiFi Cards
- Camera
- Bluetooth Cards
- GPS Modules
- SD Memory Cards
- MMC Memory Cards
- SDIO Cards
- MMCMobile cards
- RS-MMC Cards
- miniSD Cards

It supports the MMC4.0 (MMC+) standard and can boot from MMC or SD cards. It will support both 4 and 8 bit cards. It will also support most SDHC cards as well.

5.13 Reset Button

When pressed and released, causes a power on reset of the BeagleBoard.

5.14 User/Boot Button

A button is provided on the BeagleBoard to provide two functions:

- Force a change in the boot sequence of the OMAP3530.
- Used as an application button that can be used by SW as needed.

When used in conjunction with the RESET button, it will force a change to the order in which boot sources are checked as viable boot sources.

If the button is pressed while the RESET button is released, the sequence becomes:

- USB
- UART
- MMC1
- NAND

Even though the NAND may have a program in it, if a card is placed in the MMC slot, it will try to boot from it first. If it is not there, it will boot from NAND.

There is also the option to have a serial download application that will program the NAND if connected to the serial or USB ports. In this scenario the internal ROM will

stop on either the serial or USB port and start the download process from there. It does require an application to be run on the host PC in order to perform this function.

If the user button is not pressed at reset, the sequence in which the internal ROM looks for viable boot sources is as follows:

- NAND
- USB
- UART3
- MMC1

In this case, NAND overrides every option and will always boot from NAND if there is data in the NAND. If the NAND is empty, then the other sources are available to be used based on the boot order.

To force a boot from the SD/MMC card, the reset button must be pushed and the reset button pushed and reelased.

5.15 Indicators

There are three green LEDs on the BeagleBoard that can be controlled by the user.

- One on the TPS65950 that is programmed via the I2C interface
- Two on the OMAP3530 Processor controlled via GPIO pins

There is a fourth LED on the BeagleBoard that provides an indication that power is supplied to the board and is not controlled via software.

5.16 Power Connector

Power will be supplied via the USB OTG connector and if a need arises for additional power, such as when a board is added to the expansion connectors, a larger wall supply 5V can be plugged into the optional power jack. When the wall supply is plugged in, it will remove the power path from the USB connector and will be the power source for the whole board. The power supply is not provided with the BeagleBoard.

When using the USB OTG port in the host mode, the DC supply must be connected as the USB port will be used to provide limited power to the hub at a maximum of 100mA, so a hub must be powered. The 100mA is not impacted by having a higher amperage supply plugged into the DC power jack. The 100mA is a function of the OTG port itself.

WARNING: DO NOT PLUG IN ANYTHING BUT 5V TO THE DC CONNECTOR OR THE BOARD WILL BE DAMAGED!

Make sure the DC supply is regulated and a clean supply.

5.17 JTAG Connector

A 14 pin JTAG header is provided on the BeagleBoard to facilitate the SW development and debugging of the board by using various JTAG emulators. The interface is at 1.8V on all signals. Only 1.8V Levels are supported. **DO NOT expose the JTAG header to 3.3V.**

5.18 RS232 Header

Support for RS232 via UART3 is provided by a 10 pin header on the BeagleBoard for access to an onboard RS232 transceiver. It does require an IDC to DB9 flat cable, which is not provided, to access the serial port.

5.19 Expansion Header

An option for a single 28 pin header is provided on the board to allow for the connection of various expansion cards that could be developed by the users or other sources. Due to multiplexing, different signals can be provided on each pin. This header is not populated on the BeagleBoard so that based on the usage scenario it can be populated as needed.

5.20 BeagleBoard Mechanical Specifications

Size:	3.0” x 3.1”
Max height:	TBM
Layers:	6
PCB thickness:	.062”
RoHS Compliant:	Yes
Weight:	TBW

5.21 Electrical Specifications

Table 3 is the electrical specification of the external interfaces to the Rev C4 BeagleBoard.

Table 3. BeagleBoard Electrical Specification Rev C4

Specification	Min	Typ	Max	Unit
Power				
Input Voltage USB		5	5.2	V
Current USB		350		mA
Input Voltage DC	4.8	5	5.2	V
Current DC		350		mA
Expansion Voltage (5V)	4.8	5	5.2	V
Current (Depends on source current available)		1		A
Expansion Voltage (1.8V)	1.75	1.8	1.85	V
Current			30	mA
USB Host (Same as the DC supplied by the power plug or USB 5V)	4.8	5	5.2	V
Current (Depends on what the DC source can supply over what the board requires)		Varies		
USB OTG				
High Speed Mode			480	Mb/S
Full Speed Mode			12.5	Mb/S
Low Speed Mode			1.5	Mb/S
USB Host				
High Speed Mode			480	Mb/S
RS232				
Transmit				
High Level Output Voltage		5	5.4	V
Low Level output voltage		-5	-5.5	V
Output impedance		+/-35	+/-60	mA
Maximum data rate	250			Kbit/S
Receive				
High level Input Voltage	-2.7	-3.2		V
Lo Level Input Voltage			.4	
Input resistance	3	5	7	Kohms
JTAG				
Realview ICE Tool			30	MHz
XDS560			30	MHz
XDS510			30	MHz
Lauterbach(tm)			30	MHz
SD/MMC				
Voltage Mode 1.8V	1.71	1.8	1.89	V
Voltage Mode 3.0V	2.7	3.0		V
Current			220	mA
Clock			48	MHz
DVI-D				
Pixel Clock Frequency	25		65	MHz
High level output voltage		3.3		V
Swing output voltage	400		600	mVp-p
Maximum resolution			1024 x 768	

S-Video				
Full scale output voltage (75ohm load)	.7	.88	1	V
Offset voltage		50		mV
Output Impedance	67.5	75	82.5	Ohms
Audio In				
Peak-to-peak single-ended input voltage (0 dBFs)			1.5	Vpp
Total harmonic distortion (sine wave @ 1.02 kHz @ -1 dBFs)		-80	-75	dB
Total harmonic distortion (sine wave @ 1.02 kHz) 2 0 Hz to 20 kHz, A-weighted audio, Gain = 0 dB		-85	-78	dB
Audio Out				
Load Impedance @100 pF	14	16		ohms
Maximum Output Power (At 0.53 Vrms differential output voltage and load impedance = 16 Ohms)		17.56		mW
Peak-to-Peak output voltage			1.5	Vpp
Total Harmonic Distortion @ 0 dBFs		-80	-75	dB
Idle channel noise (20Hz to 20KHz)		-90	-85	dB

6.0 Product Contents

Under this section is a description of what comes in the box when the BeagleBoard is purchased.

6.1 BeagleBoard In the Box Rev C4

The final packaged Rev C4 product will contain the following:

- 1 Box
- 1 BeagleBoard in an ESD Bag

NO CABLES ARE PROVIDED WITH THE BEAGLEBOARD.

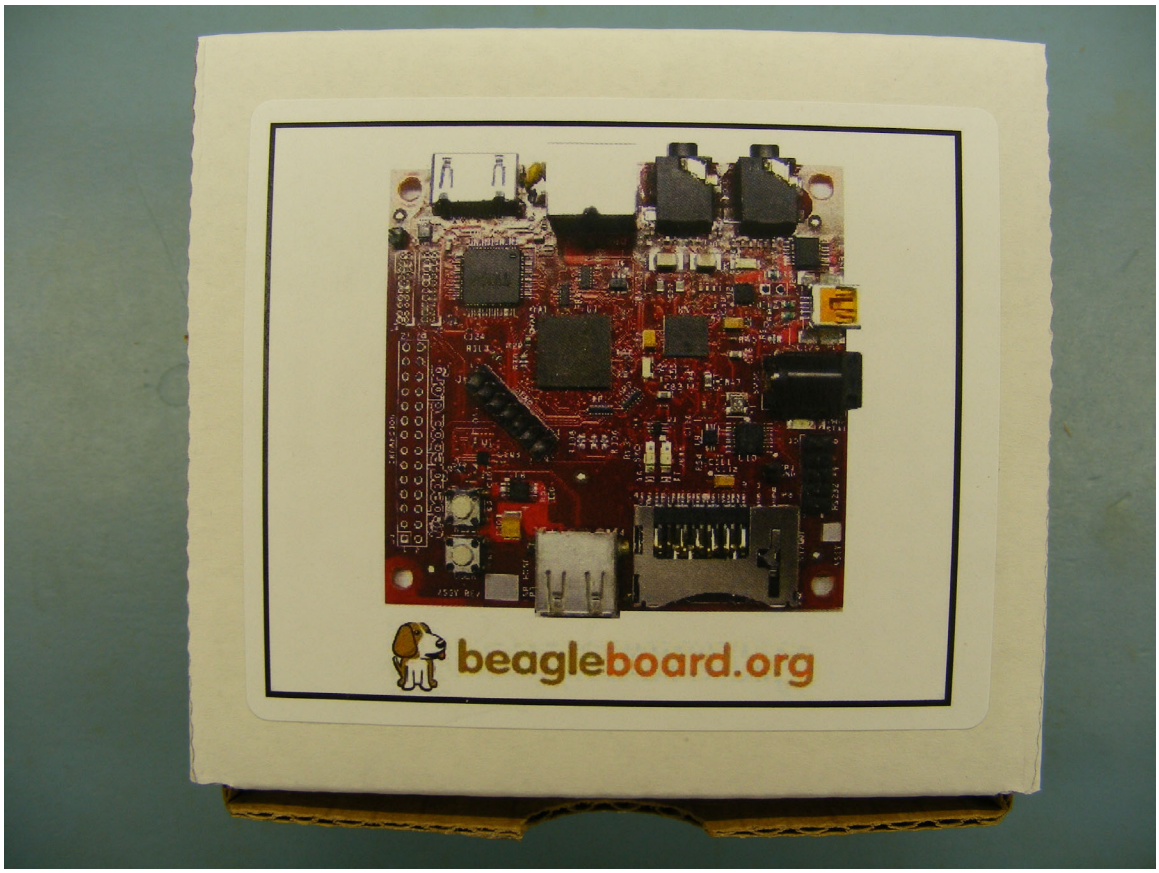

Figure 3. The Rev C4 Box

Figure 4. Rev C4 Box Contents

6.2 Software on the BeagleBoard

The board ships with U-Boot and X-Loader flashed onto the BeagleBoard.

6.3 Repair

If you feel the board is in need of repair, follow the RMA Request process found at http://beagleboard.org/support/rma

7.0 BeagleBoard Hookup

This section provides an overview of all of the connectors on the BeagleBoard and how they should be used.

7.1 Connecting USB OTG

The USB OTG port connects to the PC host and uses a miniAB cable through which power is provided to the BeagleBoard. If desired, the BeagleBoard may also be connected to a self powered USB hub. **Figure 5** shows where the cable is connected to the BeagleBoard.

If the OTG Port is to be used as a Host, the ID pin must be grounded. This means that you must have a 5 pin cable connected to the OTG port on the BeagleBoard and you must use a USB powered HUB. There is also an option to ground the ID on the board and is discussed later.

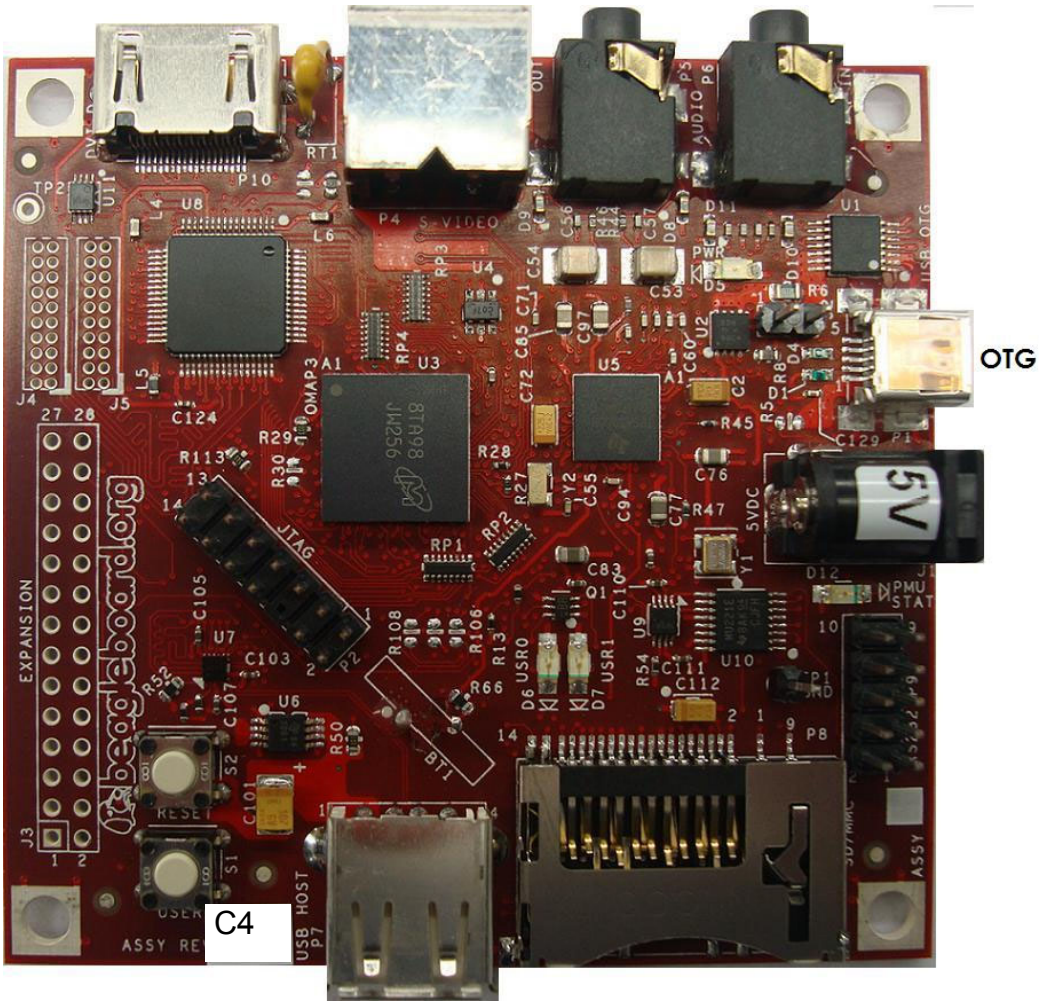

Figure 5. USB OTG Connection

7.2 Connecting USB Host

The Rev C4 Beagle is equipped with a USB Host only connector and can be used to support USB based devices. In order to connect multiple devices a Hub is required. The hub can be powered or un-powered if the total current on the devices connected to the hub do not exceed the available power from the DC power supply that is used. If the board is powered from the OTG connector, then the power available from this port is extremely limited and will not be able to provide sufficient power to run most USB devices. It may be possible to run a USB keyboard or mouse, but that is about all it will have the power to supply. The USB Host port is HS only and does not support LS or FS devices without a hub.

Figure 6 below shows the location of the USB Host connector.

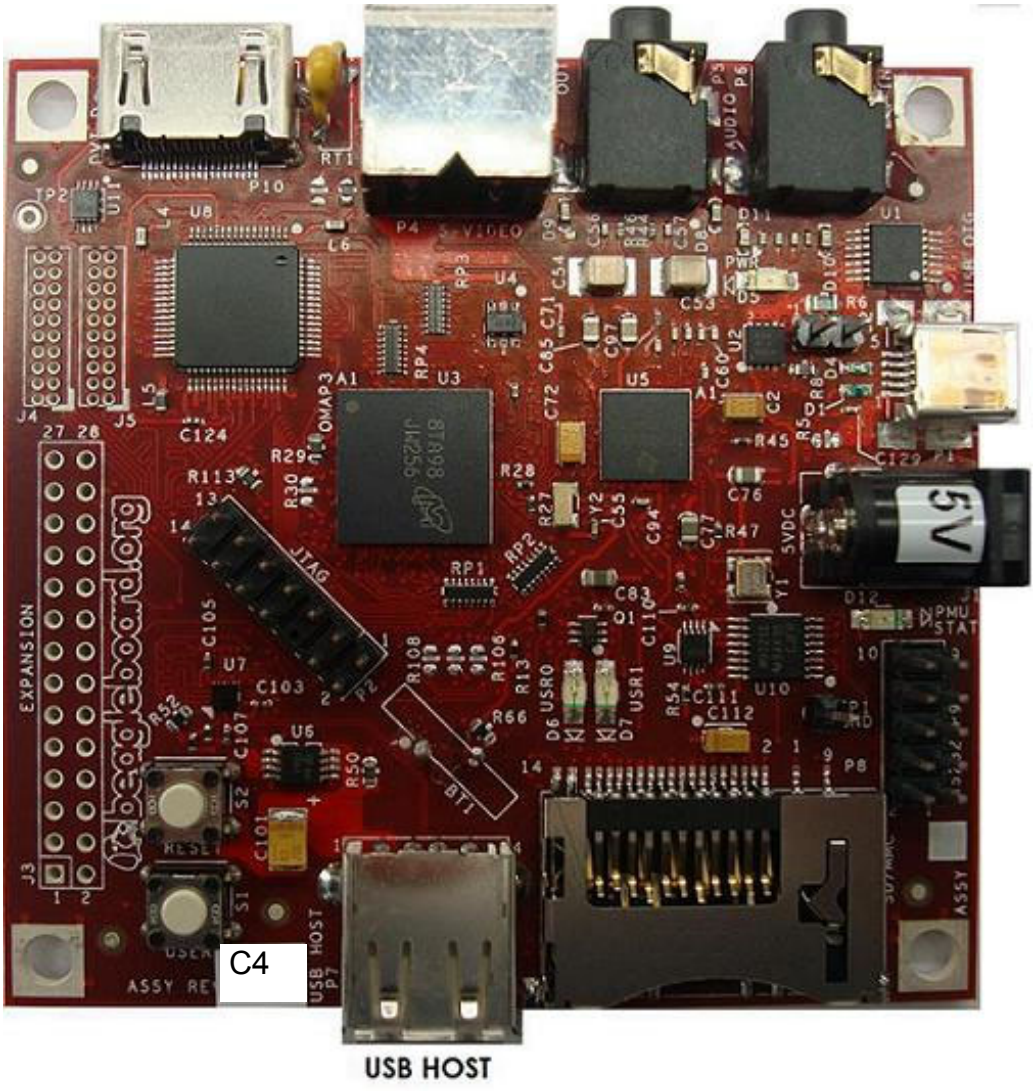

Figure 6. USB Host Connection

7.3 Connecting Optional Power

An optional DC supply can be used to power the BeagleBoard by plugging it into the power jack of the BeagleBoard. The power supply is not provided with the BeagleBoard, but can be obtained from various sources. You need to make sure the supply is a regulated 5V supply. **Figure 7** shows where to insert the power supply into the power jack.

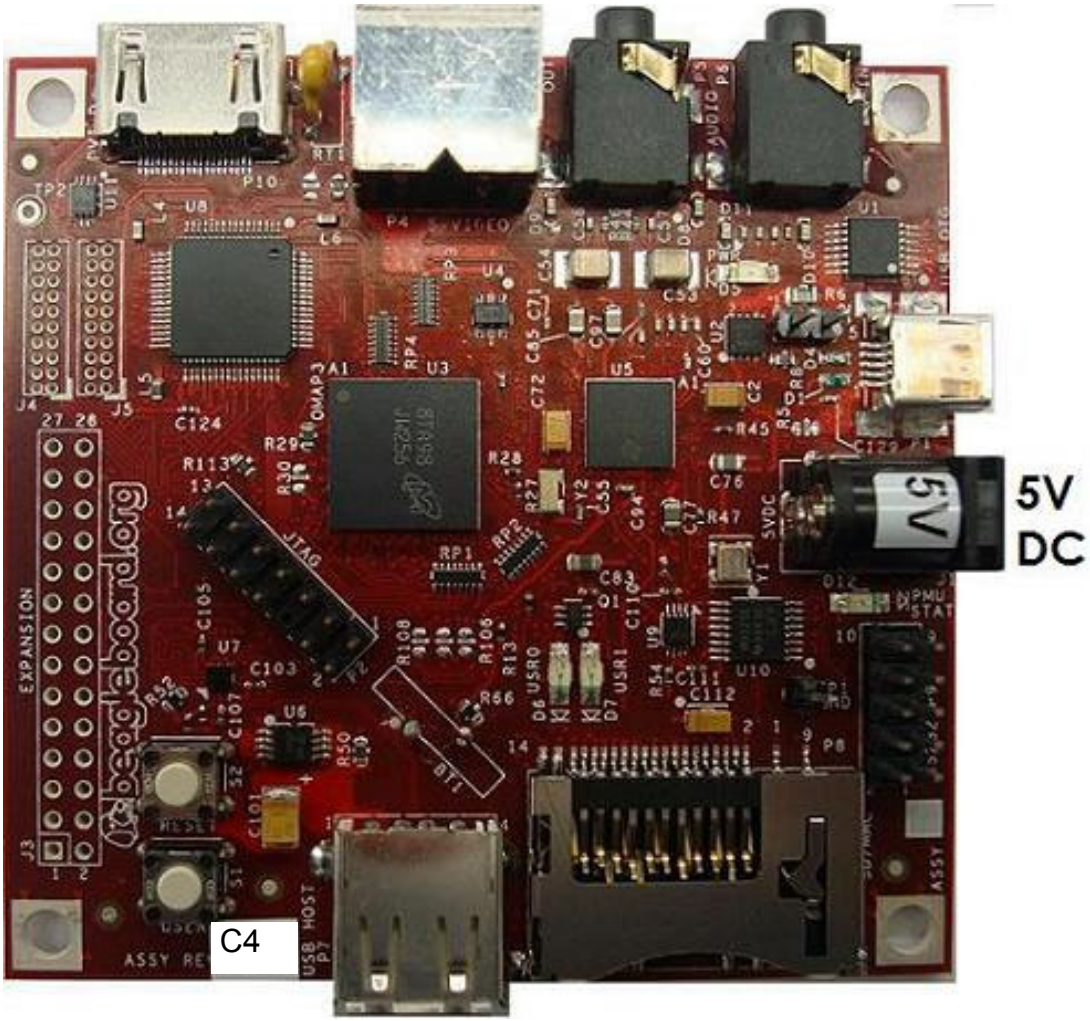

Figure 7. DC Power Connection

The power supply must have a 2.1mm I.D x 5.5mm O.D. x 9.5mm and can be either straight or right angle. Connecting anything other than 5V will result in damage to the board. If you are using the USB OTG port in the OTG or host mode, you must have an external DC supply powering the BeagleBoard.

It is highly recommended that on the Rev C4 version of the board that an external power supply or double USB cable be used if the USB Host is to be used. Most USB supplies will not be able to supply the required current over a single USB port.

7.4 Connecting JTAG

A JTAG emulator can be used for advanced debugging by connecting it to the JTAG header on the BeagleBoard. Only the 14pin version of the JTAG is supported and if a 20pin version is needed, you will to contact your emulator supplier for the appropriate adapter. **Figure 8** shows the connection of the **JTAG** cable to the BeagleBoard.

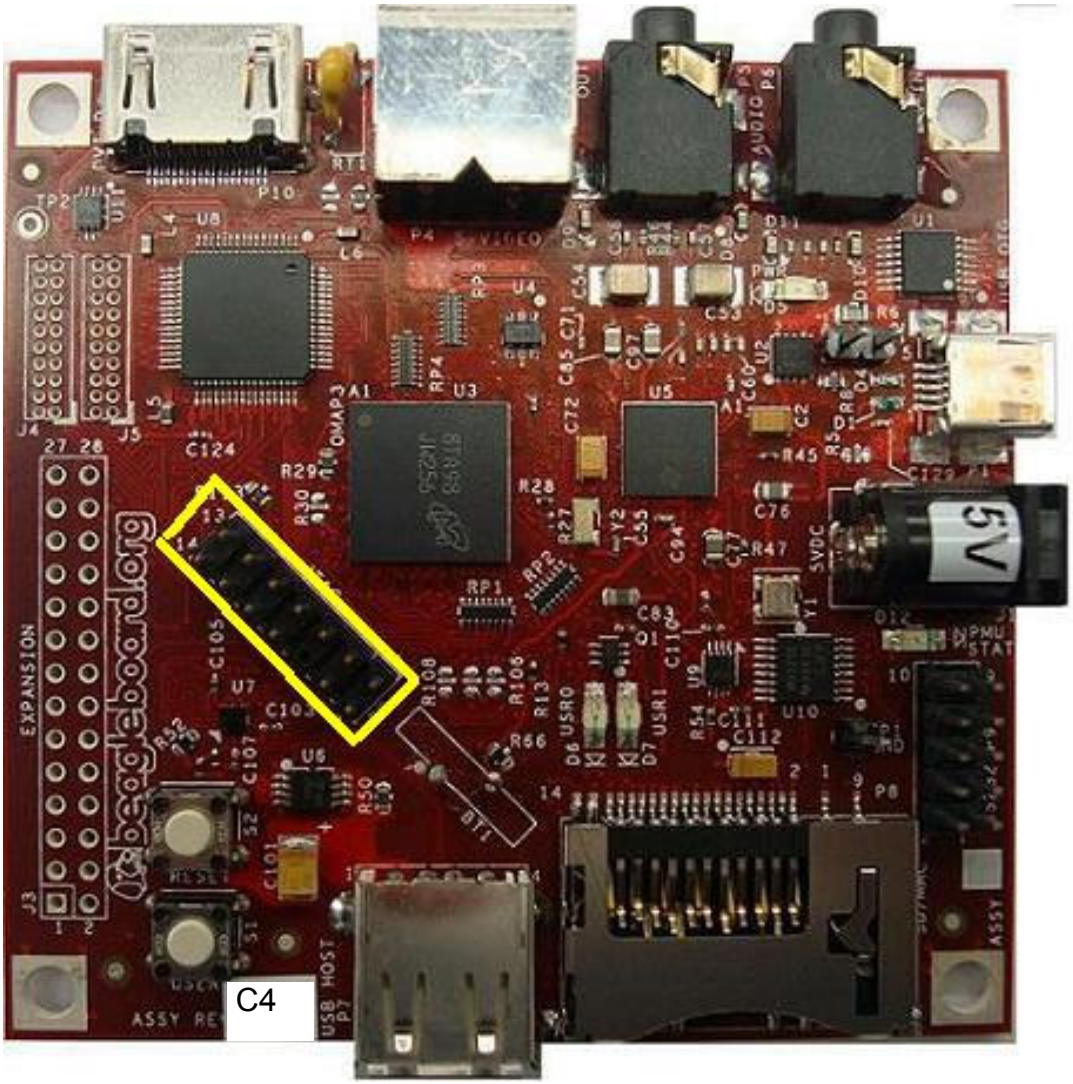

Figure 8. BeagleBoard JTAG Connection

DO NOT expose the JTAG header to 3.3V. It supports 1.8V only.

7.5 Connecting Serial Cable

In order to access the serial port of the BeagleBoard a flat cable is required to connect to a PC. The adapter will not plug directly into the PC and will require an external Female to Female twisted cable (Null Modem) in order to connect it to the PC. The ribbon cable is not supplied with the BeagleBoard but can be obtained from numerous sources. **Figure 9** shows where the ribbon cable is to be installed.

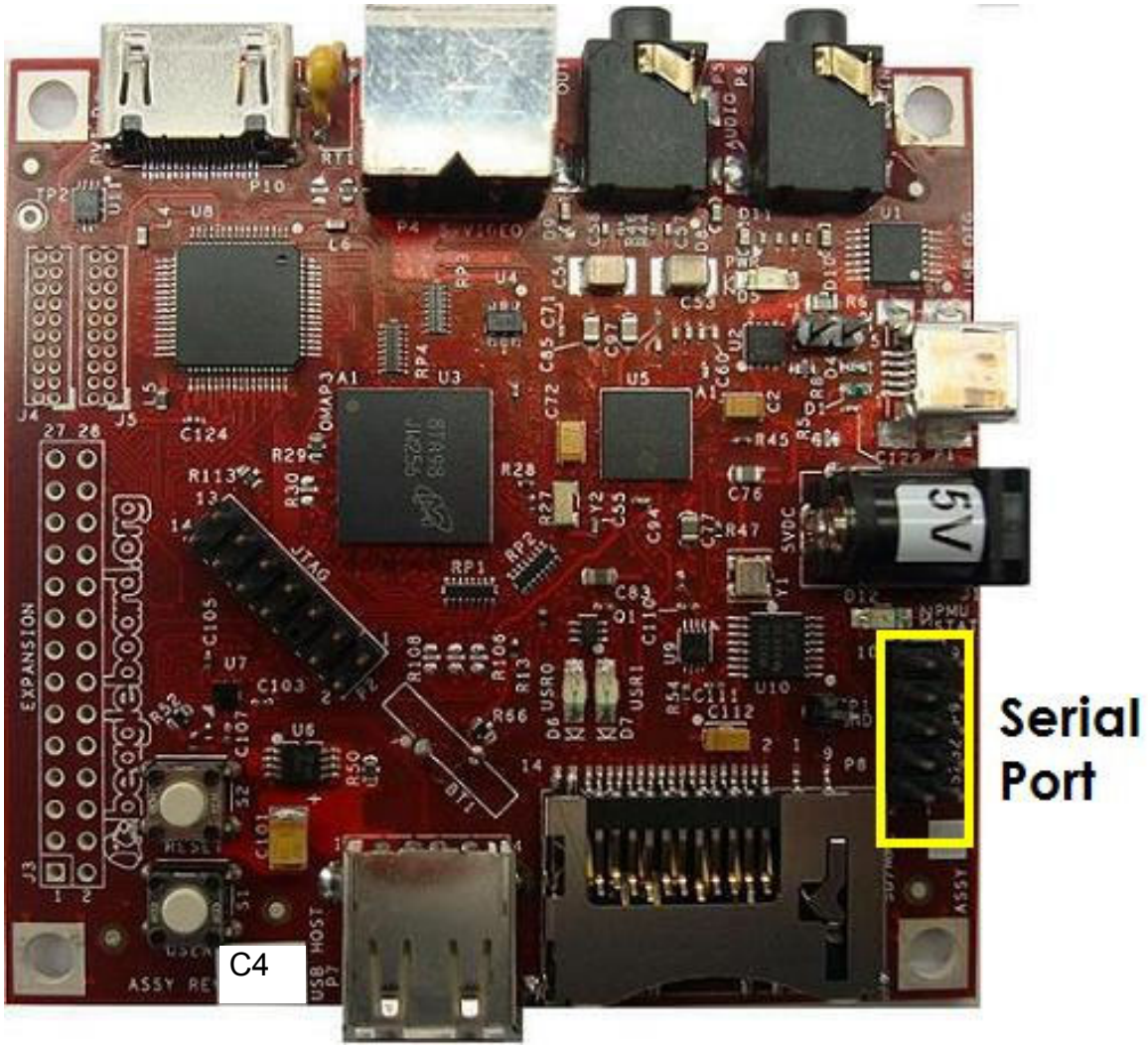

Figure 9. BeagleBoard Serial Cable Connection

7.6 Connecting S-Video

An S-Video cable can be connected to the BeagleBoard and from there is can be connected to a TV or monitor that supports an S-Video input. This cable is not supplied with the BeagleBoard. **Figure 10** shows the connector for the S-Video cable.

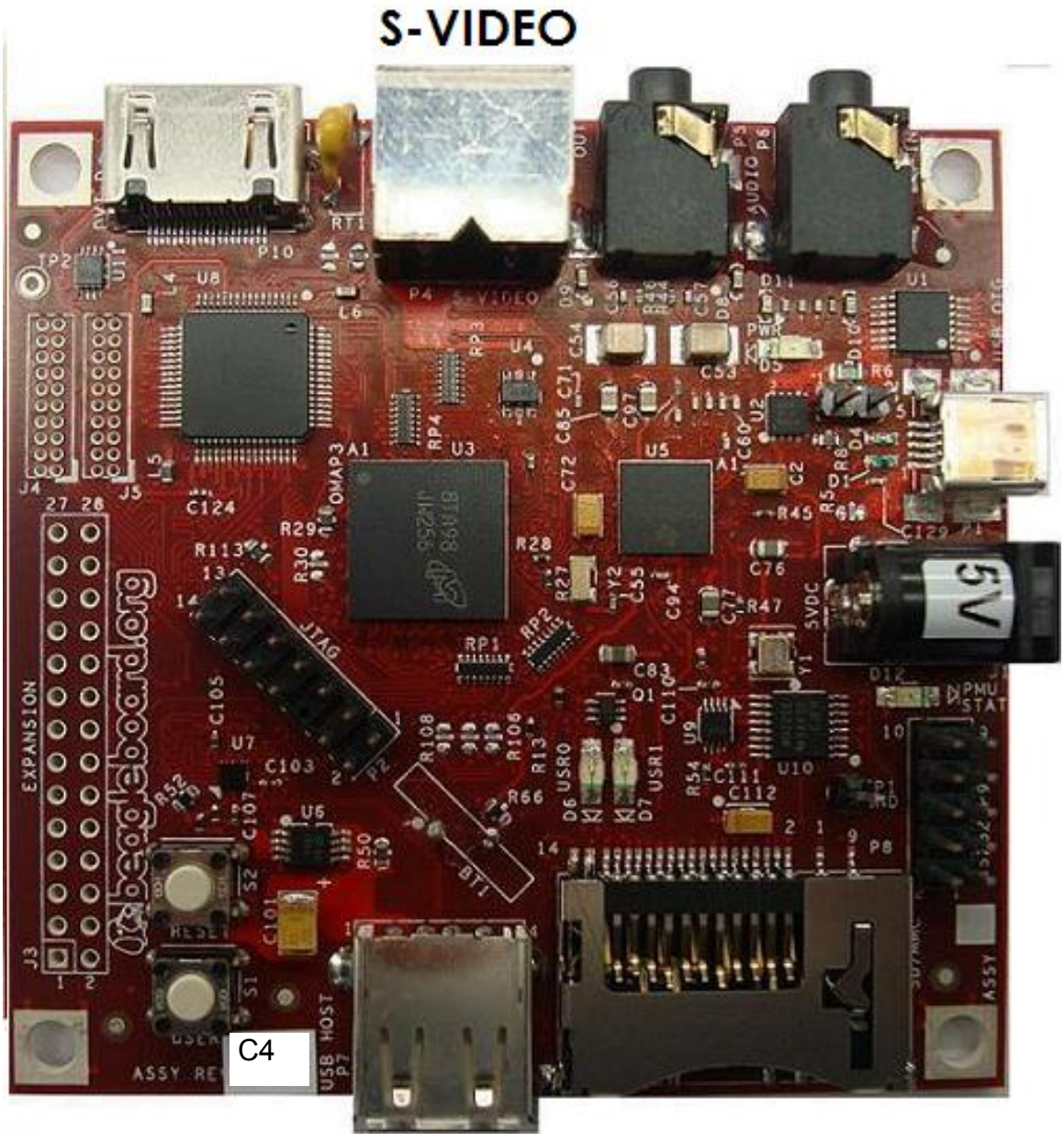

Figure 10. BeagleBoard S-Video Connection

7.7 Connecting DVI-D Cable

In order to connect the DVI-D output to a monitor, a HDMI to DVI-D cable is required. This cable is not supplied with BeagleBoard but can be obtained through numerous sources. **Figure 11** shows the proper connection point for the cable.

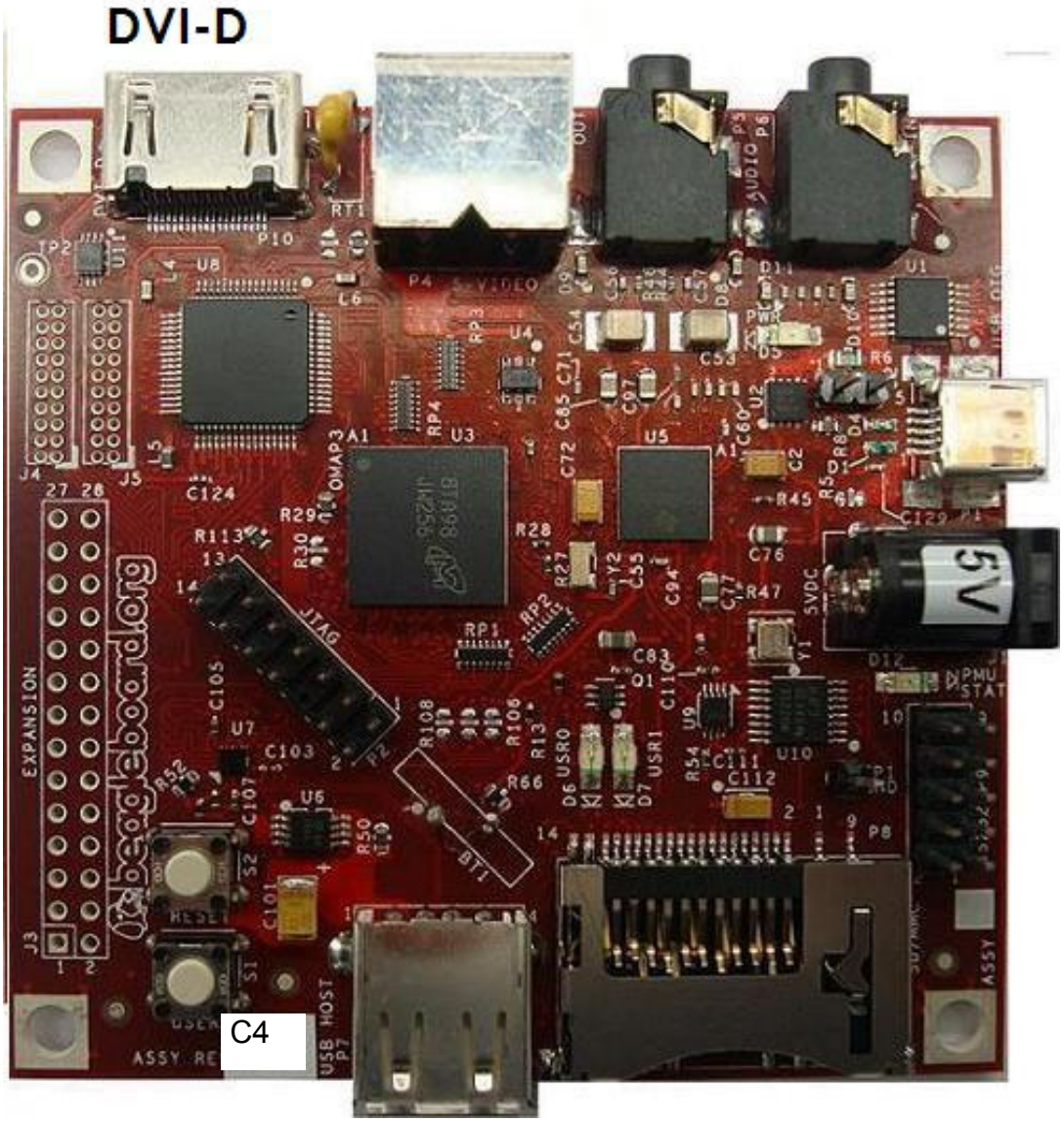

Figure 11. BeagleBoard DVI-D Connection

DO NOT PLUG IN THE DVI-D CONNECTOR TO A DISPLAY WITH THE BEAGLEBAORD POWERED ON. PLUG IN THE CABLE TO THE DISPLAY AND THEN POWER ON THE BEAGLEBOARD.

Only the digital portion of HDMI is supported on the BeagleBoard.

7.8 Connecting Stereo Out Cable

An external Audio output device, such as external stereo powered speakers, can be connected to the BeagleBoard via a 3.5mm jack. The audio cables are not provided with BeagleBoard, but can be obtained from just about anywhere. **Figure 12** shows how the cable connected to the stereo out jack.

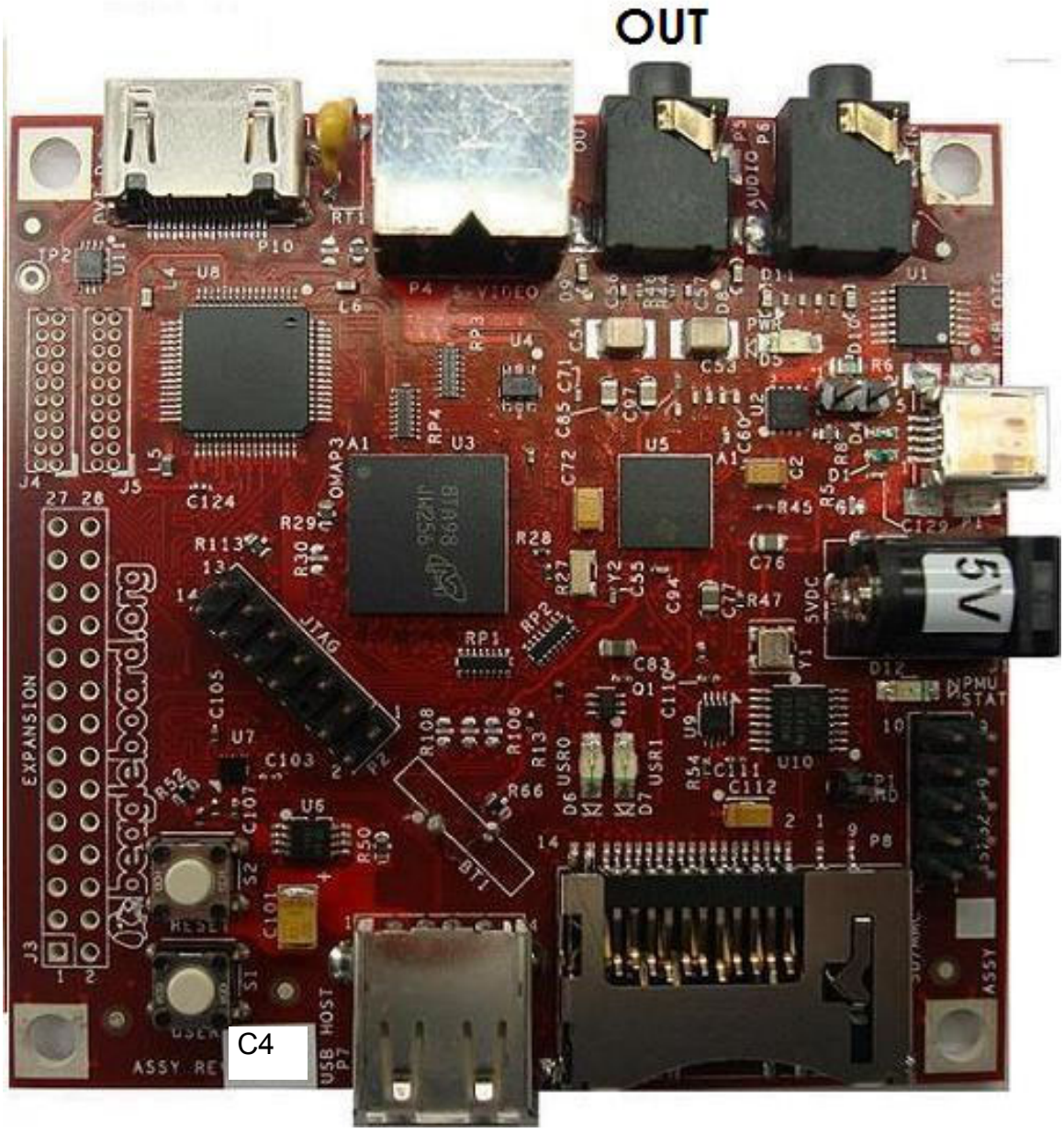

Figure 12. BeagleBoard Audio Out Cable Connection

7.9 Connecting Stereo In Cable

External Audio input devices, such as a powered microphone or the audio output of a PC or MP3 player, can be connected to the via a 3.5mm jack. The audio cables are not provided with BeagleBoard, but can be obtained from just about any source. **Figure 13** shows how the cable is connected to the stereo input jack.

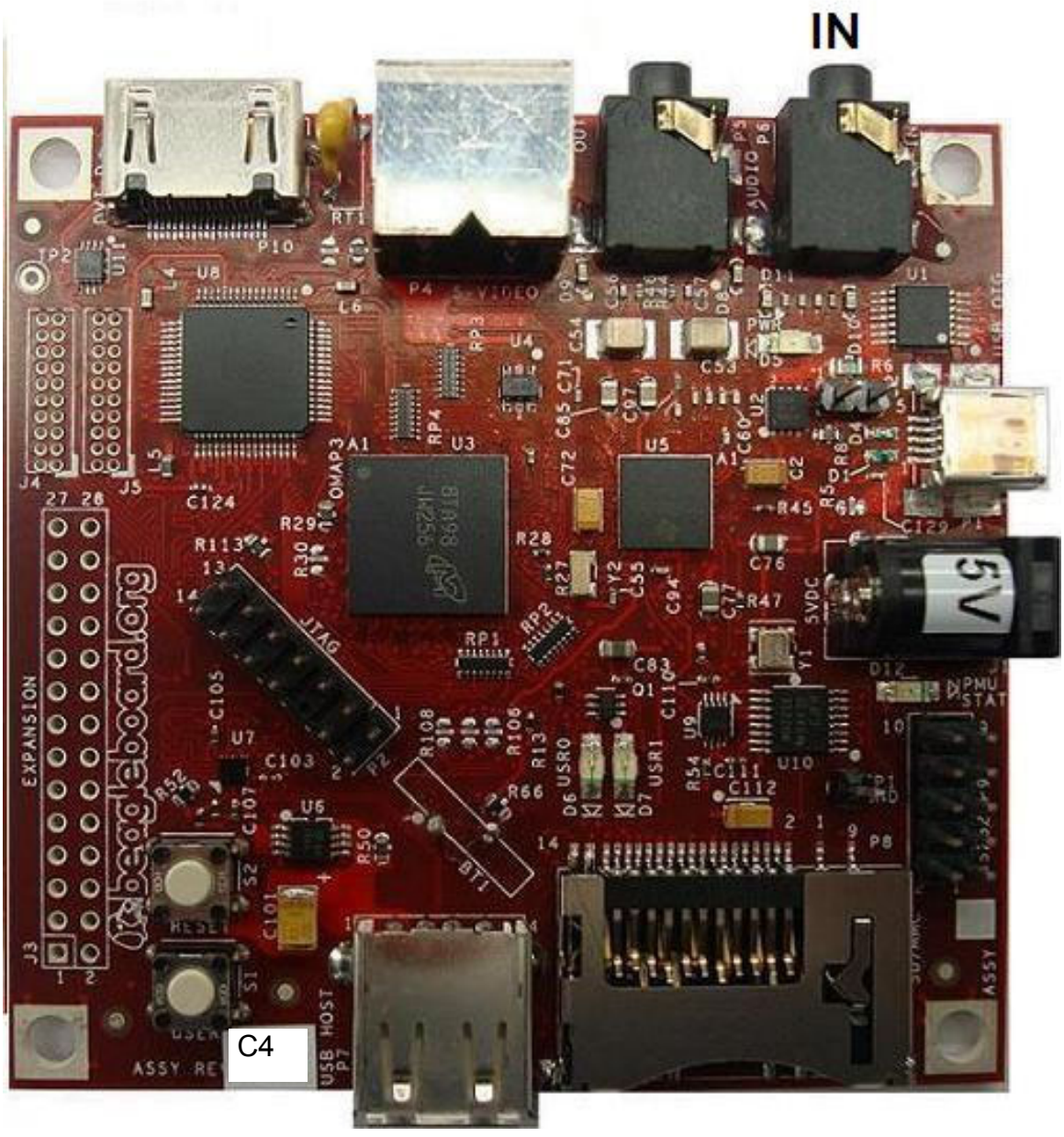

Figure 13. BeagleBoard Audio In Cable Connection

7.10 Indicator Locations

There are four green indicators on the BeagleBoard. One of them, POWER, indicates that the main supply is active. The other three can be controlled by the software. **Figure 14** shows the location of each indicator.

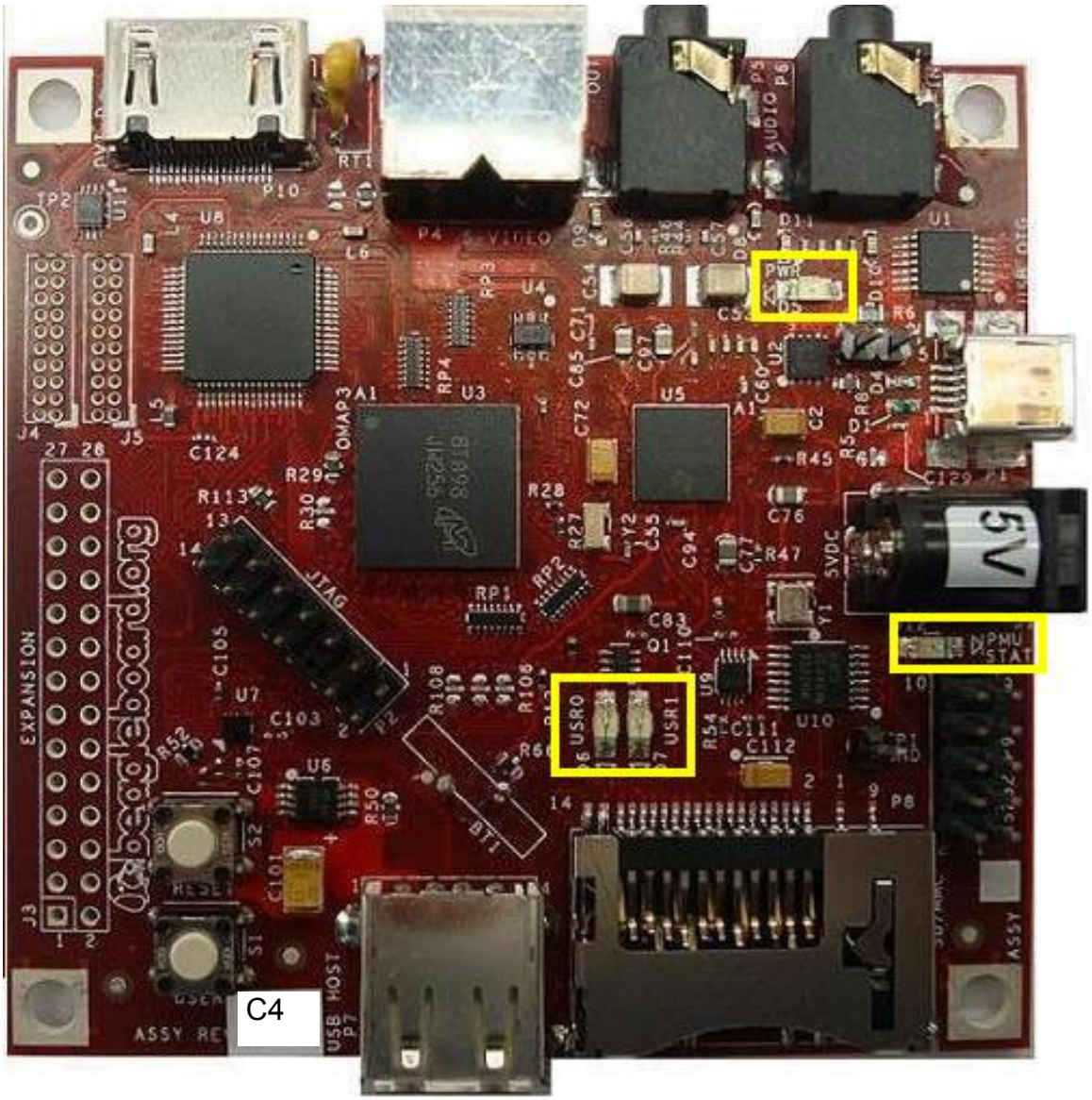

Figure 14. BeagleBoard Indicator Locations

7.11 Button Locations

There are two buttons on the BeagleBoard; the **RESET** button when pressed will force a board reset and the **USER** button which can be used by the SW for user interaction. If the user holds the **USER** button down while pressing and releasing the **RESET** button, the BeagleBoard will enter the ROM boot loader mode allowing it to boot from other sources than the onboard NAND. **Figure 15** shows the location of the buttons.

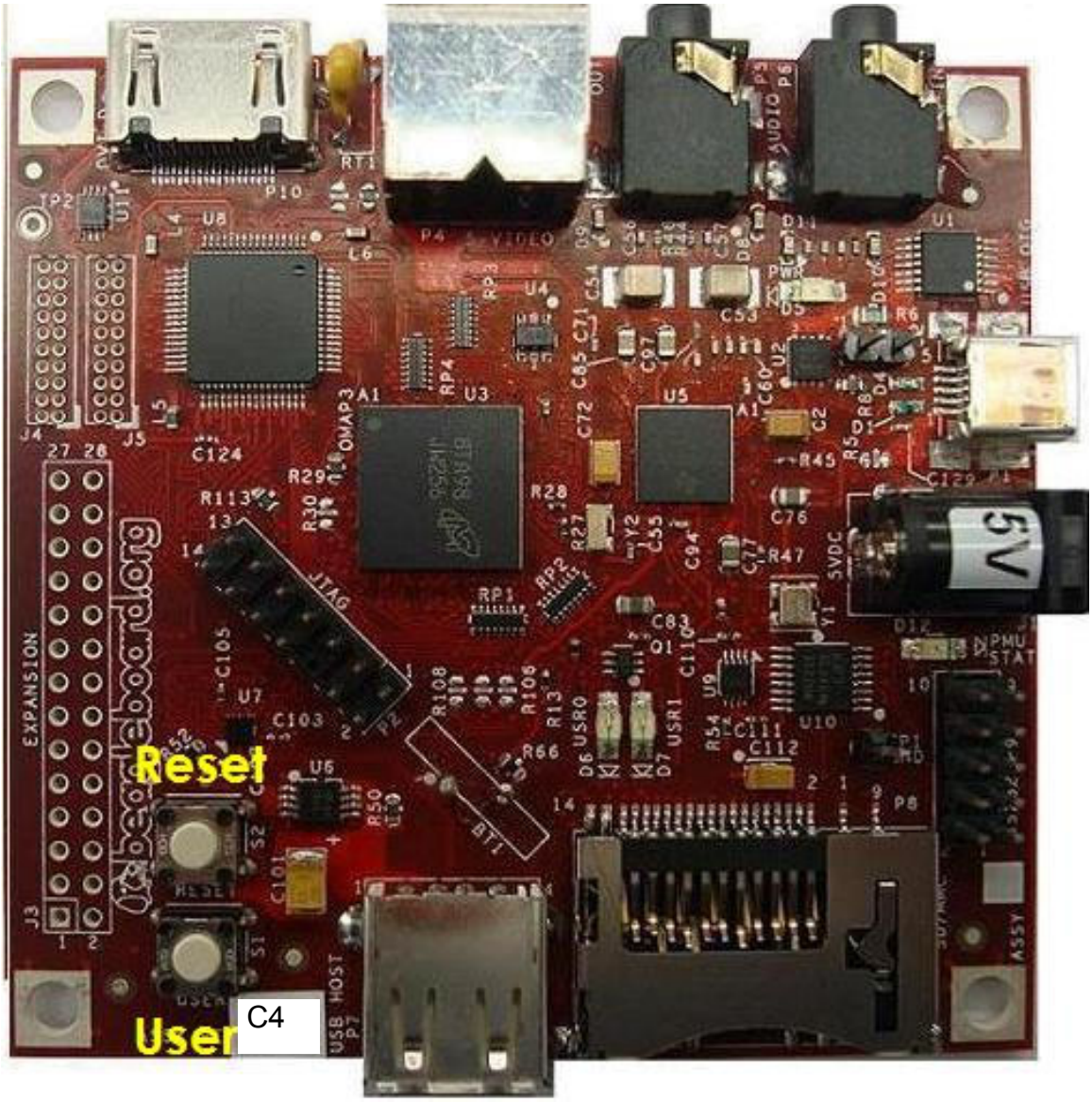

Figure 15. BeagleBoard Button Location

7.12 SD/MMC Connection

The SD/MMC connector can be used for Memory or SDIO type cards. This is a full size connector and will support various cards. Whether a particular card is supported or not, is dependent on the available software drivers. **Figure 16** shows the location of the SD/MMC connector.

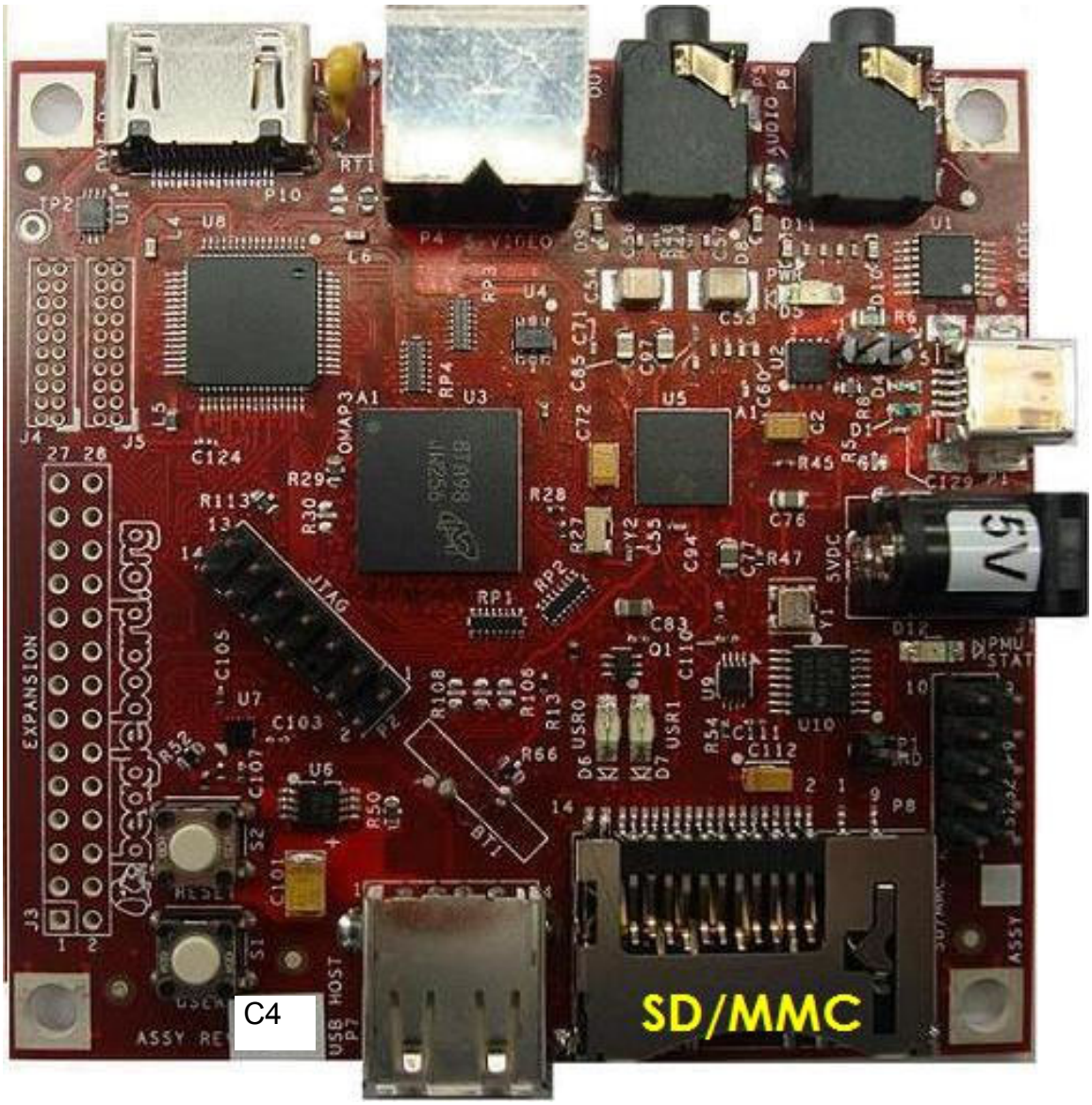

Figure 16. BeagleBoard SD/MMC Location

7.13 LCD Connection

There are two headers provided to allow access to the LCD signals on the BeagleBoard. These headers are 2x10 headers with a spacing of .05 (1.27mm) pitch. How these connectors are used is determined by the design of the adapter board. **Figure 17** shows the location of the LCD headers on the Beagle.

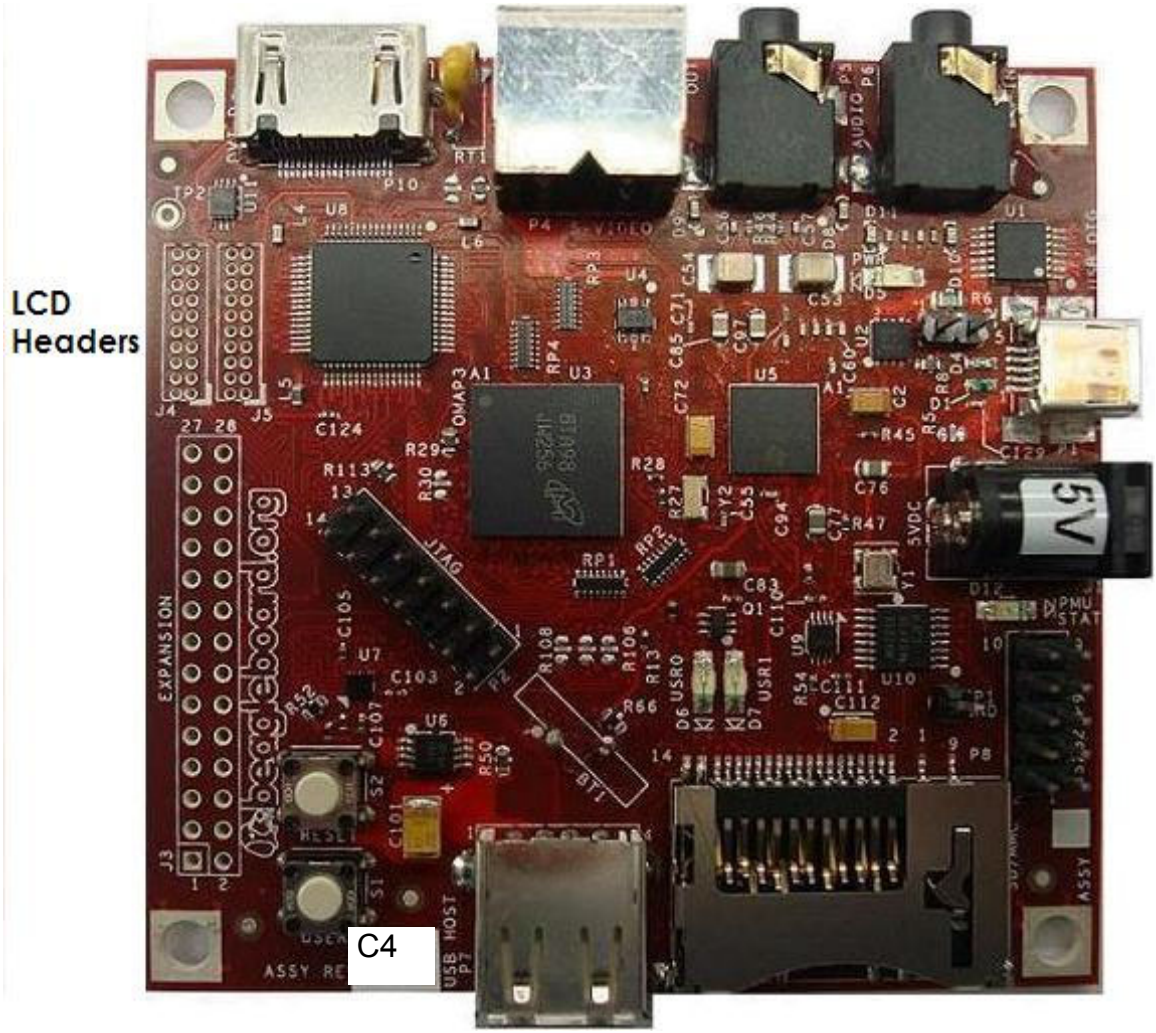

Figure 17. BeagleBoard LCD Header Location

8.0 BeagleBoard System Architecture and Design

This section provides a high level description of the design of the BeagleBoard and its overall architecture.

8.1 System Block Diagram

Figure 18 is the high level block diagram of the BeagleBoard. If you will notice, the block diagram is configured to match the component placement of the BeagleBoard.

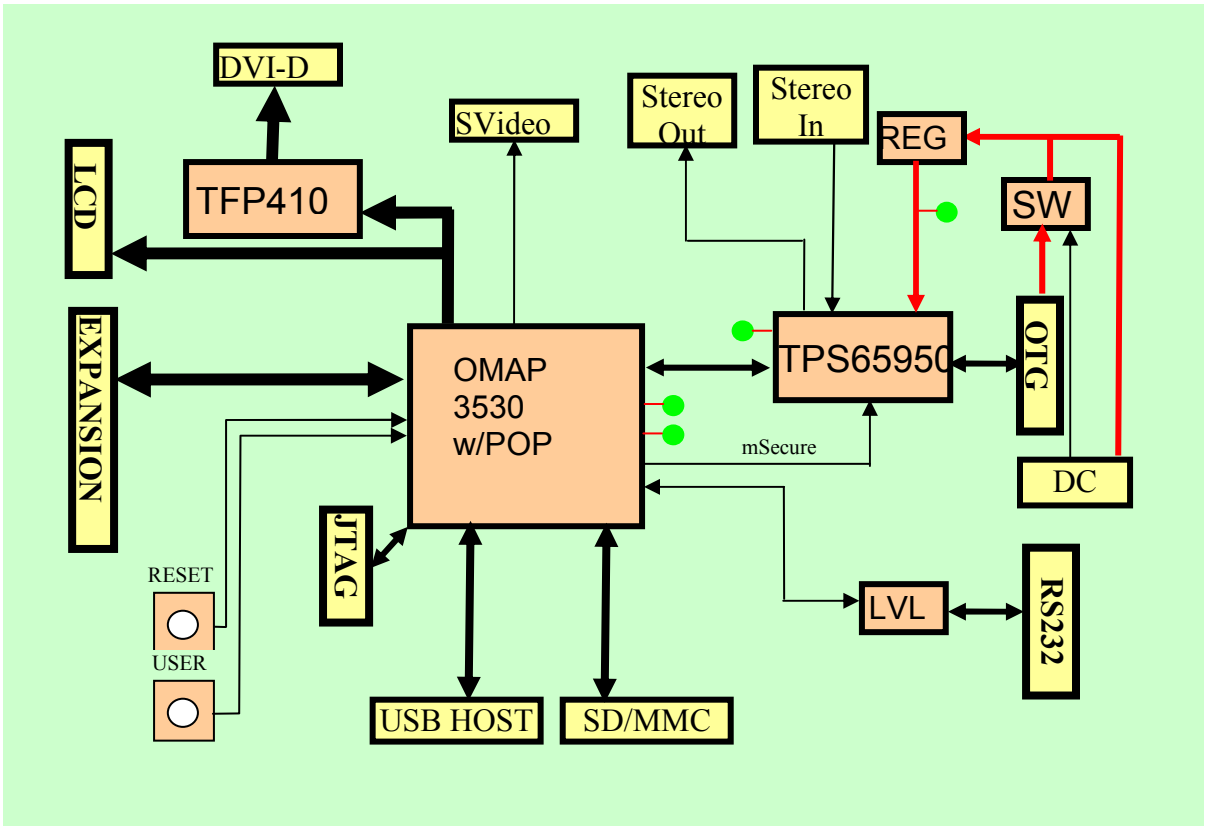

Figure 18. BeagleBoard High Level Block Diagram

Figure 19 shows the location of the components as shown in the block diagram.

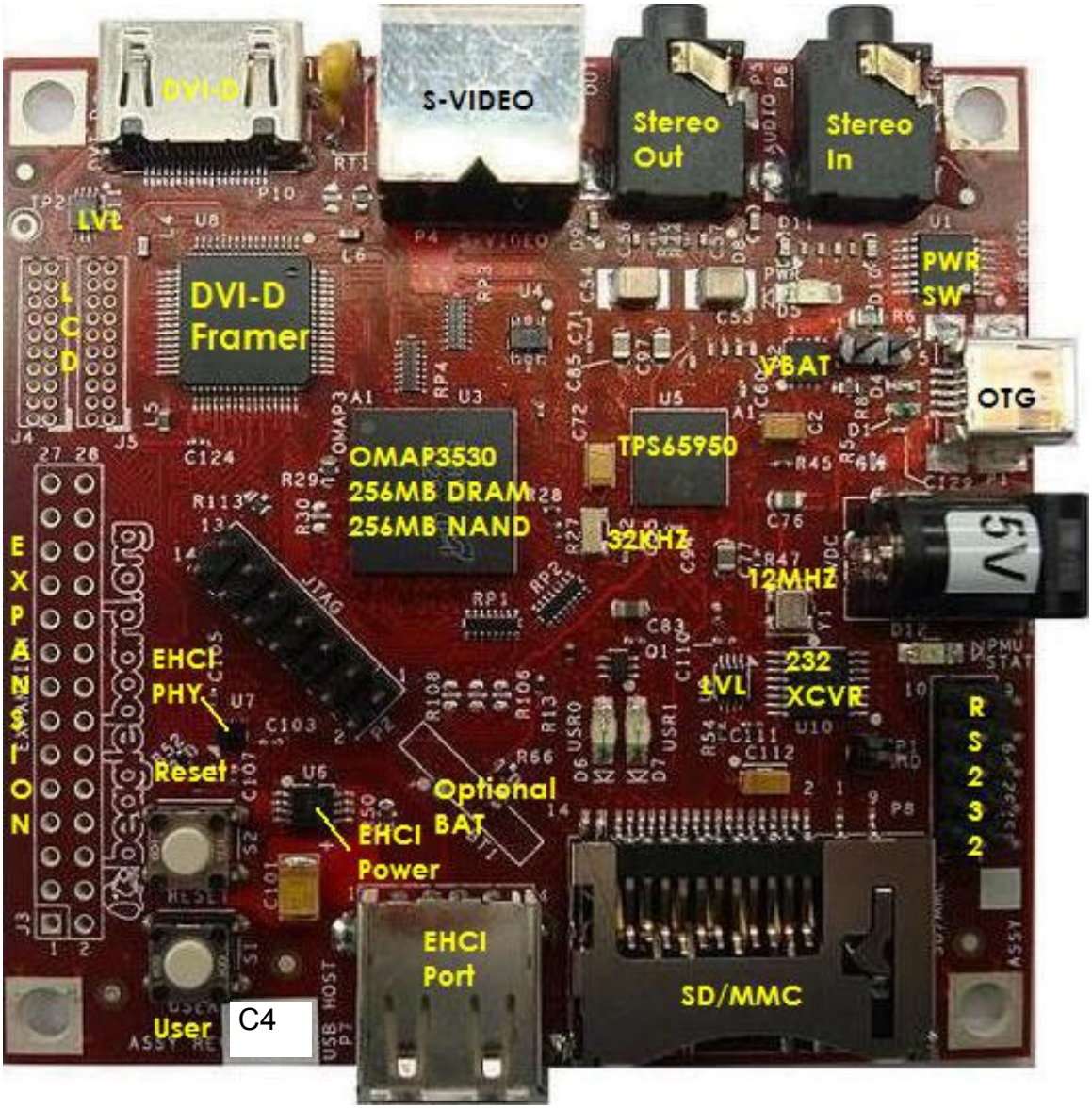

Figure 19. BeagleBoard Top Side Components

There are no key components on the back of the BeagleBoard, but **Figure 20** has been provided for completeness.

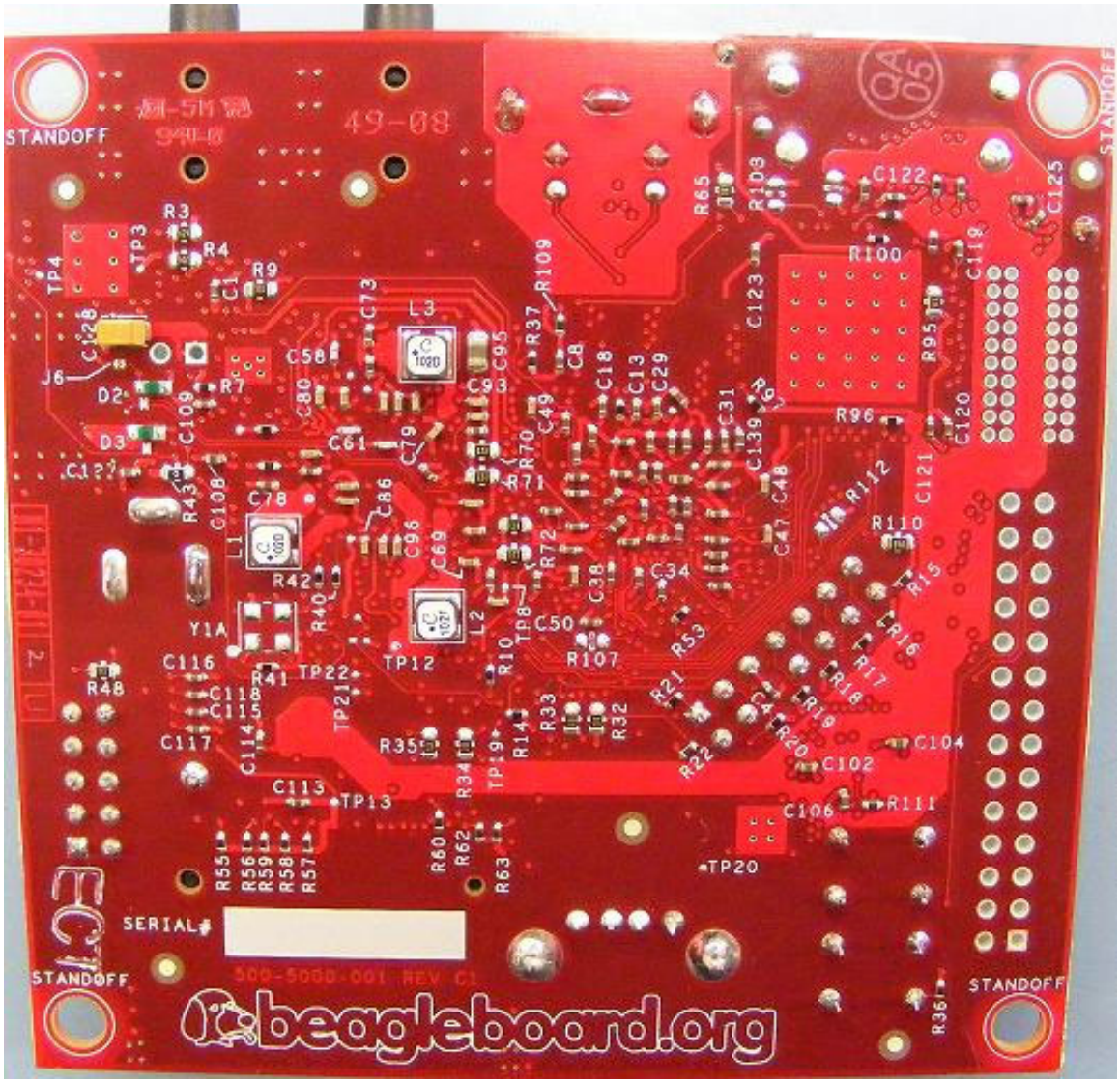

Figure 20. BeagleBoard Backside Components

This remainder of this section describes in detail the architecture and design of the BeagleBoard.

You will notice certain things in this section.

- The schematic has been created for each section showing only the pertinent components and their connections.
- The pin names differ from the actual schematic. For ease of reading, the names have been truncated to only show the specific functions of that pin as used in the design.

8.2 Input Power

There are two possible sources of the 5V required by the BeagleBoard. It can come from the USB OTG port connected to a PC, powered USB HUB, or a 5V DC supply. The USB supply is sufficient to power the BeagleBoard. However, depending on the load needed by the expansion port on BeagleBoard, additional power may be required. This is where the DC supply comes in to play.

WARNING: DO NOT PLUG IN ANYTHING BUT 5V TO THE DC CONNECTOR OR THE BOARD WILL BE DAMAGED!

It should also be noted that if an OTG configuration is used, for example tying two BeagleBoards together via a UBS OTG cable, both of the BeagleBoards must be powered by the DC supply. If the OTG port is used as a Host port, then the DC supply must also be used.

Figure 21 is the design of the power input section.

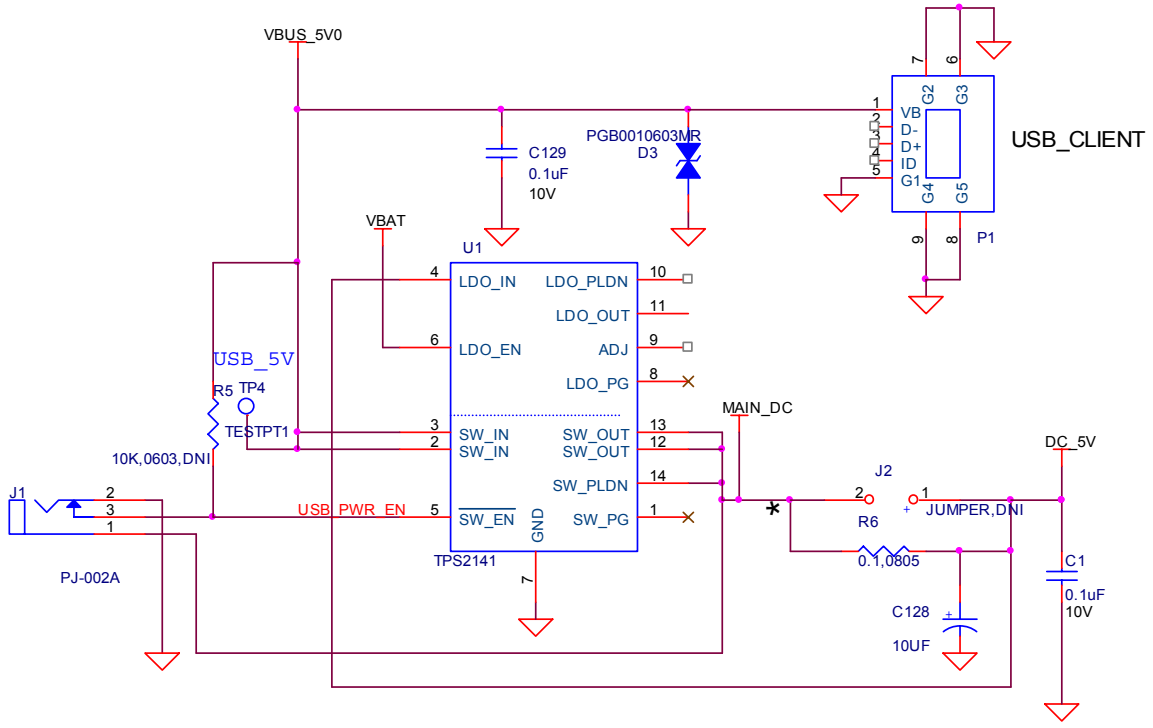

Figure 21. Input Power Section

8.2.1 USB DC Source

The USB specification requires that the current consumed prior to enumeration be limited to 100mA @ 5V (500mW). The 5V DC from the USB is routed through the **TPS2141** switch to insure that this requirement is met as uncharged capacitors on the BeagleBoard can exhibit a large current drain during start up that could exceed this requirement. The **TPS2141** is a USB 2.0 Specification-compatible IC containing a dual-current limiting power switch and an adjustable low dropout regulator (LDO). Both the switch and LDO limit inrush current by controlling the turn on slew rate. The dual-current-limiting feature of the switch allows USB peripherals to utilize high-value capacitance at the output of the switch, while keeping the inrush current low.

During turn on, the switch limits the current delivered to the capacitive load to less than 100 mA. When the output voltage from the switch reaches about 93% of the input voltage, the switch current limit increases to 800mA (minimum), at which point higher current loads can be turned on. The higher current limit provides short circuit protection while allowing the peripheral to draw maximum current from the USB bus.

When in the USB powered mode and no DC supply is connected, the **TPS2141** is enabled, allowing the power to be supplied to the board from the OTG port through the integrated switch inside the **TPS2141**.

8.2.2 Wall Supply Source

A wall supply can be used to provide power to the board. A regulated 5V DC supply of at least 500mA is required. It needs to have a 2.1mm plug with a center hot configuration.

WARNING: DO NOT PLUG IN ANYTHING BUT 5V TO THE DC CONNECTOR OR THE BOARD WILL BE DAMAGED!

In the event that a higher DC load is required due to the addition of a Daughtercard a higher current supply can be used. The maximum current should not exceed 2A.

8.2.3 DC Source Control

Unlike when powering from the USB OTG port, in the case of the DC voltage, the current limiting is not required. As long as the DC supply is not connected, the switch for the USB is enabled. When the DC supply is plugged in, the switch is disabled because the ground is removed from **pin 5** of the **TPS2141**. This insures that the 5V from the USB is not connected by disabling the internal FET. In the case where there is no USB plugged in, there is no 5V available to be routed so the removal of the pullup in **pin 5** has no affect.

When in the DC mode of operation, the USB OTG can be used in the Host or Client modes. The **TPS65950** will be responsible for handling the supply of the **VBUS_5V0** rail in the OTG or Host modes. As this is limited to 100mA, a powered hub must be used to support peripherals on the OTG port.

8.2.4 3.3V Supply

The **TPS2141** has an integrated 3.3V LDO which is being used to supply the **3.3V** as required on the BeagleBoard for the **DVI-D** interface and the **UART**. The input to the LDO is supplied by the main **DC_5V**. This insures that the power to the LDO can be supplied by either the USB or the DC wall supply and that the current measurement includes the 3.3V supply.

8.2.5 Meter Current Measurement

Jumper **J2** is a header that allows for the voltage drop across the resistor to be measured using a meter, providing a way to measure the current consumption of the BeagleBoard from the main voltage rails, either USB or DC. The resistor, **R6**, is a .1 ohm resistor across which the voltage is measured. The reading you get is .1mV per mA of current.

8.2.6 Processor Current Measurement

The resistor across **J2** can also be used to measure the current of the board by reading the voltage drop across **R6** from software. There are two pairs of resistors provided on the TPS65950 that measure the voltage on either side of R6. This is done via the I2C control bus to the TPS65950 from the OMAP3530 processor. These values along with resistance of R6, are used to calculate the current consumption of the board. **Figure 22** is the schematic of the measurement circuitry.

The maximum value that can be input to the ADC inputs is based on the setting of the **VINTANA2.OUT** voltage rail which defaults to 2.5V. In order to prevent the voltage levels from exceeding this value a pair of resistors of 1.2K and 1.0K is used to scale the voltage down.

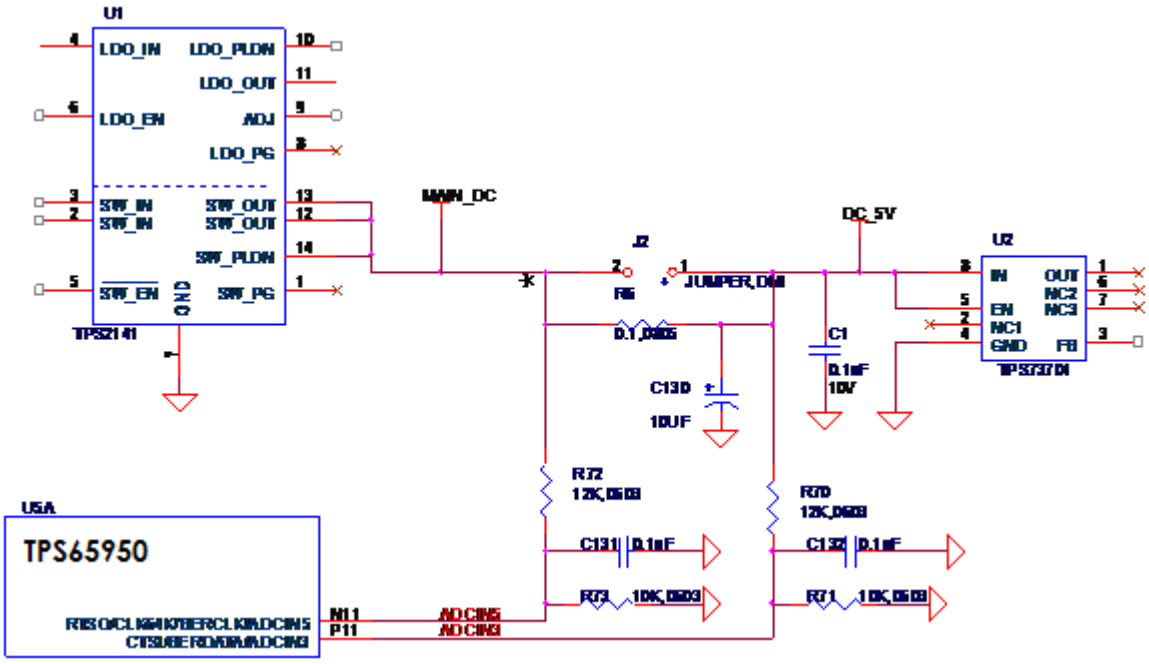

Figure 22. Processor Current Measurement

This results in a value that is 46% of the actual value. So, for a maximum value of 5.25V, the voltage read would be 2.415V which keeps it below the 2.5V pint.

The voltage drop across **R6** will be small as the value of the resistor is 0.1 ohms. For every 100 mA of current a voltage of the .01V will be detected. In order to determine the actual power, the input voltage and the voltage drop must be measured.

8.3 Power Conditioning

This circuitry regulates the DC input to a nominal 4.2VDC level. This is required in order to meet the maximum DC voltage level as specified by the **TPS65950** Power Management device which is 4.7V. Using 4.2V gives us some margin and meets the nominal 4.2V rating of the **TPS65950**.

Figure 23 is the power conditioning section of the BeagleBoard.

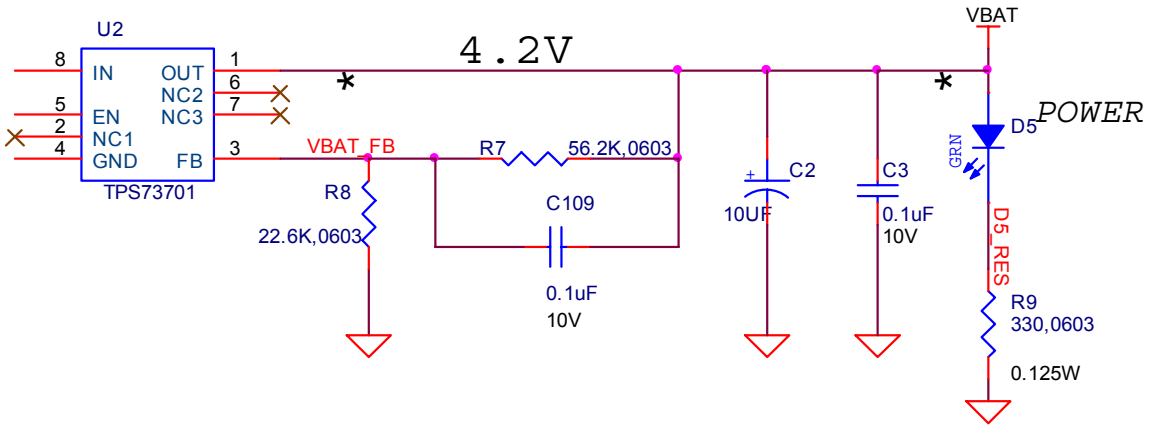

Figure 23. Power Conditioning

The **TPS65950** provides the main power rails to the board and has a maximum limit of 4.7V on its VBAT input and a nominal of 4.2V. **U2**, the **TPS73701**, is used to convert the DC_5V, which can come from a DC wall supply or the USB, to 4.2V to meet this requirement. The **TPS737701** is a linear low-dropout (LDO) voltage regulator and is thermal shutdown and current limit protected. It has the ability to deliver 1A of current, although this is far and above the requirements of the board. By adjusting the values of **R7** and **R8**, the actual voltage can be adjusted if needed. The LED **D5** is an indication that the 4.2V is present.

8.4 TPS65950 Reset and Power Management

The **TPS65950** supplies several key functions on the BeagleBoard. This section covers a portion of those functions centered on the power and reset functions. Included in this section is:

- Main Core Voltages
- Peripheral Voltages
- Power Sequencing
- Reset
- Current measurement via SW

The other functions are covered in other sections in this document and are grouped by their overall board functions. The explanation of the various regulators found on the **TPS65950** is based upon how they are used in the board design and are not intended to reflect the overall capability of the **TPS65950** device. Please refer to the **TPS65950** documents for a full explanation of the device operation.

8.4.1 Main Core Voltages

The **TPS65950** supplies the three main voltage rails for the **OMAP3530** processor and the board:

- VOCORE_1V3 (1.2V, adjustable)
- VDD2 (1.3V)
- VIO_1V8 (1.8V)

The **VOCORE_1V3** defaults to **1.2V** at power up, but can be adjusted by software to the **1.3V** level. **Figure 24** is the interfacing of the **TPS65950** to the system as it provides the three main rails.

8.4.2 Main DC Input

The main supply to the **TPS65950** for the main rails is the **VBAT** rail which is a nominal 4.2V. Each rail has a filter cap of **10uF** connected to each of the three inputs. A **.1uF** cap is also provided for high frequency noise filtering.

8.4.3 OMAP3530 I2C Control

The various components in the **TPS65950** are controlled from the OMAP3530 via the I2C interface. I2C_0 is used to control the **TPS65950** device.

8.4.4 VIO_1V8

The **VIO_1V8** rail is generated by the **TPS65950 VIO** regulator. The **VIO** output is a stepdown converter with a choice of two output voltage settings: 1.8 V or 1.85 V. The voltage is set by configuring the VSEL bit (VIO_VSEL[0]). When the VSEL bit is set to 0, the output voltage is 1.8 V, and when it is set to 1, the output voltage is 1.85 V.

When the **TPS65950** resets, the default value of this LDO is 1.80 V; the OMAP3530 must write 1 to the VSEL field to change the output to 1.85 V. The default for the BeagleBoard is 1.8V. This regulator output is used to supply power to the system memories and I/O ports. It is one of the first power supplies to be switched on in the power-up sequence. VIO does not support the SmartReflex voltage control schemes. VIO can be put into sleep or off mode by configuring the SLEEP_STATE and OFF_STATE fields of the VIO_REMAP register.

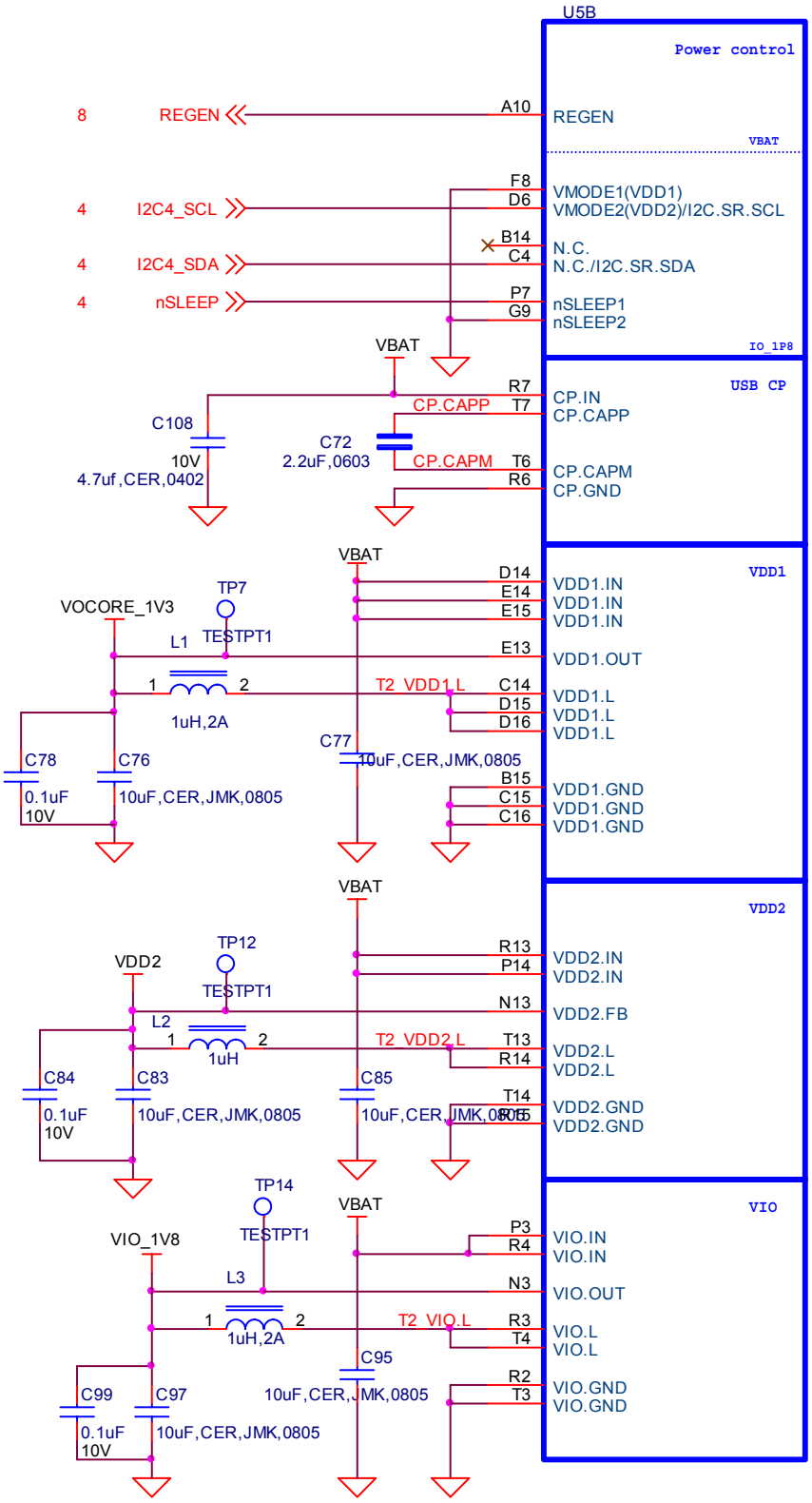

Figure 24. Main Power Rails

8.4.5 Main Core Voltages Smart Reflex

VDD1 and **VDD2** regulators on the **TPS65950** provide SmartReflex-compliant voltage management. The SmartReflex controller in the **OMAP3530** interfaces with the **TPS65950** counterpart through the use of a dedicated **I2C** bus. The **OMAP3530** computes the required voltage and informs the **TPS65950** using the SmartReflex I2C interface.

SmartReflex control of the **VDD1** and **VDD**2 regulators can be enabled by setting the SMARTREFLEX_ENABLE bit (DCDC_GLOBAL_CFG[3]) to 1. To perform **VDD1** voltage control through the SmartReflex interface, the TPS65950 provides the VDD1_SR_CONTROL register. The MODE field of the VDD1_SR_CONTROL register can be set to 0 to put VDD1 in an ACTIVE state; setting the field to 1 moves **VDD1** to a SLEEP state. **VDD1** output voltage can be programmed by setting the VSEL field of the VDD1_SR_ CONTROL register. The **VDD1** output voltage is given by VSEL*12.5 mV + 600 mV.

8.4.6 VOCORE_1V3

The **VOCORE_1V3** rail is supplied by the **VDD1** regulator of the **TPS65950**. The **VDD1** regulator is a 1.1A stepdown power converter with configurable output voltage between 0.6 V and 1.45 V in steps of 12.5 mV. This regulator is used to power the **OMAP3530** core.

The **OMAP3530** can request the **TPS65950** to scale the **VDD1** output voltage to reduce power consumption. The default output voltage at power-up depends on the boot mode settings, which in the case of the BeagleBoard is 1.2V. The output voltage of the **VDD1** regulator can be scaled by software or hardware by setting the ENABLE_VMODE bit (VDD1_VMODE_CFG[0]). In each of these modes, the output voltage ramp can be single-step or multiple-step, depending on the value of the STEP_REG field of the VDD1_STEP[4:0] register. The VOCORE_1V3 rail should be set to 1.3V after boot up.

Apart from these modes, the **VDD1** output voltage can also be controlled by the **OMAP3530** through the SmartReflex I2C interface between the OMAP3530 and the **TPS65950**. The default voltage scaling method selected at reset is a software-controlled mode. Regardless of the mode used, **VDD1** can be configured to the same output voltage in sleep mode as in active mode by programming the DCDC_SLP bit of the VDD1_VMODE_CFG[2] register to 0. When the DCDC_SLP bit is 1, the sleep mode output voltage of **VDD1** equals the floor voltage that corresponds to the VFLOOR field (VDD1_VFLOOR[6:0]).

8.4.7 VDD2

The **VDD2** voltage rail is generated by the **TPS65950** using the **VDD2** regulator. The **VDD2** regulator is a stepdown converter with a configurable output voltage of between

0.6 V and 1.45 V and is used to power the OMAP3530 core. **VDD2** differs from **VDD1** in its current load capabilities with an output current rating of 600 mA in active mode.

The **VDD2** provides different voltage regulation schemes. When **VDD2** is controlled by the VMODE2 signal or with the SmartReflex interface, the range of output voltage is 0.6 V to 1.45 V. The use of the VMODE2 signal and the VDD2_VMODE_CFG, VDD2_STEP, VDD2_FLOOR, and VDD2_ROOF registers is similar to the use of the corresponding signals and registers for **VDD1**. **VDD2** shares the same SmartReflex I2C bus to provide voltage regulation. The VDD2_SR_CONTROL register is provided for controlling the **VDD2** output voltage in SmartReflex mode.

When the **VDD2** is used in software-control mode, the VSEL (VDD2_ DEDICATED[4:0]) field can be programmed to provide output voltages of between 0.6 V and 1.45 V. The output voltage for a given value of the VSEL field is given by VSEL*12.5 mV + 600 mV. If the VSEL field is programmed so that the output voltage computes to more than 1.45 V, the TPS65950 sets the **VDD2** output voltage to 1.5 V.

8.5 Peripheral Voltages

There are six additional voltages used by the system that are generated by the **TPS65950**. These are:

- VDD_PLL2
- VDD_PLL1
- VDAC_1V8
- VDD_SIM
- VMMC1
- VAUX2

Figure 25 shows the peripheral voltages supplied by the **TPS65950**.

8.5.1 VDD_PLL2

This programmable LDO is used to power the OMAP3530 PLL circuitry. The **VPLL2** LDO can be configured through the I2C interface to provide output voltage levels of 1.0 V, 1.2 V, 1.3 V, or 1.8 V, based on the value of the VSEL field (VPLLI_DEDICATED[3:0]). On the board this rail is used to power DVI output for pins DSS_DATA(0:5), DSS_DATA(10:15) and DSS_DATA(22:23). The VPLL2 must be set to 1.8V for proper operation of the **DVI-D** interface.

8.5.2 VDD_PLL1

The VPLL1 programmable LDO regulator is low-noise, linear regulator used for the OMAP3530 PLL supply. The VDD_PLL1 rail is initialized to 1.8V.

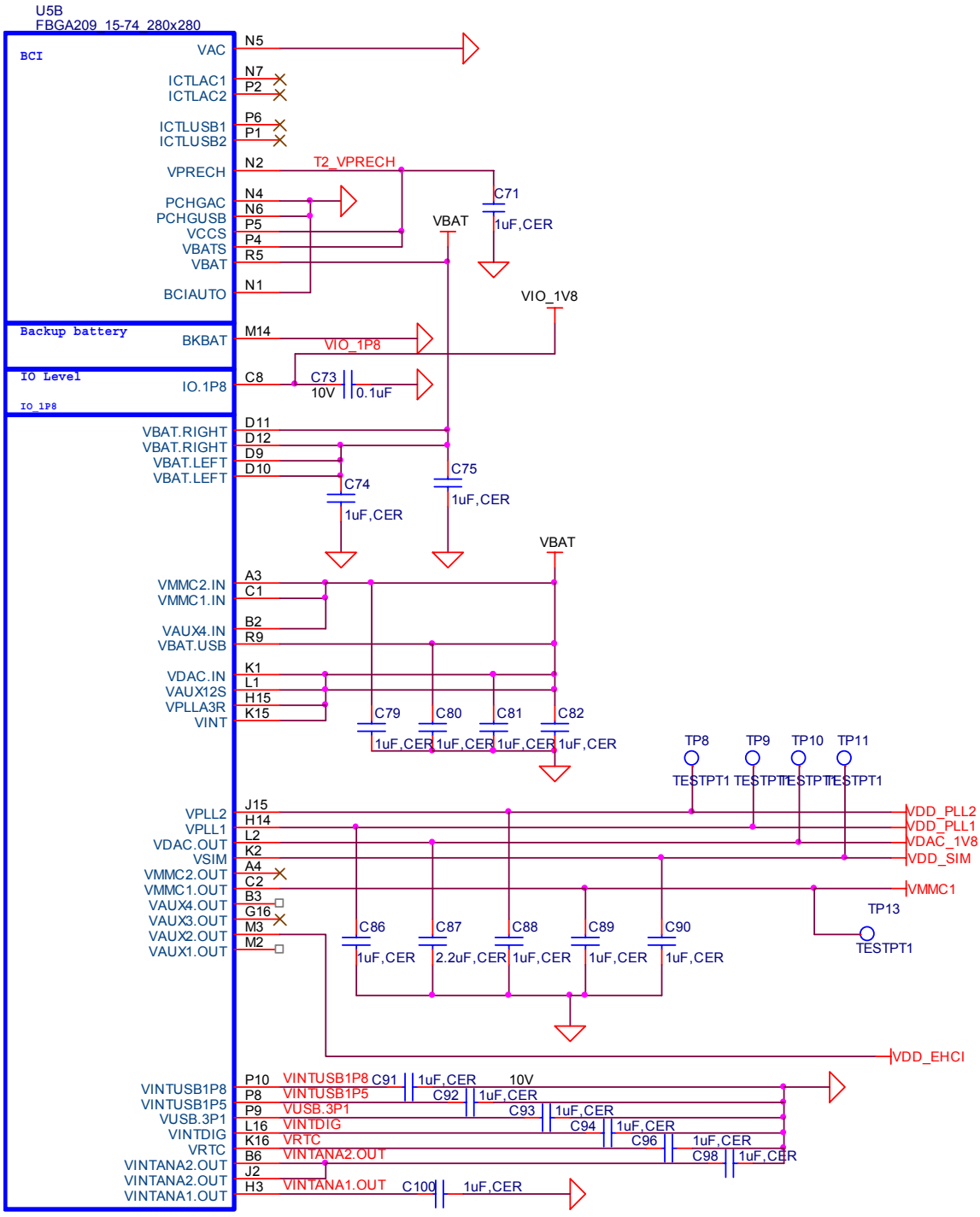

Figure 25. Peripheral Voltages

8.5.3 VDAC_1V8

The **VDAC** programmable LDO regulator is a high-PSRR, low-noise, linear regulator that powers the OMAP3530 dual-video DAC. It is controllable with registers via I2C and can be powered down if needed. The **VDAC** LDO can be configured to provide 1.2V, 1.3 V, or 1.8 V in on power mode, based on the value of the VSEL field (VDAC_DEDICATED[3:0]). The **VDAC_1V8** rail should be set to 1.8V for the BeagleBoard.

8.5.4 VDD_SIM

This voltage regulator is a programmable, low dropout, linear voltage regulator supplying the bottom 4 bits of the 8 bit **SD/MMC** card slot. The VSEL field (VSIM_DEDICATED[3:0]) can be programmed to provide output voltage of 1.0 V, 1.2 V, 1.3 V, 1.8 V, 2.8 V, or 3.0 V and can deliver up to 50mA. The default output voltage of this LDO as directed by the **TPS65950** boot pins is 1.8V.

8.5.5 VMMC1

The **VMMC1** LDO regulator is a programmable linear voltage converter that powers the MMC1 slot and includes a discharge resistor and overcurrent protection (short-circuit). This LDO regulator can also be turned off automatically when the MMC card extraction is detected. The VMMC1 LDO is powered from the main **VBAT** rail. The **VMMC1** rail defaults to 3.0V as directed by the **TPS65950** boot pins and will deliver up to 220mA. It can be set to 3.0V in the event 3V cards are being used.

8.5.6 VAUX2

The **VAUX2** LDO regulator is a programmable linear voltage converter that powers the 1.8V I/O rail of the USB PHY and includes a discharge resistor and overcurrent protection (short-circuit). The VAUX2 LDO is powered from the main **VBAT** rail. The **VMMC1** rail defaults to 3.0V as directed by the **TPS65950** boot pins and will deliver up to 220mA. The voltage rail is labeled **VDD_EHCI** on the schematic.

8.5.7 Boot Configuration

The boot configuration pins on the **TPS65950** determine the power sequence of the device. For the OMAP3530 support, the boot pin configuration is fixed at:

- **BOOT0** tied to VBAT
- **BOOT1** tied to Ground.

8.5.8 RTC Backup Battery

An optional battery to backup the Real Time Clock that is in the **TPS65950**. The board does not come equipped with the battery. The battery can be purchased from DigiKey or other component suppliers. When the battery is not installed, **R66** must be installed. You must make sure that prior to installing the battery that R66 is removed.

Refer to section **9.11** for information on the battery selection and installation.

8.5.9 Power Sequencing

Based on the boot configuration pins, the **TPS65950** knows the type of OMAP processor that it needs to support, in this case the OMAP3530. The voltages are ramped in a sequence that is compatible with the OMAP3530 processor. **Figure 26** is the sequence in which the power rails, clocks, and reset signal come up.

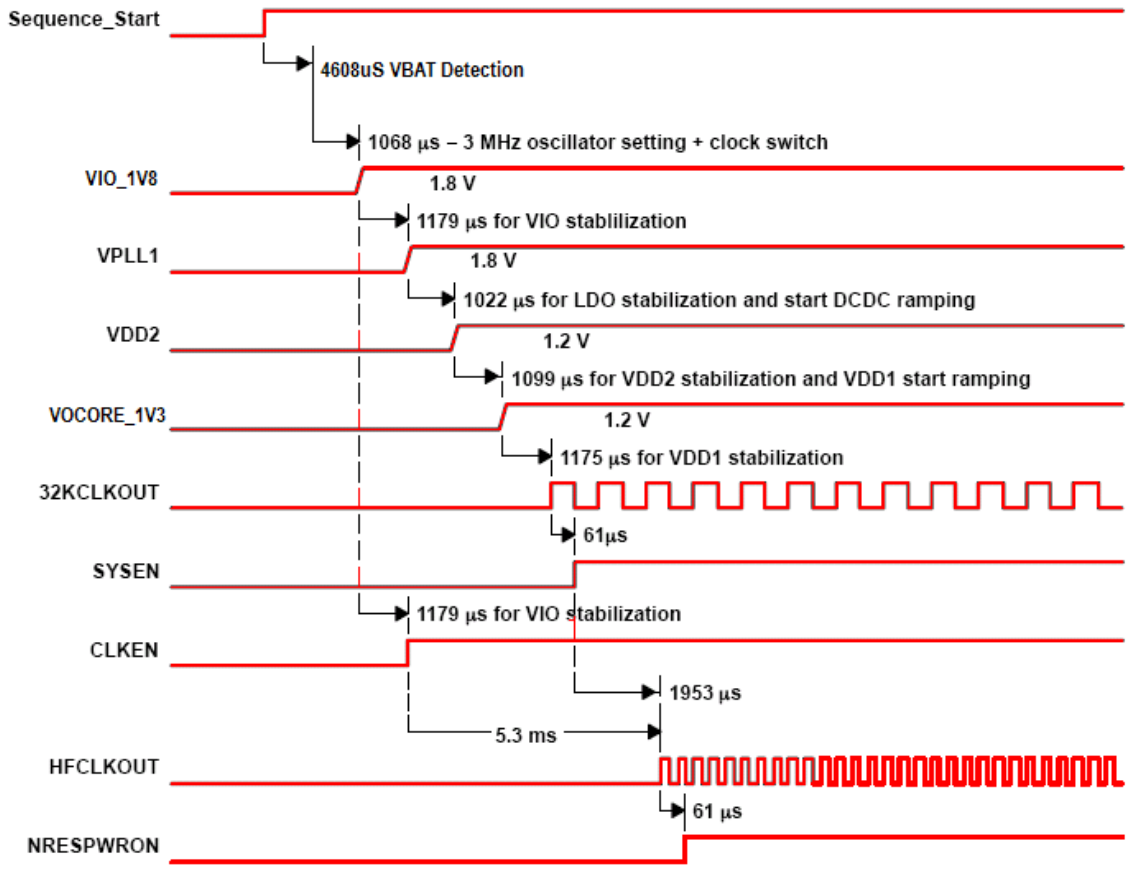

Figure 26. Power Sequencing

8.5.10 Reset Signals

The BeagleBoard uses three distinct reset circuits:

- Warm Reset
- Cold Reset
- User Reset

Figure 27 shows the connections for the Reset interfaces.

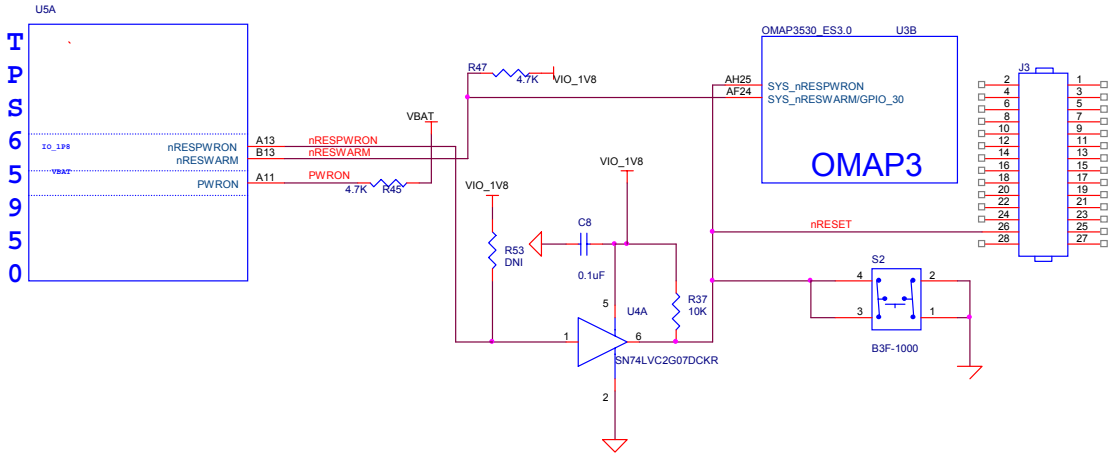

Figure 27. Reset Circuitry

8.5.10.1 Warm Reset

The warm reset is generated by the **OMAP3530** processor on power up. The **nRESWARM** signal is a bidirectional reset. When an internal reset occurs, **nRESWARM** goes low and resets all the peripherals and the **TPS65950**. The **TPS65950** can be configured to perform a warm reset of the device to bring it into a known defined state by detecting a request for a warm reset on the **NRESWARM** pin. The minimum duration of the pulse on the **nRESWARM** pin should be two 32-kHz clock cycles. The **nRESWARM** output is open-drain; consequently, an external pullup resistor is required. There is no way for the user to generate a warm reset on the BeagleBoard.

8.5.10.2 Cold Reset

On power up as shown in **Figure 27**, the **TPS65950** generates **nRESPWRON**, power on reset. The signal from the **TPS65950** is an output only and is not an open drain signal. By running the signal through a buffer, **SN74LVC2G07**, the signal becomes open drain, which requires a pullup on the signal. This will allow the **nRESPWRON** signal to be

pulled low, by pressing the reset switch **S2**, to force a reset to the **OMAP3530** processor and to any device on the expansion card that require a reset.
It also allows for the reset signal to be pulled low or held low for an extended time by circuitry on the expansion card if needed.

8.5.10.3 User Reset

The USER RESET button can be used to request a Warm Reset from the processor. After initialization, this pin becomes an input to the processor. By pushing the Reset button, an interrupt is generated into the OMAP3530 processor. The software that is run as a result of this can then do whatever housekeeping is required and then send the processor into a reset mode.

8.5.10.4 PWRON

You will notice another signal on the **TPS65950** called **PWRON**. This signal is referenced in the **TPS65950** documentation. In the BeagleBoard design it is not used but it is pulled high to insure the desired operation is maintained.

8.5.11 mSecure Signal

This signal provides for protection of the **RTC registers** in the **TPS65950** be disabling that function via a control signal form the **OMAP353**0 processor.

For more information on the operation on the signal, please refer to the OMAP3530 Technical Reference Manual.

8.6 OMAP3530 Processor

The heart of BeagleBoard is the OMAP3530 processor. **Figure 28** is a high level block diagram of the OMAP3530.

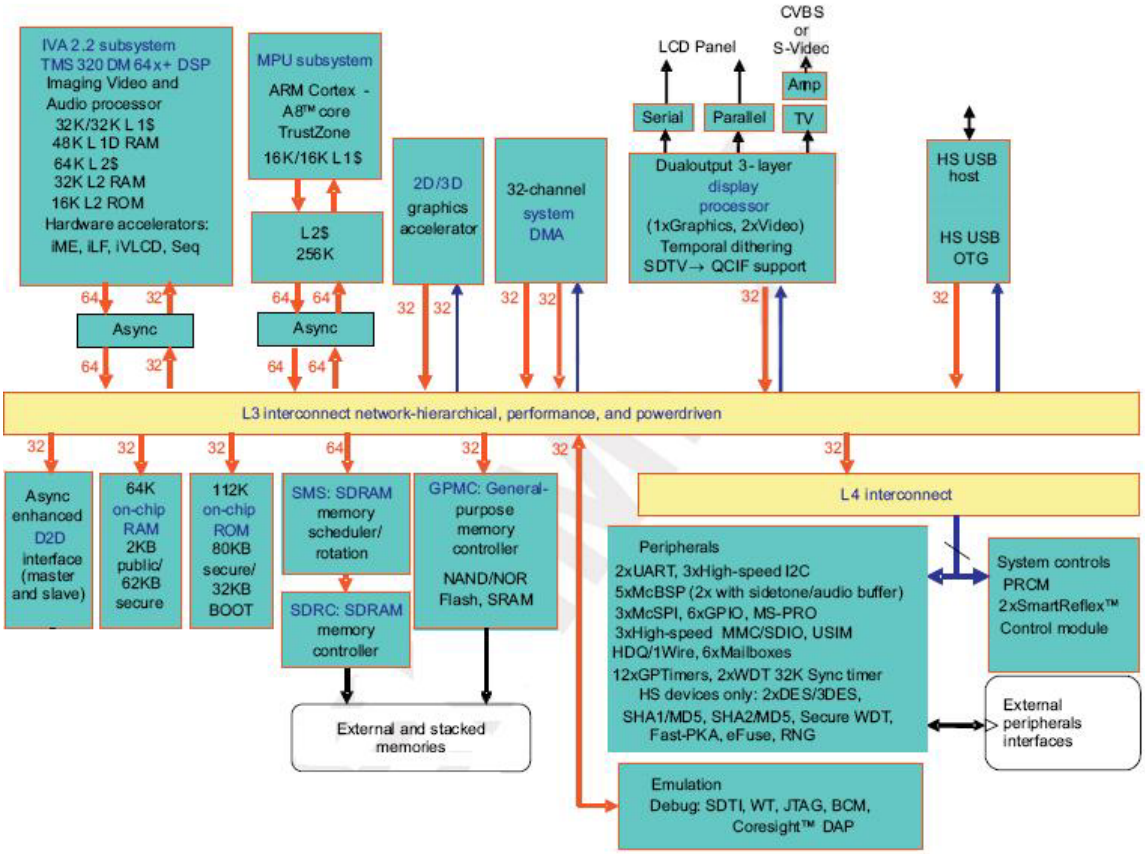

Figure 28. OMAP3530 Block Diagram

8.6.1 Overview

The OMAP3530 high-performance, multimedia application device is based on the enhanced OMAP™ 3 architecture and is integrated on TI's advanced 65-nm process technology. The OMAP3530 architecture is configured with different sets of features in different tier devices. Some features are not available in the lower-tier devices. For more information, refer to the OMAP3530 Technical Reference Manual (TRM).The architecture is designed to provide best-in-class video, image, and graphics processing sufficient to various applications.

The OMAP3530 supports high-level operating systems (OSs), such as:

- Windows CE

- Linux
- QNX
- Symbian
- Others

This OMAP3530 device includes state-of-the-art power-management techniques required for high-performance low power products. The OMAP3530 supports the following functions and interfaces on the BeagleBoard:

- Microprocessor unit (MPU) subsystem based on the ARM Cortex-A8™ microprocessor
- POP Memory interface
  - 2Gb MDDR (256Mbytes)
  - 2Gb NAND Flash (256Mbytes)
- 24 Bit RGB Display interface (DSS)
- SD/MMC interface
- USB OTG interface
- NTSC/PAL/S-Video output
- Power management
- Serial interface
- I^2C interface
- I^2S Audio interface (McBSP2)
- Expansion McBSP1
- JTAG debugging interface

8.6.2 SDRAM Bus

The SDRAM bus is not accessible on the BeagleBoard. Its connectivity is limited to the POP memory access on the top of the OMAP3530 and therefore is only accessible by the SDRAM memory.

The base address for the DDR SDRAM in the POP device is **0x8000 0000**.

8.6.3 GPMC Bus

The GPMC bus is not accessible on the BeagleBoard. Its connectivity is limited to the POP memory access on the top of the OMAP3530 and therefore is only accessible by the NAND memory.

The memory on the GPMC bus is NAND and therefore will support the classical NAND interface. The address of the memory space is programmable.

8.6.4 DSS Bus

The display subsystem provides the logic to display a video frame from the memory frame buffer in SDRAM onto a liquid-crystal display (LCD) display via the DVI-D interface or to a standalone LCD panel via the LCD interface connectors. The logic levels of the LCD expansion connectors are 1.8V so it will require buffering of the signals to drive most LCD panels. The DSS is configured to a maximum of 24 bits, but can be used in lower bit modes if needed.

8.6.5 McBSP2

The multi-channel buffered serial port (McBSP) McBSP2 provides a full-duplex direct serial interface between the OMAP3530 and the audio CODEC in the **TPS65950** using the I2S format. Only four signals are supported on the McBSP2 port. **Figure 29** is a depiction of McBSP2.

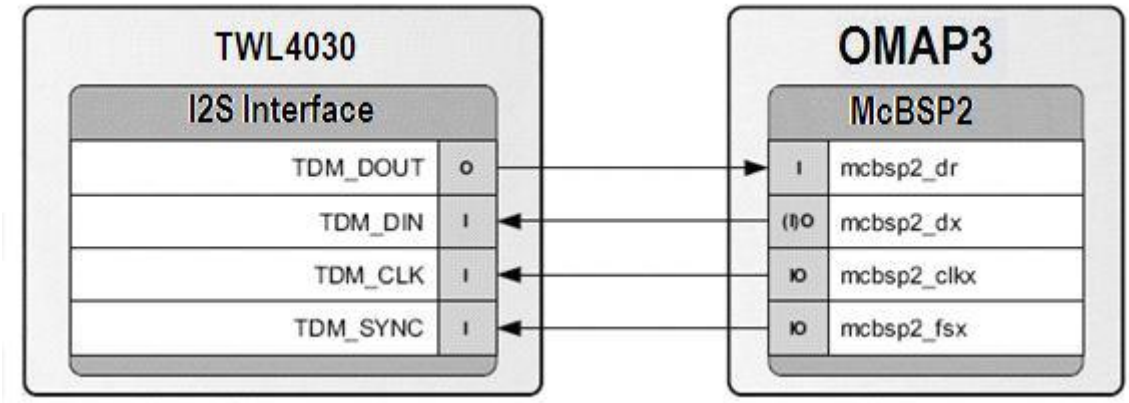

Figure 29. McBSP2 Interface

8.6.6 McBSP1

McBSP1 provides a full-duplex direct serial interface between the OMAP3530 and the expansion interface. There are 6 signals supported on McBSP1, unlike the 4 signals on the other ports. **Figure 30** is a diagram of McBSP1.

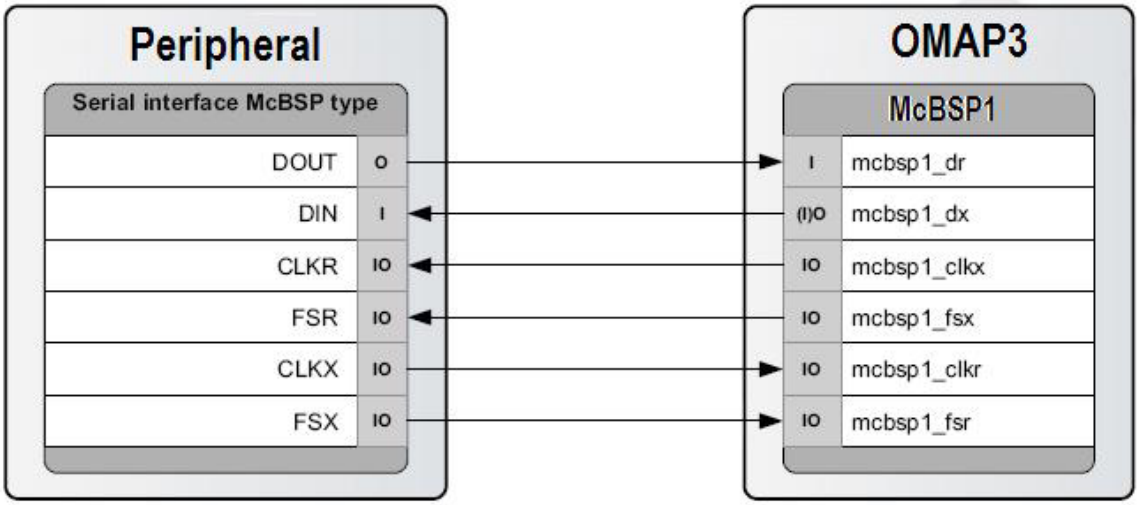

Figure 30. McBSP1 Interface

8.6.7 McBSP3

McBSP3 provides a full-duplex direct serial interface between the OMAP3530 and the expansion interface. **Figure 31** is a diagram of McBSP3.

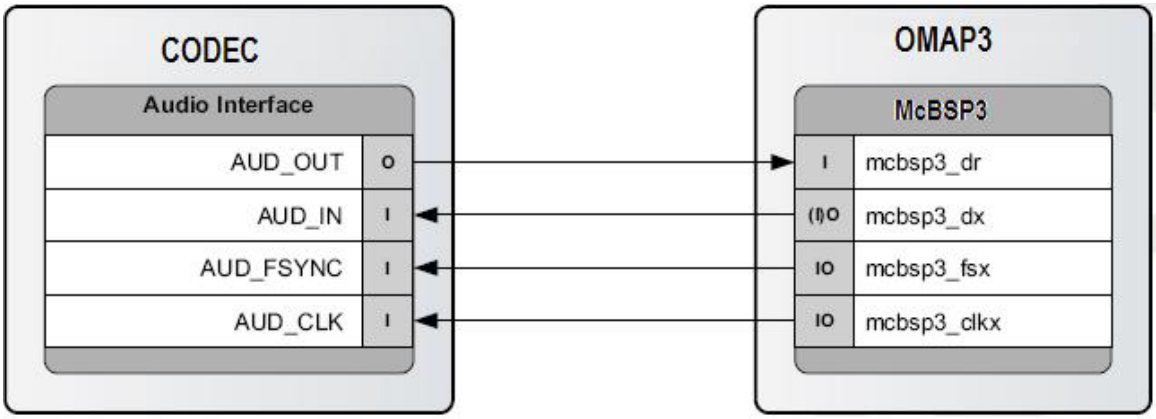

Figure 31. McBSP3 Interface

8.6.8 Pin Muxing

On the OMAP3530, the majority of pins have multiple configurations that the pin can be set to. In essence, the pin can become different signals depending on how they are set in the software. In order for the BeagleBoard to operate, the pins used must be set to the correct signal. In some cases, the default signal is the correct signal. Each pin can have a maximum of 8 options on the pin. This is called the pin mode and is indicated by a three

bit value (0:3). In the case of the signals going to the expansion connector, the settings required for those pins depends on how they are to be used. For an explanation of the options, please refer to the Expansion Header section. Each pin can be set to a different mode independent of the other pins on the connector.

Table 4 is a list of all of the signals used on the OMAP3530 for the BeagleBoard and the required mode setting for each pin. Where the default setting is needed, it will be indicated. The USER notation under mode indicates that this is an expansion signal and can be set at the discretion of the user. A FIXED indicates that there is only one function for that signal and that it cannot be changed,

Table 4. OMAP3530 Pin Muxing Settings

Signal	Mode
DSS	Default
MMC1	Default
MMC2	User
UART3	Default
GPMC	Default
UART1	Default
I2C1	Default
I2C2	Default
I2C3	Default
I2C4	Default
JTAG	FIXED
TV_OUT	Default
SYS_nRESPWRON	Default
SYS_nRESWARM	Default
SYS_nIRQ	Default
SYS_OFF	Default
SYS_CLKOUT	Default
SYS_CLKOUT2	Default
SYS_CLKREQ	Default
SYS_XTALIN	FIXED
GPIO_149	4
GPIO_150	4
McBSP1	Default
McBSP2	User
McBSP3	Default
GPIO_171	4
GPIO_172	4

8.6.9 GPIO Mapping

There are a number of GPIO pins from the OMAP3530 that are used on the BeagleBoard design. **Table 5** shows which of these GPIO pins are used in the design and whether they are inputs or outputs. While GPIO pins can be used as interrupts, the table only covers the GPIO pin mode. If it is an interrupt, then it is covered in the interrupt section.

Table 5. OMAP3530 GPIO Pins

OMAP PIN	INT/GPIO	I/O	Signal	USAGE
AA9	GPIO_149	O	LED_GPIO149	Controls User LED0
W8	GPIO_150	O	LED_GPIO149	Controls User LED1
AG9	GPIO_23	I	MMC1_WP	SD/MMC card slot Write protect
J25	GPIO_170	O	DVI_PUP	Controls the DVI-D interface. A Hi = DVI-D enabled.
AE21	GPIO_7	I	SYSBOOT_5	Used to put the device in the boot mode or as a user button input

Other signals, such as those that connect to the expansion connector, may also be set as a GPIO pin. For information on those, refer to the Expansion Connector section.

8.6.10 Interrupt Mapping

There are a small number of pins on the OMAP3530 that act as interrupt. Some of these interrupts are connected to the TPS65950 and their status is reflected through the main TPS65950 interrupt. **Table 6** lists the interrupts.

Table 6. OMAP3530 Interrupt Pins

TPS65950 Pin	OMAP PIN	INT/GPIO	USAGE
	AF26	SYS_nIRQ	Interrupt from the TPS65950
	AH8	GPIO_29	SD Write protect lead. Can be polled or set to an interrupt.
P12		GPIO0	MMC1 card detect input. Goes to the OMAP3530 over the SYS_nIRQ pin.

8.7 POP Memory Device

The OMAP3530 uses what is called POP (Package-on-Package) memory. The memory is a MCP (Multi Chip Package) that contains both the Mobile DDR SDRAM and the NAND Flash. **Figure 32** shows the POP Memory concept.

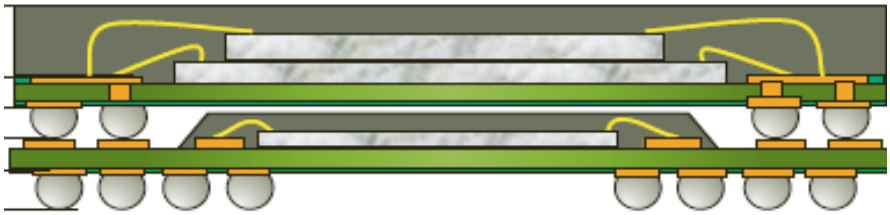

Figure 32. POP Memory

The Memory device mounts on top of the OMAP3530 device. The configuration used on the board is a 2Gb NAND Flash plus 2Gb MDDR SDRAM device from Micron.

8.8 System Clocks

There are three clocks needed for the operation of the BeagleBoard, 32KHz, 26MHz and McBSP_CLKS. **Figure 33** shows the components that make up the System Clocks.

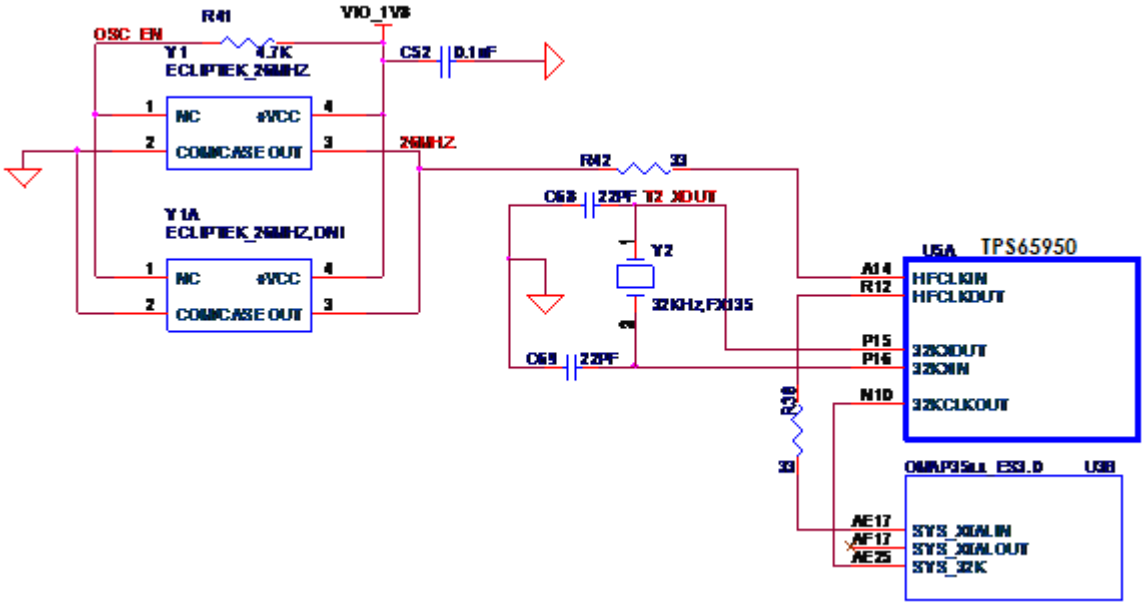

Figure 33. System Clocks

8.8.1 32KHz Clock

The 32KHz clock is needed for the TPS65950 and the **OMAP3530** and is provided by the **TPS65950** via the external 32KHz crystal, **Y2**. The **TPS65950** has a separate output

from the crystal to drive the OMAP3530 that buffers the resulting 32-kHz signal and provides it as **32KCLKOUT**, which is provided to the OMAP3530 on ball **AE25**. The default mode of the 3**2KCLKOUT** signal is active, but it can be disabled if desired under SW control.

The 32.768-kHz clock drives the RTC embedded in the **TPS65950**. The RTC is not enabled by default; the host processor must set the correct date and time to enable the RTC.

8.8.2 26MHz Clock

This section describes the 26MHz clock section of the BeagleBoard.

8.8.2.1 26MHz Source

The BeagleBoard is designed to support two suppliers of the 26MHz oscillator. The **26MHz** clock is provided by an onboard oscillator, **Y1**. The **TPS65950** receives the external **HFCLKIN** signal on ball **A14** and uses it to synchronize or generate the clocks required to operate the TPS65950 subsystems. The **TPS65950** must have this clock in order to function to the point where it can power up the BeagleBoard. This is the reason the **26MHz** clock is routed through the TPS65950. You will also notice an oscillator labeled **Y1A**. This is an alternate footprint for another oscillator that is listed as a second source. You should not have both devices installed at the same time if you plan to use this design.

8.8.2.2 TPS65950 Setup

When the TPS65950 enters an active state, the OMAP3530 must immediately indicate the **HFCLKIN** frequency (26 MHz) by setting the HFCLK_FREQ bit field (bits [1:0]) in the CFG_BOOT register of the TPS65950. HFCLK_FREQ has a default of being not programmed, and in that condition, the USB subsection does not work. The three DCDC switching supplies (VIO, VDD1, and VDD2) operate from their free-running 3-MHz (RC) oscillators, and the PWR registers are accessed at a default 1.5-M byte. HFCLK_FREQ must be set by the OMAP3530 during the initial power-up sequence. On the BeagleBoard, this is done by the internal boot ROM on startup.

8.8.2.3 OMAP3530 26MHz

The 26MHz clock for the **OMAP3530** is provided by the TPS65950 on ball **R12** through **R38**, a 33 ohm resistor is providing to minimize any reflections on the clock line. The clock signal enters via ball **AE17** on the **OMAP3530**.

8.8.3 McBSP_CLKS

An additional clock is also provided by the **TPS65950** called **McBSP_CLKS**. This clock is provided to the OMAP3530 in order to insure synchronization of the I2S interface between the **OMAP3530** and the **TPS65950**.

8.9 USB OTG Port

The BeagleBoard has a USB OTG (On-the-Go) port. It can be used as an OTG port, Client port, or Host port. The main use is as a client port, as that is the mode that will supply the power needed to power the BeagleBoard.

NOTE: In order to use the OTG in the Host mode, the BeagleBoard must be powered from the DC supply.

8.9.1 USB OTG Overview

USB OTG is a supplement to the USB 2.0 specification. The standard USB uses a master/slave architecture, a USB host acting as a master and a USB peripheral acting as a slave. Only the USB host can schedule the configuration and data transfers over the link. The USB peripherals cannot initiate data transfers, they only respond to instructions given by a host.

USB OTG works differently in that gadgets don't need to be pure peripherals because they can sometimes act as hosts. An example might be connecting a USB keyboard or printer to BeagleBoard or a USB printer that knows how to grab documents from certain peripherals and print them. The USB OTG compatible devices are able to initiate the session, control the connection and exchange Host/Peripheral roles between each other.

The USB OTG supplement does not prevent the use of a hub, but it describes role swapping only in the case of a one-to-one connection where two OTG devices are directly connected. If a standard hub is used, the supplement notes that using it will lead to losing USB OTG role-swap capabilities making one device as the Default-Host and the other as the Default-Peripheral until the hub is disconnected.

The combination of the **OMAP3530** and the **TPS65950** allows the BeagleBoard to work as an OTG device if desired. The primary mode of operation however, is intended to be a client mode in order to pull power from the USB host which is typically a PC. As the Rev B does not have a Host USB port, this port will be used as a Host port in many applications.

8.9.2 USB OTG Design

Figure 34 is the design of the USB OTG port on the BeagleBoard.

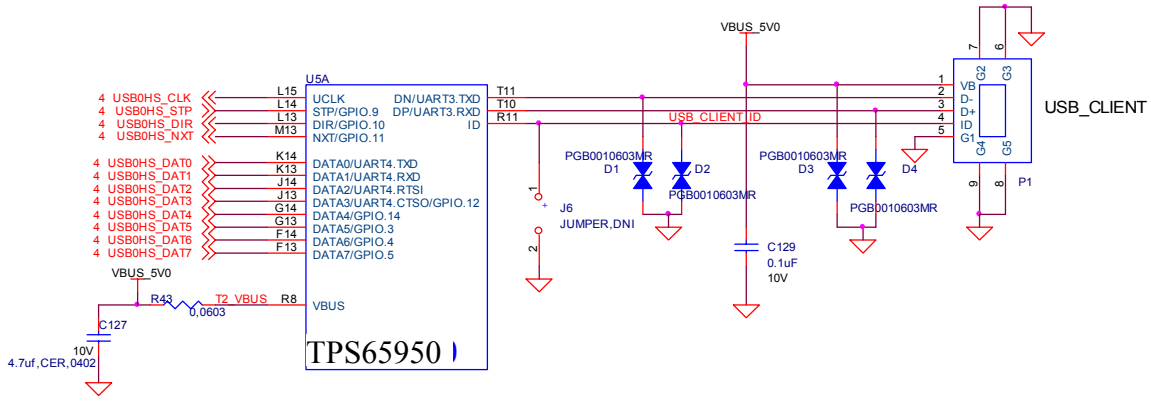

Figure 34. USB OTG Design

8.9.3 OTG ULPI Interface

ULPI is an interface standard for high-speed USB 2.0 systems. It defines an interface between USB link controller (**OMAP3530**) and the **TPS6595**0 that drives the actual bus. ULPI stands for UTMI+ low pin interface and is designed specifically to reduce the pin count of discrete high-speed USB PHYs. Pin count reductions minimize the cost and footprint of the PHY chip on the PCB and reduce the number of pins dedicated to USB for the link controller.

.

Unlike full- and low-speed USB systems, which utilize serial interfaces, high-speed requires a parallel interface between the controller and PHY in order to run the bus at 480Mbps. This leads to a corresponding increase in complexity and pin count. The ULPI used on the BeagleBoard keeps this down to only 12 signals because it combines just three control signals, plus clock, with an 8-bit bi-directional data bus. This bus is also used for the USB packet transmission and for accessing register data in the ULPI PHY.

8.9.3.1 OMAP3530 Interface

The controller for the ULPI interface is the OMAP3530. It provides all of the required signals to drive the interface. **Table 7** describes the signals from the OMAP3530 that are used for the USB OTG interface.

Table 7. OMAP3530 ULPI Interface

Signal	Description	Type	Ball
hsusb0_clk	Dedicated for external transceiver 60-MHz clock input from PHY	I	T28
hsusb0_stp	Dedicated for external transceiver Stop signal	O	T25
hsusb0_dir	Dedicated for external transceiver Data direction control from PHY	I	R28
hsusb0_nxt	Dedicated for external transceiver Next signal from PHY	I	T26
hsusb0_data0	Transceiver Bidirectional data bus	I/O	T27
hsusb0_data1	Transceiver Bidirectional data bus	I/O	U28
hsusb0_data2	Transceiver Bidirectional data bus	I/O	U27
hsusb0_data3	Transceiver Bidirectional data bus	I/O	U26
hsusb0_data4	Transceiver Bidirectional data bus	I/O	U25
hsusb0_data5	Transceiver Bidirectional data bus	I/O	V28
hsusb0_data6	Transceiver Bidirectional data bus	I/O	V27
hsusb0_data7	Transceiver Bidirectional data bus	I/O	V26

8.9.3.2 TPS65950 Interface

The TPS65950 USB interfaces to the OMAP3 over the ULPI interface. **Table 8** is a list of the signals used on the TPS65950 for the ULPI interface.

Table 8. OMAP3530 ULPI Interface

Signal	Description	Type	Ball
UCLK	High speed USB clock	I/O	L15
STP	High speed USB stop	I	L14
DIR	High speed USB dir	O	L13
NXT	High speed USB direction	O	M1
DATA0	High speed USB Data bit 0	I/O	K14
DATA1	High speed USB Data bit 0	I/O	K13
DATA2	High speed USB Data bit 0	I/O	J14
DATA3	High speed USB Data bit 0	I/O	J13
DATA4	High speed USB Data bit 0	I/O	G14
DATA5	High speed USB Data bit 0	I/O	G13
DATA6	High speed USB Data bit 0	I/O	F14
DATA7	High speed USB Data bit 0	I/O	F13

8.9.4 OTG Charge Pump

When the **TPS65950** acts as an A-device, the USB charge pump is used to provide 4.8 V/100 mA to the VBUS pin. When the **TPS65950** acts as a B-device, the USB charge pump is in high impedance. If used in the OTG mode as an A-device, the BeagleBoard will need to be powered from the DC supply. If acting as a B-device, there will not be a voltage source on the USB OTG port to drive the BeagleBoard. **Table 9** describes the charge pump pins.

Table 9. USB OTG Charge Pump Pins

Signal	Description	Type	Ball
CP.IN	The charge pump input voltage. Connected to VBAT.	Power	R7
CP.CAPP	The charge pump flying capacitor plus.	O	L14
CP.CAPM	The charge pump flying capacitor minus.	O	T6
CP.GND	The charge pump ground.	GND	R6

The charge pump is powered by the **VBAT** voltage rail. The charge pump generates a 4.8-V (nominal) power supply voltage to the **VBUS** pin. The input voltage range is 2.7 V to 4.5 V so the 4.2V VBAT is within this range. The charge pump operating frequency is 1 MHz. The charge pump integrates a short-circuit current limitation at 450 mA.

8.9.5 OTG USB Connector

The OTG USB interface is accessed through the miniAB USB connector. If you want to use the OTG port as a USB Host, **pin 4** of the connector must be grounded. The Rev C4 version of Beagle provides jumper pad, **J6** that allows for a small piece of solder to be placed on the pads to perform this function. It should be noted that with the USB Host port on the Rev C4 Beagle, the need to convert the OTG port to a host mode is greatly diminished.

8.9.6 OTG USB Protection

Each lead on the USB port has ESD protection. In order for the interface to meet the USB 2.0 Specification Eye Diagram, these protection devices must be low capacitance.

8.10 USB Host Port

The Rev C4 is equipped with a High Speed USB Host interface connected to the ULPI port 2 on the OMAP3530. It uses a SMSC PHY as the physical interface and provides power control to the USB connector. This port is a High Speed only port and will not support low speed or full speed devices plugged directly into the connector. **Figure 35** is the design of the USB Host port.

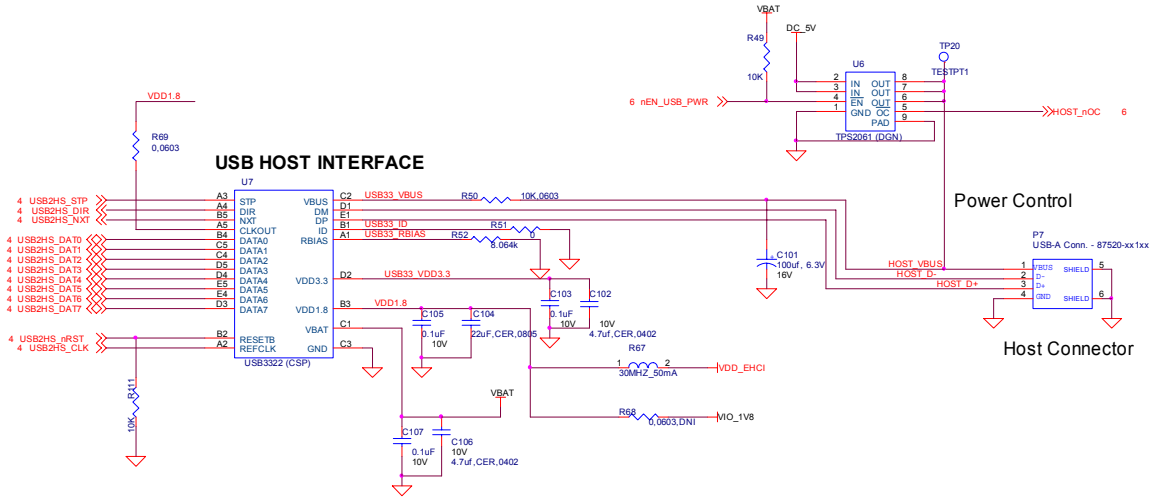

Figure 35. USB Host Design

8.10.1 Host USB OMAP3 Interface

The interface to the OMAP3 is the HSUSB2 interface. The signals used on this interface are contained in **Table 10**.

Table 10. USB Host Port OMAP Signals

Signal	Description	Input/Output
Hsusb2_clk	External transceiver 60-MHz clock output to PHY	O
Hsusb2_stp	External transceiver Stop signal	O
Hsusb2_dir	Transceiver data direction control from PHY	I
Hsusb2_nxt	Next signal from PHY	I
Hsusb2_data0	Bidirectional data bus signal for 12-pin ULPI operation	I/O
Hsusb2_data1	Bidirectional data bus signal for 12-pin ULPI operation	I/O
Hsusb2_data2	Bidirectional data bus signal for 12-pin ULPI operation	I/O
Hsusb2_data3	Bidirectional data bus signal for 12-pin ULPI operation	I/O
Hsusb2_data4	Bidirectional data bus signal for 12-pin ULPI operation	I/O
Hsusb2_data5	Bidirectional data bus signal for 12-pin ULPI operation	I/O
Hsusb2_data6	Bidirectional data bus signal for 12-pin ULPI operation	I/O
Hsusb2_data7	Bidirectional data bus signal for 12-pin ULPI operation	I/O
Gpio_147	Enable/reset line to the USB PHY.	O

The **husb2_clk** signal is an output only and is used to support a HS USB PHY that supports an input clock mode. The SMSC PHY device supports this mode and is used on the Beagle.

8.10.2 Host USB PHY

The PHY used in the design is a USB3322/26 series device from SMSC. The USB3322 is a highly integrated Hi-Speed USB2.0 Transceiver (PHY) that meets all of the electrical

requirements to be used as a Hi-Speed USB Host, Device, or an On-the-Go (OTG) transceiver. In this design, only the host mode of operation is being supported. The USB3322 uses the industry standard UTMI+ Low Pin Interface (ULPI) to connect the USB PHY to the OMAP3. ULPI uses a method of in-band signaling and status byte transfers between the Link and PHY to facilitate a USB session with only 12 pins.

In order to interface to the **OMAP3530**, the device must be used in the 60MHz clock mode. This is done by tying the **CLKOUT** signal on the USB PHY to VIO_1V8. On Rev C4, a zero ohm series resistor was added. This is not required, but was added as a "just in case" option if the CLKOUT signal was a source of noise in the PHY. It was proven not to be the case. The clock for the PHY is derived from the 60MHz signal generated by the **OMAP3530**. All of the signals and their functions align with the descriptions found in the **OMAP3530** interface section.

The USB3322 device requires two voltages, the **VIO_1V8** rail to power the I/O rails and the **VBAT**, which needs to be between 3.1V and 5.1V, to power the rest of the device. On the board the **VBAT** is a regulated 4.2V DC. The 3.3V rail for the device is generated internally and requires a filter and bypass cap to be connected externally. Unlike the Rev C3 version, the Rev C4 version derives its 1.8V from the **VAUX2** rail supplied by the **TPS65950** PMIC. It also uses a ferrite bead, R67, to provide additional filtering for noise. This is the fix for the EHCI noise issue. There is an option to connect the 1.8V rail to the **VIO_1V8** rail, but that has not been populated in the Rev C4 design.

The **RBIAS** block in the PHY consists of an internal bandgap reference circuit used for generating the driver current and the biasing of the analog circuits. This block requires an external 8.06KΩ, 1% tolerance, reference resistor connected from **RBIAS** to ground. The nominal voltage at **RBIAS** is 0.8V and therefore the resistor will dissipate approximately 80µW of power.

The USB3322 can detect **ID** grounded and **ID** floating to determine if an A or B cable has been inserted. The A plug will ground the **ID** pin while the B plug will float the **ID** pin. As we are not using this device to support the OTG protocol but instead as a host device, we ground the **ID** pin to force it into a Host mode at all times. The **ID** signal is not present on the USB connector.

The USB3322 transceiver fully integrates all of the USB termination resistors on both **DP** and **DM**. This includes 1.5kΩ pull-up resistors, 15kΩ pull-down resistors and the 45Ω high speed termination resistors. These resistors require no tuning or trimming.

8.10.3 Host USB Connector

The USB connector used is a Type A receptacle and provides connections for four signals, DP, DM, VBUS, and Ground. This is the same connector you will see on the back of a USB hub. You will notice that there are no external ESD devices on the connector. The ESD protection is integrated into the USB PHY.

8.10.4 Host USB Power Control

Power is provided through the USB Host connector to power devices that are plugged into the USB host connector. This power can be controlled by the **OMAP3530** via the **TPS2061** power switch.

The **TPS2061** power-distribution switch is intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. This device incorporates a 70-mW N-channel MOSFET power switch. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The switch is controlled by the **TPS65950** using the **LED.A** signal. The **OMAP3530** uses the I2C interface to activate the signal in the **TPS65950**.

The amount of available current to be supplied depends on the remaining current available when in USB mode or the DC supply. The switch will not be able to supply more current than is available from the DC source being used.

The **TPS2061** also provides an overcurrent indicator and protection circuit. When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent (OC) logic output low. This is read by the **TPS65950** via the **CD2** pin. The **CD2** pin can be set to generate an interrupt to the **OMAP3530** to alert it of this condition.

When continuous heavy overloads and short-circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures that the switch remains off until valid input voltage is present. This power-distribution switch is designed to set current limit at 1.5 A typically. As mentioned, the amount of current available depends on the current source.

8.11 SD/MMC

The board provides an SD/MMC interface. Its primary use is for proving the boot source for SW but it can be used for other things such as cameras and Wireless LAN cards. Typical users prefer to use the USB port for these functions and as such, the SD card function is the primary us of this connector.

The connector supports 7 different types of cards.

- **SD-** Secure Digital (SD) is a flash memory card format developed by Matsushita, SanDisk and Toshiba for use in portable devices. As of 2007, SD card capacities range from 8 MB to 16 GB. Several companies have announced SD cards with 32 GB. Cards with 4-32 GB are considered high-capacity. The format has proven to be very popular. However, compatibility issues between older devices and the

newer 4 GB and larger cards and the SDHC format have caused considerable confusion for some users. SD card have a write protect tab to prevent the data from being overwritten. SD supports 1-bit SD, 4-bit SD, and SPI modes.

- **miniSD-** Has the same features as the SD with the exceptions that it is in a smaller size and the support for 4-bit mode is optional amongst suppliers.

- **SDIO** - SDIO stands for Secure Digital Input Output. SD slots can actually be used for more than flash memory cards. Devices that support **SDIO** can use small devices designed for the SD form factor, like GPS receivers, Wi-Fi or Bluetooth adapters, modems, Ethernet adapters, barcode readers, IrDA adapters, FM radio tuners, TV tuners, RFID readers, digital cameras, or other mass storage media such as hard drives. SDIO cards are fully compatible with SD Memory Card host controller (including mechanical, electrical, power, signaling and software). When an SDIO card is inserted into a non SDIO-aware host, it will cause no physical damage or disruption to device or host controller. It should be noted that SPI bus topology is mandatory for SDIO, unlike SD Memory and most of the SD Memory commands are not supported in SDIO. **Figure 36** is an example of a SDIO camera card.

Figure 36. Example of an SDIO Card

- **MMC**- The Multi Media Card (**MMC**) is a flash memory card standard. Unveiled in 1997 by Siemens AG and SanDisk, it is based on Toshiba's NAND-based flash memory, and is therefore much smaller than earlier systems based on Intel NOR-based memory such as CompactFlash. MMC is about the size of a postage stamp:

24 mm x 32 mm x 1.4 mm. MMC originally used a 1-bit serial interface, but newer versions of the specification allow transfers of 4 at a time. MMCs are currently available in sizes up to and including 4 GB an 8 GB models.

- **MMCplus**- The version 4.x of the MMC standard, introduced in 2005, brought in two very significant changes to compete against SD cards. These were support for running at higher speeds (26MHz, 52MHz) than the original MMC (20MHz) or SD (25MHz, 50MHz). Version 4.x cards are fully backward compatible with existing readers but require updated hardware/software to use their new capabilities; even though the 4 bit wide bus and high-speed modes of operation are deliberately electrically compatible with SD, the initialization protocol is different, so firmware/software updates are required to allow these features to be enabled when the card is used in an SD reader.

- **MMCmobile** – Is basically the same as MMCplus except that it supports 8 bit data mode.

- **RS-MMC** –This alternate form factor is known as Reduced-Size MultiMediaCard, or RS-MMC, and was introduced in 2004. This form factor is a smaller form factor, of about half the size: 24 mm × 18 mm × 1.4 mm. RS-MMCs are simply smaller MMCs. RS-MMCs are currently available in sizes up to and including 4 GB. Nokia used to use RS-MMC in the Nokia 770 Internet Tablet. **Figure 37** is a side by side comparison of the RS-MMC and MMC card.

Figure 37. RS-MMC and Card

Figure 38 is the SD/MMC interface design on the BeagleBoard.

8.11.1 MMC Power

The SD/MMC connector is supplied power from the **TPS65950** using the **VMMC1** rail. The default setting on this rail is 3.0V as set by the Boot ROM and under SW control, can be set to 1.80V for use with 1.8V cards. The maximum current this rail can provide is

220mA as determined by the TPS65950 regulator. Maximum current can be limited by the overall current available from the USB interface of the PC.

8.11.2 OMAP3530 Interface

There are no external buffers required for the SD/MC operation. The **OMAP3530** provides all of the required interfaces for the SD/MMC interface.

The main features of the MMC/SD/SDIO host controller are:

- Full compliance with MMC command/response sets as defined in the *Multimedia Card System Specification*, v4.0
- Full compliance with SD command/response sets as defined in the *SD Memory Card Specifications*, v1.10d
- Full compliance with SDIO command/response sets and interrupt/read-wait mode as defined in the *SDIO Card Specification, Part E1*, v1.10
- Compliance with sets as defined in the *SD Card Specification, Part A2, SD Host Controller Standard Specification*, v1.00
- Full compliance with MMC bus testing procedure as defined in the *Multimedia Card System Specification*, v4.0
- Full compliance with CE-ATA command/response sets as defined in the *CE-ATA Standard Specification*
- Full compliance with ATA for MMCA specification
- Flexible architecture allowing support for new command structure
- Support:
  - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards
  - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards
- Built-in 1024-byte buffer for read or write
- 32-bit-wide access bus to maximize bus throughput
- Single interrupt line for multiple interrupt source events
- Two slave DMA channels (1 for TX, 1 for RX)
- Programmable clock generation
- Support SDIO Read Wait and Suspend/Resume functions
- Support Stop at block gap
- Support command completion signal (CCS) and command completion signal disable (CCSD) management as specified in the *CE-ATA Standard Specification*

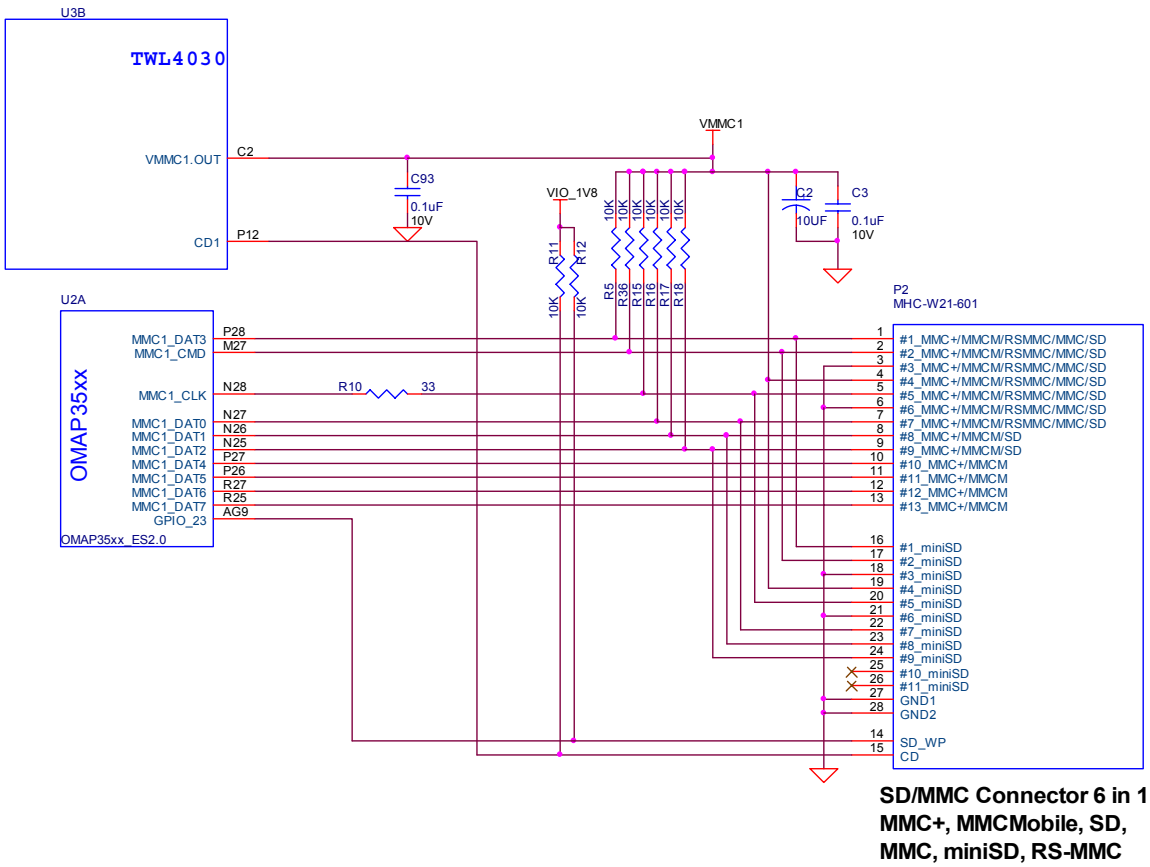

Figure 38. SD/MMC Interface

The known limitations are as follows:

- No built-in hardware support for error correction codes (ECC). See the *Multimedia Card System Specification*, v4.0, and the *SD Memory Card Specifications*, v1.10d, for details about ECC.
- The maximum block size defined in the *SD Memory Card Specifications*, v1.10d that the host driver can read and write to the buffer in the host controller is 2048 bytes. MMC supports a maximum block size of 1024 bytes. Up to 512 byte transfers, the buffer in MMC is considered as a double buffering with ping-pong management; half of the buffer can be written while the other part is read. For 512 to 1024 byte transfers, the entire buffer is dedicated to the transfer (read only or write only).

Table 11 provides a description of the signals on the MMC card.

Table 11. SD/MMC OMAP Signals

Signal Name	Description	I/O	Pin
MMC1_CLK	SD/MMC Clock output.	O	N28
MMC1_CMD	SD/MMC Command pin	I/O	M27
MMC1_DAT(0..7)	SD/MMC Data pins	I/O	N27,N26,N25,P28,P27, P26,R27,R25
MMC_WP	Write Protect detect	I	AG9

8.11.3 Card Detect

When a card is inserted into the SD/MMC connector, the **Card Detect** pin is grounded. This is detected on pin **P12** of the **TPS65950**. An interrupt, if enabled, is sent to the **OMAP3530** via the interrupt pin. The SW can be written such that the system comes out of sleep or a reduced frequency mode when the card is detected.

8.11.4 Write Protect

If an SD card is inserted into the SD/MMC connector and the write protect pin is active, the Write Detect pin is grounded. This is detected **GPIO_29** of the OMAP3530. The SW can then determine if the card is write protected and act accordingly.

8.11.5 8 Bit Mode

The BeagleBoard also supports the new 8-bit cards. The upper 4 bits are supplied by the VDD_SIM power rail and as such the 8-bit mode is only supported in 1.8V modes. This requires that both the VMMC1 and VDD_SIM rails must be set to 1.8V when using 8 bit cards.

8.11.6 Booting From SD/MMC Cards

The ROM code supports booting from MMC and SD cards with some limitations:

- Support for MMC/SD cards compliant with the Multimedia Card System Specification v4.2 from the MMCA Technical Committee and the Secure Digital I/O Card Specification v2.0 from the SD Association. Including high-capacity (size >2GB) cards: HC-SD and HC MMC.
- 3-V power supply, 3-V I/O voltage on port 1
- Initial 1-bit MMC mode, 4-bit SD mode.
- Clock frequency:
  - Identification mode: 400 kHz
  - Data transfer mode: 20 MHz
- Only one card connected to the bus
- FAT12/16/32 support, with or without master boot sector (MBR).

The high-speed MMC/SD/SDIO host controllers handle the physical layer while the ROM code handles the simplified logical protocol layer (read-only protocol). A limited range of commands is implemented in the ROM code. The MMC/SD specification defines two operating voltages for standard or high-speed cards. The ROM code only supports standard operating voltage range (3-V) (both modes supported). The ROM code reads out a booting file from the card file system and boots from it.

8.12 Audio Interface

The BeagleBoard supports stereo in and out through the **TPS65950** which provides the audio CODEC.

Figure 39 is the Audio circuitry design on the BeagleBoard.

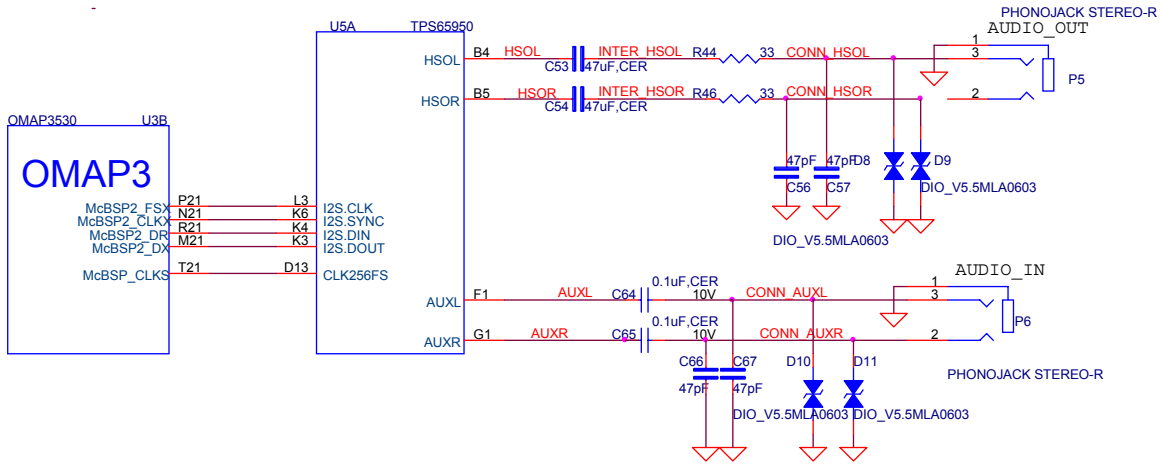

Figure 39. Audio Circuitry

8.12.1 OMAP3530 Audio Interface

There are five McBSP modules called McBSP1 through McBSP5 on the OMAP3530. **McBSP2** provides a full-duplex, direct serial interface between CODEC inside the **TPS65950**. It supports the I2S format to the TPS65950. In **Table 12** are the signals used on the **OMAP3530** to interface to the CODEC.

Table 12. OMAP3530 Audio Signals

Signal Name	Description	I/O	Pin
mcbsp2_dr	Received serial data	I	R21
mcbsp2_dx	Transmitted serial data	I/O	M21
mcbsp2_clkx	Combined serial clock	I/O	N21
mcbsp2_fsx	Combined frame synchronization	I/O	P21
Mcbsp_clks	External clock input. Used to synchronize with the TPS65950	I	T21

8.12.2 TPS65950 Audio Interface

The **TPS65950** acts as a master or a slave for the I2S interface. If the **TPS65950** is the master, it must provide the frame synchronization (I2S_SYNC) and bit clock (I2S_CLK) to the **OMAP3530**. If it is the slave, the **TPS65950** receives frame synchronization and bit clock. The TPS65950 supports the I2S left-justified and right-justified data formats, but doesn't support the TDM slave mode.

In **Table 13** are all the signals used to interface to the **OMAP3530**.

Table 13. OMAP3530 Audio Signals

Signal Name	Description	I/O	Pin
I2S.CLK	Clock signal (audio port)	I/O	L3
I2S.SYNC	Synchronization signal (audio port)	IO	K6
I2S.DIN	Data receive (audio port)	I	K4
I2S. DOUT	Data transmit (audio port)	O	K3
CLK256FS	Synchronization frame sync to the OMAP3530	O	D13

8.12.3 Audio Output Jack

A single 3.5mm jack is provided on BeagleBoard to support external stereo audio output devices such as headphones and powered speakers.

8.12.4 Audio Input Jack

A single 3.5mm jack is supplied to support external audio inputs including stereo or mono.

8.13 DVI-D Interface

The LCD interface on the **OMAP3530** is accessible from the **DVI-D** interface connector on the board. **Figure 40** is the DVI-D interface design.

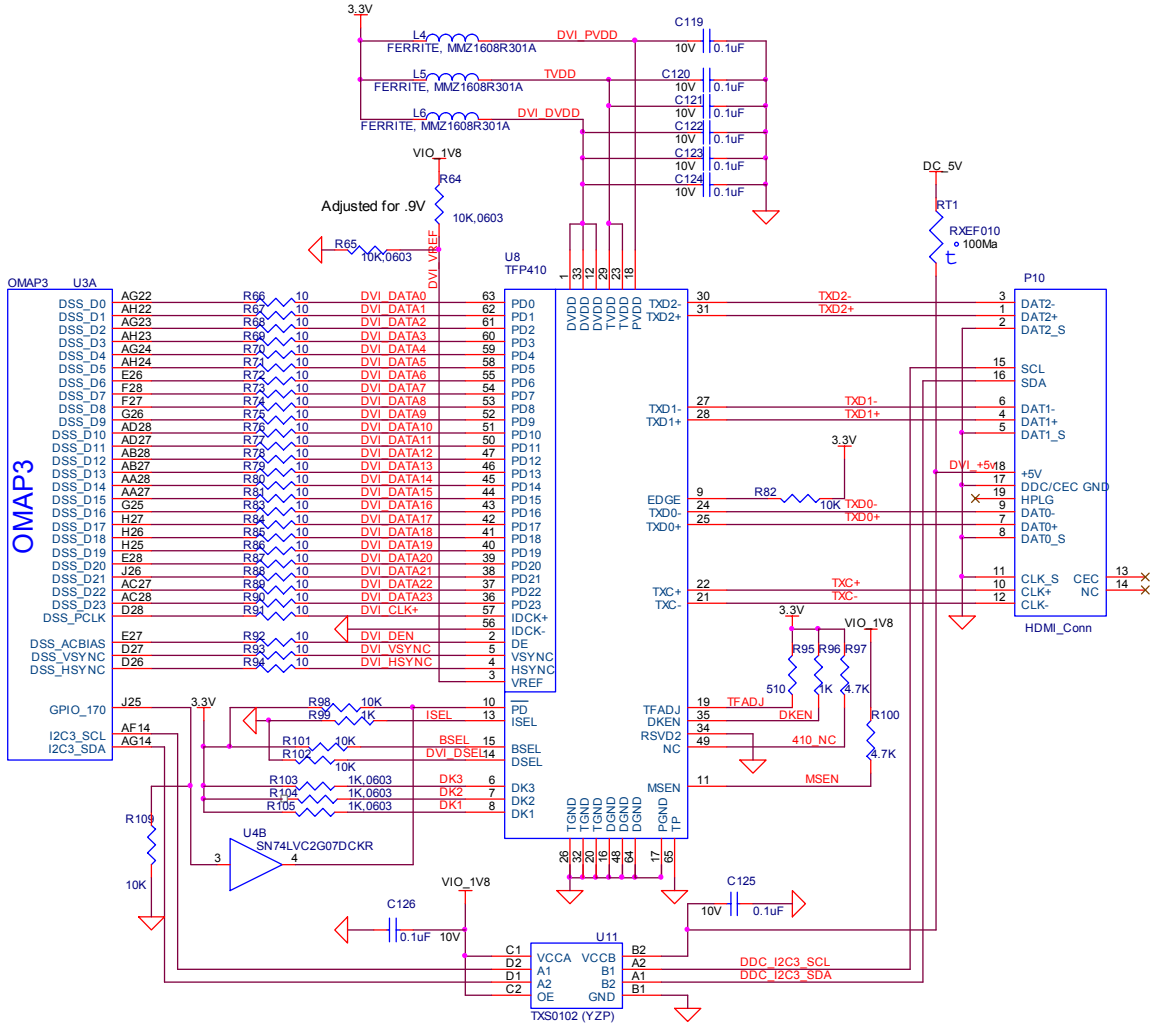

Figure 40. DVI-D Interface

8.13.1 OMAP3530 LCD Interface

The main driver for the DVI-D interface originates at the **OMAP3530** via the **DSS** pins. The OMAP3530 provides 24 bits of data to the DVI-D framer chip, **TFP410**. There are three other signals used to control the DVI-D that originate at the **OMAP3530**. These are I2C3_SCL, I2C3_SDA, and GPIO_170. All of the signals used are described in **Table 14.**

Table 14. OMAP3530 LCD Signals

Signal Name	Description		Type	Ball
dss_pclk	LCD Pixel Clock		O	D28
dss_hsync	LCD Horizontal Synchronization		O	D26
dss_vsync	LCD Vertical Synchronization		O	D27
dss_acbias	Pixel data enable (TFT) output		O	E27
dss_data0	LCD Pixel Data bit 0	BLUE0	O	AG22
dss_data1	LCD Pixel Data bit 1	BLUE1	O	AH22
dss_data2	LCD Pixel Data bit 2	BLUE2	O	AG23
dss_data3	LCD Pixel Data bit 3	BLUE3	O	AH23
dss_data4	LCD Pixel Data bit 4	BLUE4	O	AG24
dss_data5	LCD Pixel Data bit 5	BLUE5	O	AH24
dss_data6	LCD Pixel Data bit 6	BLUE6	O	E26
dss_data7	LCD Pixel Data bit 7	BLUE7	O	F28
dss_data8	LCD Pixel Data bit 8	GREEN0	O	F27
dss_data9	LCD Pixel Data bit 9	GREEN1	O	G26
dss_data10	LCD Pixel Data bit 10	GREEN2	O	AD28
dss_data11	LCD Pixel Data bit 11	GREEN3	O	AD27
dss_data12	LCD Pixel Data bit 12	GREEN4	O	AB28
dss_data13	LCD Pixel Data bit 13	GREEN5	O	AB2
dss_data14	LCD Pixel Data bit 14	GREEN6	O	AA28
dss_data15	LCD Pixel Data bit 15	GREEN7	O	AA27
dss_data16	LCD Pixel Data bit 16	RED0	O	G25
dss_data17	LCD Pixel Data bit 17	RED1	O	H27
dss_data18	LCD Pixel Data bit 18	RED2	O	H26
dss_data19	LCD Pixel Data bit 19	RED3	O	H25
dss_data20	LCD Pixel Data bit 20	RED4	O	E28
dss_data21	LCD Pixel Data bit 21	RED5	O	J26
dss_data22	LCD Pixel Data bit 22	RED6	O	AC27
dss_data23	LCD Pixel Data bit 23	RED7	O	AC28
GPIO_170	Powers down the TFP410 when Lo. TFP410 is active when Hi.		O	J25
I2C3_SCL	I2C3 clock line. Used to communicate with the monitor to determine setting information.		I/O	AF14
I2C3_SDA	I2C3 data line. Used to communicate with the monitor to determine setting information.		I/O	AG14

10ohm series resistors are provide in the signal path to minimize reflections in the high frequency signals from the **OMAP3530** to the **TFP410**. These resistors are in the form of resistor packs on the BeagleBoard. The maximum clock frequency of these signals is 65MHz.

8.13.2 OMAP3530 LCD Power

In order for the DSS outputs to operate correctly out of the **OMAP3530**, two voltage rails must be active, **VIO_1V8 and VDD_PLL2**. Both of these rails are controlled by the **TPS65950** and must be set to 1.8V. By default, **VDD_PLL2** is not turned and must be activated by SW. Otherwise some of the bits will not have power supplied to them.

8.13.3 TFP410 Framer

The **TFP410** provides a universal interface to allow a glue-less connection to provide the DVI-D digital interface to drive external LCD panels. The adjustable 1.1-V to 1.8-V digital interface provides a low-EMI, high-speed bus that connects seamlessly with the 1.8V and 24-bit interface output by the **OMAP3530**. The DVI interface on the BeagleBoard supports flat panel display resolutions up to XGA at 65 MHz in 24-bit true color pixel format.

Table 15 is a description of all of the interface and control pins on the **TFP410** and how they are used on BeagleBoard.

Table 15. TFP410 Interface Signals

Signal Name	Description	Type	Ball
DATA[23:12]	The upper 12 bits of the 24-bit pixel bus.	I	36–47
DATA[11:0]	The bottom 12 bits of the 24-bit pixel bus.	I	50–55.56-53
IDCK+	Single ended clock input.	I	57
IDCK-	Tied to ground to support the single ended mode.	I	56
DE	Data enable. During active video (DE = high), the transmitter encodes pixel data, DATA[23:0]. During the blanking interval (DE = low), the transmitter encodes HSYNC and VSYNC.	I	2
HSYNC	Horizontal sync input	I	4
VSYNC	Vertical sync input	I	5
DK3	These three inputs are the de-skew inputs DK[3:1], used to adjust the setup and hold times of the pixel data inputs DATA[23:0], relative to the clock input IDCK±.	I	6
DK2		I	7
DK1		I	8
MSEN	A low level indicates a powered on receiver is detected at the differential outputs. A high level indicates a powered on receiver is not detected.	O	11
ISEL	This pin disables the I2C mode on chip. Configuration is specified by the configuration pins (BSEL, DSEL, EDGE, VREF) and state pins (PD, DKEN).	I	13
BSEL	Selects the 24bit and single-edge clock mode.	I	13
DSEL	Lo to select the single ended clock mode.	I	14
EDGE	A high level selects the primary latch to occur on the rising edge of the input clock IDCK	I	9
DKEN	A HI level enables the de-skew controlled by DK[1:3]	I	35
VREF	Sets the level of the input signals from the OMAP3530.	I	3
PD	A HI selects normal operation and a LO selects the powerdown mode.	I	10
TGADJ	This pin controls the amplitude of the DVI output voltage swing, determined by the value of the pullup resistor RTFADJ connected to 3.3V.	I	19

8.13.4 TFP410 Power

Power to the TFP410 is supplied from the 3.3V regulator in **U1**, the **TPS2141**. In order to insure a noise free signal, there are three inductors, **L4**, **L5**, and **L6** that are used to filter the 3.3V rail into the TFP410.

8.13.5 TFP410 Control Pins

There are twelve control pins that set up the TFP410 to operate with the **OMAP3530**. Most of these pins are set by HW and do not require any intervention by the **OMAP3530** to set them.

8.13.5.1 ISEL

The **ISEL** pin is pulled LO via **R99** to place the TFP410 in the control pin mode with the I2C feature disabled. This allows the other modes for the TFP410 to be set by the other control pins.

8.13.5.2 BSEL

The **BSEL** pin is pulled HI to select the 24 bit mode for the Pixel Data interface from the OMAP3530.

8.13.5.3 DSEL

The **DSEL** pin is pulled low to select the single ended clock mode from the **OMAP3530**.

8.13.5.4 EDGE

The **EDGE** signal is pulled HI through **R82** to select the rising edge on the IDCK+ lead which is the pixel clock from the **OMAP3530**.

8.13.5.5 DKEN

The **DKEN** signal is pulled HI to enable the de-skew pins. The de-skew pins, **DK1-DK3,** are pulled low by the internal pulldown resistors in the **TFP410**. This is the default mode of operation. If desired, the resistors can be installed to pull the signals high. However, it is not expected that any of the resistors will need to be installed. The DK1-DK3 pins adjust the timing of the clock as it relates to the data signals.

8.13.5.6 MSEN

The **MSEN** signal, when low, indicates that there is a powered monitor plugged into the DVI-D connector. This signal is not connected to the **OMAP3530** and is provided as a test point only.

8.13.5.7 VREF

The **VREF** signal sets the voltage level of the **DATA**, **VSYNC**, **HSYNC**, **DE**, and **IDCK+** leads from the OMAP3530. As the **OMAP3530** is 1.8V, the level is set to .9V by **R64** and **R65**.

8.13.5.8 PD

The **PD** signal originates from the **OMAP3530** on the **GPIO_170** pin. Because the **P**D signal on the **TFP410** is 3.3V referenced, this signal must be converted to **3.3V**. This is done by **U4**, **SN74LVC2G07**, a non-inverting open drain buffer. If the **GPIO_170** pin is HI, then the open drain signal is inactive, causing the signal to be pulled HI by **R98**. When **GPIO_170** is taken low, the output of **U4** will also go LO, placing the **TFP410** in the power down mode. Even though **U4** is running at 1.8V to match the **OMAP3530**, the output will support being pulled up to **3.3V**. On power up, the TFP410 is disabled by **R109**, a 10K resistor. When the **OMAP3530** powers on, pin **J25** comes in the safe mode, meaning it is not being driven. **R109** insures that the signal is pulled LO, putting the TFP410 in the power down mode.

8.13.5.9 TFADJ

The **TFADJ** signal controls the amplitude of the DVI output voltage swing, determined by the value of **R95**.

8.13.5.10 RSVD2

This unused pin is terminated to ground as directed by the TFP410 data manual.

8.13.5.11 NC

This unused pin is pulled HI as directed by the TFP410 data manual.

8.13.6 DVI-D Connector

In order to minimize board size, a HDMI connector was selected for the DVI-D connection. The BeagleBoard does not support HDMI but only the DVI-D component of HDMI. The Cable is not supplied with the BeagleBoard but is available from numerous cable suppliers and is required to connect a display to the BeagleBoard.

8.13.6.1 Shield Wire

Each signal has a shield wire that is used in the cable to provide signal protection for each differential pair. This signal is tied directly to ground.

8.13.6.2 DAT0+/DAT0-

The differential signal pair **DAT0+/DAT0-** transmits the 8-bit blue pixel data during active video and HSYNC and VSYNC during the blanking interval.

8.13.6.3 DAT1+/DAT1-

The differential signal pair **DAT1+/DAT1-** transmits the 8-bit green pixel data during active video.

8.13.6.4 DAT2+/DAT2-

The differential signal pair **DAT2+/DAT2-** transmits the 8-bit red pixel data during active.

8.13.6.5 TXC+/TXC-

The differential signal pair **TXC+/TXC-** transmits the differential clock from the TFP410.

8.13.6.6 DDC Channel

The **Display Data Channel** or **DDC (**sometimes referred to as EDID Enhanced Display ID**)** is a digital connection between a computer display and the **OMAP3530** that allows the display specifications to be read by the **OMAP3530**. The standard was created by the Video Electronics Standards Association (VESA). The current version of DDC, called DDC2B, is based on the I²C bus. The monitor contains a read-only memory (ROM) chip programmed by the manufacturer with information about the graphics modes that the monitor can display. This interface in the LCD panel is powered by the +5V pin on the connector through **RT1**, a resetable fuse. As the **OMAP3530** is 1.8V I/O, the I2C bus is level translated by **U11**, a **TXS0102**. It provides for a split rail to allow the signals to interface on both sides of the circuit. Inside of **TXS0102** is a pullup on each signal, removing the need for an external resistor.

8.13.6.7 HDMI Support

The digital portion of the DVI-D interface is compatible with HDMI and is electrically the same. A standard HDMI cable may be used to connect to the HDMI input of monitors or televisions. Whether or not the Beagle will support those monitors is dependent on the timings that are used on the BeagleBoard and those that are accepted by the monitor. This may require a change in the software running on the Beagle. The audio and encryption features of HDMI are not supported by the BeagleBoard.

8.13.6.8 DVI to VGA

The analog portion of DVI which provides RGB analog signals is **not supported** by the BeagleBoard. Buying a DVI to VGA adapter connector will not work on a VGA display. You will need an active DVI-D to VGA adapter. Another option for these signals is to find a board that connects to the J4 and J5 expansion connectors and generates the RGB signals for the VGA display.

8.14 LCD Expansion Headers

Access is provided on the Rev C4 to allow access to the LCD signals. **Table 16** shows the signals that are on the J4 connector. You will notice that the signals are not in a logical order or grouping. This is due to the routing on the PCB where we allowed the routing to take president to get it to route with no addition of layers to the design.

Table 16. J4 LCD Signals

Pin#	Signal	I/O	Description
1	DC_5V	PWR	DC rail from the Main DC supply
2	DC_5V	PWR	DC rail from the Main DC supply
3	DVI_DATA1	O	LCD Pixel Data bit
4	DVI_DATA0	O	LCD Pixel Data bit
5	DVI_DATA3	O	LCD Pixel Data bit
6	DVI_DATA2	O	LCD Pixel Data bit
7	DVI_DATA5	O	LCD Pixel Data bit
8	DVI_DATA4	O	LCD Pixel Data bit
9	DVI_DATA12	O	LCD Pixel Data bit
10	DVI_DATA10	O	LCD Pixel Data bit
11	DVI_DATA23	O	LCD Pixel Data bit
12	DVI_DATA14	O	LCD Pixel Data bit
13	DVI_DATA19	O	LCD Pixel Data bit
14	DVI_DATA22	O	LCD Pixel Data bit
15	I2C3_SDA	I/O	I2C3 Data Line
16	DVI_DATA11	O	LCD Pixel Data bit
17	DVI_VSYNC	O	LCD Vertical Sync Signal
18	DVI_PUP	O	Control signal for the DVI controller. When Hi, DVI is enabled. Can be used to activate circuitry on adapter board if desired.
19	GND	PWR	Ground bus
20	GND	PWR	Ground bus

The current available on the DC_5V rail is limited to the available current that remains from the DC supply that is connected to the DC power jack on the board. Keep in mind that some of that power is needed by the USB Host power rail and if more power is

needed for the expansion board, the main DC power supply current capability may need to be increased. All signals are 1.8V except the DVI_PUP which is a 3.3V signal.

Table 17 shows the signals that are on connector J5.

Table 17. J5 LCD Signals

Pin#	Signal	I/O	Description
1	3.3V	PWR	3.3V reference rail
2	VIO_1V8	PWR	1.8V buffer reference rail.
3	DVI_DATA20	O	LCD Pixel Data bit
4	DVI_DATA21	O	LCD Pixel Data bit
5	DVI_DATA17	O	LCD Pixel Data bit
6	DVI_DATA18	O	LCD Pixel Data bit
7	DVI_DATA15	O	LCD Pixel Data bit
8	DVI_DATA16	O	LCD Pixel Data bit
9	DVI_DATA7	O	LCD Pixel Data bit
10	DVI_DATA13	O	LCD Pixel Data bit
11	DVI_DATA8	O	LCD Pixel Data bit
12	NC		No connect
13	DVI_DATA9		LCD Pixel Data bit
14	I2C3_SCL	I/O	I2C3 Clock Line
15	DVI_DATA6	O	LCD Pixel Data bit
16	DVI_CLK+	O	DVI Clock
17	DVI_DEN	O	Data Enable
18	DVI_HSYNC	O	Horizontal Sync
19	GND	PWR	Ground bus
20	GND	PWR	Ground bus

The 1.8V rail is for level translation only and should not be used to power circuitry on the board. The 3.3V rail also has limited capacity on the power as well. If the **TFP410** is disabled on the Beagle, then 80mA is freed up for use on an adapter card connected to the LCD signals connectors. It is not required that the **TFP410** be disabled when running an adapter card, but the power should be taken into consideration when making this decision.

It is suggested that the 5V rail be used to generate the required voltages for an adapter card.

8.15 S-Video

A single S-Video port is provided on the BeagleBoard. **Figure 41** is the design of the S-Video interface.

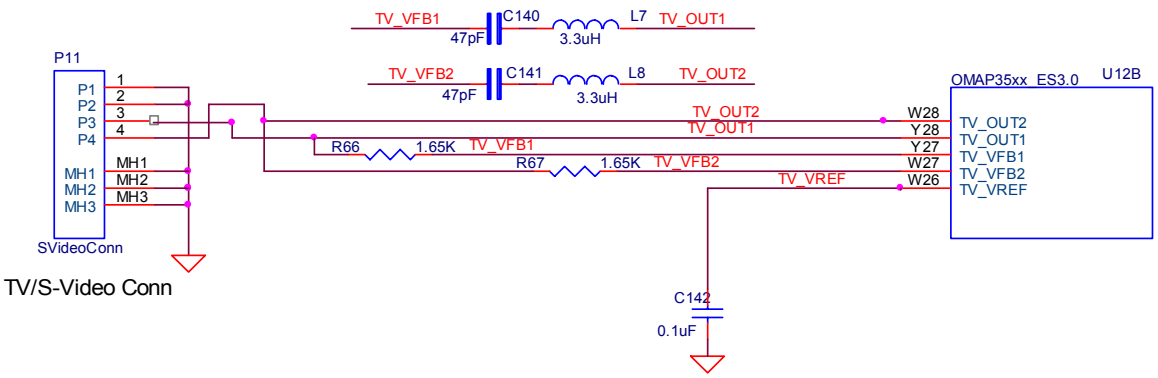

Figure 41. S-Video Interface

Table 18 is the list of the signals on the S-Video interface and their definitions.

Table 18. S-Video Interface Signals

Signal	I/O	Description
tv_out1	O	TV analog output composite
tv_out2	O	TV analog output S-VIDEO
tv_vref	I	Reference output voltage from internal bandgap
tv_vfb1	O	Amplifier feedback node
tv_vfb2	O	Amplifier feedback node

Power to the internal DAC is supplied by the **TPS65950** via the **VDAC_1V8** rail. **Figure 37** reflects the filtering that is used on these rails, including the input VBAT rail.
A **47pf** CAP and **3.3uh** inductor are across the feedback resistors to improve the quality of the S-Video signal.

8.16 RS232 Port

A single RS232 port is provided on the BeagleBoard and provides access to the TX and RX lines of **UART3** on the OMAP3530. **Figure 42** shows the design of the RS232 port.

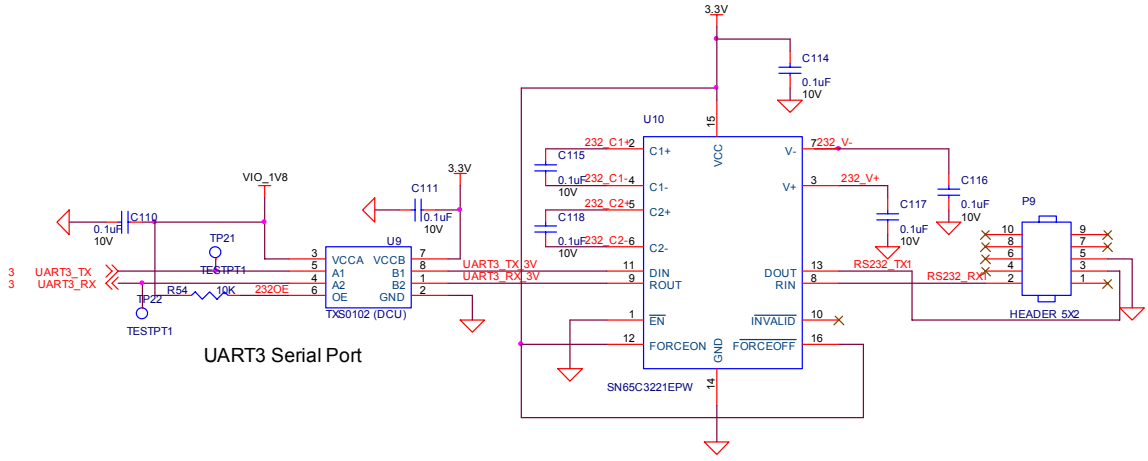

Figure 42. RS232 Interface Design

8.16.1 OMAP3530 Interface

Two lines, **UART3_Tx** and **UART3_Rx**, are provided by the **OMAP3530**. The **UART3** function contains a programmable baud generator and a set of fixed dividers that divide the 48-MHz clock input down to the expected baud rate and also supports auto bauding.

8.16.2 OMAP3530 Level Translator

All of the I/O levels from the **OMAP3530** are **1.8V** while the transceiver used runs at 3.3V. This requires that the voltage levels be translated. This is accomplished by the **TXS0102** which is a two-bit noninverting translator that uses two separate configurable power-supply rails. The A port tracks VCCA, 1.8V and the B port tracks VCCB, 3.3V. This allows for low-voltage bidirectional translation between the two voltage nodes. When the output-enable (OE) input is low, all outputs are placed in the high-impedance state. In this design, the OE is tied high via a 10K ohm resistor to insure that it is always on.

8.16.3 RS232 Transceiver

The RS232 transceiver used is the **SN65C322** which consists of one line driver, one line receiver, and a dual charge-pump circuit with ±15-kV IEC ESD protection pin to pin (serial-port connection pins, including GND). These devices provide the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a

single 3-V to 5.5-V supply. The **SN65C3221** operates at data signaling rates up to 1 Mbit/s and a driver output slew rate of 24 V/ms to 150 V/ms. While the **OMAP3530** can easily drive a 1Mbit/S rate, your results may vary based on cabling, distance, and the loads and drive capability on the other end of the RS232 port.

The transceiver is powered from the 3.3V rail and is active at power up. This allows the port to be used for UART based peripheral booting over the port.

8.16.4 Connector

Access to the RS232 port is through a 10pin header, **P9**. Connection to the header is through a 10 pin IDC to 9 pin D-sub cable. This header requires the use of an **ATI-Everex** type cable. This is the only cable that will work. This cable is readily available from a number of sources and is commonly found on many PC motherboards and is not supplied with the BeagleBoard. **Figure 43** is a picture of what the cable assembly looks like.

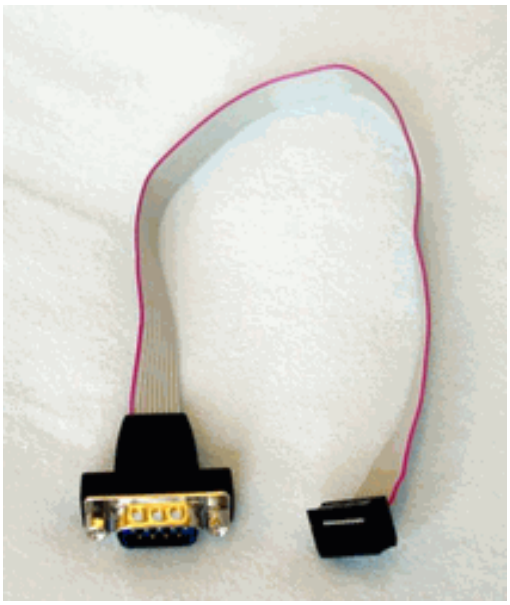

Figure 43. RS232 Cable

When purchasing, make sure the ATI-Everex or pass through cable is ordered.

8.17 Indicators

There are four green indicators on the BeagleBoard:

- Power
- PMU_STAT
- USER0
- USER1

Three of these are programmable under software control and the fourth one is tied to the main power rail. **Figure 44** shows the connection of all of these indicators.

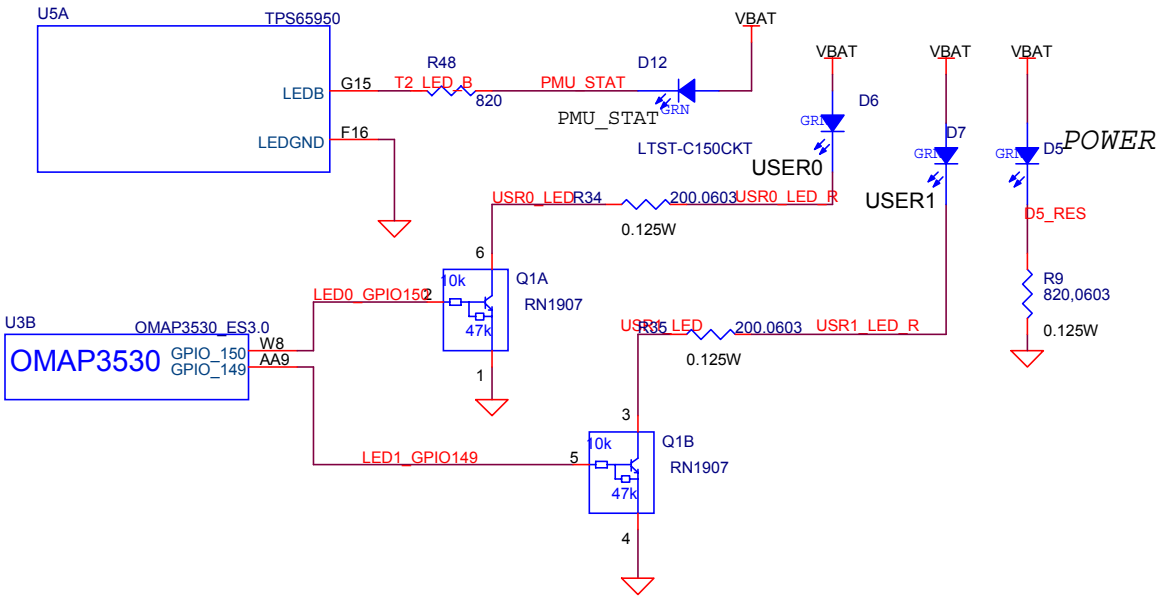

Figure 44. Indicator Design

8.17.1 Power Indicator

This indicator, **D7**, connects across the **VBAT** supply and ground. It indicates that the entire power path is supplying the power to the board. The **VBAT** regulator can be driven from either the USB Client port or an external 5VDC power supply. Indicator **D7** does not indicate which power source is being used to supply the main power to the board but only that it is active.

8.17.2 PMU Status Indicator

This output is driven from the **TPS65950** using the **LED.B** output. The **TPS65950** provides LED driver circuitry to power two LED circuits that can provide user indicators. The first circuit can provide up to 160 mA and the second, 50 mA. Each LED circuit is independently controllable for basic power (on/off) control and illumination level (using PWM). The second driver, **LED.B**, is used to drive an LED that is connected to the VBAT rail through a resistor.

The PWM inside the **TPS65950** can be used to alter the brightness of the LED if desired or it can be turned on or off by the **OMAP3530** using the I2C bus. The PWM is programmable, register-controlled, duty cycle based on a nominal 4-Hz cycle which is

derived from an internal 32-kHz clock. It is possible to set the LED to flash automatically without software control if desired.

8.17.3 User Indicators

There are two user LEDs that can be driven directly from a GPIO pin on the **OMAP3530**. These can be used for any purpose by the software. The output level of the **OMAP3530** is 1.8V and the current sink capability is not enough to drive an LED with any level of brightness. A transistor pair, **RN1907** is used to drive the LEDs from the **VBAT** rail. A logic level of 1 will turn the LED on.

8.18 JTAG

A JTAG header is provided to allow for advanced debugging on the BeagleBoard by using a JTAG based debugger **Figure 45** shows the interconnection to the **OMAP3530** processor.

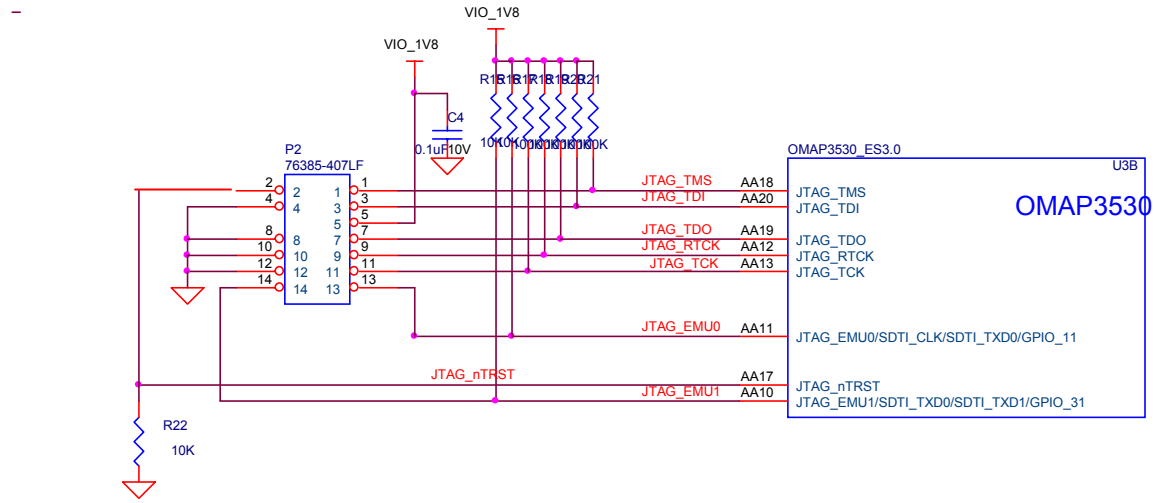

Figure 45. JTAG Interface

8.18.1 OMAP3530 Interface

The JTAG interface connects directly to the OMAP processor. All signals are a 1.8V level. **Table 19** describes the signals on the JTAG connector.

Table 19. JTAG Signals

Signal	Description	I/O
JTAG_TMS	Test mode select	I/O
JTAG_TDI	Test data input	I
JTAG_TDO	Test Data Output	O
JTAG_RTCK	ARM Clock Emulation	O
JTAG_TCK	Test Clock	I
JTAG_nTRST	Test reset	I
JTAG_EMU0	Test emulation 0	I/O
JTAG_EMU1	Test emulation 1	I/O

8.18.2 Connector

The JTAG interface uses a 14 pin connector. All JTAG emulator modules should be able to support this interface. Contact your emulator supplier for further information or if an adapter is needed.

8.19 Expansion Header

The expansion header is provided to allow a limited number of functions to be added to the BeagleBoard via the addition of a daughtercard.

Figure 46 is the design of the expansion connector and the interfaces to the OMAP3530.

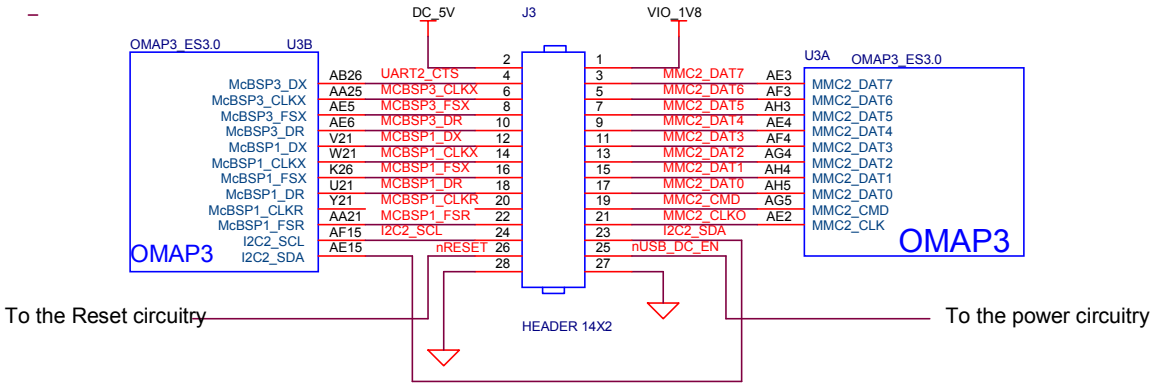

Figure 46. Expansion Header

NOTE: The Expansion header itself is NOT provided on the BeagleBoard. This is user installed option. This header is not populated on the BeagleBoard so that based on the usage scenario the user chooses; it can be populated as needed (Top, Bottom, Top right angle, or Bottom Right angle). The user should take care in installing this header.

CAUTION: The voltage levels on the expansion header are 1.8V. Exposure of these signals to a higher voltage will result in damage to the board and a voiding of the warranty.

8.19.1 OMAP3530 Interface

The main purpose of the expansion connector is to route additional signals from the **OMAP3530** processor. **Table 20** shows all of the signals that are on the expansion header. As the **OMAP3530** has a multiplexing feature, multiple signals can be connected to certain pins to add additional options as it pertains to the signal available. Each pin can be set individually for a different mux mode. This allows any of the listed mux modes to be set on a pin by pin basis by writing to the pin mux register in software. Following is the legend for **Table 20**.

X= there is no signal connected when this mode is selected
Z= this is the safe mode meaning neither input to output. This is the default mode on power up.
***=** this indicates that there is a signal connected when this mode is selected, but it has no useful purpose without other pins being available. Access to these other pins is not provided on the expansion connector.

The first column is the pin number of the expansion connector.

The second column is the pin number of the OMAP3530 processor.

The columns labeled 0-7 represent each of the pin mux modes for that pin. By setting this value in the control register, this signal will be routed to the corresponding pin of the expansion connector. These setting are on a pin by pin basis. Any pin can be set with the mux register setting, and the applicable signal will be routed to the pin on the expansion connector.

Table 20. Expansion Connector Signals

EXP	OMAP	0	1	2	3	4	5	6	7
1		VIO_1V8							
2		DC_5V							
3	AE3	MMC2_DAT7	*	*	*	GPIO_139	*	*	Z
4	AB26	UART2_CTS	McBSP3_DX	GPT9_PWMEVT	X	GPIO_144	X	X	Z
5	AF3	MMC2_DAT6	*	*	*	GPIO_138	*	X	Z
6	AA25	UART2_TX	McBSP3_CLKX	GPT11_PWMEVT	X	GPIO_146	X	X	Z
7	AH3	MMC2_DAT5	*	*	*	GPIO_137	*	X	Z
8	AE5	McBSP3_FSX	UART2_RX	X	X	GPIO_143	*	X	Z
9	AE4	MMC2_DAT4	*	X	*	GPIO_136	X	X	Z
10	AB25	UART2_RTS	McBSP3_DR	GPT10_PWMEVT	X	GPIO_145	X	X	Z
11	AF4	MMC2_DAT3	McSPI3_CS0	X	X	GPIO_135	X	X	Z
12	V21	McBSP1_DX	McSPI4_SIMO	McBSP3_DX	X	GPIO_158	X	X	Z
13	AG4	MMC2_DAT2	McSPI3_CS1	X	X	GPIO_134	X	X	Z
14	W21	McBSP1_CLKX	X	McBSP3_CLKX	X	GPIO_162	X	X	Z
15	AH4	MMC2_DAT1	X	X	X	GPIO_133	X	X	Z
16	K26	McBSP1_FSX	McSPI4_CS0	McBSP3_FSX	x	GPIO_161	X	X	Z
17	AH5	MMC2_DAT0	McSPI3_SOMI	X	X	GPIO_132	X	X	Z
18	U21	McBSP1_DR	McSPI4_SOMI	McBSP3_DR	X	GPIO_159	X	X	Z
19	AG5	MMC2_CMD	McSPI3_SIMO	X	X	GPIO_131	X	X	Z
20	Y21	McBSP1_CLKR	McSPI4_CLK	X	X	GPIO_156	X	X	Z
21	AE2	MMC2_CLKO	McSPI3_CLK	X	X	GPIO_130	X	X	Z
22	AA21	McBSP1_FSR	X	*	Z	GPIO_157	X	X	Z
23	AE15	I2C2_SDA	X	X	X	GPIO_183	X	X	Z
24	AF15	I2C2_SCL	X	X	X	GPIO_168	X	X	Z
25	25	REGEN							
26	26	nRESET							
27	27	GND							
28	28	GND							

8.19.2 Expansion Signals

This section provides more detail on each of the signals available on the expansion connector. They are grouped by functions in **Table 21** along with a description of each signal and the MUX setting to activate the pin. If you use these signals in their respective groups and that is the only function you use, all of the signals are available. Whether or not the signals you need are all available, depends on the muxing function on a per-pin basis. Only one signal per pin is available at any one time.

Table 21. Expansion Connector Signal Groups

Signal	Description	I/O	EXP	OMAP	Mux
SD/MMC Port 2					
MMC2_DAT7	SD/MMC data pin 7.	I/O	3	AE3	1
MMC2_DAT6	SD/MMC data pin 6.	I/O	5	AF3	1
MMC2_DAT5	SD/MMC data pin 5.	I/O	7	AH3	1
MMC2_DAT4	SD/MMC data pin 4.	I/O	9	AE4	1
MMC2_DAT3	SD/MMC data pin 3.	I/O	11	AF4	1
MMC2_DAT2	SD/MMC data pin 2.	I/O	13	AG4	1
MMC2_DAT1	SD/MMC data pin 1.	I/O	15	AH4	1
MMC2_DAT0	SD/MMC data pin 0.	I/O	17	AH5	1
MMC2_CMD	SD/MMC command signal.	I/O	19	AG5	1
MMC_CLKO	SD/MMC clock signal.	O	21	AE2	1
McBSP Port 1					
McBSP1_DR	Multi channel buffered serial port receive	I	18		
McBSP1_CLKS	----------	N/A	N/A		
McBSP1_FSR	Multi channel buffered serial port transmit frame sync RCV	I/O	22		
McBSP1_DX	Multi channel buffered serial port transmit	I/O	12		
McBSP1_CLKX	Multi channel buffered serial port transmit clock	I/O	14		
McBSP1_FSX	Multi channel buffered serial port transmit frame sync XMT	I/O	16		
McBSP1_CLKR	Multi channel buffered serial port receive clock	I/O	20		
I2C Port 2					
I2C2_SDA	I2C data line.	IOD	23		
I2C2_SCL	I2C clock line	IOD	24		
McBSP Port 3					
McBSP3_DR	Multi channel buffered serial port receive	I	10,18		
McBSP3_DX	Multi channel buffered serial port transmit	I/O	4,12		
McBSP3_CLKX	Multi channel buffered serial port receive clock	I/O	6,14		
McBSP3_FSX	Multi channel buffered serial port frame sync transmit	I/O	8,16		
General Purpose I/O Pins					
GPIO_130	GP Input/Output pin. Can be used as an interrupt pin.	I/O	21		
GPIO_131	GP Input/Output pin. Can be used as an interrupt pin.	I/O	19		
GPIO_132	GP Input/Output pin. Can be used as an interrupt pin.	I/O	17		
GPIO_133	GP Input/Output pin. Can be used as an interrupt pin.	I/O	15		
GPIO_134	GP Input/Output pin. Can be used as an interrupt pin.	I/O	13		
GPIO_135	GP Input/Output pin. Can be used as an interrupt pin.	I/O	11		
GPIO_136	GP Input/Output pin. Can be used as an interrupt pin.	I/O	9		
GPIO_137	GP Input/Output pin. Can be used as an interrupt pin.	I/O	7		
GPIO_138	GP Input/Output pin. Can be used as an interrupt pin.	I/O	5		
GPIO_139	GP Input/Output pin. Can be used as an interrupt pin.	I/O	3		
GPIO_143	GP Input/Output pin. Can be used as an interrupt pin.	I/O	8		
GPIO_144	GP Input/Output pin. Can be used as an interrupt pin.	I/O	4		
GPIO_145	GP Input/Output pin. Can be used as an interrupt pin.	I/O	10		
GPIO_146	GP Input/Output pin. Can be used as an interrupt pin.	I/O	6		
GPIO_156	GP Input/Output pin. Can be used as an interrupt pin.	I/O	20		
GPIO_157	GP Input/Output pin. Can be used as an interrupt pin.	I/O	22		
GPIO_158	GP Input/Output pin. Can be used as an interrupt pin.	I/O	12		
GPIO_159	GP Input/Output pin. Can be used as an interrupt pin.	I/O	18		
GPIO_161	GP Input/Output pin. Can be used as an interrupt pin.	I/O	16		
GPIO_162	GP Input/Output pin. Can be used as an interrupt pin.	I/O	14		
GPIO_168	GP Input/Output pin. Can be used as an interrupt pin.	I/O	24		
GPIO_183	GP Input/Output pin. Can be used as an interrupt pin.	I/O	23		
McSPI Port 3					
McSPI3_CS0	Multi channel SPI chip select 0	O	11		
McSPI3_CS1	Multi channel SPI chip select 1	O	13		
McSPI3_SIMO	Multi channel SPI slave in master out	I/O	19		
McSPI3_SOMI	Multi channel SPI slave out master in	I/O	17		
McSPI3_CLK	Multi channel SPI clock	I/O	21		
McSPI Port 4					
McSPI4_SIMO	Multi channel SPI slave in master out	I/O	12		
McSPI4_SOMI	Multi channel SPI slave out master in	I/)	18		
McSPI4_CS0	Multi channel SPI chip select 0	O	16		
McSPI4_CLK	Multi channel SPI clock	I/O	20		
UART Port 2					
UART2_CTS	UART clear to send.	I/O	4		

UART2_RTS	UART request to send	O	10		
UART2_RX	UART receive	I	8		
UART2_TX	UART transmit	O	6		
GPT PWM					
GPT9_PWMEVT	PWM or event for GP timer 9	O	4		
GPT11_PWMEVT	PWM or event for GP timer 11	O	10		
GPT10_PWMEVT	PWM or event for GP timer 10	O	6		

8.19.3 Power

The expansion connector provides two power rails. The first is the **VIO_1.8V** rail which is supplied by the **TPS65950**. This rail is limited in the current it can supply from the **TPS65950** and what remains from the current consumed by the BeagleBoard and is intended to be used to provide a rail for voltage level conversion only. It is not intended to power a lot of circuitry on the expansion board. All signals from the BeagleBoard are at 1.8V.

The other rail is the **DC_5V**. The same restriction exits on this rail as mentioned in the USB section. The amount of available power to an expansion board depends on the available power from the DC supply or the USB supply from the PC.

8.19.4 Reset

The **nRESET** signal is the main board reset signal. When the board powers up, this signal will act as an input to reset circuitry on the expansion board. After power up, a system reset can be generated by the expansion board by taking this signal low. This signal is a 1.8V level signal.

8.19.5 Power Control

There is an additional open-drain signal on the connector called **REGEN**. The purpose of this signal is to provide a means to control power circuitry on the expansion card to turn on and off the voltages. This insures that the power on the expansion board is turned on at the appropriate time. Depending on what circuitry is provided on the expansion board, an additional delay may be needed to be added before the circuitry is activated. Refer to the **OMAP3530** and **TPS65950** documentation for more information.

8.20 Additional Expansion Header

If you choose not to use the LCD headers for access to the LCD signals or for the DVI-D interface, they can also be used for other functions on the board based on the pin mux setting of each pin. **Table 22** shows the options for **J4** and **Table 23** shows the options for **J5**. The MUX: column indicates which MUX mode must be set for each pin to make the respective signals accessible on the pins of the **OMAP3530**.

Table 22. J4 GPIO Signals

Pin#	Signal	MUX:0	MUX:2	MUX:4
3	DVI_DATA1	DATA1	UART1_RTS	GPIO71
4	DVI_DATA0	DATA0	UART1_CTS	GPIO70
5	DVI_DATA3	DATA3	-	GPIO73
6	DVI_DATA2	DATA2	-	GPIO72
7	DVI_DATA5	DATA5	UART3_TX	GPIO75
8	DVI_DATA4	DATA4	UART3_RX	GPIO74
9	DVI_DATA12	DATA12		GPIO82
10	DVI_DATA10	DATA10	-	GPIO79
11	DVI_DATA23	DATA23	-	GPIO93
12	DVI_DATA14	DATA14	-	GPIO84
13	DVI_DATA19	DATA19	McSPI3_SIMO	GPIO89
14	DVI_DATA22	DATA22	McSPI3_CS1	GPIO92
15	I2C3_SDA	I2C3_SDA	-	-
16	DVI_DATA11	DATA11	-	GPIO81
17	DVI_VSYNC	VSYNC	-	GPIO68
18	DVI_PUP	DVI_PUP	-	-

Table 23. J5 GPIO Signals

Pin#	Signal	MUX:0	MUX:2	MUX:4
3	DVI_DATA20	DATA20	McSPI3_SOMI	GPIO90
4	DVI_DATA21	DATA21	McSPI3_CS0	GPIO91
5	DVI_DATA17	DATA17	-	GPIO87
6	DVI_DATA18	DATA18	McSPI3_CLK	GPIO88
7	DVI_DATA15	DATA15	-	GPIO85
8	DVI_DATA16	DATA16	-	GPIO86
9	DVI_DATA7	DATA7	UART1_RX	GPIO77
10	DVI_DATA13	DATA13	-	GPIO83
11	DVI_DATA8	DATA8	-	GPIO78
12	NC	-	-	-
13	DVI_DATA9	DATA9	-	GPIO79
14	I2C3_SCL	I2C3_SCL		-
15	DVI_DATA6	DATA6	UART1_TX	GPIO_76
16	DVI_CLK+	PCLK	-	GPIO66
17	DVI_DEN	DEN	-	GPIO69
18	DVI_HSYNC	HSYNC	-	GPIO67

9.0 Connector Pinouts and Cables

This section provides a definition of the pinouts and cables to be used with all of the connectors and headers on the BeagleBoard.

THERE ARE NO CABLES SUPPLIED WITH THE BEAGLEBOARD.

9.1 Power Connector

Figure 47 is a picture of the BeagleBoard power connector with the pins identified. The supply must have a 2.1mm center hot connector with a 5.5mm outside diameter.

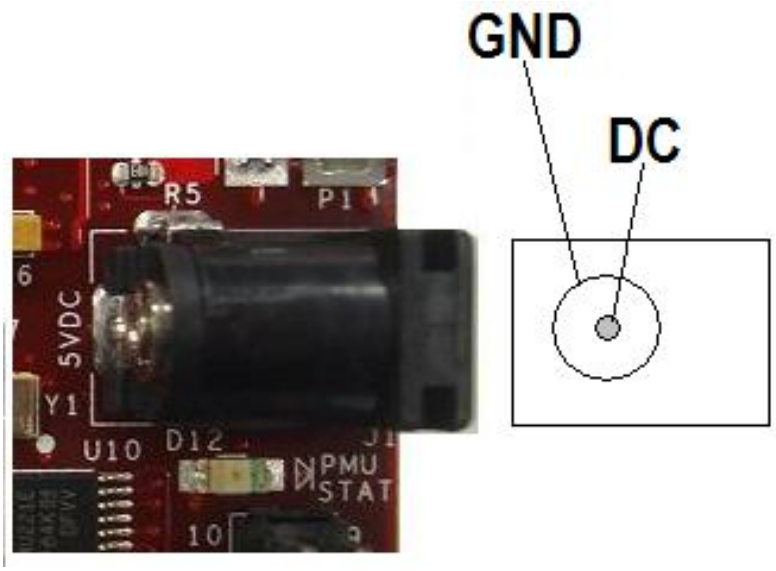

Figure 47. Power Connector

The supply must be at least 500mA with a maximum of 2A. If the expansion connector is used, more power will be required depending on the load of the devices connected to the expansion connector.

WARNING: DO NOT PLUG IN ANYTHING BUT 5V TO THE DC CONNECTOR OR THE BOARD WILL BE DAMAGED!!!!

9.2 USB OTG

Figure 48 is a picture of the BeagleBoard USB OTG connector with the pins identified.

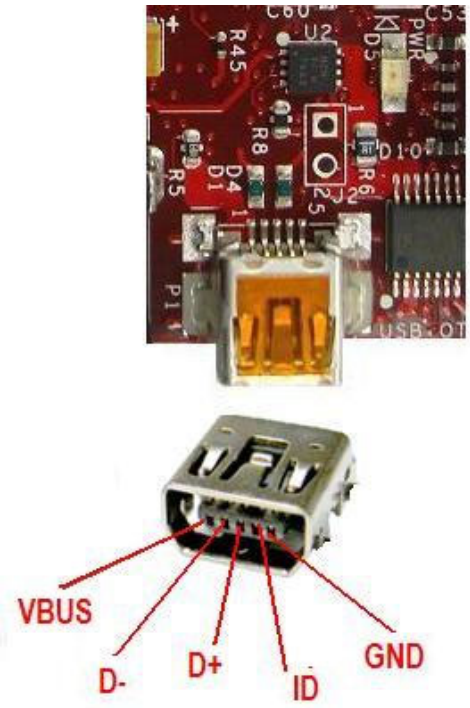

Figure 48. USB OTG Connector

The shorting pads to convert the OTG port to a Host mode are found in **Figure 49**.

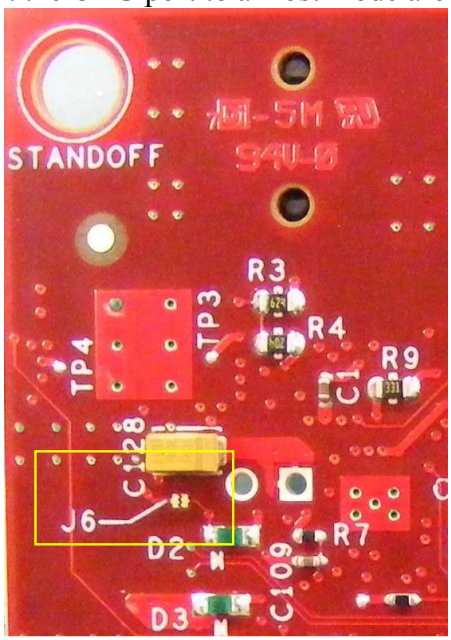

Figure 49. OTG Host Shorting Pads

9.3 S-Video

Figure 50 is the S-Video connector on the BeagleBoard.

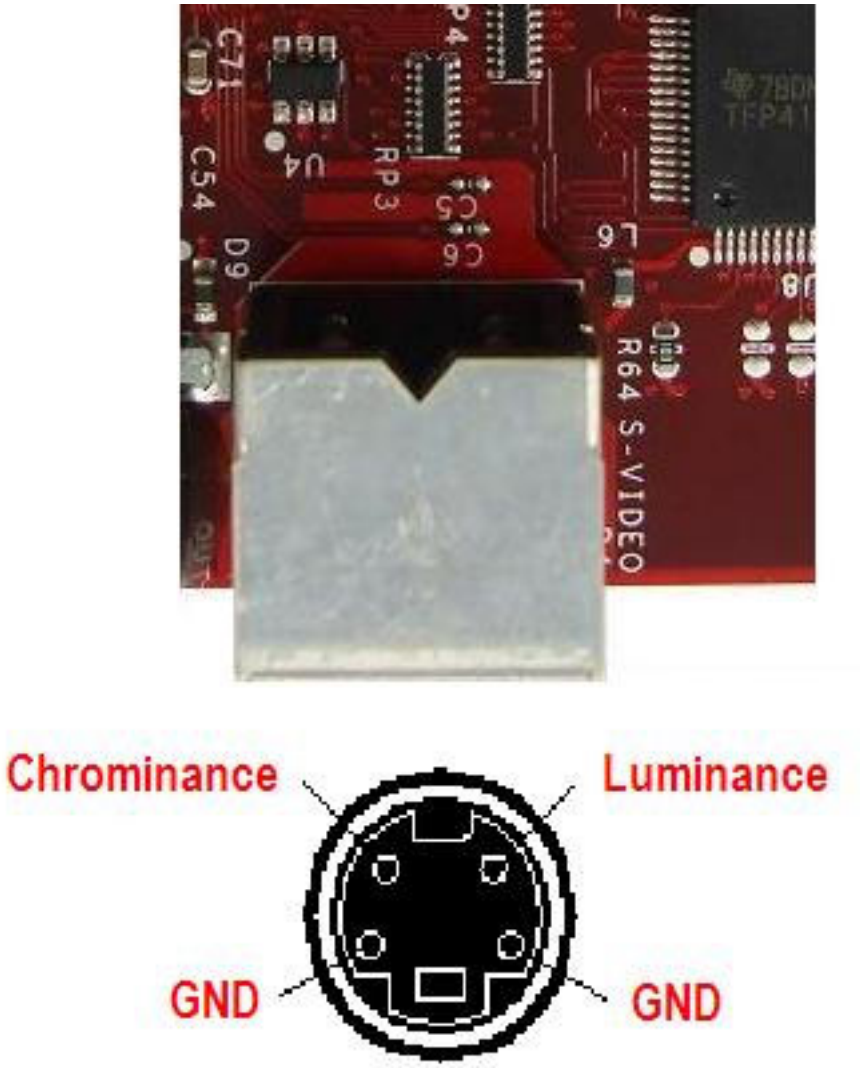

Figure 50. S-Video Connector

9.4 DVI-D

Figure 51 is the pinout of the DVI-D connector on BeagleBoard.

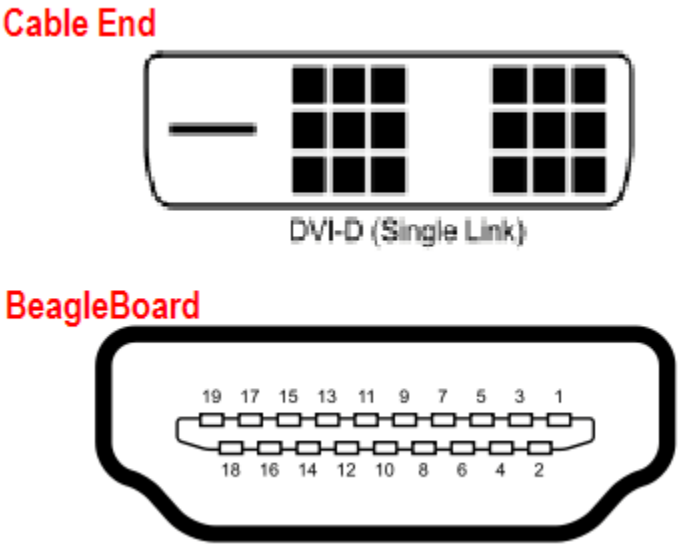

Figure 51. DVI-D Connector

Table 24 is the pin numbering of the two ends of the cable as it relates to the signals used in the DVI-D interface itself.

Table 24. DVI-D to HDMI Cable

SIGNAL	DVI-D PIN#	HDMI PIN#
DATA 2-	1	3
DATA 2+	2	1
SHIELD	3	2
	4	
	5	
DDS CLOCK	6	15
DDS DATA	7	16
	8	
DATA 1-	9	6
DATA 1+	10	4
SHIELD	11	5
	12	
	13	
5V	14	18
GROUND (5V)	15	17
	16	
DATA 0-	17	9
SIGNAL	DVI-D PIN#	DVI-D PIN#
DATA 0+	18	7

SHIELD	19	5
	20	
	21	
	22	
CLOCK+	23	10
CLOCK-	24	12

DO NOT PLUG IN THE DVI-D CONNECTOR TO A DISPLAY WITH THE BEAGLEBAORD POWERED ON. PLUG IN THE CABLE TO THE DISPLAY AND THEN POWER ON THE BEAGLEBOARD.

Figure 52 is the cable to be used to connect to an LCD monitor.

Figure 52. DVI-D Cable

9.5 LCD

This section covers the pair of headers that provide access to the raw 1.8V DSS signals from the OMAP3530 processor. This provides the ability to create adapters for such things as different LCD panels, LVDS interfaces, etc.

9.5.1 Connector Pinout

The **Table 25** and **26** define the pinout of the LCD connectors. All signal levels are 1.8V with the exception of DVI_PUP signal which is 3.3V.

Table 25. J4 LCD Signals

Pin#	Signal	I/O	Description
1	DC_5V	PWR	DC rail from the Main DC supply
2	DC_5V	PWR	DC rail from the Main DC supply
3	DVI_DATA1	O	LCD Pixel Data bit
4	DVI_DATA0	O	LCD Pixel Data bit
5	DVI_DATA3	O	LCD Pixel Data bit
6	DVI_DATA2	O	LCD Pixel Data bit
7	DVI_DATA5	O	LCD Pixel Data bit
8	DVI_DATA4	O	LCD Pixel Data bit
9	DVI_DATA12	O	LCD Pixel Data bit
10	DVI_DATA10	O	LCD Pixel Data bit
11	DVI_DATA23	O	LCD Pixel Data bit
12	DVI_DATA14	O	LCD Pixel Data bit
13	DVI_DATA19	O	LCD Pixel Data bit
14	DVI_DATA22	O	LCD Pixel Data bit
15	I2C3_SDA	I/O	I2C3 Data Line
16	DVI_DATA11	O	LCD Pixel Data bit
17	DVI_VSYNC	O	LCD Vertical Sync Signal
18	DVI_PUP	O	Control signal for the DVI controller. When Hi, DVI is enabled. Can be used to activate circuitry on adapter board if desired.
19	GND	PWR	Ground bus
20	GND	PWR	Ground bus

Table 26. J5 LCD Signals

Pin#	Signal	I/O	Description
1	3.3V	PWR	3.3V reference rail
2	VIO_1V8	PWR	1.8V buffer reference rail.
3	DVI_DATA20	O	LCD Pixel Data bit
4	DVI_DATA21	O	LCD Pixel Data bit
5	DVI_DATA17	O	LCD Pixel Data bit
6	DVI_DATA18	O	LCD Pixel Data bit
7	DVI_DATA15	O	LCD Pixel Data bit
8	DVI_DATA16	O	LCD Pixel Data bit
9	DVI_DATA7	O	LCD Pixel Data bit
10	DVI_DATA13	O	LCD Pixel Data bit
11	DVI_DATA8	O	LCD Pixel Data bit
12	NC		No connect
13	DVI_DATA9		LCD Pixel Data bit
14	I2C3_SCL	I/O	I2C3 Clock Line
15	DVI_DATA6	O	LCD Pixel Data bit
16	DVI_CLK+	O	DVI Clock
17	DVI_DEN	O	Data Enable
18	DVI_HSYNC	O	Horizontal Sync
19	GND	PWR	Ground bus
20	GND	PWR	Ground bus

9.5.2 Connector Suppliers

The actual connector to be used will be determined by the supplier of the board to be plugged into the Beagle. **Table 27** below list a few of the part numbers and suppliers that can be used for the connectors on the LCD interface. All of the listed connectors are in a vertical mount configuration

Table 27. J4 and J5 Connector Sources

Supplier	Header	Socket (Thru Hole)	Socket (SMT)
Major League	TSHC-510-D-06-340-G-LF	SSHS-510-D-04-G-LF	LSSHS-510-D-06-G-LF
“	TSHC-510-D-06-340-T-LF	SSHS-510-D-04-T-LF	LSSHS-510-D-06-T-LF
“	TSHC-510-D-06-340-GT-LF	SSHS-510-D-04-TG-LF	LSSHS-510-D-06-F-LF
“	TSHC-510-D-06-340-H-LF	SSHS-510-D-04-H-LF	
“	TSHC-510-D-06-340-F-LF	SSHS-510-D-04-F-LF	
SAMTEC	FTS-110-01-L-D		FLE-110-01-G-DV
“	FTS-110-03-L-D		
Sullins	GRPB052VWVN-RC		

Major League http://www.mlelectronics.com/
Samtec http://www.samtec.com
Sullins http://www.sullinscorp.com

9.5.3 Dimensions

Figure 53 provides some of the dimensions that can assist in the location of the LCD headers. It is strongly recommended that the CAD data be used in order to determine their location exact. **Table 28** provides the values for each lettered dimension.

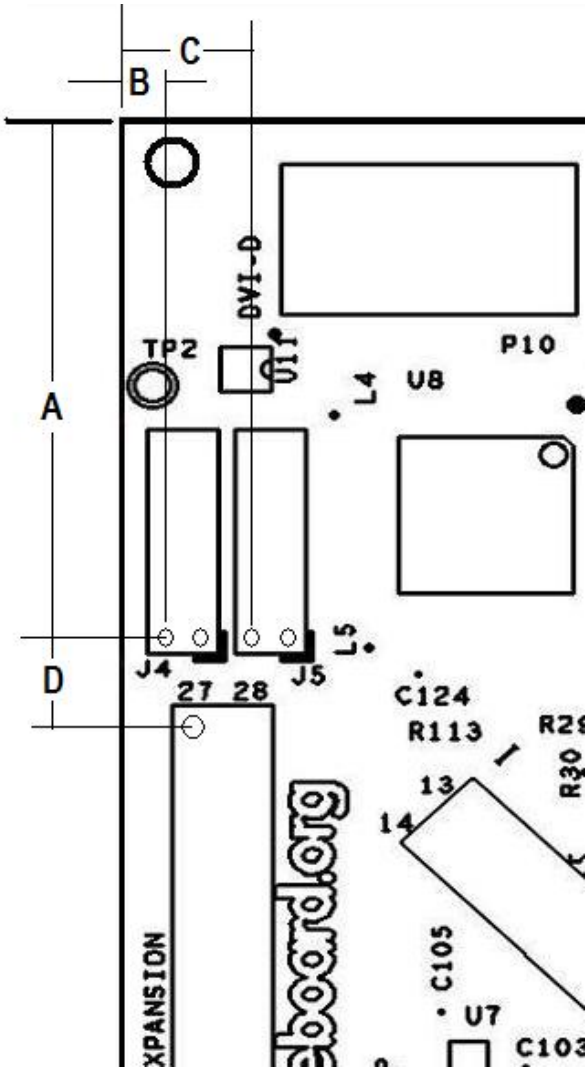

Figure 53. Top Mount LCD Adapter

Table 28. Connector Dimensions

Dimension	Inches	Millimeters
A	1.085	27.56
B	0.118	2.99
C	0.296	7.52
D	0.190	4.83

9.5.4 Mounting Scenarios

This section provides a few possible mounting scenarios for the LCD connectors. It should be noted that the voltage level of these signals are 1.8V. It will require that they be buffered in order to drive other voltage levels.

9.5.4.1 Top Mounting

Figure 54 shows the board being mounted on top of the BeagleBoard.

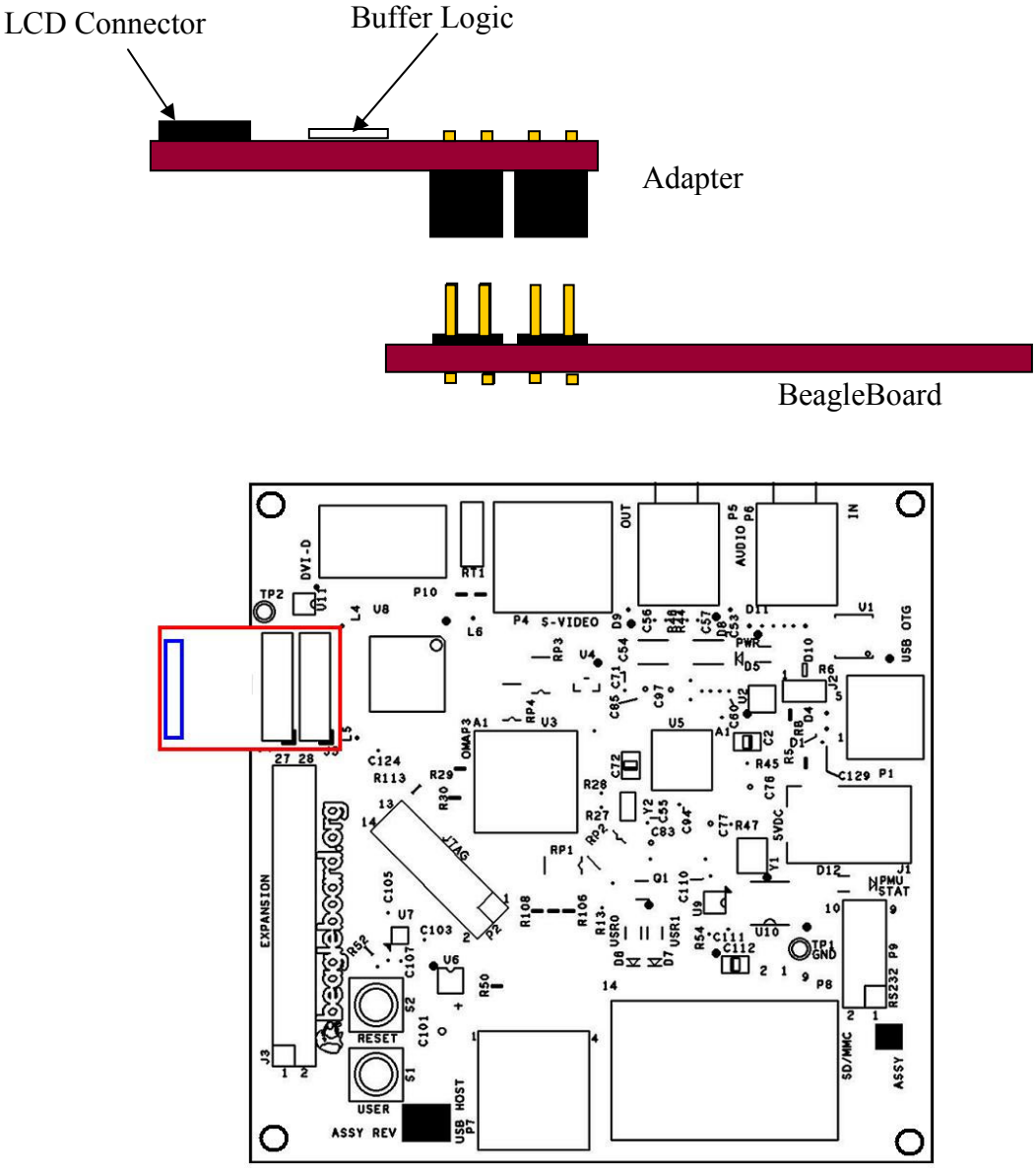

Figure 54. Top Mount LCD Adapter

9.5.4.2 Bottom Mounting

Figure 55 shows the board being mounted under the BeagleBoard.

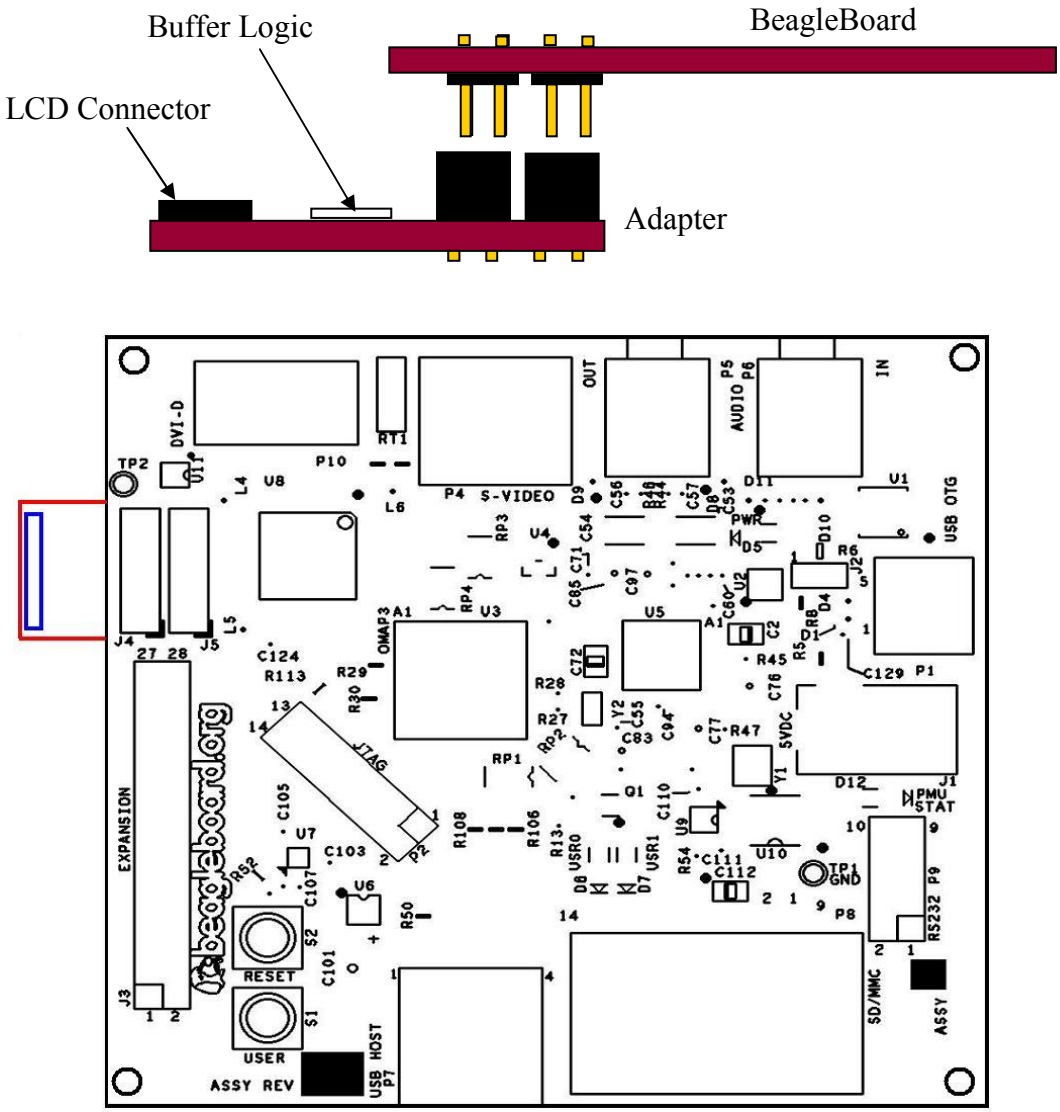

Figure 55. Bottom Mount LCD Adapter

9.6 Audio Connections

Figure 56 is the audio input jack required to connect to the BeagleBoard.

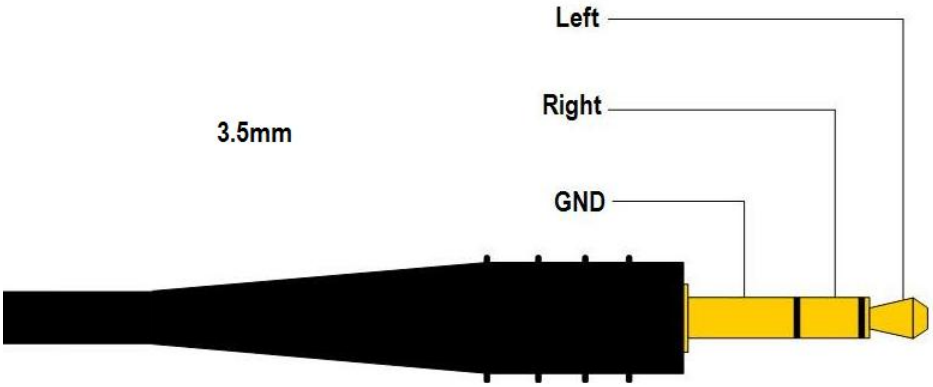

Figure 56. Audio In Plug

Figure 57 is the actual connector used on the BeagleBoard.

Figure 57. Audio In Plug

9.7 Audio Out

Figure 58 is the audio out jack required to connect to the BeagleBoard.

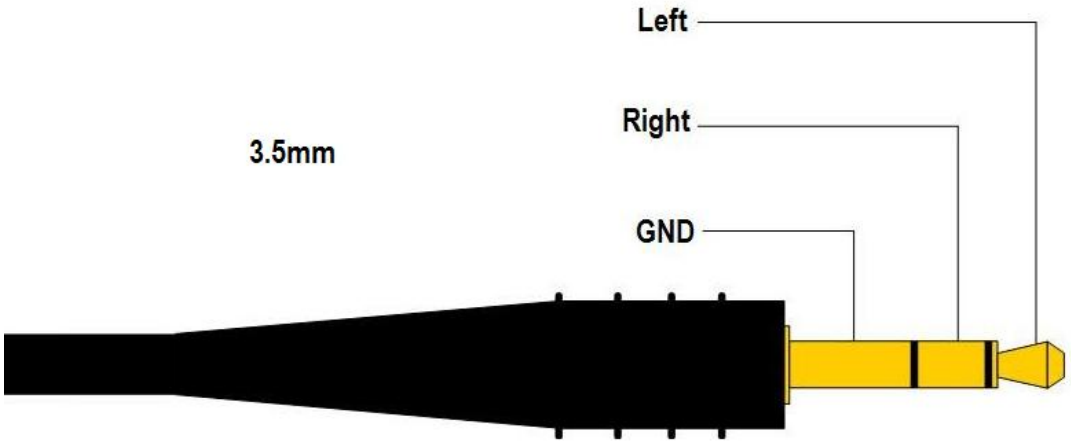

Figure 58. Audio Out Plug

Figure 59 is the actual connector used on the BeagleBoard.

Figure 59. Audio In Plug

9.8 JTAG

Figure 60 is the JTAG connector pin out showing the pin numbering.

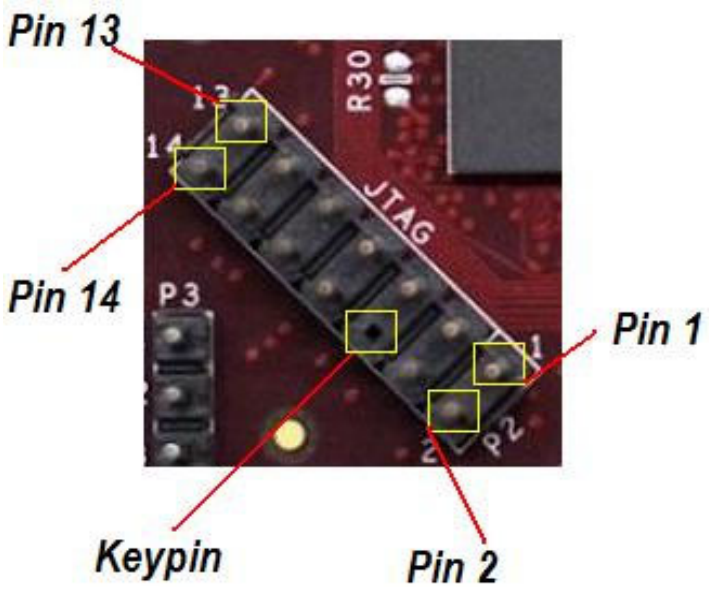

Figure 60. JTAG Connector Pinout

Table 29 gives a definition of each of the signals on the JTAG header.

Table 29. JTAG Signals

Pin	Signal	Description	I/O
1	JTAG_TMS	Test mode select	I/O
3	JTAG_TDI	Test data input	I
7	JTAG_TDO	Test Data Output	O
9	JTAG_RTCK	ARM Clock Emulation	O
11	JTAG_TCK	Test Clock	I
2	JTAG_nTRST	Test reset	I
13	JTAG_EMU0	Test emulation 0	I/O
14	JTAG_EMU1	Test emulation 1	I/O
5	VIO	Voltage pin	PWR
4,8,10,12,14	GND	Ground	PWR

All of the signals are 1.8V only. The JTAG emulator must support 1.8V signals for use on the BeagleBoard.

If a 20 pin connector is provided on the JTAG emulator, then a 20 pin to 14 pin adapter must be used. You may also use emulators that are either equipped with a 14 pin connector or are universal in nature.

Figure 61 shows an example of a 14 pin to 20 pin adapter.

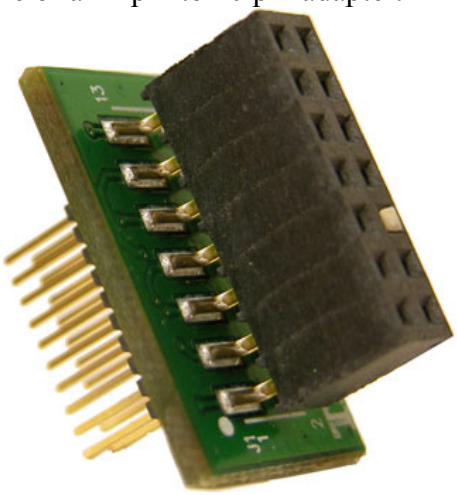

Figure 61. JTAG 14 to 20 Pin Adapter

Figure 62 shows how the JTAG cable is to be routed when connected to the BeagleBoard.

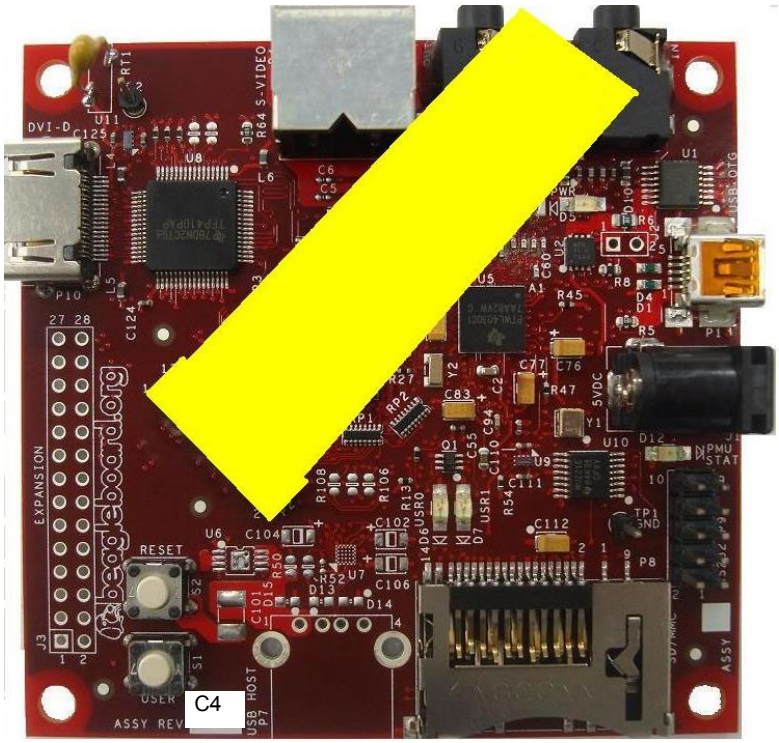

Figure 62. JTAG Connector Pinout

9.9 RS232

Figure 63 is the RS232 header on the BeagleBoard with the pin numbers identified.

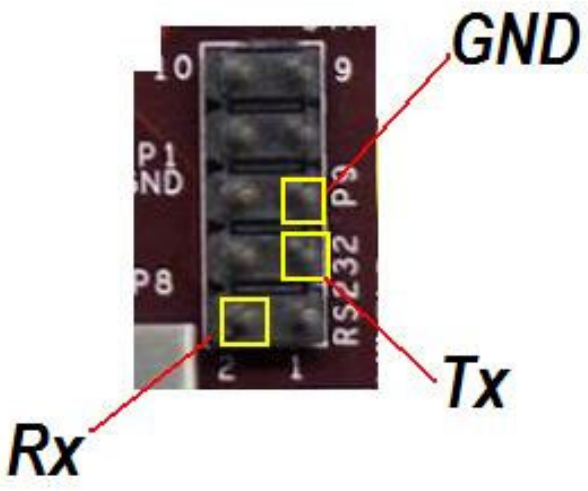

Figure 63. RS232 Header

Figure 64 is the cable that is required in order to access the RS232 header. This cable can be purchased from various sources and is referred to as the ATI/Everex type cable.

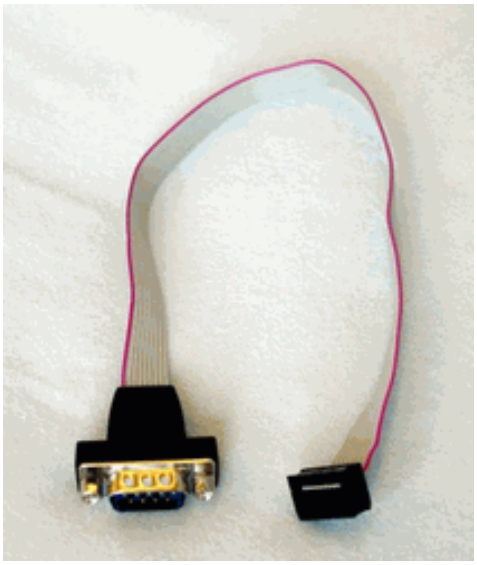

Figure 64. RS232 Flat Cable

9.10 Expansion

We are changing the configuration of the expansion header on all Beagle boards. This will standardize on the configuration for compatibility with expansion cards. The socket will be mounted on the BACKSIDE of the board.

Figure 65 is a drawing and picture of the socket that is specified.

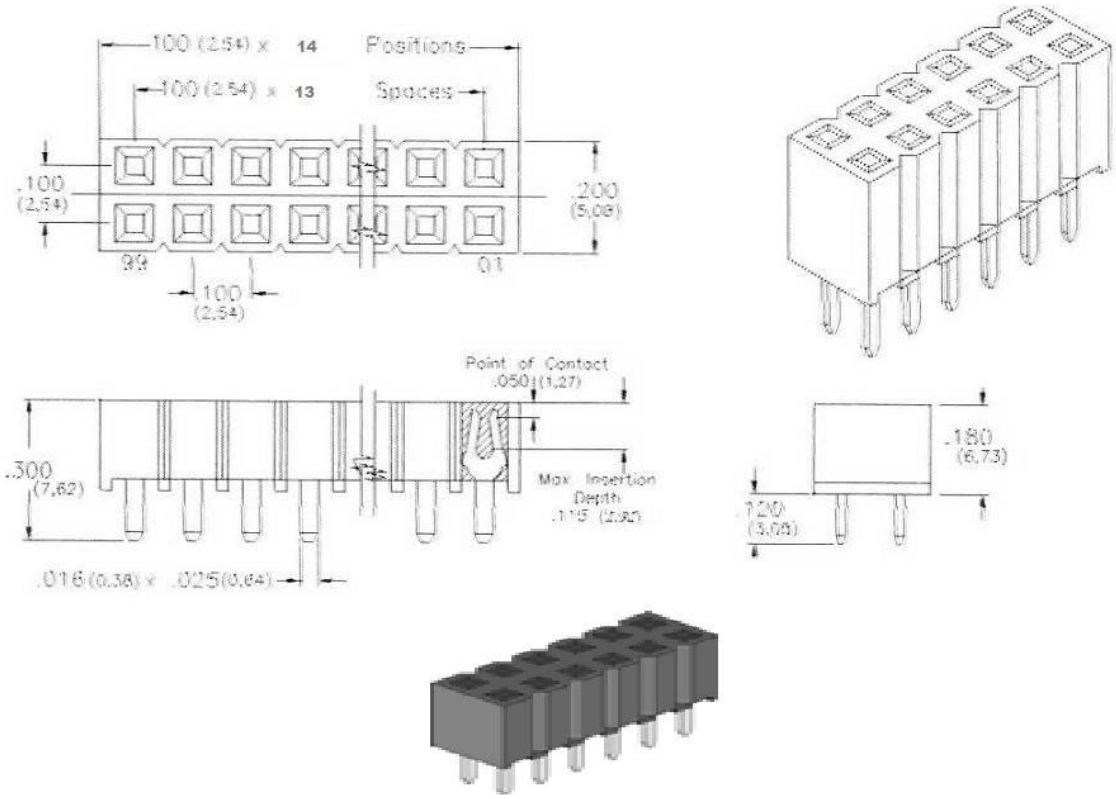

Figure 65. Expansion Sockets

The selected supplier for this socket is Major League Electronics http://www.mlelectronics.com/ and the part number is **LSWSS-114-D-02-T-LF**. Other suppliers may be available as well and can be used as long as it is compatible with this socket. This socket is mounted on the BACK of the BeagleBoard.

9.11 Battery Installation

9.11.1 Battery

The board was designed to use the VL-1220/VCN battery from Panasonic-BSG. This is a Vanadium Pentoxide Lithium Rechargeable Battery with a 7mAH capacity. **Figure 66** is a picture of the battery.

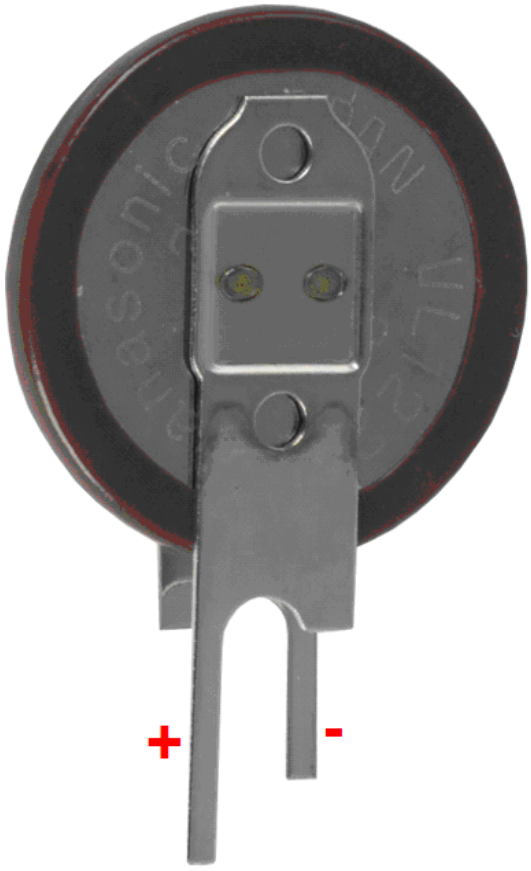

Figure 66. Optional Battery

9.11.2 Battery Installation

THE FOLLOWING STRUCTIONS ASSUME THE USER HAS PREVIOUS EXPERIENCE WITH BATTERIES. BATTERY INSTALLATION IS THE SOLE RESPONSABILTY OF THE USER. INSTALLATION OF THE BATTERY BY THE USER IS AT THEIR OWN RISK. FAILURE TO FOLLOW THE INSTRUCTIONS CAN RESULT IN DAMAGE TO THE BOARD. THIS DAMAGE IS NOT COVERED UNDER THE WARRANTY.

Figure 67 shows the location of the battery on the Beagle Board.

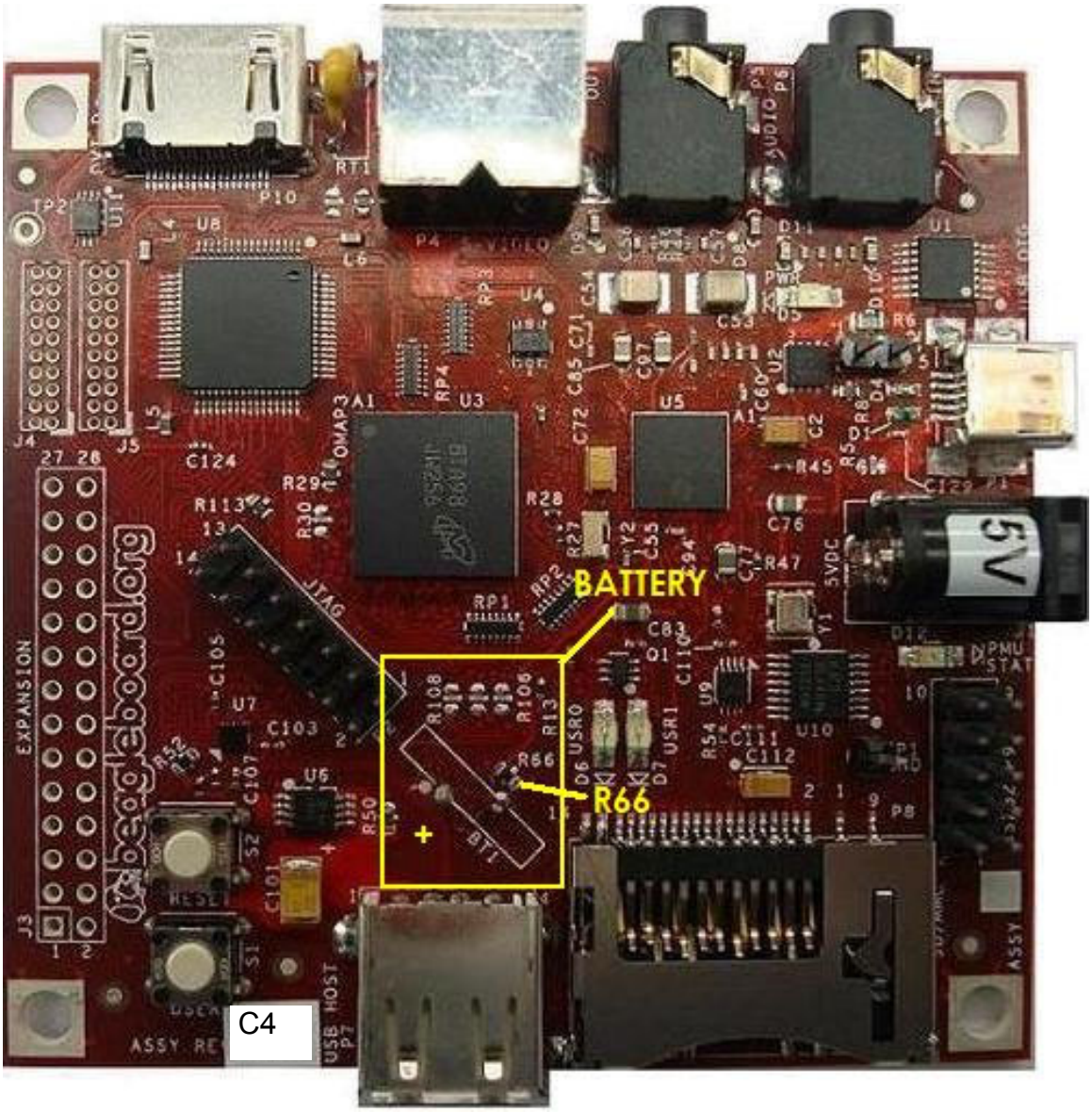

Figure 67. Optional Battery Location

Following are the steps required to install the battery.

1) Remove all cables from the board.
2) Remove R66 from the board as shown on **Figure 67**.
3) Using Figure 66, locate the positive (+) lead of the battery.
4) Insert the (+) lead into the hole that is marked (+) on **Figure 67**.

10.0 BeagleBoard Accessories

Throughout this manual various items are mentioned as not being provided with the standard BeagleBoard package or as options to extend the features of the BeagleBoard. The concept behind BeagleBoard is that different features and functions can be added to BeagleBoard by bringing your own peripherals. This has several key advantages:

- User can choose which peripherals to add.
- User can choose the brand of peripherals based on driver availability and ability to acquire the particular peripheral
- User can add these peripherals at a lower cost than if they were integrated into the BeagleBoard.

This section covers these accessories and add-ons and provides information on where they may be obtained. Obviously things can change very quickly as it relates to devices that may be available. Please check BeagleBoard.org for an up to date listing of these peripherals.

Inclusion of any products in this section does not guarantee that they will operate with all SW releases. It is up to the user to find the appropriate drivers for each of these products. Information provided here is intended to expose the capabilities of what can be done with the BeagleBoard and how it can be expanded.

All pricing information provided is subject to change an din most cases is likely to be lower depending on the products purchased and from where they are purchased.

Covered in this section are the following accessories:

- DC Power Supplies
- Serial Ribbon cable
- USB Hubs
- USB Thumb Drives
- DVI-D Cables
- DVI-D Monitors
- SD/MMC Cards
- USB to Ethernet
- USB to WiFi
- USB Bluetooth
- Expansion Cards

NO CABLES OR POWER SUPPLIES ARE PROVIDED WITH THE BEAGLEBOARD.

10.1 DC Power Supply

Tabletop or wall plug supplies can be used to power BeagleBoard. **Table 30** provides the specifications for the BeagleBoard DC supply. Supplies that provide additional current than what is specified can be used if additional current is needed for add on accessories. The amount specified is equal to that supplied by a USB port.

Table 30. DC Power Supply Specifications

Specification	Requirement	Unit
Voltage	5.0	V
Current	500mA (minimum)	mA
Connector	2.1mm x 5.5mm Center hot	

It is recommended that a supply higher than 500mA be used if higher current peripherals are expected to be used or if expansion boards are added.

Table 31 lists some power supplies that will work with the BeagleBoard.

Table 31. DC Power Supplies

Part #	Manufacturer	Supplier	Price
EPS050100-P6P	CUI	Digi-Key	$7
DPS050200UPS-P5P-SZ	CUI	Digi-Key	$16

Figure 68 is a picture of the type of power supply that will be used on the BeagleBoard.

Figure 68. DC Power Supply

10.2 Serial Ribbon Cable

Figure 69 and **Figure 70** is an example of the serial ribbon cable for the BeagleBoard. Other serial cables that will work on the board may have a different appearance.

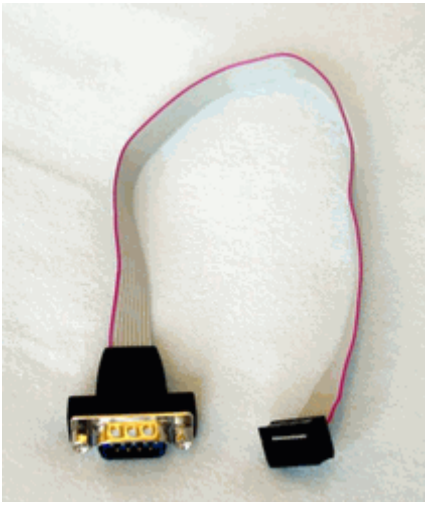

Figure 69. RS232 Cable

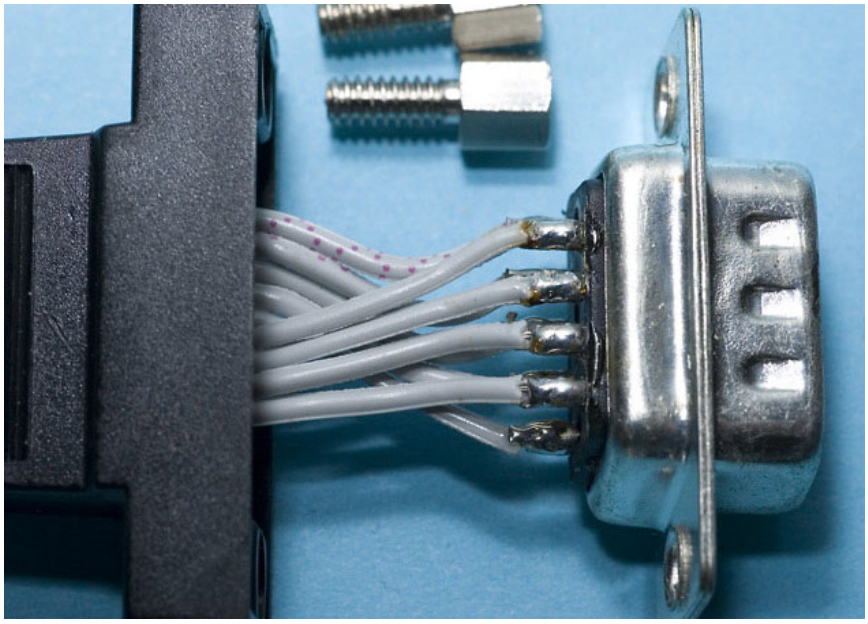

Figure 70. RS232 Cable Wiring

Table 32 shows the pinout of the ribbon cable connector.

Table 32. Cable Pinout

Ribbon Cable	DB9
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10

10.3 USB Hubs

There are no known or anticipated issues with USB hubs. However, it should be noted that a self powered hub is highly recommended. **Table 33** is a list of Hubs that have been tested on the BeagleBoard.

Table 33. USB Hubs Tested

Supplier	Part Number
IOGEAR	GUH274
D-Link	DUB-H4 2.0
Vakoss	TC-204-NS

10.4 DVI Cables

In order to connect the DVI-D interface to a LCD monitor, a HDMI to DVI-D cable is required. **Figure 71** is a picture of a HDMI to DVI-D cable.

Figure 71. HDMI to DVI-D Cable

10.5 DVI-D Monitors

There are many monitors that can be used with the BeagleBoard. With the integrated EDID feature, timing data is collected from the monitor to enable the SW to adjust its timings. **Table 34** shows a short list of the monitors that have been tested to date on the BeagleBoard at the 1024x768 resolution. Please check on BeagleBoard.org for an up to date listing of the DVI-D monitors as well as information on the availability of drivers.

Table 34. DVI-D Monitors Tested

Manufacturer	Part Number	Status
Dell	2407WFPb	Tested
Insignia	NS-LCD15	Tested
Dell	1708FP	Tested

DO NOT PLUG IN THE DVI-D CONNECTOR TO A DISPLAY WITH THE BEAGLEBAORD POWERED ON. PLUG IN THE CABLE TO THE DISPLAY AND THEN POWER ON THE BEAGLEBOARD.

The digital portion of the DVI-D interface is compatible with HDMI and is electrically the same. A standard HDMI cable may be used to connect to the HDMI input of monitors. Whether or not the Beagle will support those monitors is dependent on the timings that are used on the Beagle and those that are accepted by the monitor. This may require a change in the software running on the Beagle. The audio and encryption features of HDMI are not supported by the Beagle.

The analog portion of DVI which provides RGB analog type signals is not supported by the Beagle. Buying a DVI to VGA adapter connector will not work on a VGA display. You will need an active DVI-D to VGA adapter.

10.6 SD/MMC Cards

Table 36 is a list of SD/MMC cards that have been tested on BeagleBoard. Please check BeagleBoard.org for an up to date listing of the SD/MMC cards that have been tested as well as information on the availability of drivers if required.

Table 35. SD/MMC Cards Tested

Manufacturer	Type	Part Number	Status
Patriot	SD	1GB	Tested
Microcenter	SD	1GB/2GB	Tested

10.7 USB to Ethernet

There are several USB to Ethernet adapters on the market and **Figure 72** shows a few of these devices. These devices can easily add Ethernet connectivity to BeagleBoard by using the USB OTG port in the host. This will require a special cable to convert the miniAB connector to a Type A or a hub can also be used. These are provided as examples only. Check BeagleBoard.org for information on devices that have drivers available for them.

Figure 72. USB to Ethernet Adapters

Table 36 provides examples of USB to Ethernet Adapters that **might** be used with the BeagleBoard. This list has not been verified. Inclusion of these items in the table does not guarantee that they will work, but is provided as examples only. Please check BeagleBoard.org for an up to date listing of the USB to Ethernet devices as well as information on the availability of drivers.

Table 36. USB to Ethernet Adapters

Product	Manufacturer	Status
ASOHOUSB	Airlink	Not Tested
TU-ET100C 10/100Mbps	TRENDnet	Not Tested
SABRENT	NB-USB20	Not Tested
Zonet	ZUN2210	Not Tested
StarTech	USB2105S	Not Tested

MOSCHIP is the silicon provider for USB to Ethernet devices. The product that has been tested uses the 7830 from MOSCHIP and has a vendor ID of 9710 and a product ID of 7830. The devices above that are based upon the MOSCHIP device are highlighted in red.

10.8 USB to WiFi

There are several USB to WiFi adapters on the market and **Figure 73** shows a few of these devices. These devices can easily add WiFi connectivity to BeagleBoard by using the USB OTG port in the host mode. This will require a special cable to convert the miniAB connector to a Type A or a hub can also be used. These are provided as examples

only. Check BeagleBoard.org for information on devices that have drivers available for them.

Figure 73. USB to WiFi

Table 37 provides a list of USB to WiFi adapters that could be used with the BeagleBoard. Inclusion of these items in the table does not guarantee that they will work, but is provided as examples only. Please check BeagleBoard.org for an up to date listing of the USB to WiFi devices as well as information on the availability of drivers.

Table 37. USB to WiFi Adapters

Product	Manufacturer	Status
4410-00-00AF	Zoom	Not Tested
HWUG1	Hawkins	Not Tested
TEW-429Uf	Trendnet	Not Tested

It should be noted that the availability of Linux drivers for various WiFi devices is limited. Before purchasing a particular device, please verify the availability of drivers for that device.

10.9 USB to Bluetooth

There are several USB to Bluetooth adapters on the market and **Figure 74** shows a few of these devices. These devices can easily add Bluetooth connectivity to BeagleBoard by using the USB OTG port in the host mode. This will require a special cable to convert the miniAB connector to a Type A or a hub can also be used. These are provided as examples only. Check BeagleBoard.org for information on devices that have drivers available for them and their test status.

Figure 74. USB to Bluetooth

Table 39 provides a list of USB to Bluetooth adapters that could be used with the BeagleBoard. Inclusion of these items in the table does not guarantee that they will work, but is provided as examples only. Please check BeagleBoard.org for an up to date listing of the USB to Bluetooth devices as well as information on the availability of drivers.

Table 38. USB to Bluetooth Adapters

Product	Manufacturer
TBW-105UB	Trendnet
ABT-200	Airlink
F8T012-1	Belkin

11.0 Mechanical Information

11.1 BeagleBoard Dimensions

This section provides information on the mechanical aspect of the BeagleBoard. **Figure 75** is the dimensions of the BeagleBoard.

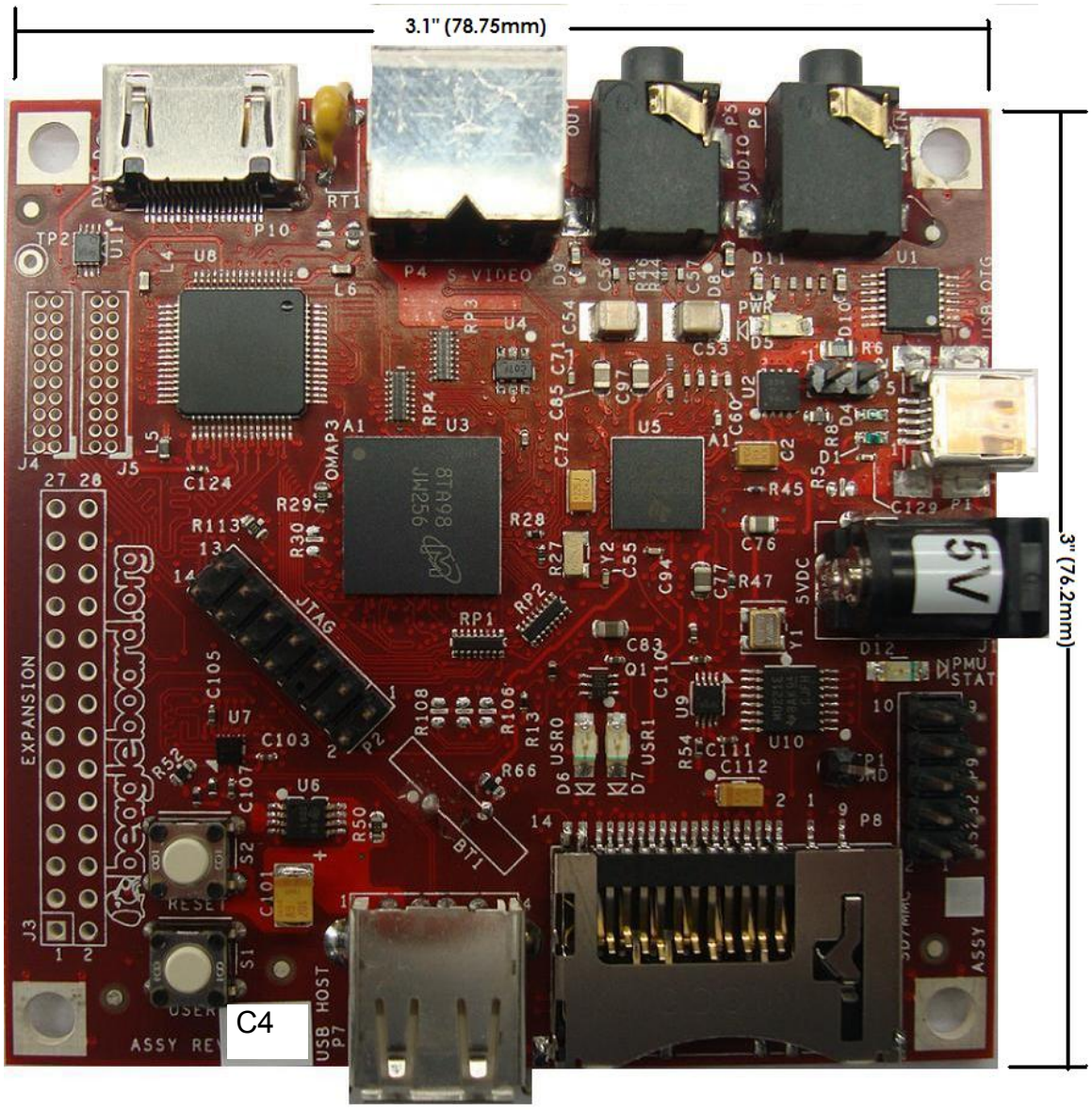

Figure 75. BeagleBoard Dimension Drawing

11.2 BeagleBoard Expansion Card Design Information

This section provides information on what is required from a mechanical and electrical aspect to create expansion cards for the BeagleBoard that are designed to connect to the Expansion header on the BeagleBoard. Users are free to create their own cards for private or commercial use, but in order to be supported by the Software they must conform to these standards if such support is desired.

11.2.1 Mounting Method

The standard method to provide a daughtercard for the BeagleBoard is for it to be mounted UNDER the Beagle Board as described in **Figure 76.**

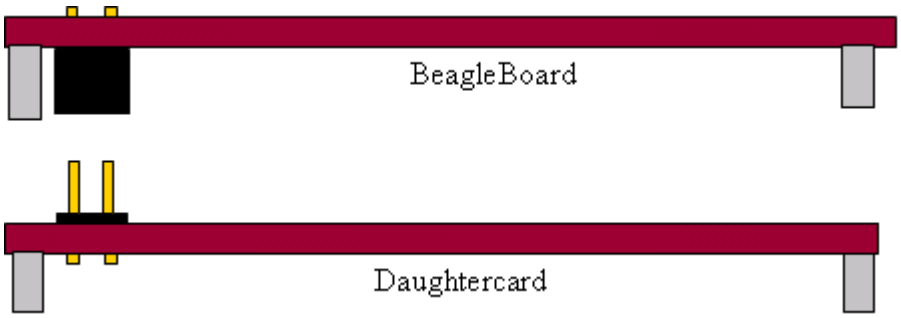

Figure 76. BeagleBoard Bottom Stacked Daughter Card

At the next letter revision of the board, all BeagleBoards produced will have the connectors pre mounted onto the bottom of the BeagleBoard.

11.2.2 Expansion EEPROM

All expansion cards designed for use with the BeagleBoard are required to have a EEPROM located on the board. This is to allow for the identification of the card by the Software in order to set the pin muxing on the expansion connector to be compatible with the expansion card.

The schematic for the EEPROM is in **Figure 77** below.

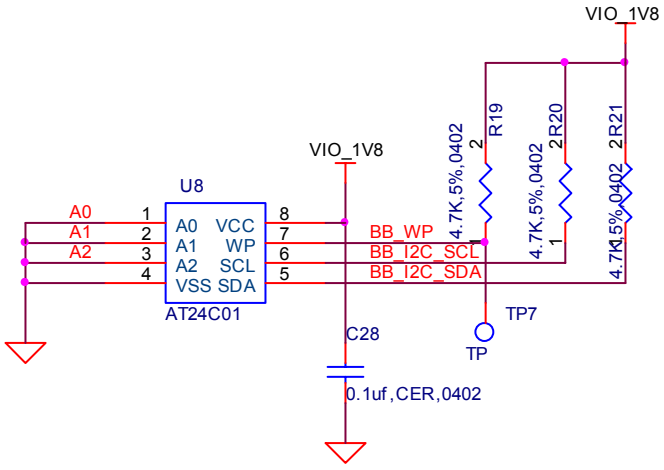

Figure 77. BeagleBoard Expansion Board EEPROM Schematic

The EEPROM must be write protected. It is suggested that a testpoint be used to allow for the WP to be disabled during test to allow the required data to be written to the EEPROM. The EEPROM is to be connected to I2C2 as found on the main expansion connector.

The EEPROM that is designated is the AT24C01 or ATC24C01B. The AT24C01 is designated as "Not Recommended for New Design" but can still be used. The AT24C01B is the replacement part and is available in several different packages, all of which can be used.

- TSSOP 8
- PDIP 8
- UDFN 8
- SOIC 8
- SOT23 5
- dBGA2 8

The contents of the EEPROM are not specified in this document.

12.0 Board Verification

This section provides a step by step process to be followed to verify that the hardware is working. This is the same basic process the board is taken through in production testing.

For an up to date listing of common questions and their answers, please refer to http://elinux.org/BeagleBoardFAQ

12.1 Equipment

To run these tests you will need the following components:

- BeagleBoard
- 5V DC supply with a 2.1mm I.D. and 5.5mm O.D. connector
- SD Card
- PC
- USB miniA to A cable
- USB HUB
- DVI-D Monitor
- DVI-D to HDMI cable
- Speakers
- 3.5mm stereo cable with connectors on both ends
- DB9 Null-Modem Cable
- DB9 to IDC-10 cable ATI/Everex configuration

12.2 Out of the Box

Each BeagleBoard comes pre-loaded with the XLoader and UBoot in Flash. When powered up, it will do the following:

1. Plug in either a USB cable to the board and then to a PC or plug in a 5V power supply.
2. Power LED (D5) will turn on.
3. On the terminal window the following will be printed:

```
Texas Instruments X-Loader 1.4.2 (Feb 19 2009 - 12:01:24)
Loading u-boot.bin from nand

U-Boot 2009.01-dirty (Feb 19 2009 - 12:22:31)

I2C:   ready
OMAP3530-GP rev 2, CPU-OPP2 L3-165MHz
OMAP3 Beagle board + LPDDR/NAND
DRAM:  256 MB
NAND:  256 MiB
*** Warning - bad CRC or NAND, using default environment

MUSB: using high speed
In:    serial usbtty
Out:   serial usbtty
Err:   serial usbtty
```

   The warning message is not an indication of an error condition and is normal. The UBoot is configured to look for a script file on the SD card for booting instructions. If not found, it will then look for the environment variables. As these are not loaded at the factory, you will see the warning message.

4. At this point the following LEDS will turn on:
   - USR0
   - USR1
   - PMU

5. Then the following will be sent to the terminal window and a countdown will commence. To stop the countdown, hit any key on the terminal

```
Board revision C
Serial #4860000300000000004013f8a17019010
Hit any key to stop autoboot: 10
```

   The revision of the board should be identified as a Rev C. The Serial# is NOT the board serial number, but a unique ID for the processor.

6. The DVI-D monitor will turn orange and the color bars will appear on the S-Video Port.

7. If you do not stop the booting process by hitting a key, the following will be printed to the terminal.

```
No MMC card found
Booting from nand ...

NAND read: device 0 offset 0x280000, size 0x400000
 4194304 bytes read: OK
Wrong Image Format for bootm command
ERROR: can't get kernel image!
OMAP3 beagleboard.org #
```

12.3 SD Card Configuration

In order to boot from the SD card, it must be formatted and the files loaded. The following steps explain that process.

1. Format the MMC/SD Card for FAT32 File System using the HP USB Disk Storage Format Tool 2.0.6: http://selfdestruct.net/misc/usbboot/SP27213.exe
2. Insert the Card writer/reader into the Windows machine.
3. Insert MMC/SD card into the card reader/writer
4. Open the HP USB Disk Storage Format Tool.
5. Select "FAT as File System". Click on "Start".
6. After formatting is done Click "OK"
7. Copy the following files on to MMC in the exact order listed. COPY THE MLO FIRST! Make sure you name the file as indicated in the **BOLD** type. These files can be found at http://code.google.com/p/beagleboard/wiki/BeagleboardRevCValidation

   MLO as **MLO**

   u-boot as **u-boot.bin**

   u-boot for flash as **u-boot-f.bin**

   ramdisk image as **ramdisk.gz**

   Kernel (uImage) as **uImage.bin**

   reset.scr as **boot.scr**

   x-loader image as **x-load.bin.ift**

   Regular script file as **normal.scr**

12.4 Setup

This step sets up the board for the tests to follow.

1. Make sure Beagle power is in OFF state by removing the 5V supply and the USB host connection.
2. Connect the IDC UART cable the BeagleBoard and using a Null-Modem serial cable connect it to a SERIAL port on a Window/Linux/Mac machine
3. Have terminal program, such as TeraTerm, HyperTerminal, or Minicom, running on the host machine.
4. Configure the terminal program for (BAUD RATE - 115200, DATA - 8 bit, PARITY- none, STOP - 1bit, FLOW CONTROL - none)
5. Insert the MMC/SD card (that is prepared as described above) into MMC/SD slot on Beagle Board.
6. Connect a LCD Monitor to DVI/HDMI port on the Beagle Board.
7. Connect an externally powered speaker to audio out jack on Beagle Board.
8. Connect a Line-in cable from PC or any player to Audio In jack on Beagle Board.
9. Connect a TV (NTSC-M) to S-video port.
10. Power ON LCD, TV and audio speakers.

12.5 Factory Boot Verification

The BeagleBoard comes pre-Flashed with the Xloader and UBoot in Flash. This step verifies that the board will boot properly from NAND. If the board has been flashed and the default code removed or overwritten, then you should proceed to the next step.

1. Connect the USB cable to the Host PC,
2. The power LED should come on.
3. On the terminal window the following should be printed out by the BeagleBoard:

```
Texas Instruments X-Loader 1.4.2 (Feb 19 2009 - 12:01:24)
Loading u-boot.bin from nand


U-Boot 2009.01-dirty (Feb 19 2009 - 12:22:31)

I2C:   ready
OMAP3530-GP rev 2, CPU-OPP2 L3-165MHz
OMAP3 Beagle board + LPDDR/NAND
DRAM:  256 MB
NAND:  256 MiB
*** Warning - bad CRC or NAND, using default environment

MUSB: using high speed
In:    serial usbtty
Out:   serial usbtty
Err:   serial usbtty
```

```
Board revision C
Serial #4860000300000000004013f8a17019010
Hit any key to stop autoboot: 10
No MMC card found
Booting from nand ...

NAND read: device 0 offset 0x280000, size 0x400000
 4194304 bytes read: OK
Wrong Image Format for bootm command
ERROR: can't get kernel image!
OMAP3 beagleboard.org #
OMAP3 beagleboard.org #
```

4. The USER LEDS and the PMU LED should be on.
5. The S-Video output should display color bars.
6. The DVI-D monitor should display a solid orange screen.

12.6 Board SD Boot

This test will force the BeagleBoard to boot from the SD card instead of the onboard Flash.

1. Press and hold the USER button while pressing and releasing the RESET button.
2. The following should be printed to the terminal window:

```
40V

Texas Instruments X-Loader 1.4.2 (Feb 19 2009 - 12:01:24)
Reading boot sector
Loading u-boot.bin from mmc



U-Boot 2009.01-dirty (Feb 19 2009 - 12:23:21)

I2C:   ready
OMAP3530-GP rev 2, CPU-OPP2 L3-165MHz
OMAP3 Beagle board + LPDDR/NAND
DRAM:  256 MB
NAND:  256 MiB
Using default environment


MUSB: using high speed
In:    serial usbtty
Out:   serial usbtty
Err:   serial usbtty
Board revision C
Serial #4860000300000000004013f8a17019010
Hit any key to stop autoboot: 10
```

3. The USER LEDS and the PMU LED should be on.

Hitting any key on the terminal before the countdown reaches 10, will stop the booting process. If no key is hit, it will continue and flash the SW into the NAND. Go to the next section for a description of this.

12.7 Factory Boot Reinstall

This section tells you how to restore the information in the Flash to the factory default. This is the same test that is run in production when the board is new. The erase process is automatically run before the Flashing process starts.

Prior to getting to this section, follow the process and section 12.6 and do not hit any key on the terminal.

1. As long as no key is pressed on the terminal, the following will be displayed:

```
reading boot.scr

679 bytes read
Running bootscript from mmc ...
## Executing script at 80200000
reading x-load.bin.ift

20392 bytes read
```

2. The x-load.bin.ift contains the XLoader file that will be flashed into the NAND in the following steps. The following will be displayed:

```
***** Replacing x-load *****
Usage:
nand - NAND sub-system

HW ECC selected

NAND erase: device 0 offset 0x0, size 0x80000

Erasing at 0x0 --  25% complete.
Erasing at 0x20000 --  50% complete.
Erasing at 0x40000 --  75% complete.
Erasing at 0x60000 -- 100% complete.
OK

NAND write: device 0 offset 0x0, size 0x20000
 131072 bytes written: OK

NAND write: device 0 offset 0x20000, size 0x20000
 131072 bytes written: OK
```

```
NAND write: device 0 offset 0x40000, size 0x20000
 131072 bytes written: OK

NAND write: device 0 offset 0x60000, size 0x20000
 131072 bytes written: OK
```

3. The u-boot-f.bin contains the UBoot file that will be flashed into the NAND in the following steps. The following will be displayed:

```
reading u-boot-f.bin

275928 bytes read
***** Replacing u-boot *****
Usage:
nand - NAND sub-system

SW ECC selected

NAND erase: device 0 offset 0x80000, size 0x160000

Erasing at 0x80000 --   9% complete.
Erasing at 0xa0000 --  18% complete.
Erasing at 0xc0000 --  27% complete.
Erasing at 0xe0000 --  36% complete.
Erasing at 0x100000 --  45% complete.
Erasing at 0x120000 --  54% complete.
Erasing at 0x140000 --  63% complete.
Erasing at 0x160000 --  72% complete.
Erasing at 0x180000 --  81% complete.
Erasing at 0x1a0000 --  90% complete.
Erasing at 0x1c0000 -- 100% complete.
OK

NAND write: device 0 offset 0x80000, size 0x160000
 1441792 bytes written: OK
```

4. After the XLoader and UBot are flashed, the environment variables are erased to insure proper booting of the Kernel image that is on the SD card. . The following will be displayed:

```
***** Erasing environment settings *****
Usage:
nand - NAND sub-system


NAND erase: device 0 offset 0x160000, size 0x20000

Erasing at 0x160000 -- 100% complete.
OK
```

5. At this point you can remove power to stop the Kernel from booting, or just let it continue the Kernel boot process. For information on the Kernel booting process, proceed to the next section.

12.8 Booting the Kernel

This section describes how to boot the kernel from the SD card. In order to complete this section, you must have completed section 12.7 and do not hit any keys or remove power after the NAND has been flashed.

1. After the NAND has been flashed, the normal.scr script is read form the SD card and the first step after that is to load in the uImage.bin file into the SDRAM. Beagle will print the following to the terminal:

```
***** Executing normal.scr *****
## Executing script at 80200000
reading uImage.bin

2578044 bytes read
***** Kernel: /dev/mmcblk0p1/uImage.bin *****
```

2. Then the root filesystem is read into SDRAM. The BeagleBoard will output the following:

```
reading ramdisk.gz

7999649 bytes read
***** RootFS: /dev/mmcblk0p1/ramdisk.gz *****
1856680 bytes read
```

3. At this point, the booting process will start. The following will be printed to the terminal:

```
## Booting kernel from Legacy Image at 80200000 ...
   Image Name:   Linux-2.6.28-omap1
   Image Type:   ARM Linux Kernel Image (uncompressed)
   Data Size:    2577980 Bytes =  2.5 MB
   Load Address: 80008000
   Entry Point:  80008000
   Verifying Checksum ... OK
   Loading Kernel Image ... OK
OK

Starting kernel ...

Uncompressing
Linux.....................................................................................................................
..... done, booting the kernel.

Linux version 2.6.28-omap1 (root@tiioss) (gcc version 4.2.1 (CodeSourcery Sourcery G++ Lite
2007q3-51)) #2 Thu Feb 19 12:45:34 IST 2009
CPU: ARMv7 Processor [411fc083] revision 3 (ARMv7), cr=10c5387f
CPU: VIPT nonaliasing data cache, VIPT nonaliasing instruction cache
```

```
Machine: OMAP3 Beagle Board
Memory policy: ECC disabled, Data cache writeback
OMAP3430 ES3.0
SRAM: Mapped pa 0x40200000 to va 0xd7000000 size: 0x100000
Reserving 15728640 bytes SDRAM for VRAM
Built 1 zonelists in Zone order, mobility grouping on.  Total pages: 65024
Kernel command line: console=ttyS2,115200n8 console=tty0 root=/dev/ram0 rw ramdisk_size=32768
initrd=0x81600000,32M
Clocking rate (Crystal/DPLL/ARM core): 26.0/332/500 MHz
GPMC revision 5.0
IRQ: Found an INTC at 0xd8200000 (revision 4.0) with 96 interrupts
Total of 96 interrupts on 1 active controller
OMAP34xx GPIO hardware version 2.5
PID hash table entries: 1024 (order: 10, 4096 bytes)
OMAP clockevent source: GPTIMER12 at 32768 Hz
Console: colour dummy device 80x30
console [tty0] enabled
Dentry cache hash table entries: 32768 (order: 5, 131072 bytes)
Inode-cache hash table entries: 16384 (order: 4, 65536 bytes)
Memory: 128MB 128MB = 256MB total
Memory: 206080KB available (4776K code, 425K data, 168K init)
Calibrating delay loop... 473.71 BogoMIPS (lpj=1851392)
Mount-cache hash table entries: 512
CPU: Testing write buffer coherency: ok
net_namespace: 532 bytes
regulator: core version 0.5
NET: Registered protocol family 16
Found NAND on CS0
Registering NAND on CS0
OMAP DMA hardware revision 4.0
USB: No board-specific platform config found
OMAP DSS rev 2.0
OMAP DISPC rev 3.0
OMAP VENC rev 2
OMAP DSI rev 1.0
i2c_omap i2c_omap.1: bus 1 rev3.12 at 2600 kHz
twl4030: PIH (irq 7) chaining IRQs 368..375
twl4030: power (irq 373) chaining IRQs 376..383
twl4030: gpio (irq 368) chaining IRQs 384..401
i2c_omap i2c_omap.3: bus 3 rev3.12 at 400 kHz
SCSI subsystem initialized
twl4030_usb twl4030_usb: Initialized TWL4030 USB module
usbcore: registered new interface driver usbfs
usbcore: registered new interface driver hub
usbcore: registered new device driver usb
musb_hdrc: version 6.0, musb-dma, otg (peripheral+host), debug=0
musb_hdrc: USB OTG mode controller at d80ab000 using DMA, IRQ 92
regulator: VMMC1: 1850 <--> 3150 mV normal standby
regulator: VDAC: 1800 mV normal standby

regulator: VUSB1V5: 1500 mV normal standby
regulator: VUSB1V8: 1800 mV normal standby
regulator: VUSB3V1: 3100 mV normal standby
regulator: VSIM: 1800 <--> 3000 mV normal standby
Bluetooth: Core ver 2.13
NET: Registered protocol family 31
Bluetooth: HCI device and connection manager initialized
Bluetooth: HCI socket layer initialized
cfg80211: Using static regulatory domain info
cfg80211: Regulatory domain: US
        (start_freq - end_freq @ bandwidth), (max_antenna_gain, max_eirp)
        (2402000 KHz - 2472000 KHz @ 40000 KHz), (600 mBi, 2700 mBm)
        (5170000 KHz - 5190000 KHz @ 40000 KHz), (600 mBi, 2300 mBm)
        (5190000 KHz - 5210000 KHz @ 40000 KHz), (600 mBi, 2300 mBm)
        (5210000 KHz - 5230000 KHz @ 40000 KHz), (600 mBi, 2300 mBm)
        (5230000 KHz - 5330000 KHz @ 40000 KHz), (600 mBi, 2300 mBm)
        (5735000 KHz - 5835000 KHz @ 40000 KHz), (600 mBi, 3000 mBm)
cfg80211: Calling CRDA for country: US
```

```
NET: Registered protocol family 2
IP route cache hash table entries: 2048 (order: 1, 8192 bytes)
TCP established hash table entries: 8192 (order: 4, 65536 bytes)
TCP bind hash table entries: 8192 (order: 3, 32768 bytes)

TCP: Hash tables configured (established 8192 bind 8192)
TCP reno registered
NET: Registered protocol family 1
checking if image is initramfs...it isn't (no cpio magic); looks like an initrd
Freeing initrd memory: 32768K
VFS: Disk quotas dquot_6.5.1
Dquot-cache hash table entries: 1024 (order 0, 4096 bytes)
JFFS2 version 2.2. (NAND) (SUMMARY)  Â© 2001-2006 Red Hat, Inc.
msgmni has been set to 467
alg: No test for stdrng (krng)
io scheduler noop registered
io scheduler anticipatory registered
io scheduler deadline registered
io scheduler cfq registered (default)
Serial: 8250/16550 driver4 ports, IRQ sharing enabled
serial8250.0: ttyS0 at MMIO 0x4806a000 (irq = 72) is a ST16654
serial8250.0: ttyS1 at MMIO 0x4806c000 (irq = 73) is a ST16654
serial8250.0: ttyS2 at MMIO 0x49020000 (irq = 74) is a ST16654
console [ttyS2] enabled
brd: module loaded
loop: module loaded
usbcore: registered new interface driver asix
usbcore: registered new interface driver cdc_ether
usbcore: registered new interface driver rndis_host
usbcore: registered new interface driver zd1211rw
usbcore: registered new interface driver rndis_wlan
usbcore: registered new interface driver zd1201
usbcore: registered new interface driver usb8xxx
usbcore: registered new interface driver rtl8187
usbcore: registered new interface driver rt2500usb
usbcore: registered new interface driver rt73usb
usbcore: registered new interface driver p54usb
i2c /dev entries driver
input: triton2-pwrbutton as /class/input/input0
triton2 power button driver initialized
Driver 'sd' needs updating - please use bus_type methods
Driver 'sr' needs updating - please use bus_type methods
omap2-nand driver initializing
NAND device: Manufacturer ID: 0x2c, Chip ID: 0xba (Micron NAND 256MiB 1,8V 16-bit)
cmdlinepart partition parsing not available
Creating 5 MTD partitions on "omap2-nand":
0x00000000-0x00080000 : "X-Loader"
0x00080000-0x00260000 : "U-Boot"
0x00260000-0x00280000 : "U-Boot Env"
0x00280000-0x00680000 : "Kernel"
0x00680000-0x10000000 : "File System"
ehci_hcd: USB 2.0 'Enhanced' Host Controller (EHCI) Driver
ehci-omap ehci-omap.0: OMAP-EHCI Host Controller
ehci-omap ehci-omap.0: new USB bus registered, assigned bus number 1
ehci-omap ehci-omap.0: irq 77, io mem 0x48064800
ehci-omap ehci-omap.0: USB 2.0 started, EHCI 1.00
usb usb1: configuration #1 chosen from 1 choice
hub 1-0:1.0: USB hub found
hub 1-0:1.0: 3 ports detected
Initializing USB Mass Storage driver...
usbcore: registered new interface driver usb-storage
USB Mass Storage support registered.
g_ether gadget: using random self ethernet address
g_ether gadget: using random host ethernet address
usb0: MAC 22:46:4b:c2:b0:fb

usb0: HOST MAC a2:b4:44:63:f6:ae
g_ether gadget: Ethernet Gadget, version: Memorial Day 2008
g_ether gadget: g_ether ready
```

```
musb_hdrc musb_hdrc: MUSB HDRC host driver
musb_hdrc musb_hdrc: new USB bus registered, assigned bus number 2
usb usb2: configuration #1 chosen from 1 choice
hub 2-0:1.0: USB hub found
hub 2-0:1.0: 1 port detected
mice: PS/2 mouse device common for all mice
input: gpio-keys as /class/input/input1
twl4030_rtc twl4030_rtc: rtc core: registered twl4030_rtc as rtc0
twl4030_rtc twl4030_rtc: Power up reset detected.
twl4030_rtc twl4030_rtc: Enabling TWL4030-RTC.
OMAP Watchdog Timer Rev 0x31: initial timeout 60 sec
Bluetooth: HCI USB driver ver 2.10
usbcore: registered new interface driver hci_usb
Bluetooth: Broadcom Blutonium firmware driver ver 1.2
usbcore: registered new interface driver bcm203x
Bluetooth: Digianswer Bluetooth USB driver ver 0.10
usbcore: registered new interface driver bpa10x
Bluetooth: Generic Bluetooth SDIO driver ver 0.1
mmci-omap-hs mmci-omap-hs.0: Failed to get debounce clock
Registered led device: beagleboard::usr0
Registered led device: beagleboard::usr1
leds-gpio: probe of leds-gpio failed with error -22
usbcore: registered new interface driver usbhid
usbhid: v2.6:USB HID core driver
Advanced Linux Sound Architecture Driver Version 1.0.18rc3.
usbcore: registered new interface driver snd-usb-audio
ASoC version 0.13.2
OMAP3 Beagle SoC init
TWL4030 Audio Codec init
asoc: twl4030 <-> omap-mcbsp-dai-(link_id) mapping ok
ALSA device list:
  #0: omap3beagle (twl4030)
oprofile: using arm/armv7
TCP cubic registered
NET: Registered protocol family 17

NET: Registered protocol family 15
Bluetooth: L2CAP ver 2.11
Bluetooth: L2CAP socket layer initialized
Bluetooth: SCO (Voice Link) ver 0.6
Bluetooth: SCO socket layer initialized
Bluetooth: RFCOMM socket layer initialized
Bluetooth: RFCOMM TTY layer initialized
Bluetooth: RFCOMM ver 1.10
Bluetooth: BNEP (Ethernet Emulation) ver 1.3
Bluetooth: BNEP filters: protocol multicast
Bluetooth: HIDP (Human Interface Emulation) ver 1.2
RPC: Registered udp transport module.
RPC: Registered tcp transport module.
ieee80211: 802.11 data/management/control stack, git-1.1.13
ieee80211: Copyright (C) 2004-2005 Intel Corporation <jketreno@linux.intel.com>
ThumbEE CPU extension supported.
Power Management for TI OMAP3.
SmartReflex driver initialized
Disabling unused clock "sr2_fck"
Disabling unused clock "sr1_fck"
Disabling unused clock "mcbsp_fck"
Disabling unused clock "mcbsp_fck"
Disabling unused clock "mcbsp_fck"
Disabling unused clock "mcbsp_ick"
Disabling unused clock "mcbsp_ick"
Disabling unused clock "mcbsp_ick"
Disabling unused clock "gpt2_ick"
Disabling unused clock "gpt3_ick"
Disabling unused clock "gpt4_ick"
Disabling unused clock "gpt5_ick"
Disabling unused clock "gpt6_ick"
Disabling unused clock "gpt7_ick"
```

```
Disabling unused clock "gpt8_ick"
Disabling unused clock "gpt9_ick"
Disabling unused clock "wdt3_ick"
Disabling unused clock "wdt3_fck"
Disabling unused clock "gpio2_dbck"
Disabling unused clock "gpio3_dbck"
Disabling unused clock "gpio4_dbck"
Disabling unused clock "gpio5_dbck"
Disabling unused clock "gpio6_dbck"
Disabling unused clock "gpt9_fck"
Disabling unused clock "gpt8_fck"
Disabling unused clock "gpt7_fck"
Disabling unused clock "gpt6_fck"
Disabling unused clock "gpt5_fck"
Disabling unused clock "gpt4_fck"
Disabling unused clock "gpt3_fck"
Disabling unused clock "gpt2_fck"
Disabling unused clock "gpt1_ick"
Disabling unused clock "wdt1_ick"
Disabling unused clock "wdt2_ick"
Disabling unused clock "wdt2_fck"
Disabling unused clock "gpio1_dbck"
Disabling unused clock "gpt1_fck"
Disabling unused clock "cam_ick"

Disabling unused clock "cam_mclk"
Disabling unused clock "des1_ick"

Disabling unused clock "sha11_ick"
Disabling unused clock "rng_ick"

Disabling unused clock "aes1_ick"
Disabling unused clock "ssi_ick"
Disabling unused clock "mailboxes_ick"
Disabling unused clock "mcbsp_ick"
Disabling unused clock "mcbsp_ick"
Disabling unused clock "gpt10_ick"
Disabling unused clock "gpt11_ick"
Disabling unused clock "i2c_ick"
Disabling unused clock "mcspi_ick"
Disabling unused clock "mcspi_ick"
Disabling unused clock "mcspi_ick"
Disabling unused clock "mcspi_ick"
Disabling unused clock "hdq_ick"
Disabling unused clock "mspro_ick"
Disabling unused clock "des2_ick"
Disabling unused clock "sha12_ick"
Disabling unused clock "aes2_ick"
Disabling unused clock "icr_ick"
Disabling unused clock "pka_ick"
Disabling unused clock "ssi_ssr_fck"
Disabling unused clock "hdq_fck"
Disabling unused clock "mcspi_fck"
Disabling unused clock "mcspi_fck"
Disabling unused clock "mcspi_fck"
Disabling unused clock "mcspi_fck"
Disabling unused clock "mcbsp_fck"
Disabling unused clock "mcbsp_fck"
Disabling unused clock "i2c_fck"
Disabling unused clock "mspro_fck"
Disabling unused clock "gpt11_fck"
Disabling unused clock "gpt10_fck"
Disabling unused clock "dpll4_m6x2_ck"
Disabling unused clock "dpll3_m3x2_ck"
Disabling unused clock "sys_clkout1"
VFP support v0.3: implementor 41 architecture 3 part 30 variant c rev 1
Console: switching to colour frame buffer device 80x30
clock: clksel_round_rate_div: dpll4_m4_ck target_rate 48000000
clock: new_div = 9, new_rate = 48000000
```

```
omap-dss DISPC error: dispc irq error status 4024
omap-dss DISPC error: dispc irq error status 4000
omap-dss DISPC error: dispc irq error status 4000
omap-dss DISPC error: dispc irq error status 4022
omap-dss DISPC error: dispc irq error status 4000
omap-dss DISPC error: dispc irq error status 4000
omap-dss DISPC error: dispc irq error status 4022
omap-dss DISPC error: dispc irq error status 4000
omap-dss DISPC error: dispc irq error status 4022
omap-dss DISPC error: dispc irq error status 4000
omap-dss DISPC error: Excessive DISPC errors
Turning off lcd and digit
omap-dss DISPC error: Excessive DISPC errors
Turning off lcd and digit
omap-dss DISPC error: Excessive DISPC errors
Turning off lcd and digit
usb 2-1: new high speed USB device using musb_hdrc and address 2
twl4030_rtc twl4030_rtc: setting system clock to 2000-01-01 00:00:00 UTC (946684800)
RAMDISK: Compressed image found at block 0
VFS: Mounted root (ext2 filesystem).
Freeing init memory: 168K
mmc0: new high speed SD card at address b368
mmcblk0: mmc0:b368 SD    970 MiB
 mmcblk0: p1
usb 2-1: device v4146 pba01 is not supported
usb 2-1: configuration #1 chosen from 1 choice
scsi0 : SCSI emulation for USB Mass Storage devices
udevd version 124 started
uncorrectable error : <3>end_request: I/O error, dev mtdblock0, sector 0
uncorrectable error : <3>end_request: I/O error, dev mtdblock0, sector 8
uncorrectable error : <3>end_request: I/O error, dev mtdblock0, sector 16
uncorrectable error : <3>end_request: I/O error, dev mtdblock0, sector 24
uncorrectable error : <3>end_request: I/O error, dev mtdblock0, sector 0
scsi 0:0:0:0: Direct-Access     Pretec   256MB Tiny       1.30 PQ: 0 ANSI: 2
sd 0:0:0:0: [sda] 512000 512-byte hardware sectors: (262 MB/250 MiB)
sd 0:0:0:0: [sda] Write Protect is off
sd 0:0:0:0: [sda] Assuming drive cache: write through
sd 0:0:0:0: [sda] 512000 512-byte hardware sectors: (262 MB/250 MiB)
sd 0:0:0:0: [sda] Write Protect is off
sd 0:0:0:0: [sda] Assuming drive cache: write through
 sda: sda1
sd 0:0:0:0: [sda] Attached SCSI removable disk
sd 0:0:0:0: Attached scsi generic sg0 type 0

.-------.
|       |              .-.
|   |   |-----.------.-----.| |   .----..-----.-----.
|       |    |__  |  ---'| '--.|  .-'|    |     |
|   |   | | |    |---  ||  --'|  | |  ' | | | |
'---'---'--'--'--.  |-----''----''--'  '-----'-'-'-'
                -'  |
                '---'

The Angstrom Distribution beagleboard ttyS2

Angstrom 2008.1-test-20090127 beagleboard ttyS2

beagleboard login:
```

4. Type root and hit <enter>. You now are in the Linux kernel.

12.9 UBoot Tests

There are a series of tests that are run while in UBoot. This requires that the Beagle is not in the Kernel mode, but the UBoot mode. The UBoot mode is entered by hitting a key prior to the UBoot timeout reaching 10.

The following sections describe each test and how it is to be run.

12.9.1 EDID Test

This test will display the EDID (Enhanced Display ID) from the DVI-D monitor by using the I2C interface on the DVI-D connector. The DVI-D connector must be connected to a DVI-D compatible monitor in order to run this test..

1. Type the following commands:

```
OMAP3 beagleboard.org # ibus 2
OMAP3 beagleboard.org# imd 0x50 0 100
```

2. Something similar to the following will be displayed:

```
0000: 00 ff ff ff ff ff 00 10 ac 24 40 5a 39 41 41    .........$@Z9AA
0010: 1f 11 01 03 80 22 1b 78 ee ae a5 a6 54 4c 99 26    .....".x....TL.&
0020: 14 50 54 a5 4b 00 71 4f 81 80 01 01 01 01 01 01    .PT.K.qO........
0030: 01 01 01 01 01 01 30 2a 00 98 51 00 2a 40 30 70    ......0*..Q.*@0p
0040: 13 00 52 0e 11 00 00 1e 00 00 00 ff 00 50 4d 30    ..R..........PM0
0050: 36 31 37 38 32 41 41 39 5a 0a 00 00 00 fc 00 44    61782AA9Z......D
0060: 45 4c 4c 20 31 37 30 38 46 50 0a 20 00 00 00 fd    ELL 1708FP. ....
0070: 00 38 4c 1e 51 0e 00 0a 20 20 20 20 20 20 00 36    .8L.Q...      .6
```

Note the words "DELL 1708FP" which is the ID of the monitor in this example. It will be different based on the display manufacturer of your display. For more detailed information on the full EDID format, refer to: http://en.wikipedia.org/wiki/EDID

12.9.2 LED Test

This test checks out the PWM and USER0/1 LEDs on the Beagle.

1. Type the following commands followed by the <ENTER> key and verify that the correct results are seen on LEDs USR0 and USR1.

```
OMAP3 beagleboard.org # mw 0x49056090 0x00600000  [USR0 & USR1 OFF]
OMAP3 beagleboard.org # mw 0x49056094 0x00400000  [USR0 ON]
OMAP3 beagleboard.org # mw 0x49056094 0x00200000  [USR1 ON]
```

2. Type the following commands and verify that the correct results are seen on PMU LED.

```
OMAP3 beagleboard.org # ibus 0
```

```
OMAP3 beagleboard.org # imm 0x4A 0xEE  <ENTER>
000000ee: 22 ? 00       <ENTER>                    [PMU LED OFF]
<CTRL-C> <CTRL-C>
OMAP3 beagleboard.org # imm 0x4A 0xEE
000000ee: 22 ? 22  <ENTER>                         [PMU LED ON]
<CTRL-C> <CTRL-C>
```

12.9.3 DVI-D Test

This test checks the DVI-D interface for proper operation. It sends various colors to the DVI-D monitor.

1. Type the following commands followed by the <ENTER> key and very the correct results are seen.

```
OMAP3 beagleboard.org # mw 0x49058090 0x00000400 [DISPLAY TURNS OFF]
OMAP3 beagleboard.org # mw 0x49058094 0x00000400 [DISPLAY TURNS ON]
OMAP3 beagleboard.org # mw 0x80500000 07e007e0 7ffff [DISPLAY TURNS GREEN]
OMAP3 beagleboard.org # mw 0x80500000 001f001f 7ffff  [DISPLAY TURNS BLUE]
OMAP3 beagleboard.org # mw 0x80500000 00000000 7ffff [DISPLAY TURNS BLACK]
OMAP3 beagleboard.org # mw 0x80500000 ffffffff 7ffff       [DISPLAY TURNS WHITEN]
OMAP3 beagleboard.org # mw 0x80500000 f800f800 7ffff  [DISPLAY TURNS RED
```

12.10 Kernel Based Tests

The following tests require that the Kernel is loaded and that you have logged into the Kernel. [See section 12.8]

12.10.1 DVI-D Test

This test plays a short video clip to the DVI-D monitor.

1. Type the following command:

```
root@beagleboard:~# mplayer /sample_video.avi
```

2. It will display a 320x240 video on the DVI screen. The video has been downloaded from https://garage.maemo.org/download.php/54/269/2380/bug.avi

12.10.2 S-Video Test

1. Type the following command:

```
root@beagleboard:/mmc# svideo
```

2. Type the following command to start the video:

```
[root@beagleboard:/mmc# mplayer /sample_video.avi
```

3. It will display a 320x240 video on the DVI screen. The video has been downloaded from https://garage.maemo.org/download.php/54/269/2380/bug.avi

12.10.3 Audio Test

The audio test is divided into two test, one for audio in and one for audio out. Audio is recorded into the audio in port and then played out the audio out port.

12.10.3.1 Audio In

1. Make Sure your player is running and Audio Line in is connected to board.
2. Make sure that you are in the MMC directory. If you are, proceed to step 4. If not, then type the following command:

```
root@beagleboard:~# mkdir /mmc
root@beagleboard:~# mount -t vfat /dev/mmcblk0p1 /mmc
```

3. Change the directory by typing:

```
root@beagleboard:/mmc# cd /mmc
```

4. Type the following command:

```
root@beagleboard:/mmc# arecord -t wav -c 2 -r 44100 -f S16_LE -v /mmc/k
```

5. The following output is expected on the terminal window:

```
Recording WAVE '/mmc/k' : Signed 16 bit Little Endian, Rate 44100 Hz, Stereo
Plug PCM: Hardware PCM card 0 'omap3beagle' device 0 subdevice 0
Its setup is:
  stream       : CAPTURE
  access       : RW_INTERLEAVED
  format       : S16_LE
  subformat    : STD
  channels     : 2
  rate         : 44100
  exact rate   : 44100 (44100/1)
  msbits       : 16
  buffer_size  : 22052
  period_size  : 5513
  period_time  : 125011
  tstamp_mode  : NONE
  period_step  : 1
  avail_min    : 5513
  period_event : 0
```

```
start_threshold  : 1
stop_threshold   : 22052
silence_threshold: 0
silence_size : 0
boundary     : 1445199872
```

6. When you want to stop the recording process just press <CONTROL+C>.

12.10.3.2 Audio Out

NOTE: It is expected that you have previously recorded an audio file to be played and that you are still in the MMC directory.

1. Type the following command:

```
root@beagleboard:/mmc# aplay -t wav -c 2 -r 44100 -f S16_LE -v k
```

2. The recorded audio should be heard on the Speakers,

3. The following output is expected on terminal window:

```
Playing WAVE '/mmc/k' : Signed 16 bit Little Endian, Rate 44100 Hz, Stereo
Plug PCM: Hardware PCM card 0 'omap3beagle' device 0 subdevice 0
Its setup is:
  stream       : PLAYBACK
  access       : RW_INTERLEAVED

  format       : S16_LE
  subformat    : STD
  channels     : 2
  rate         : 44100
  exact rate   : 44100 (44100/1)
  msbits       : 16
  buffer_size  : 22052
  period_size  : 5513
  period_time  : 125011
  tstamp_mode  : NONE
  period_step  : 1
  avail_min    : 5513
  period_event : 0
  start_threshold  : 22052
  stop_threshold   : 22052
  silence_threshold: 0
  silence_size : 0
  boundary     : 1445199872
```

7. To stop the audio playback just press <CONTROL+C>. If you choose, you can the let the recorded audio play out. It will stop when it reaches the end of the recorded file.

12.10.3.3 Keyboard Test

This test runs on the OTG port in the Host mode. It requires that a Powered USB hub be used, and that the Hub and device (Keyboard or mouse) be connected when the Linux OS is booted. This section is broken down into two sections, one for the mouse and the other for the keyboard.

NOTE: This test is run after the OS is booted with the Hub and Keyboard plugged in.

1. Make sure that you are in the MMC directory. If you are, proceed to step 3. If not, then type the following command:

```
root@beagleboard:~]# mkdir /mmc
root@beagleboard:~]# mount -t vfat /dev/mmcblk0p1 /mnt/mmc/cd /mnt/mmc/
```

2. Change the directory by typing:

```
root@beagleboard:~# cd /mmc
```

3. Type the following command:

```
root@beagleboard:/mmc]# evtest /dev/input/event1
```

4. Press a Key on USB Keyboard and look for a printout in the terminal window.

   Example if "a" is pressed the following output is seen on Console:

```
Event: time 1657.754638, type 1 (Key), code 30 (A), value 1
Event: time 1657.754638, ---------- Report Sync ------------
Event: time 1657.964599, type 1 (Key), code 30 (A), value 0
Event: time 1657.964599, ---------- Report Sync ------------
```

5. Press <CONTROL+C> to stop the test.

12.10.3.4 Mouse Test

NOTE: This test is run after the Kernel booted with the Hub and mouse plugged in.

1. Make sure that you are in the MMC directory. If you are, proceed to step 3. If not, then type the following command:

```
root@beagleboard:~# mount -t vfat /dev/mmcblk0p1 /mmc/
```

2. Change the directory by typing:

```
root@beagleboard:~# cd /mnt/mmc/
```

3. Type the following command:

```
root@beagleboard:/mmc# evtest /dev/input/event0
```

4. Press mouse button and look for a printout in the terminal window.

   Example if Left button is pressed and released the following lines should get displayed on console

```
Event: time 1871.724792, ---------- Report Sync ------------
Event: time 1873.804687, type 1 (Key), code 272 (LeftBtn), value 1
Event: time 1873.804687, ---------- Report Sync ------------
Event: time 1873.964660, type 1 (Key), code 272 (LeftBtn), value 0
Event: time 1873.964660, ---------- Report Sync ------------
```

5. Moving the Mouse also results in Console messages

```
Event: time 1959.120635, ---------- Report Sync ------------
Event: time 1959.130676, type 2 (Relative), code 0 (X), value -21
Event: time 1959.130676, ---------- Report Sync ------------
Event: time 1959.140625, type 2 (Relative), code 0 (X), value -16
```

6. Press <CONTROL+C> to stop the test

12.10.3.5 USB EHCI Test

The following test will copy a file from the SD card to the USB EHCI port and back. The file name can be changed to anything on the SD card. You must have a USB ThumbDrive installed in the EHCI port at power up.

Start in the root directory and make sure the MMC directory is already mounted.

1. Type the following commands to set up the test:

```
root@beagleboard:~# mkdir /usb1
root@beagleboard:~# mount /dev/sda1 /usb1
```

2. Type the following commands to copy from the SD card to the USB Drive:

```
root@beagleboard:~# cp /mmc/u-boot.bin /usb1/test.bin
```

3. Type the following command to make sure the file was copied to the USB drive:

```
root@beagleboard:~# ls –al /usb1
```

   The file should be listed in the directory.

4. Type the following command to copy the file from the USB drive to the SD card.

```
root@beagleboard:~# cp /usb1/test.bin /mmc1/test.bin
```

5. Type the following command to copy to make sure the file was copied to the SD card.

```
root@beagleboard:~# ls –al /mmc
```

The file should be listed in the directory. Larger files can be used to create a longer test if desired.

13.0 Troubleshooting

This section will provide assistance in troubleshooting the BeagleBoard in the event there are questions raised as to what the sate of the BeagleBoard is. This may be due to a HW failure or the SW not initializing things properly during development. Also provided is a section of know issues. Be sure and check with BeagleBoard.org for any updates.

For an up to date listing of common questions and their answers, please refer to http://elinux.org/BeagleBoardFAQ

13.1 Access Points

This section covers the various access points where various signals and voltages can be measured.

13.1.1 Voltage Points

Figure 78 shows the test points for the various voltages on BeagleBoard.

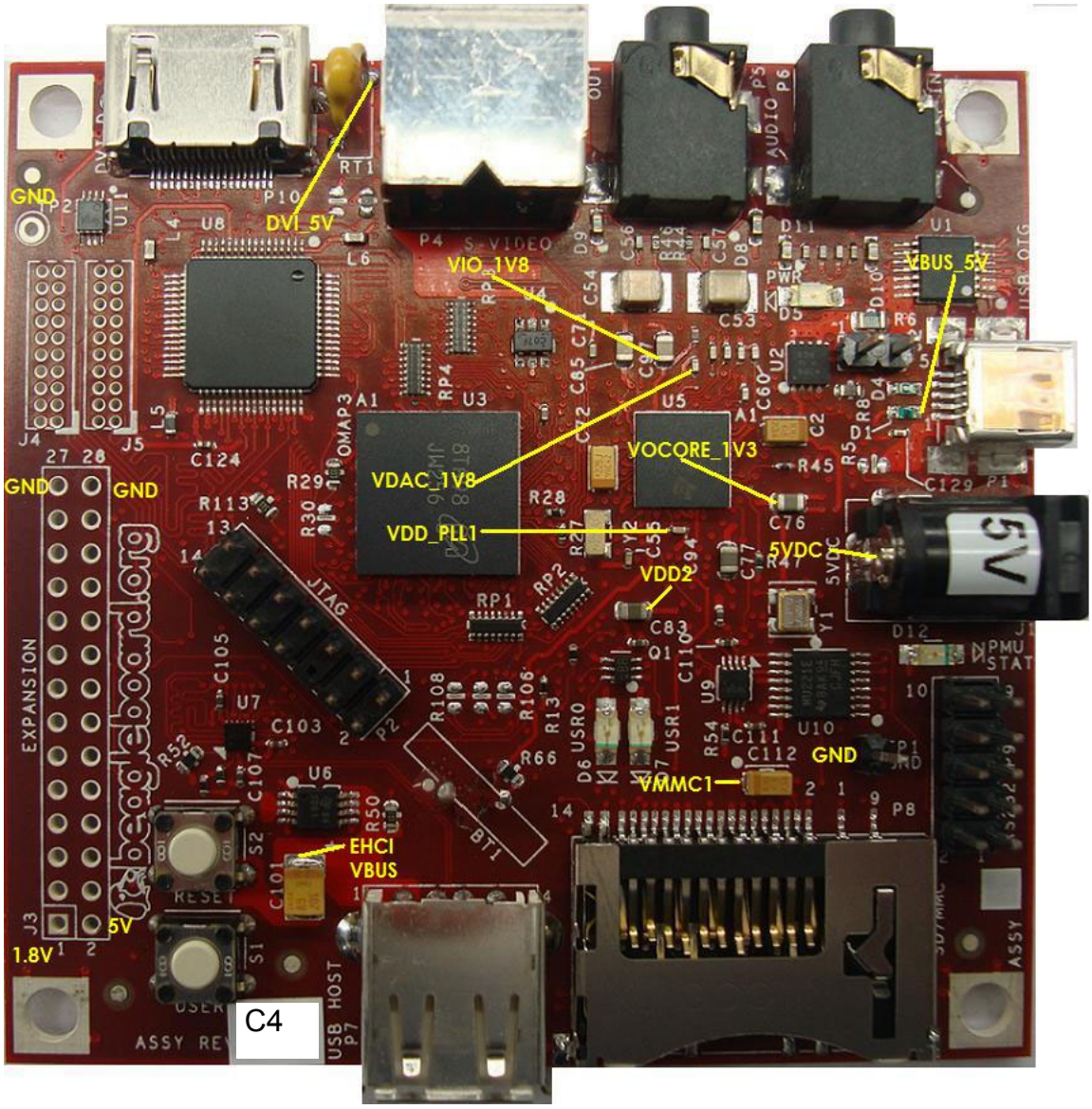

Figure 78. BeagleBoard Voltage Access Points

Some of these voltages may not be present depending on the state of the TPS65950 as set by the OMAP3530. Others may be at different voltage levels depending on the same factor.

Table 39 provides the ranges of the voltages and the definition of the conditions as applicable.

Table 39. Voltages

Voltage	Min	Nom	Max	Conditions
VIO_1V8	1.78	1.8	1.81	
VDD_SIM	1.78	1.8	1.81	
VBUS_5V0	4.9	5.0	5.2	From the host PC. May be lower or higher.
VOCORE_1V3	1.15	1.2	1.4	Can be set via SW. Voltage levels may vary.
VBAT	4.1	4.2	4.3	
VDAC_1V8	1.78	1.8	1.81	
VDD_PLL1	1.78	1.8	1.81	
VDD_PLL2	1.78	1.8	1.81	
VDD2	1.15	1.2	1.25	
3.3V	3.28	3.3	3.32	
VMMC1 (3V)	2.9	3.0	3.1	3.0V at power up. Can be set to via SW.
VMMC1(1.8V)	1.78	1.8	1.81	

13.1.2 Signal Access Points

Figure 79 shows the access points for various signals on BeagleBoard.

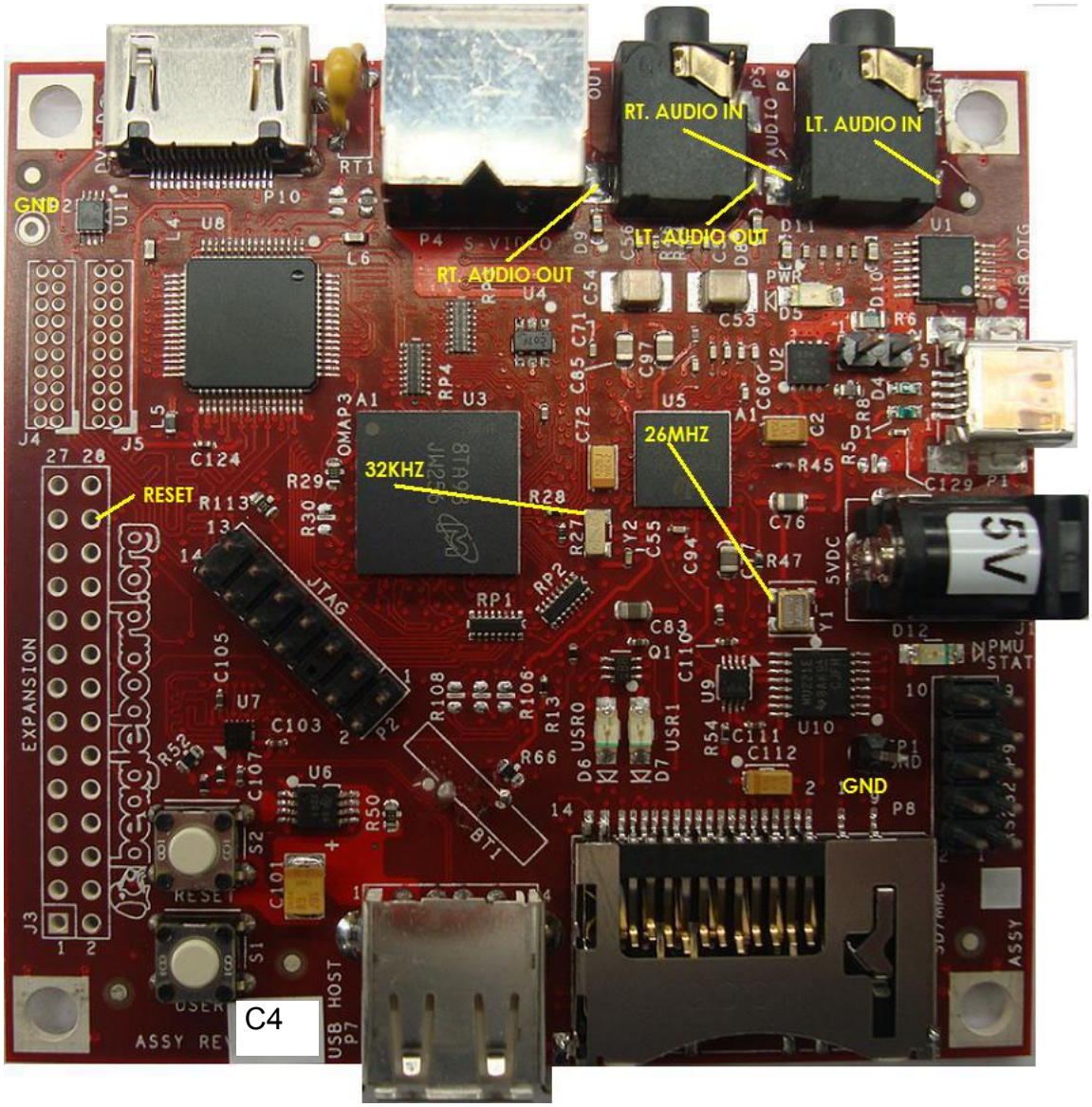

Figure 79. BeagleBoard Signal Access Points

13.2 Troubleshooting Guide

Table 40 provides a list of possible failure modes and conditions and suggestions on how to diagnose them and ultimate determine whether the HW is operational or not.

Table 40. Troubleshooting

Symptoms	Possible Problem	Action
JTAG does not connect.	Verify that the Power LED is on.	If off and running over USB, the PC may have shut down the voltage due to excessive current as related to what it is capable of providing. Remove the USB cable and re insert. If running on a DC supply make sure that voltage is being supplied.
	JTAG interface needs to be reset	Reset the BeagleBoard.
UBoot does not start, and no activity on the RS232 monitor.	Incorrect serial cable configuration.	Verify orientation of the RS232 flat cable
		Check for the right null modem cable.
	If a 40V is displayed over the serial cable, processor is booting. Issue could be the SD/MMC card.	Make sure the SD/MMC card is installed all they way into the connector.
		Make sure the card is formatted correctly and that the MLO file is the first file written to the SD card.
USB Host Connection Issues via OTG.	Cheap USB Cable. OTG cables are typically not designed for higher current. The expect 100mA max.	Measure the voltage at the card to determine the voltage drop across the cable. If it the level is below 4.35V, the USB power is not guaranteed to work,

13.3 Serial Port Issues

We have had several serial port issues in the field caused by different issues. This section attempts to provide a step by step process to identify what the issue is.

The main thing to keep in mind is that the PC and the BeagleBoard connectors are wired the same. In order for them to talk, they must have a null modem cable to connect them.

The following sections provide steps to help identify the issue.

For additional help on debugging serial issues, refer to the FAQ at
http://elinux.org/BeagleBoardFAQ#Serial_connection_.231

13.3.1 First Step

1. Review the wiring of your IDC10 to DB9M serial adapter. Only the TX, RX and GND signals are used.
2. Make sure that the cable is plugged in correctly. The red stripe should be at the bottom next to pin1 of P9. Some cables may have the flat cable extending away from the BeagleBoard and others may be extending toward the middle of the BeagleBoard. **Figure 80** shows the proper orientation of the IDC serial cable.

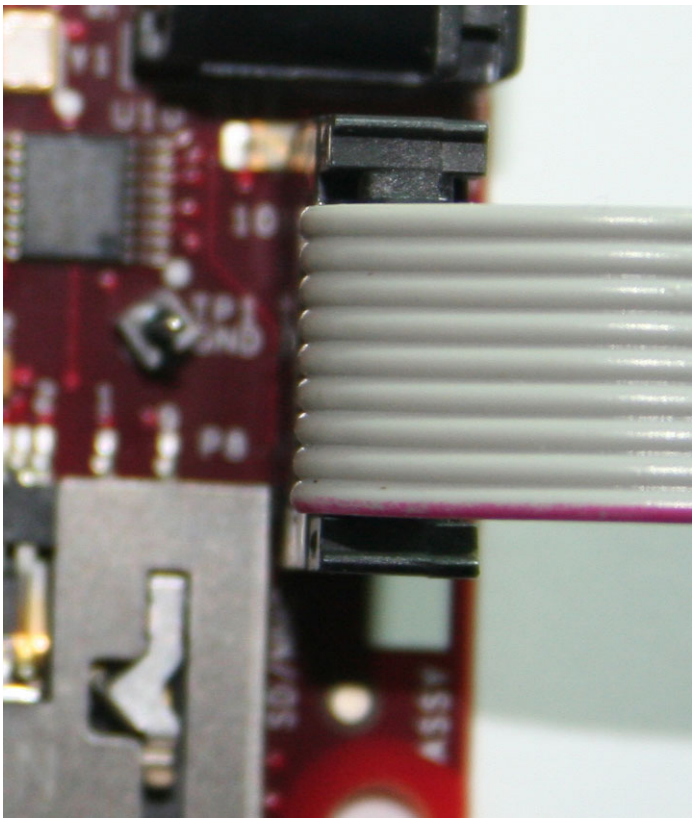

Figure 80. BeagleBoard Serial Cable Orientation

3. You must have a Null Modem cable to connect to a PC. This results in the TX and RX leads being swapped, connecting the TX of the BeagleBoard to RX of the PC and RX of the BeagleBoard to TX of the PC. This cable also must be a female to

female cable as the connectors on the BeagleBoard and PC are male. **Figure 81** shows the DB9 male connector and **Figure 82** shows the Null Modem Cable.

Figure 81. DB9 Male Connector

Figure 82. DB9 Null Modem Cable

4. If you have an ohmmeter, you can measure to see if the pins are swapped between pins 2 and 3 from each end of the cable.

13.3.2 Second Step

A simple test to verify that the cables you are using are correct to create a loopback on the cable. This checks the IDC cable and the null modem cable for connections.

1. Connect a wire across the TX and RX leads (Pins 2 and Pins 3) of the cable that plugs into the BeagleBoard (IDC Cable). **Figure 83** shows how this is done.

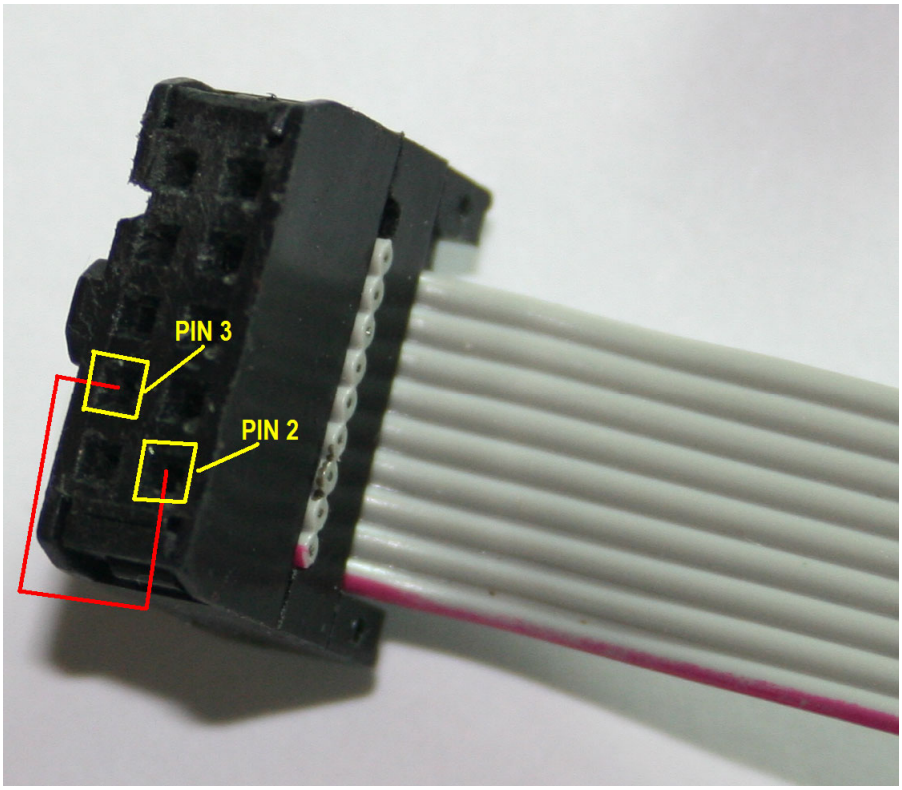

Figure 83. Serial Cable Loopback

2. On your terminal start typing.
3. If the correct characters are echoed back, then the cables are in the proper configuration. Note that this checks the electrical connection only. If the terminal program is set wrong, then serial port will still not work.

13.3.3 Third Step

1. Make sure your terminal settings are correct.

    - BAUD RATE: 115200
    - DATA: 8 bit
    - PARITY: none
    - STOP: 1bit
    - FLOW CONTROL: none (Critical)

    Make sure that the Flow Control is set to none.

13.3.4 Fourth Step

If everything checks out OK on the previous steps, then the issue may be on the BeagleBoard. Follow the steps below to determine that state of the BeagleBoard.

1. Apply power to the board.
2. LED D5 should come on indicating that power is on.
3. LEDs USR0 and USR1 will come on once the board runs UBOOT.
4. By this time data should be printed to the terminal window.
5. Below are a couple of scenarios we have seen:

    - BeagleBoard sends data but cannot receive data
    - No data is sent at all
    - No data is sent, but it can be received.

If any of these issues are present, then there is a chance that the serial driver has failed. This is an issue with the level shifter, U9, on the board that we have seen fail after 48 hours of operation. The vast majority of boards with this issue are being screened out at the manufacturing stages, but some of the early shipment of boards could still exhibit this issue.

If this is the case, complete the RMA process at http://beagleboard.org/support/rma

14.0 Known Issues

This section provides information on any know issues with the BeagleBoard HW and the overall status. **Table 41** provides a list of the know issues on the BeagleBoard. The Rev C2 and C3 are provided for reference purposes.

Table 41. Known Issues

Affected Revision	Issue	Description	Workaround	Final Fix
C2 and C3	Random USB Host Disconnects	There is a small number of boards that are shown to have random disconnects when transferring large amounts of data via the EHCI USB Host port. This requires that the board be power cycled to restore the USB port. The issue is related to noise in a specific frequency range locking up the USB PHY. Some boards are noisier than others based on the current draw of the various components on the 1.8V rail.	Some boards can be fixed by placing a 22uf capacitor in parallel with C97. This fix does not work for all boards. Others have had success by adding the 22uF capacitor to the expansion header.	C4
C4	None	None		

15.0 PCB Component Locations

Figures 84 and **Figure 85** contain the bottom and top side component locations of the BeagleBoard.

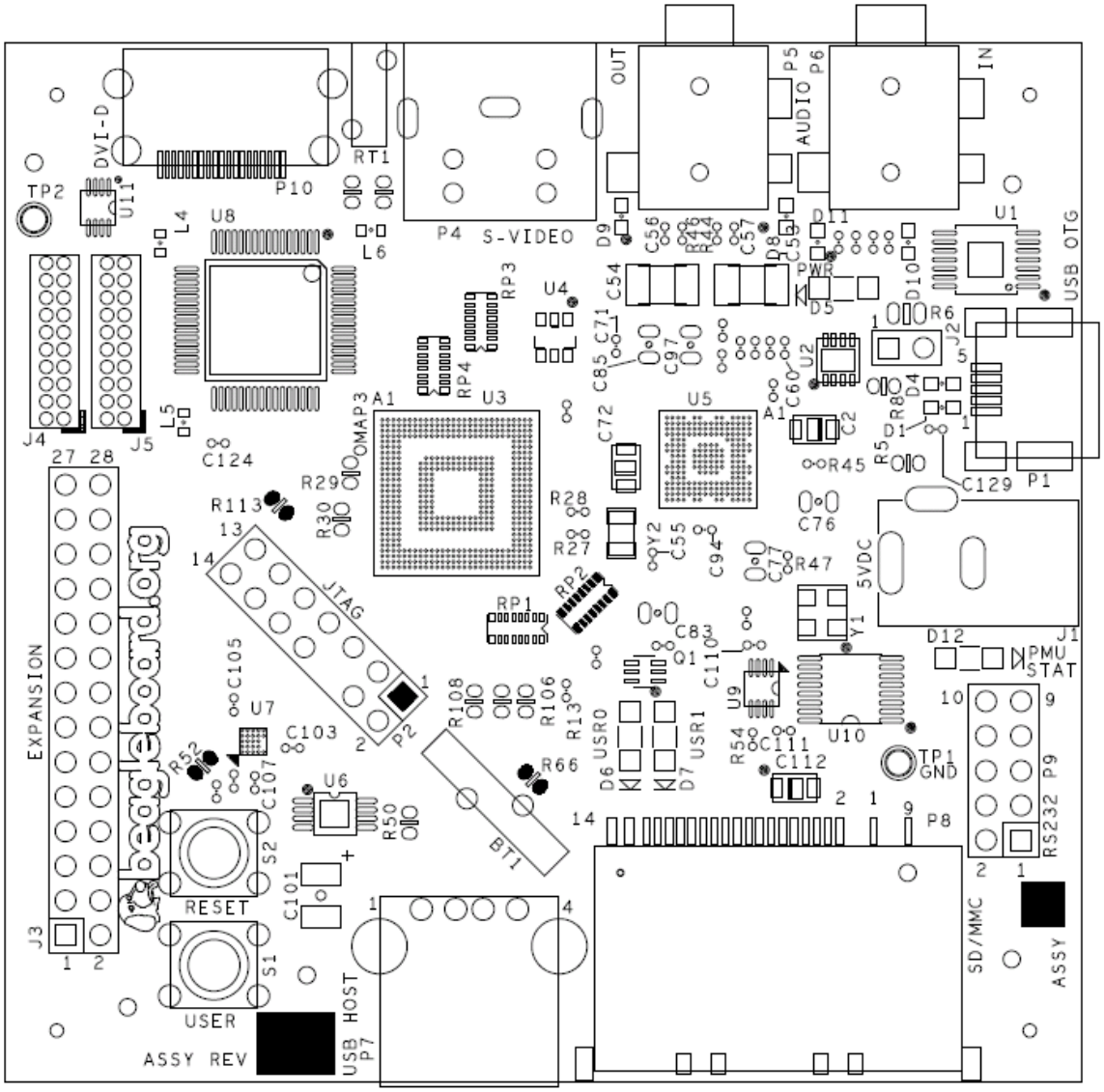

Figure 84. BeagleBoard Top Side Components

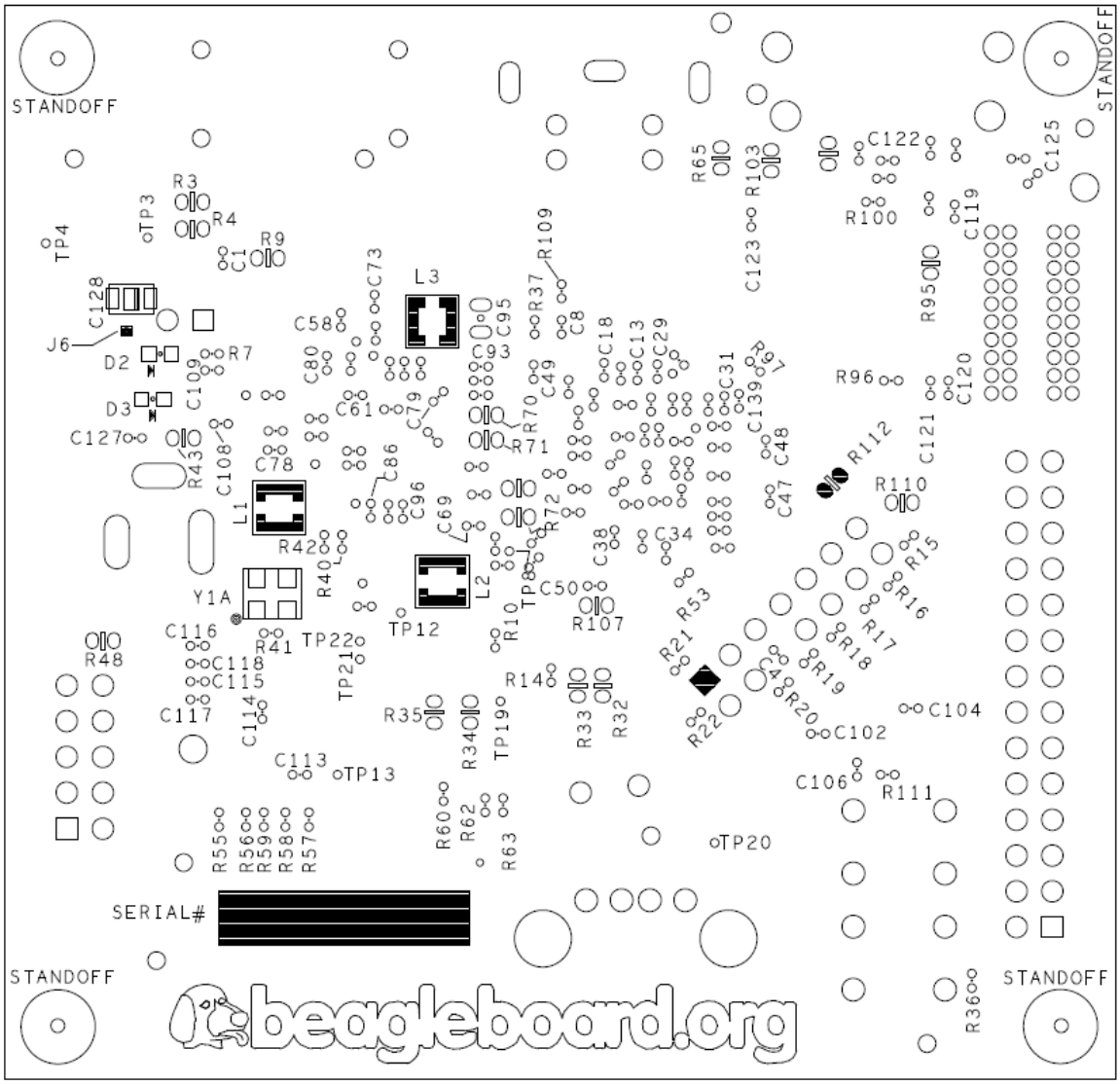

Figure 85. BeagleBoard Bottom Side Components

16.0 Schematics

The following pages contain the PDF schematics for the BeagleBoard. This manual will be periodically updated, but for the latest documentations be sure and check BeagleBoard.org for the latest schematics.

OrCAD source files are provided for BeagleBoard on BeagleBoard.org at the following link.

http://beagleboard.org/hardware/design

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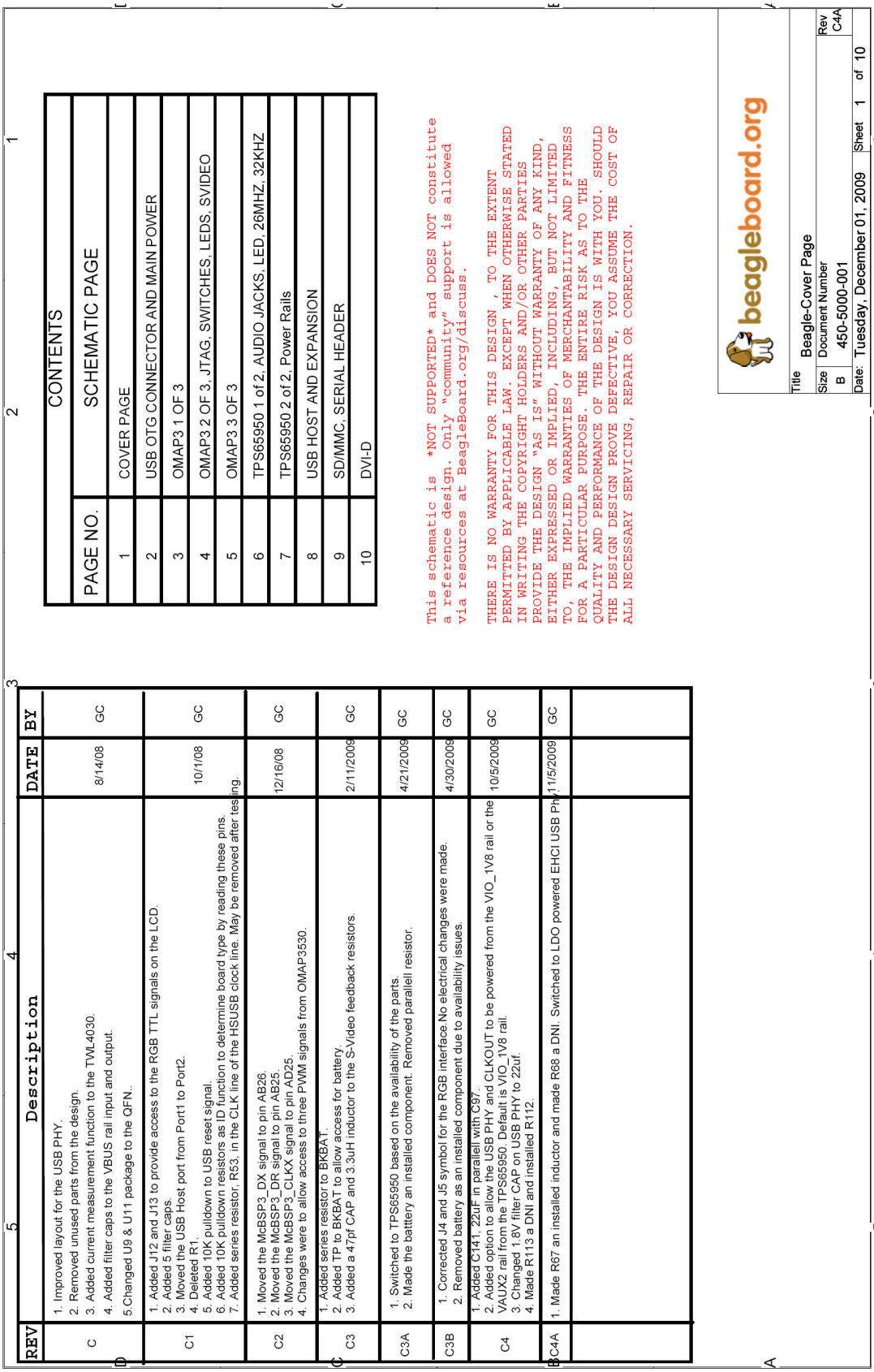
We mean it, these design materials may be totally unsuitable for any purposes.



REV	Description	DATE	BY
C	1. Improved layout for the USB PHY. 2. Removed unused parts from the design. 3. Added current measurement function to the TWL4030. 4. Added filter caps to the VBUS rail input and output. 5.Changed U9 & U11 package to the QFN..	8/14/08	GC
C1	1. Added J12 and J13 to provide access to the RGB TTL signals on the LCD. 2. Added 5 filter caps. 3. Moved the USB Host port from Port1 to Port2. 4. Deleted R1. 5. Added 10K pulldown to USB reset signal. 6. Added 10K pulldown resistors as ID function to determine board type by reading these pins. 7. Added series resistor. R53, in the CLK line of the HSUSB clock line. May be removed after testing.	10/1/08	GC
C2	1. Moved the McBSP3_DX signal to pin AB26. 2. Moved the McBSP3_DR signal to pin AB25. 3. Moved the McBSP3_CLKX signal to pin AD25. 4. Changes were to allow access to three PWM signals from OMAP3530.	12/16/08	GC
C3	1. Added series resistor to BKBAT. 2. Added TP to BKBAT to allow access for battery. 3. Added a 47pf CAP and 3.3uH inductor to the S-Video feedback resistors.	2/11/2009	GC
C3A	1. Switched to TPS65950 based on the availability of the parts. 2. Made the battery an installed component. Removed parallell resistor.	4/21/2009	GC
C3B	1. Corrected J4 and J5 symbol for the RGB interface.No electrical changes were made. 2. Removed battery as an installed component due to availability issues.	4/30/2009	GC
C4	1. Added C141, 22uF in parallell with C97. 2. Added option to allow the USB PHY and CLKOUT to be powered from the VIO_1V8 rail or the VAUX2 rail from the TPS65950. Default is VIO_1V8 rail. 3. Changed 1.8V filter CAP on USB PHY to 22uf. 4. Made R113 a DNI and installed R112.	10/5/2009	GC
C4A	1. Made R67 an installed inductor and made R68 a DNI. Switched to LDO powered EHCI USB Phy	11/5/2009	GC

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8	USB HOST AND EXPANSION
9	SD/MMC, SERIAL HEADER
10	DVI-D

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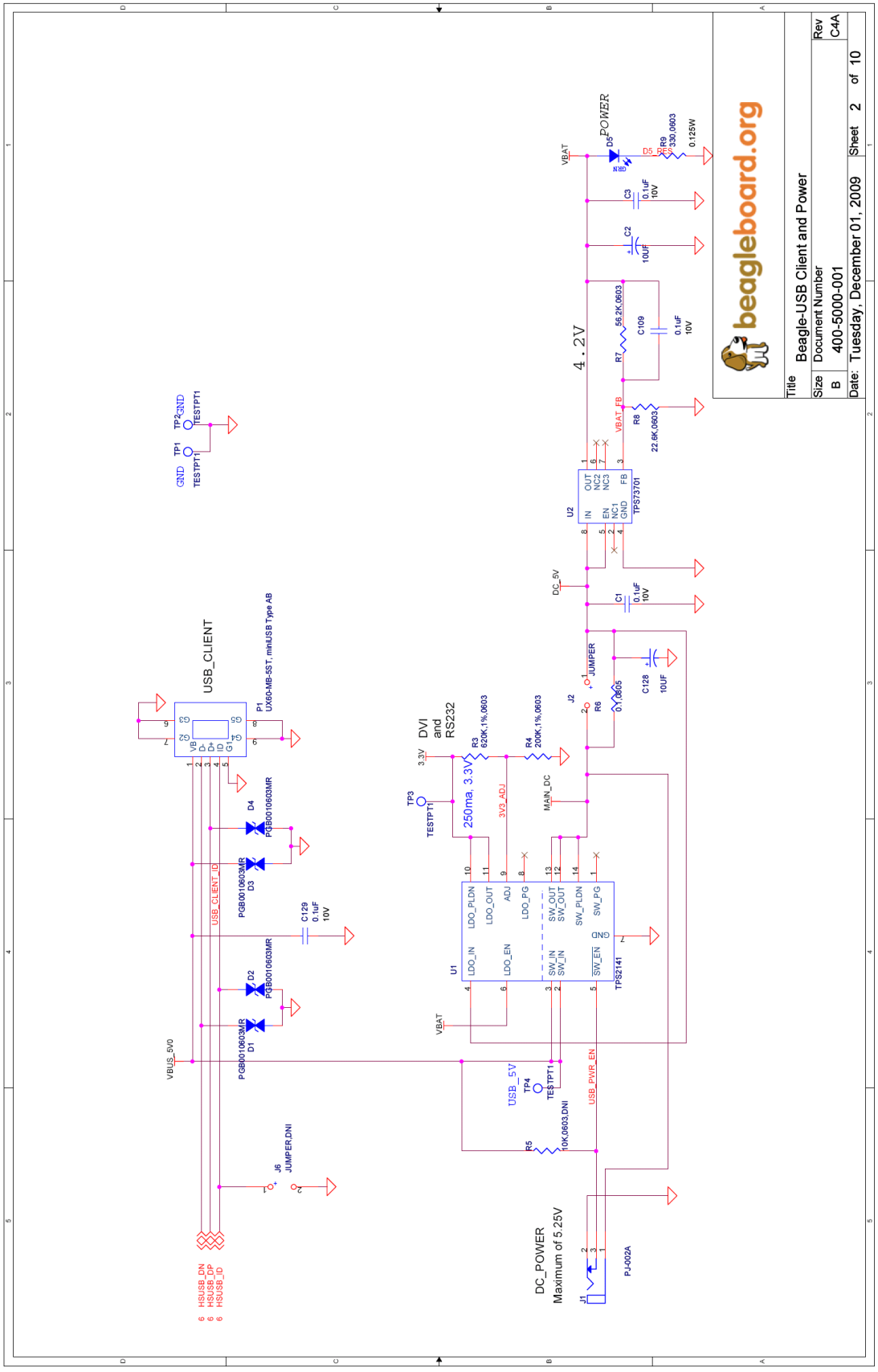
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Title
Beagle-USB Client and Power
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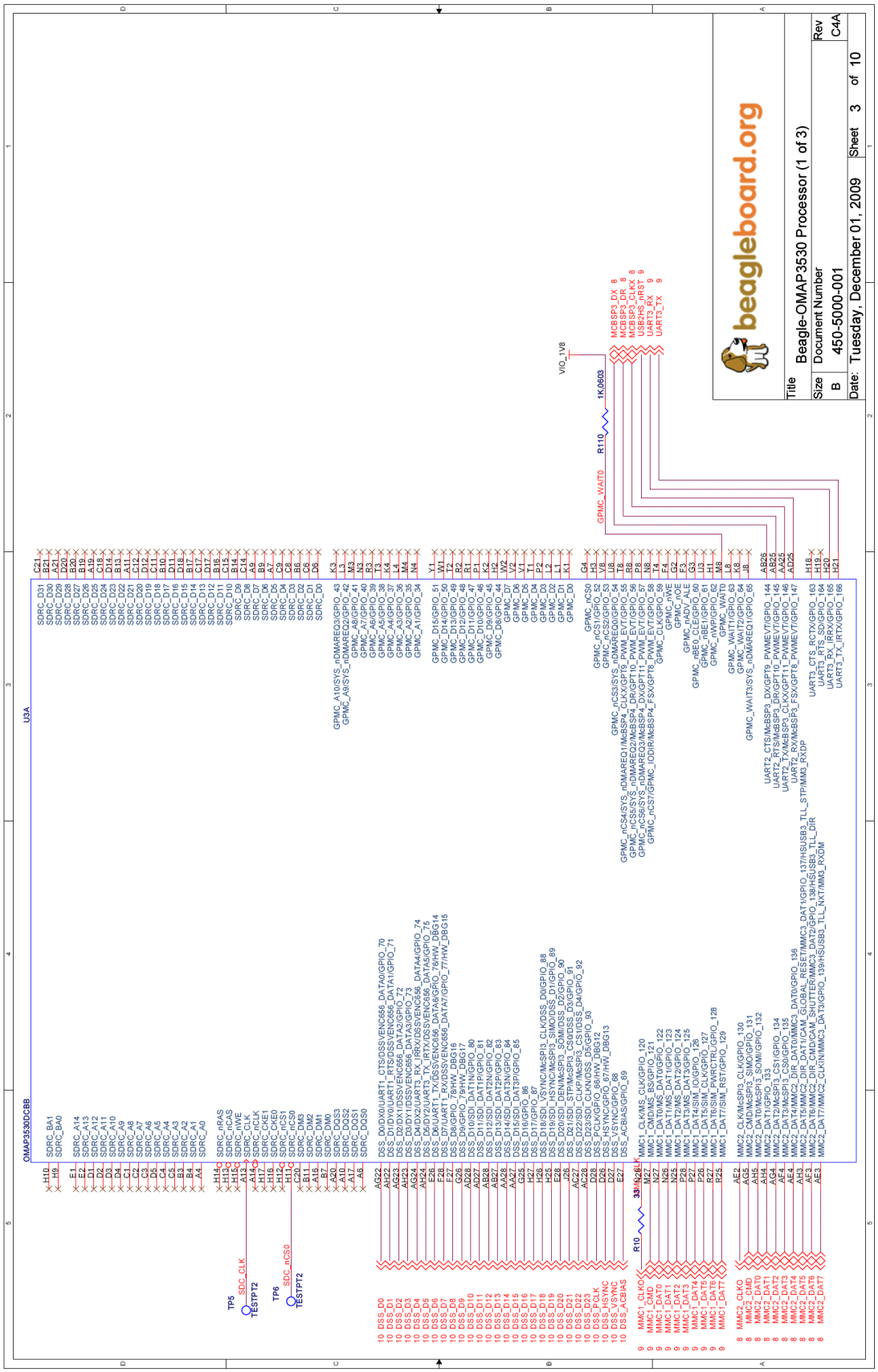
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OMAP3530DCBB
U3A
VIO_1V8
1K/0603
R110
GPMC_WAIT0
MCBSP3_DX
MCBSP3_DR
MCBSP3_CLKX
USB2HS_nRST
UART3_RX
UART3_TX
SDRC_BA1
SDRC_BA0
SDRC_A14
SDRC_A13
SDRC_A12
SDRC_A11
SDRC_A10
SDRC_A9
SDRC_A8
SDRC_A7
SDRC_A6
SDRC_A5
SDRC_A4
SDRC_A3
SDRC_A2
SDRC_A1
SDRC_A0
SDRC_nRAS
SDRC_nCAS
SDRC_nWE
SDRC_CLK
SDRC_nCLK
SDRC_CKE1
SDRC_CKE0
SDRC_nCS1
SDRC_nCS0
SDRC_DM3
SDRC_DM2
SDRC_DM1
SDRC_DM0
SDRC_DQS3
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SDRC_D31
SDRC_D30
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SDRC_D13
SDRC_D12
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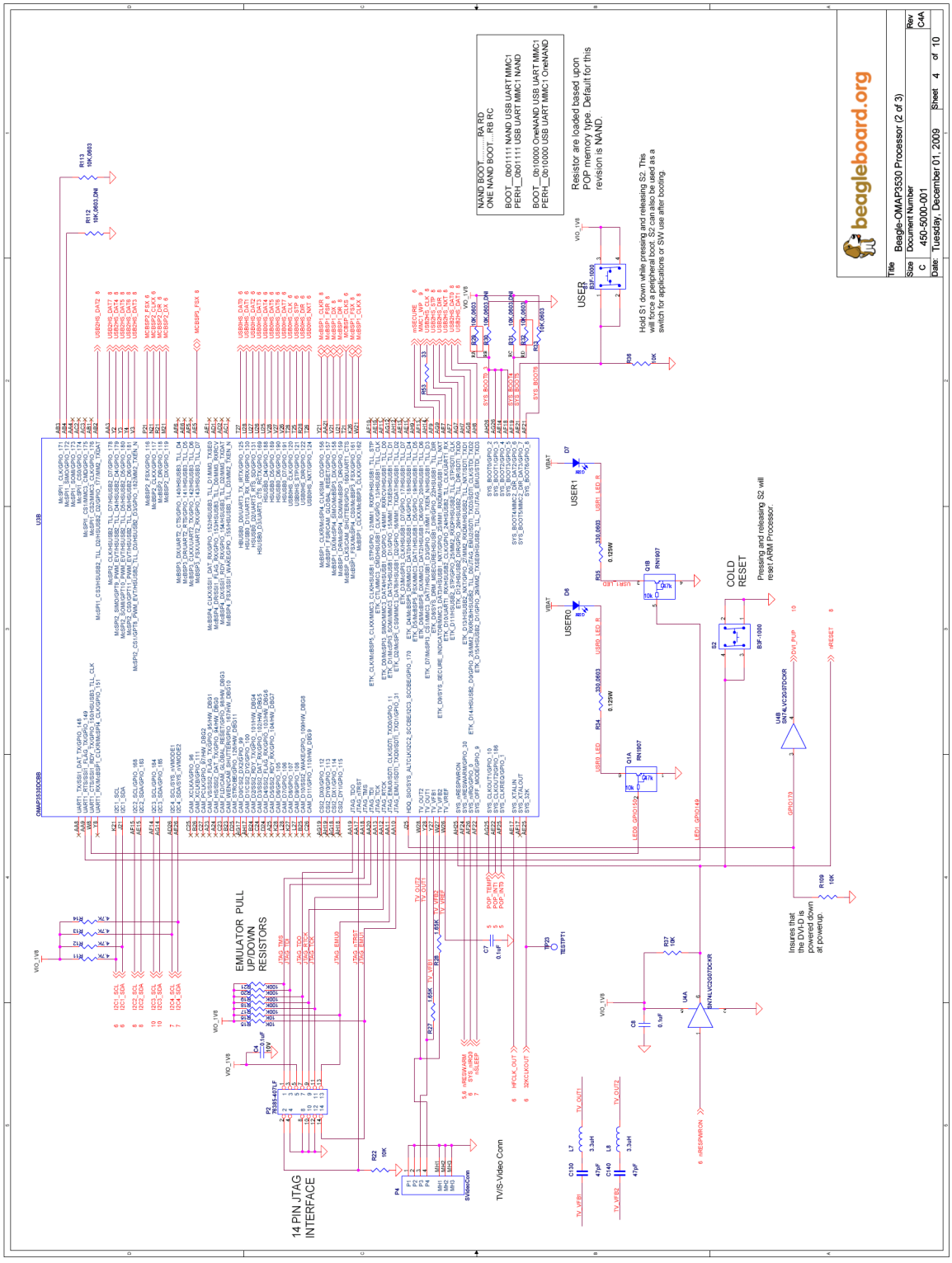
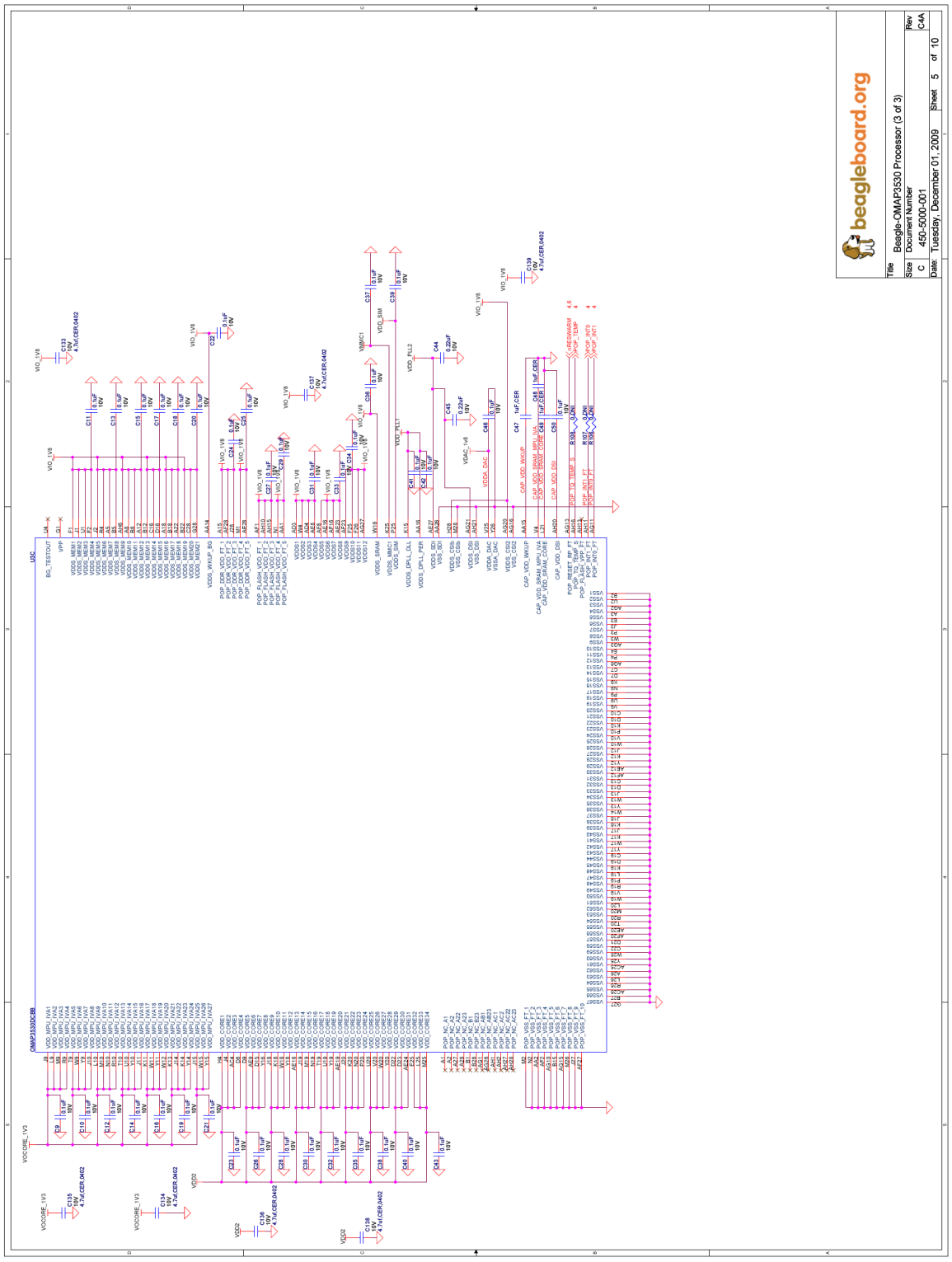
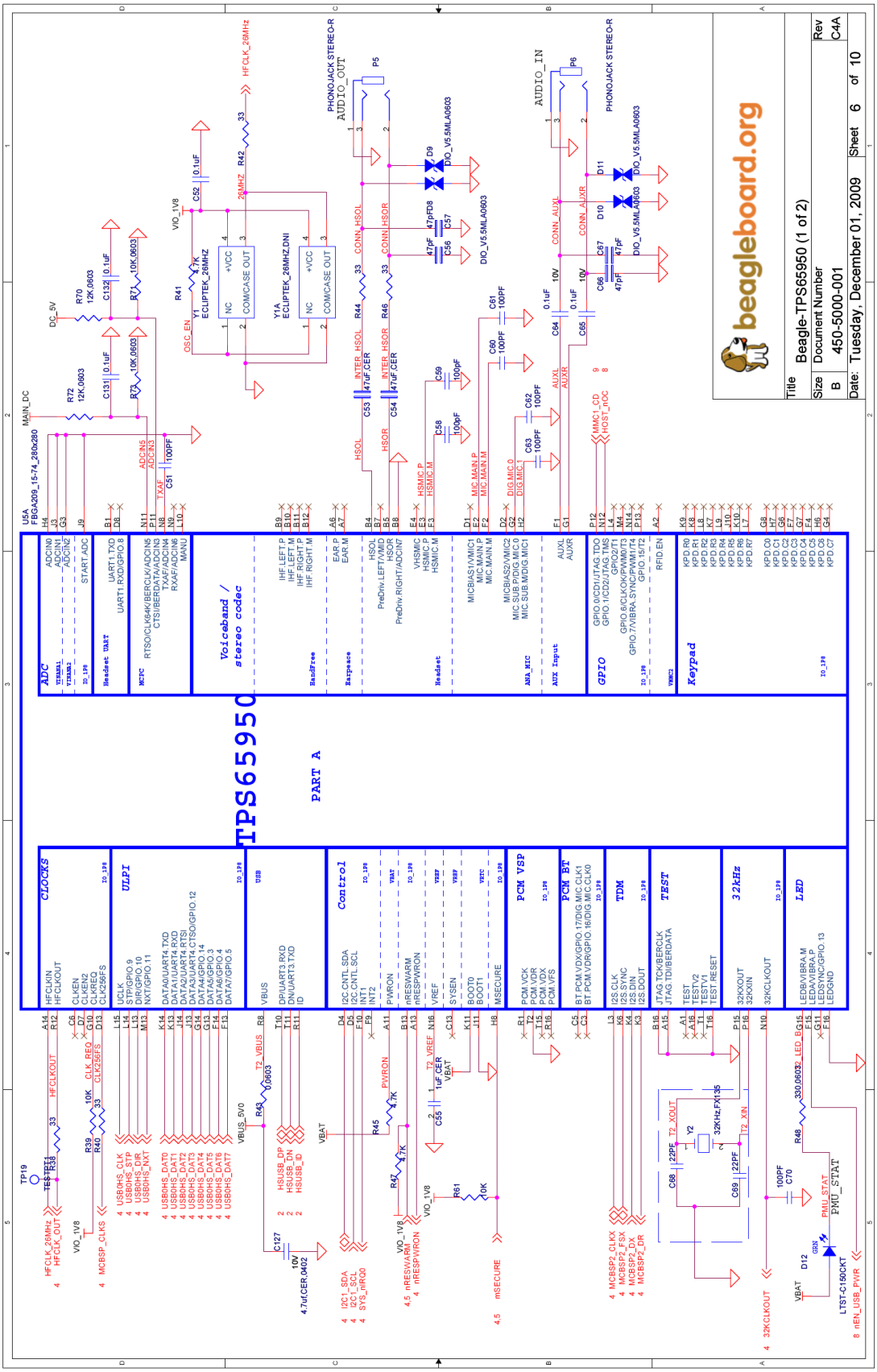
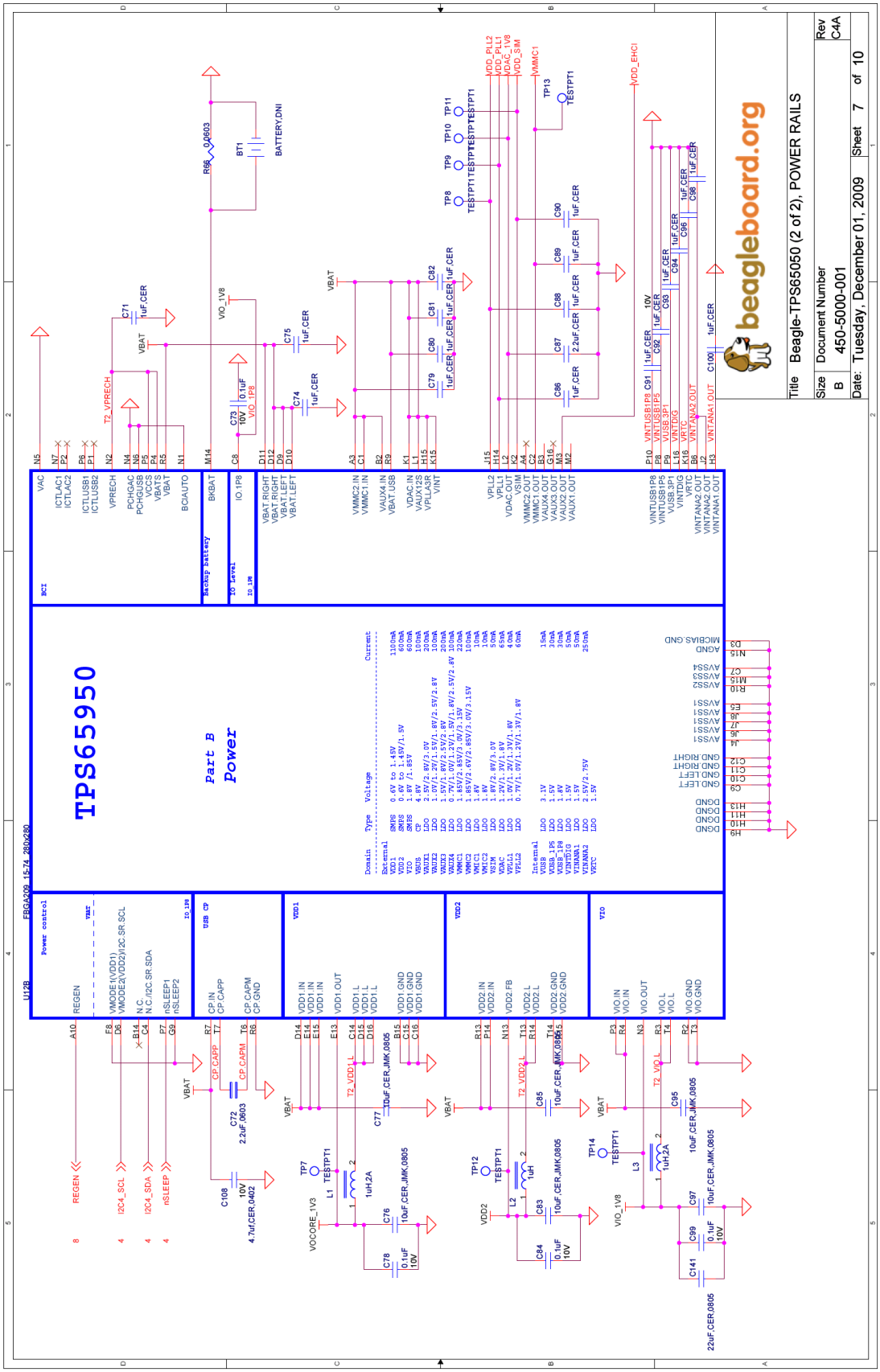
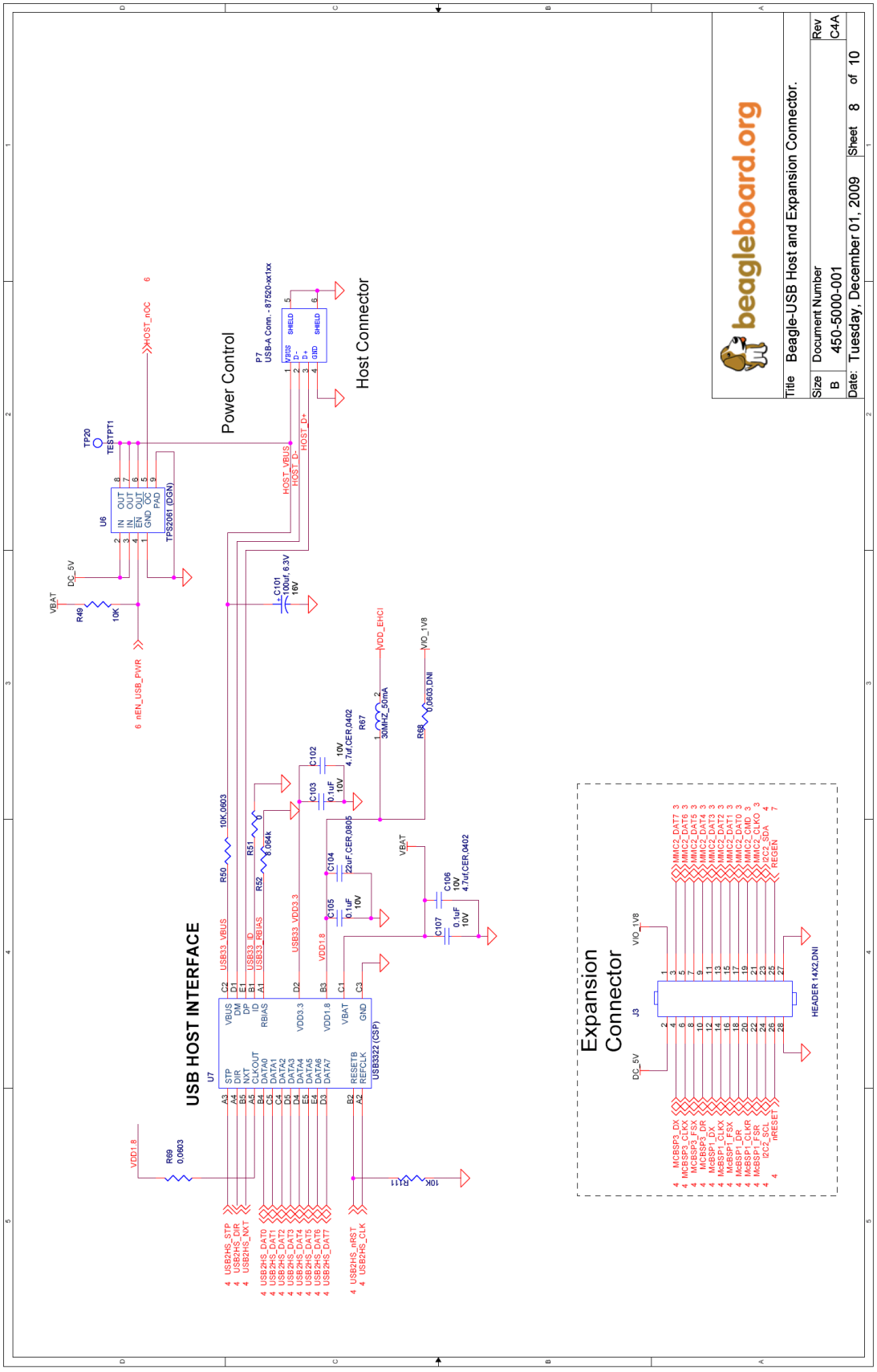
SDRC_D9
SDRC_D8
SDRC_D7
SDRC_D6
SDRC_D5
SDRC_D4
SDRC_D3
SDRC_D2
SDRC_D1
SDRC_D0
GPMC_A10/SYS_nDMAREQ3/GPIO_43
GPMC_A9/SYS_nDMAREQ2/GPIO_42
GPMC_A8/GPIO_41
GPMC_A7/GPIO_40
GPMC_A6/GPIO_39
GPMC_A5/GPIO_38
GPMC_A4/GPIO_37
GPMC_A3/GPIO_36
GPMC_A2/GPIO_35
GPMC_A1/GPIO_34
GPMC_D15/GPIO_51
GPMC_D14/GPIO_50
GPMC_D13/GPIO_49
GPMC_D12/GPIO_48
GPMC_D11/GPIO_47
GPMC_D10/GPIO_46
GPMC_D9/GPIO_45
GPMC_D8/GPIO_44
GPMC_D7
GPMC_D6
GPMC_D5
GPMC_D4
GPMC_D3
GPMC_D2
GPMC_D1
GPMC_D0
GPMC_nCS0
GPMC_nCS1/GPIO_52
GPMC_nCS2/GPIO_53
GPMC_nCS3/SYS_nDMAREQ1/GPIO_54
GPMC_nCS4/SYS_nDMAREQ01/McBSP4_CLKX/GPT9_PWM_EVT/GPIO_55
GPMC_nCS5/SYS_nDMAREQ02/McBSP4_DR/GPT10_PWM_EVT/GPIO_56
GPMC_nCS6/SYS_nDMAREQ03/McBSP4_DX/GPT11_PWM_EVT/GPIO_57
GPMC_nCS7/GPMC_IODIR/McBSP4_FSX/GPT8_PWM_EVT/GPIO_58
GPMC_CLK/GPIO_59
GPMC_nWE
GPMC_nOE
GPMC_nADV_ALE
GPMC_nBE0_CLE/GPIO_60
GPMC_nBE1/GPIO_61
GPMC_nWP/GPIO_62
GPMC_WAIT0
GPMC_WAIT1/GPIO_63
GPMC_WAIT2/GPIO_64
GPMC_WAIT3/SYS_nDMAREQ1/GPIO_65
GPMC_WAIT3/SYS_nDMAREQ1/GPIO_65
UART2_CTS/McBSP3_DX/GPT9_PWMEVT/GPIO_144
UART2_RTS/McBSP3_DR/GPT10_PWMEVT/GPIO_145
UART2_TX/McBSP3_CLKX/GPT11_PWMEVT/GPIO_146
UART2_RX/McBSP3_FSX/GPT8_PWMEVT/GPIO_147
UART3_CTS_RCTX/GPIO_163
UART3_RTS_SD/GPIO_164
UART3_RX_IRRX/GPIO_165
UART3_TX_IRTX/GPIO_166
TP5
SDC_CLK
TESTPT2
TP6
SDC_nCS0
TESTPT2
10 DSS_D0
10 DSS_D1
10 DSS_D2
10 DSS_D3
10 DSS_D4
10 DSS_D5
10 DSS_D6
10 DSS_D7
10 DSS_D8
10 DSS_D9
10 DSS_D10
10 DSS_D11
10 DSS_D12
10 DSS_D13
10 DSS_D14
10 DSS_D15
10 DSS_D16
10 DSS_D17
10 DSS_D18
10 DSS_D19
10 DSS_D20
10 DSS_D21
10 DSS_D22
10 DSS_D23
10 DSS_PCLK
10 DSS_HSYNC
10 DSS_VSYNC
10 DSS_ACBIAS
DSS_D0/DX0/UART1_CTS/DSSVENC656_DATA0/GPIO_70
DSS_D1/DR0/UART1_RTS/DSSVENC656_DATA1/GPIO_71
DSS_D2/DY1/DSSVENC656_DATA2/GPIO_72
DSS_D3/DY1/DSSVENC656_DATA3/GPIO_73
DSS_D4/DX2/UART3_RX_IRRX/DSSVENC656_DATA4/GPIO_74
DSS_D5/DR2/UART3_TX_IRTX/DSSVENC656_DATA5/GPIO_75
DSS_D6/DY2/UART3_RTS_SD/DSSVENC656_DATA6/GPIO_76/HW_DBG14
DSS_D7/UART1_RX/DSSVENC656_DATA7/GPIO_77/HW_DBG15
DSS_D8/GPIO_78/HW_DBG16
DSS_D9/GPIO_79/HW_DBG17
DSS_D10/SDI_DAT1N/GPIO_80
DSS_D11/SDI_DAT1P/GPIO_81
DSS_D12/SDI_DAT2N/GPIO_82
DSS_D13/SDI_DAT2P/GPIO_83
DSS_D14/SDI_DAT3N/GPIO_84
DSS_D15/SDI_DAT3P/GPIO_85
DSS_D16/GPIO_86
DSS_D17/GPIO_87
DSS_D18/SDI_VSYNC/McSPI3_CLK/DSS_D0/GPIO_88
DSS_D19/SDI_HSYNC/McSPI3_SIMO/DSS_D1/GPIO_89
DSS_D20/SDI_DEN/McSPI3_SOMI/DSS_D2/GPIO_90
DSS_D21/SDI_CLKN/McSPI3_CS0/DSS_D3/GPIO_91
DSS_D22/SDI_CLKP/McSPI3_CS1/DSS_D4/GPIO_92
DSS_D23/SDI_CLKN/DSS_D5/GPIO_93
DSS_PCLK/GPIO_66/HW_DBG12
DSS_HSYNC/GPIO_67/HW_DBG13
DSS_VSYNC/GPIO_68
DSS_ACBIAS/GPIO_69
R10
33/0603
MMC1_CLK/MS_CLK/GPIO_120
MMC1_CMD/MS_BS/GPIO_121
MMC1_DAT0/MS_DIO/GPIO_122
MMC1_DAT1/MS_DAT1/GPIO_123
MMC1_DAT2/MS_DAT2/GPIO_124
MMC1_DAT3/MS_DAT3/GPIO_125
MMC1_DAT4/SIM_IO/GPIO_126
MMC1_DAT5/SIM_CLK/GPIO_127
MMC1_DAT6/SIM_PWRCTRL/GPIO_128
MMC1_DAT7/SIM_RST/GPIO_129
MMC2_CLK/McSPI3_CLK/GPIO_130
MMC2_CMD/McSPI3_SIMO/GPIO_131
MMC2_DAT0/McSPI3_SOMI/GPIO_132
MMC2_DAT1/GPIO_133
MMC2_DAT2/McSPI3_CS1/GPIO_134
MMC2_DAT3/McSPI3_CS0/GPIO_135
MMC2_DAT4/UART3_RX_IRRX/GPIO_136/MMC3_DAT0/GPIO_136
MMC2_DAT5/MMC2_DIR_DAT1/CAM_GLOBAL_RESET/MMC3_DAT1/GPIO_137/HSUSB3_TLL_STP/MM3_RXDP
MMC2_DAT6/MMC2_DIR_CMD/CAM_SHUTTER/MMC3_DAT2/GPIO_138/HSUSB3_TLL_DIR
MMC2_DAT7/MMC2_CLKIN/MMC3_DAT3/GPIO_139/HSUSB3_TLL_NXT/MM3_RXDM
8 MMC2_CLKO
8 MMC2_CMD
8 MMC2_DAT0
8 MMC2_DAT1
8 MMC2_DAT2
8 MMC2_DAT3
8 MMC2_DAT4
8 MMC2_DAT5
8 MMC2_DAT6
8 MMC2_DAT7

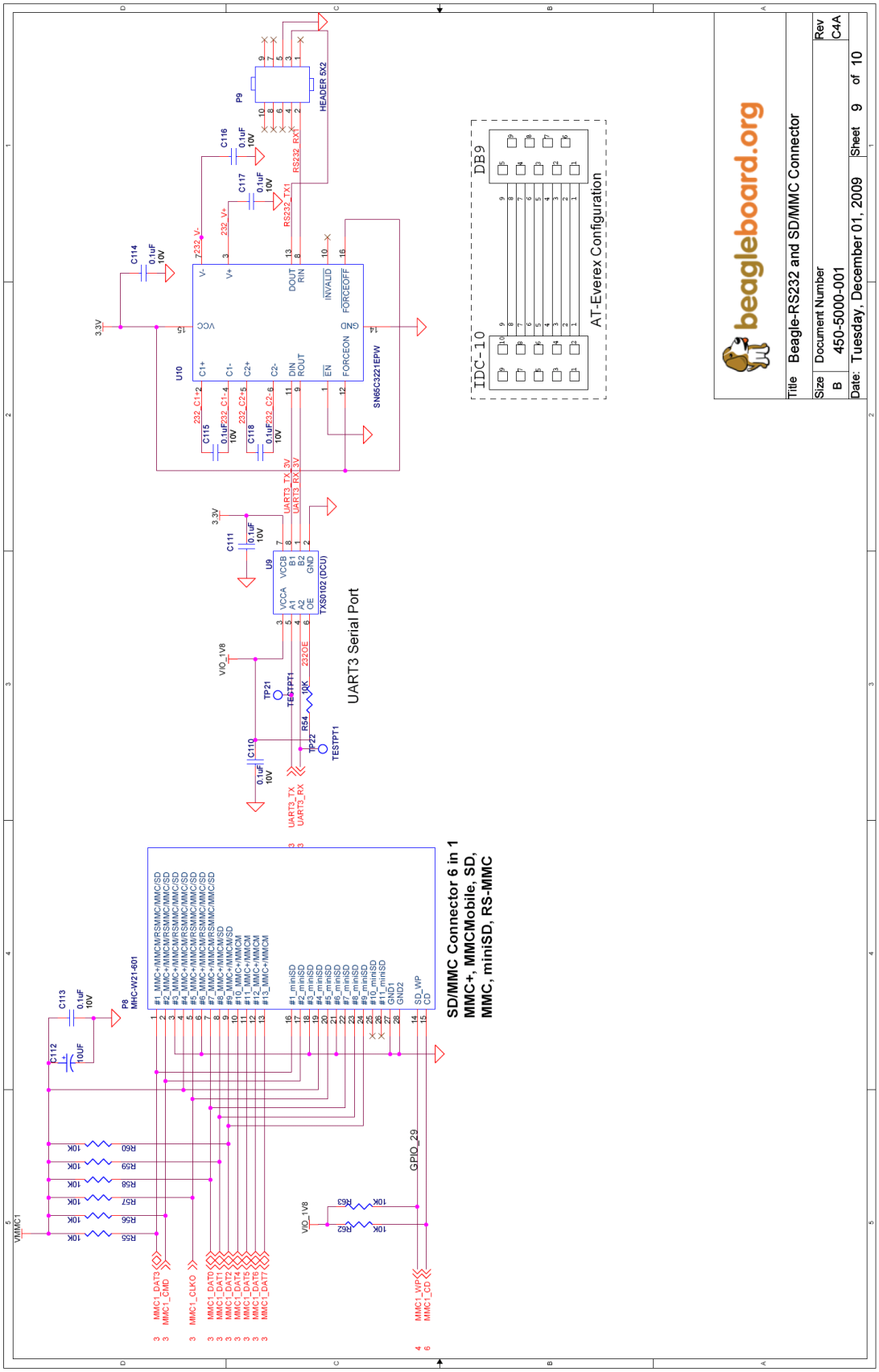

beagleboard.org
Title Beagle-OMAP3530 Processor (2 of 3)
Size C
Document Number 450-5000-001
Rev C4A
Date: Tuesday, December 01, 2009
Sheet 4 of 10
NAND BOOT.....RA RD
ONE NAND BOOT...RB RC
BOOT_0b01111 NAND USB UART MMC1
PERH_0b01111 USB UART MMC1 NAND
BOOT_0b10000 OneNAND USB UART MMC1
PERH_0b10000 USB UART MMC1 OneNAND
Resistor are loaded based upon POP memory type. Default for this revision is NAND.
USER
Hold S1 down while pressing and releasing S2. This will force a peripheral boot. S2 can also be used as a switch for applications or SW use after booting.
USER1
USER0
COLD RESET
Pressing and releasing S2 will reset ARM Processor.
EMULATOR PULL UP/DOWN RESISTORS
14 PIN JTAG INTERFACE
TV/S-Video Conn
Insures that the DVI-D is powered down at powerup.

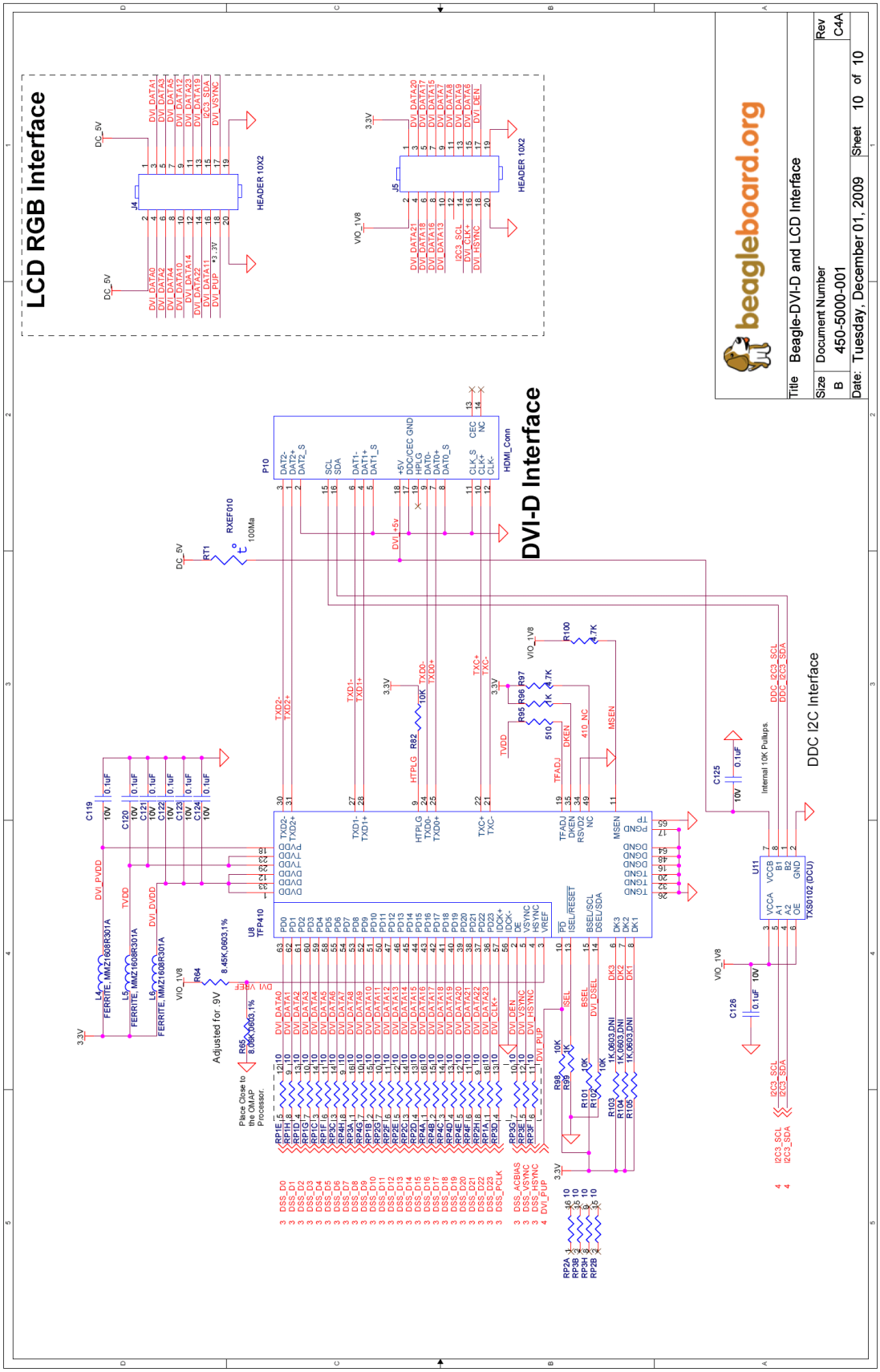

beagleboard.org
Title Beagle-OMAP3530 Processor (3 of 3)
Size C
Document Number 450-5000-001
Rev C4A
Date Tuesday, December 01, 2009
Sheet 5 of 10


TPS65950
PART A
beagleboard.org
Title Beagle-TPS65950 (1 of 2)
Size B
Document Number 450-5000-001
Rev C4A
Date: Tuesday, December 01, 2009
Sheet 6 of 10


TPS65950
Part B
Power
beagleboard.org
Title Beagle-TPS65050 (2 of 2), POWER RAILS
Size B
Document Number 450-5000-001
Rev C4A
Date: Tuesday, December 01, 2009
Sheet 7 of 10


USB HOST INTERFACE
Power Control
Host Connector
Expansion Connector
beagleboard.org
Title Beagle-USB Host and Expansion Connector.
Size B
Document Number 450-5000-001
Rev C4A
Date: Tuesday, December 01, 2009
Sheet 8 of 10


UART3 Serial Port
SD/MMC Connector 6 in 1
MMC+, MMCMobile, SD,
MMC, miniSD, RS-MMC
AT-Everex Configuration
beagleboard.org
Title Beagle-RS232 and SD/MMC Connector
Size B
Document Number 450-5000-001
Rev C4A
Date: Tuesday, December 01, 2009
Sheet 9 of 10


LCD RGB Interface
DVI-D Interface
DDC I2C Interface
HEADER 10X2
HDMI_Conn
TXS0102 (DCU)
beagleboard.org
Title Beagle-DVI-D and LCD Interface
Size B
Document Number 450-5000-001
Rev C4A
Date: Tuesday, December 01, 2009
Sheet 10 of 10
Adjusted for .9V
Place Close to the OMAP Processor.
Internal 10K Pullups

17.0 Bills of Material

The Bill of Material for the Beagle Board is provided at BeagleBoard.org at the following location:

http://beagleboard.org/hardware/design

*These design materials are ***NOT SUPPORTED*** and **DO NOT** constitute a reference design. Only "community" support is allowed via resources at BeagleBoard.org/discuss. THERE IS NO WARRANTY FOR THE DESIGN MATERIALS, TO THE EXTENT PERMITTED BY APPLICABLE LAW. EXCEPT WHEN OTHERWISE STATED IN WRITING THE COPYRIGHT HOLDERS AND/OR OTHER PARTIES PROVIDE THE DESIGN MATERIALS "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. THE ENTIRE RISK AS TO THE QUALITY AND PERFORMANCE OF THE DESIGN MATERIALS IS WITH YOU. SHOULD THE DESIGN MATERIALS PROVE DEFECTIVE, YOU ASSUME THE COST OF ALL NECESSARY SERVICING, REPAIR OR CORRECTION.*
We mean it; these design materials may be totally unsuitable for any purposes.

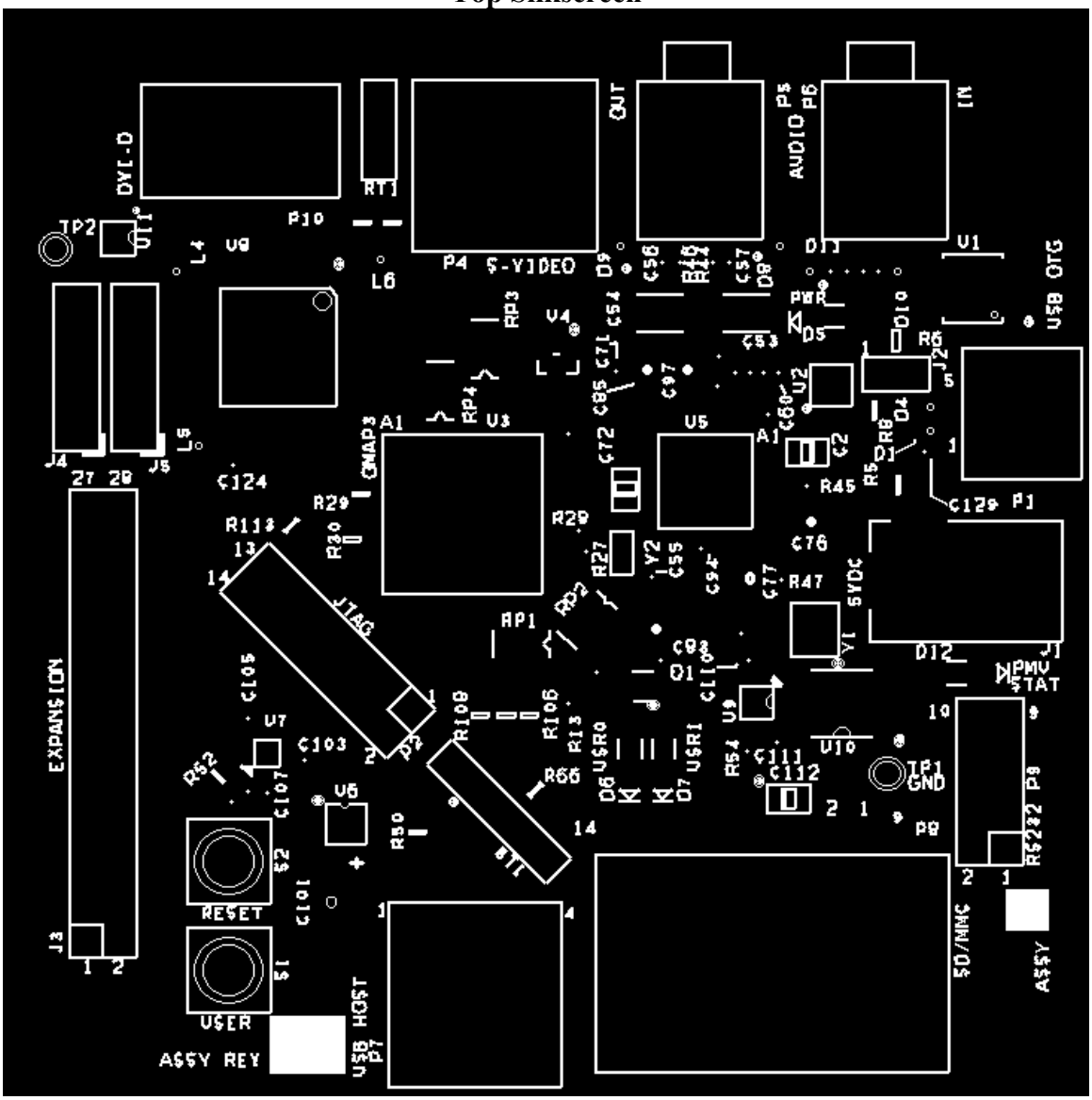
18.0 PCB Information

The following pages contain the PDF PCB layers for the BeagleBoard. Gerber files and Allegro source files are available on BeagleBoard.org at the following address.

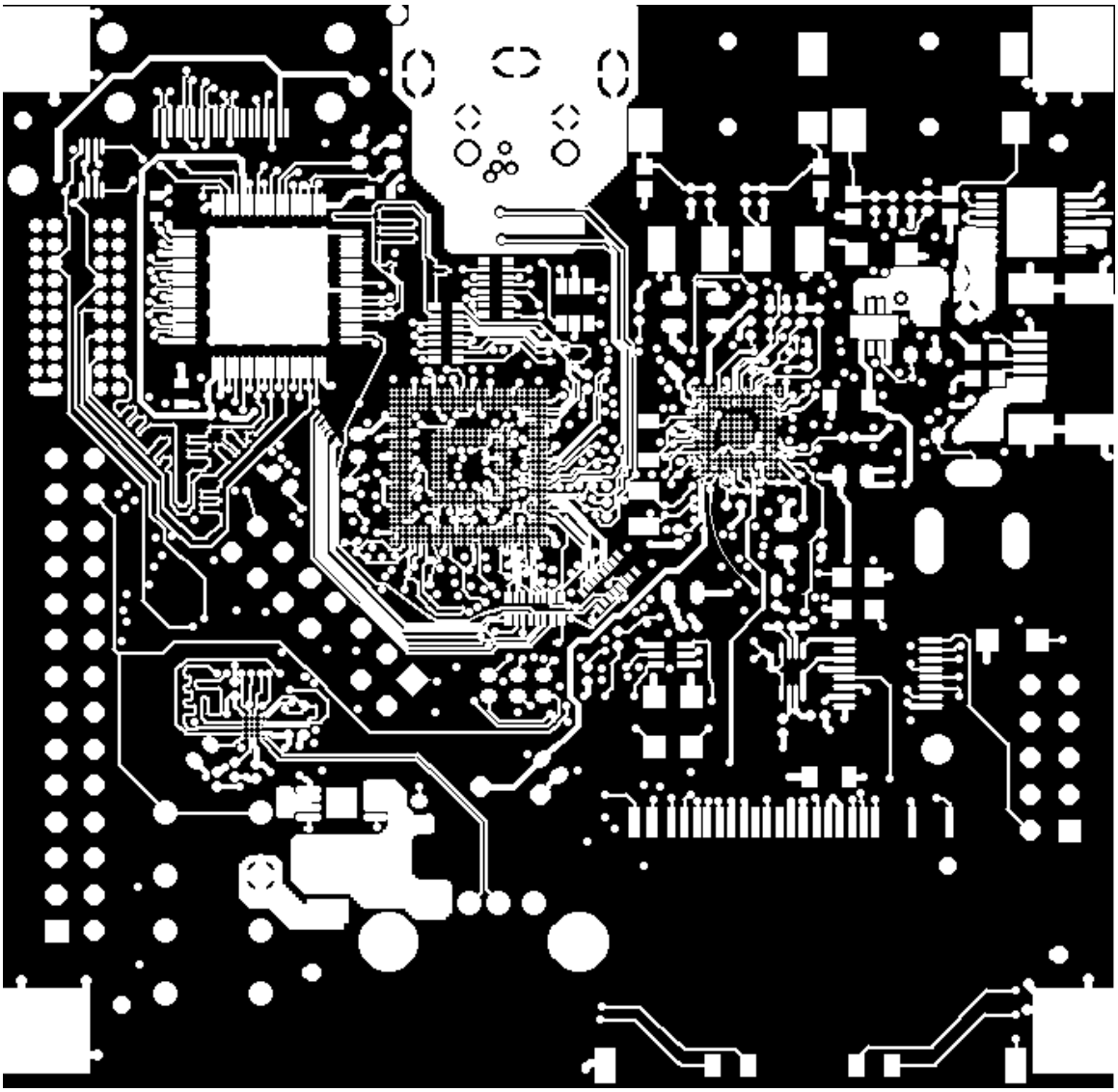
http://beagleboard.org/hardware/design

*These design materials are ***NOT SUPPORTED*** and **DO NOT** constitute a reference design. Only "community" support is allowed via resources at BeagleBoard.org/discuss. THERE IS NO WARRANTY FOR THE DESIGN MATERIALS, TO THE EXTENT PERMITTED BY APPLICABLE LAW. EXCEPT WHEN OTHERWISE STATED IN WRITING THE COPYRIGHT HOLDERS AND/OR OTHER PARTIES PROVIDE THE DESIGN MATERIALS "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. THE ENTIRE RISK AS TO THE QUALITY AND PERFORMANCE OF THE DESIGN MATERIALS IS WITH YOU. SHOULD THE DESIGN MATERIALS PROVE DEFECTIVE, YOU ASSUME THE COST OF ALL NECESSARY SERVICING, REPAIR OR CORRECTION.*
We mean it; these design materials may be totally unsuitable for any purposes.

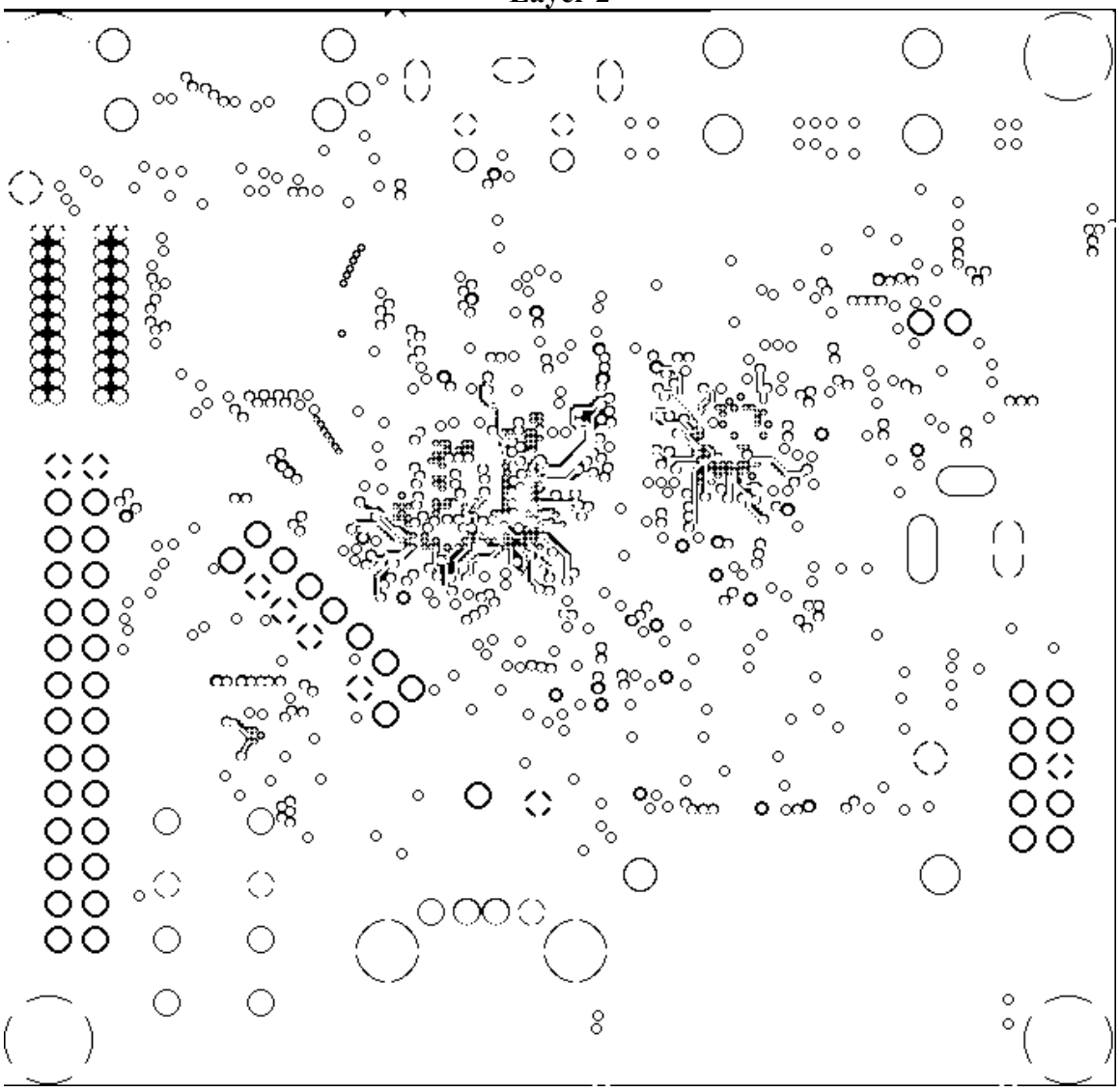
Top Silkscreen



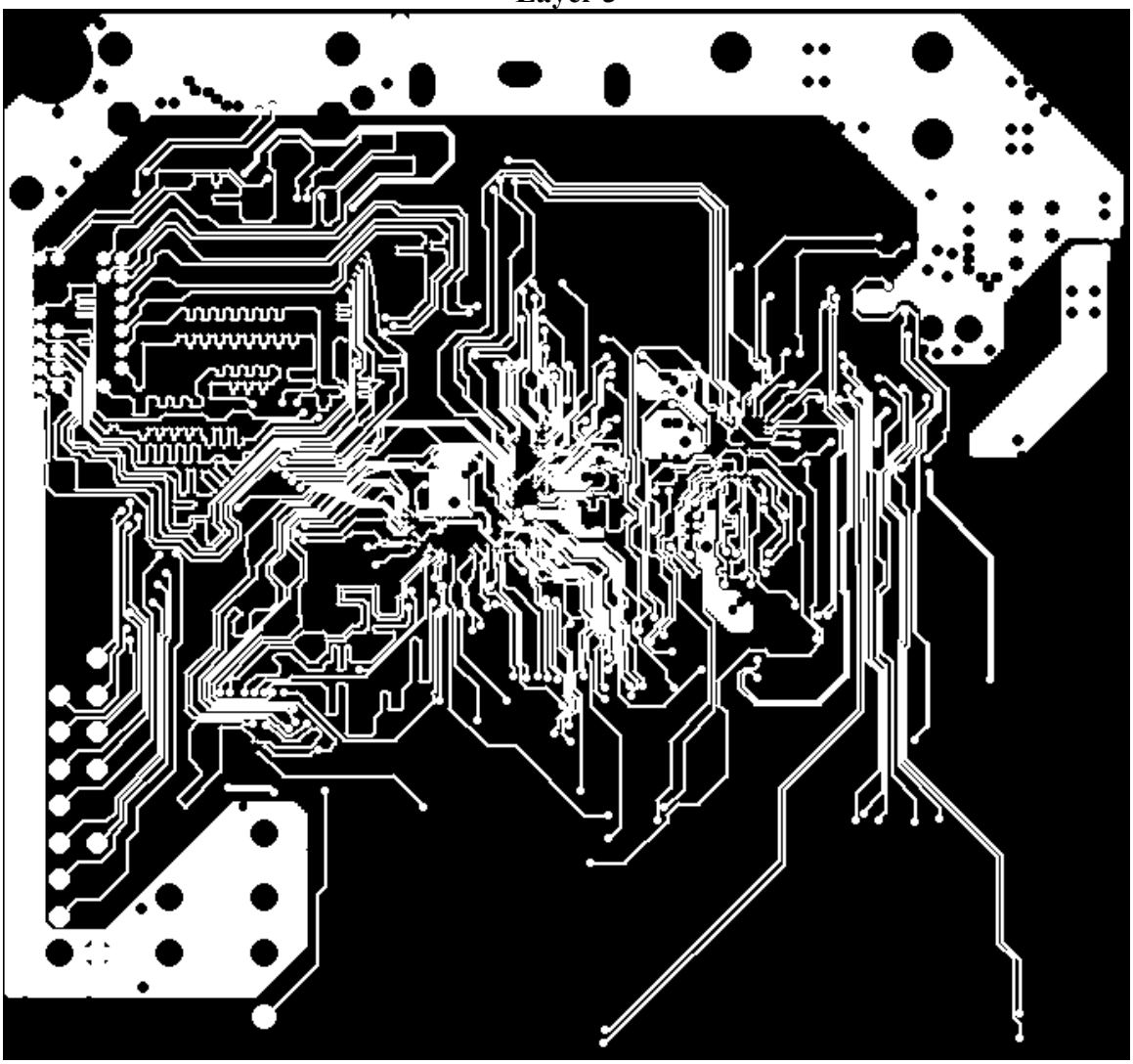
Layer 1



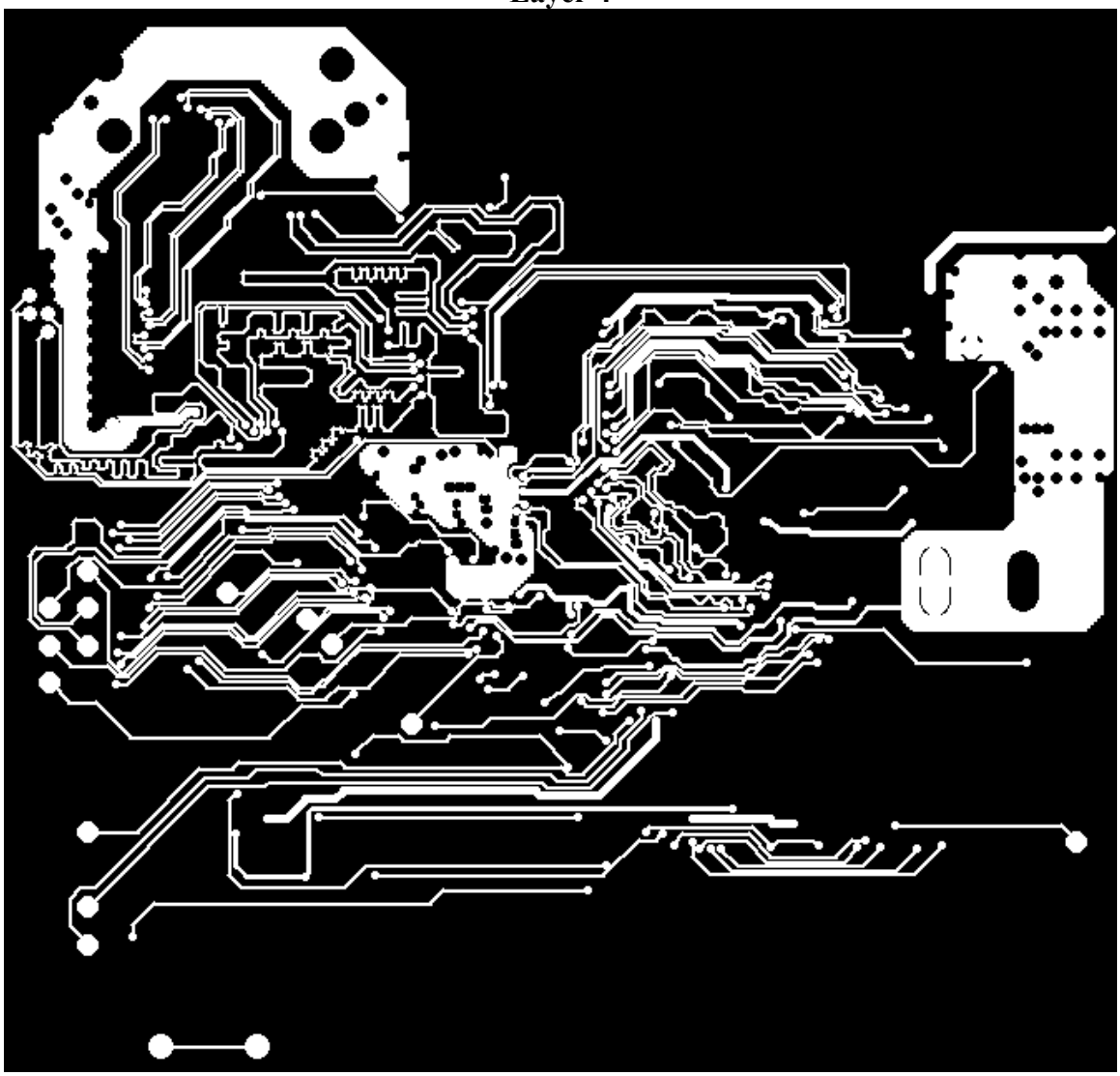
Layer 2



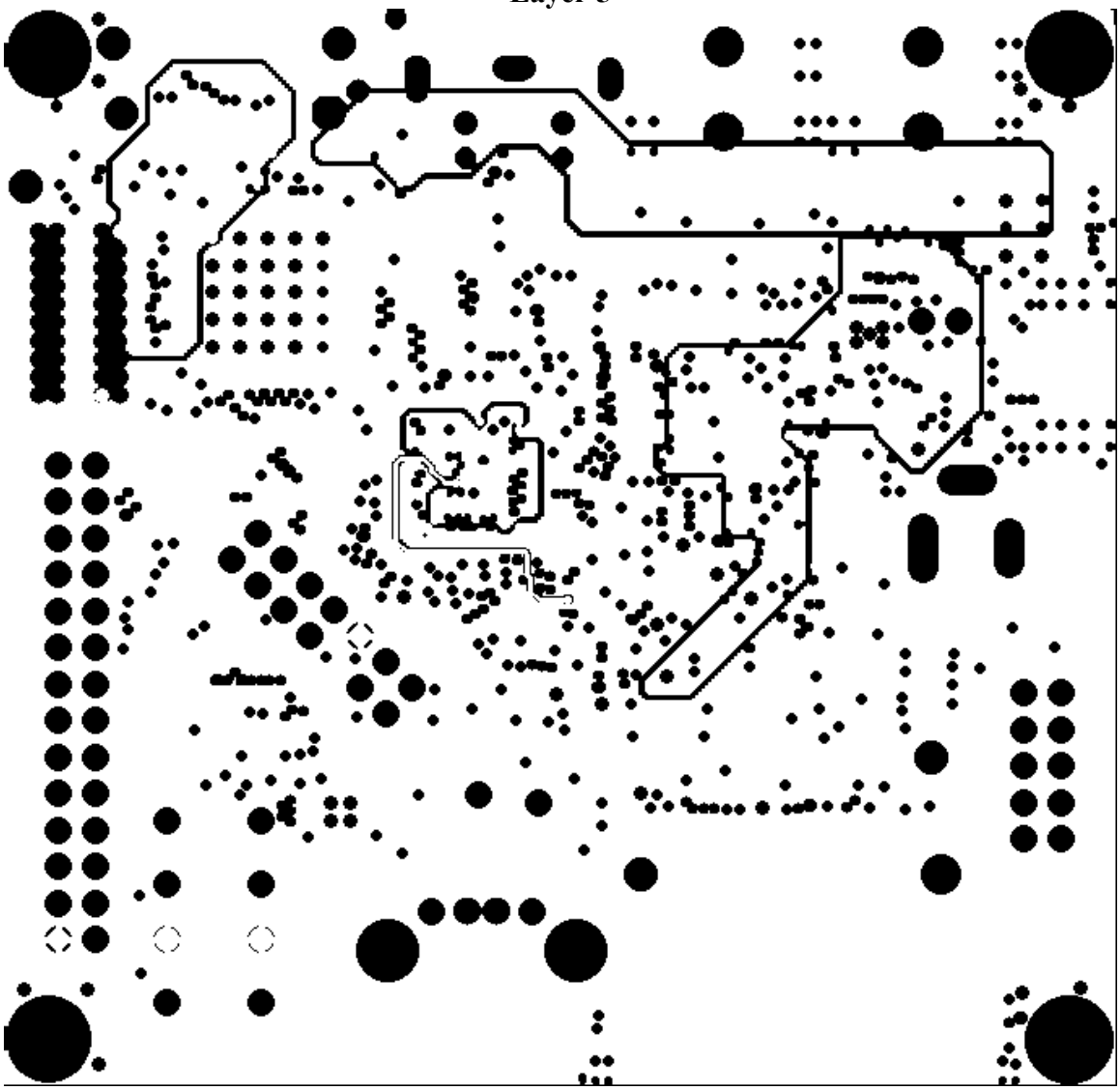
Layer 3



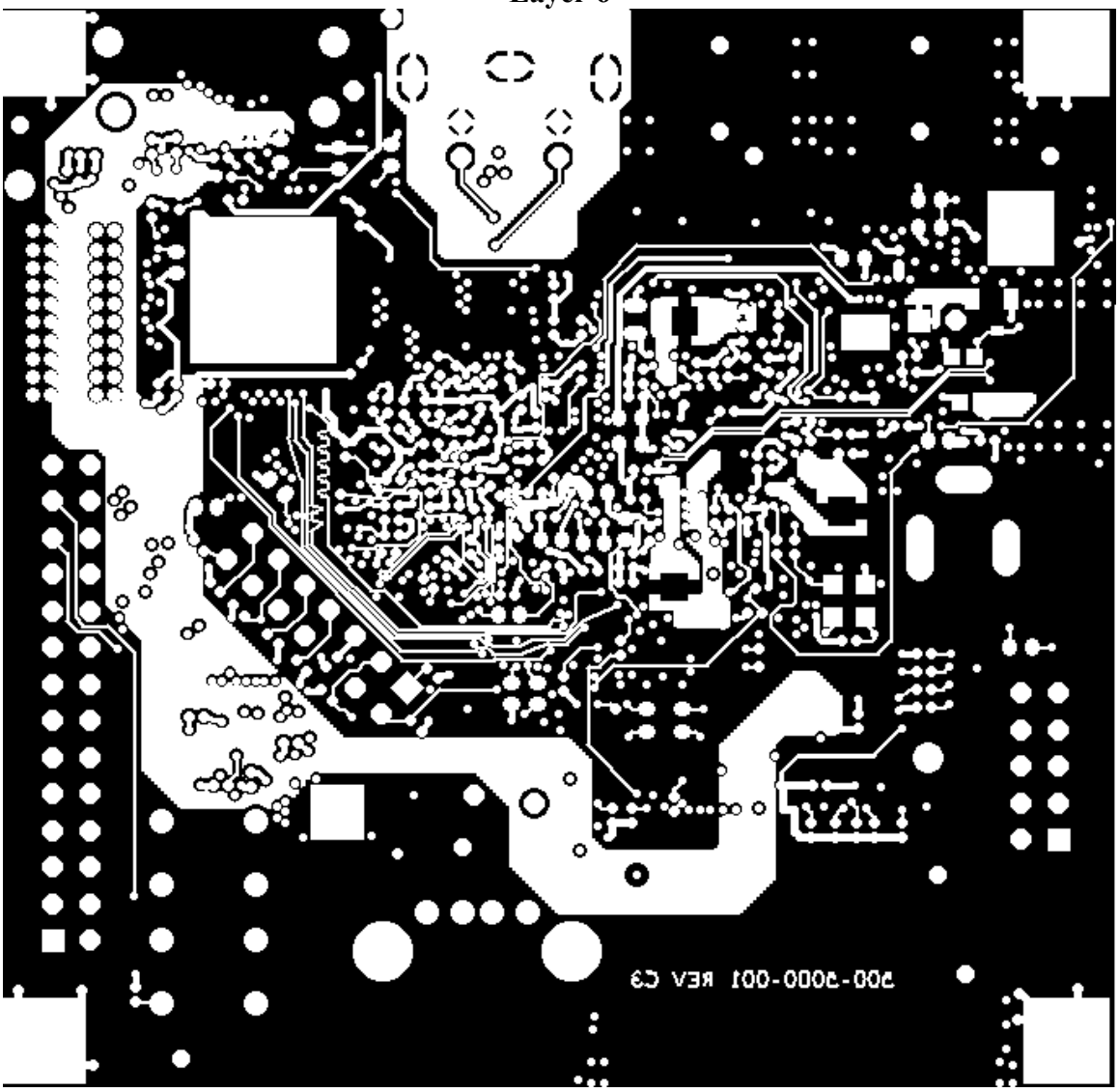
Layer 4



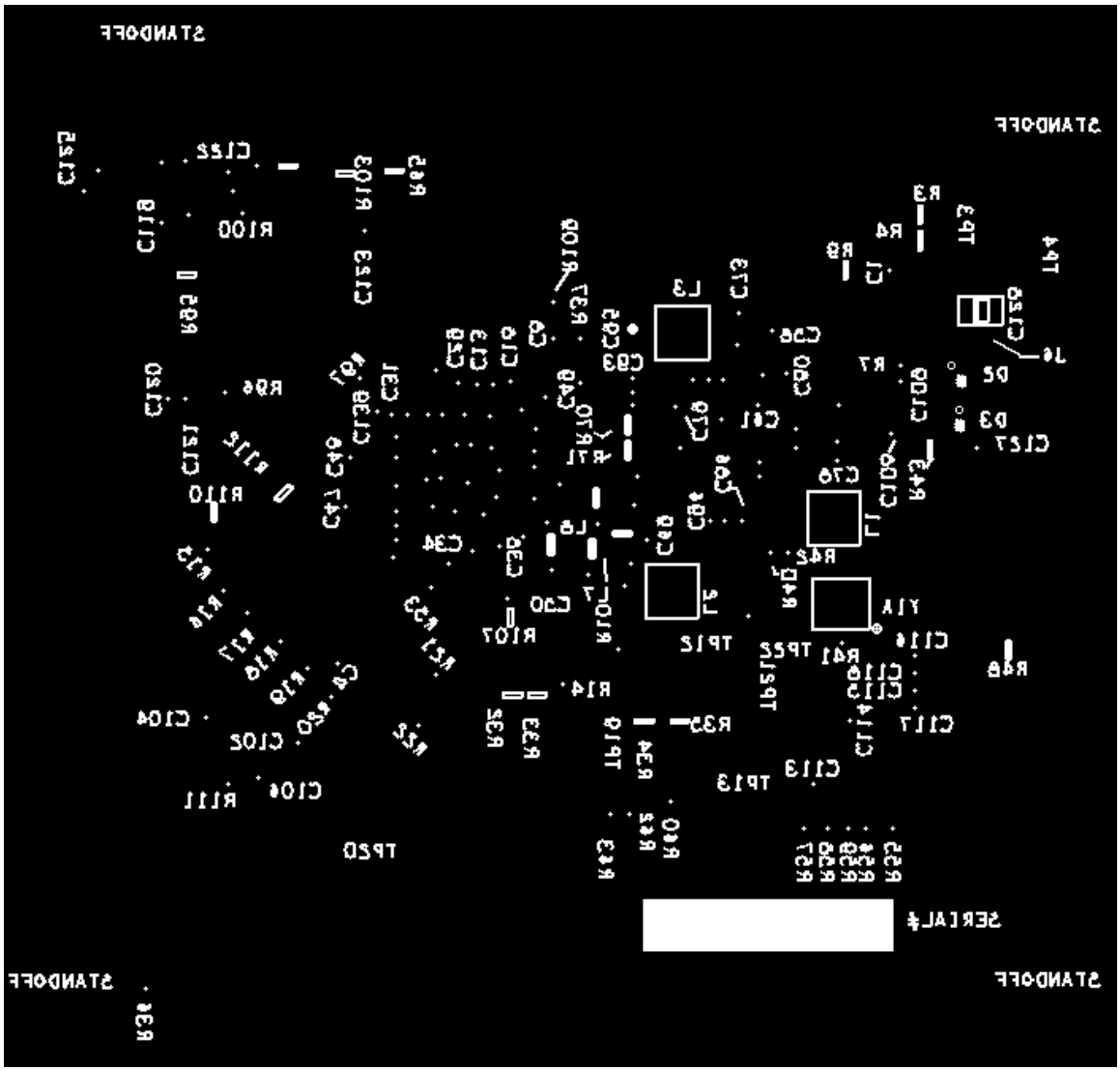
Layer 5



Layer 6



Bottom Silkscreen



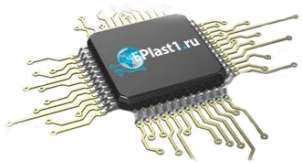
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.