

# SSM3K7002BFU

High-Speed Switching Applications

Analog Switch Applications

- Small package
- Low ON-resistance :  $R_{DS(ON)} = 3.3 \Omega$  (max) (@ $V_{GS} = 4.5 V$ )  
 :  $R_{DS(ON)} = 2.6 \Omega$  (max) (@ $V_{GS} = 5 V$ )  
 :  $R_{DS(ON)} = 2.1 \Omega$  (max) (@ $V_{GS} = 10 V$ )

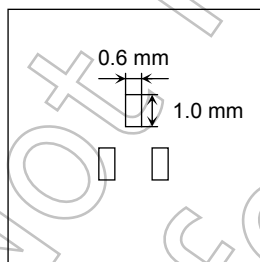
## Absolute Maximum Ratings (Ta = 25°C)

| Characteristics                     |       | Symbol         | Rating     | Unit |
|-------------------------------------|-------|----------------|------------|------|
| Drain-source voltage                |       | $V_{DSS}$      | 60         | V    |
| Gate-source voltage                 |       | $V_{GSS}$      | $\pm 20$   | V    |
| Drain current                       | DC    | $I_D$          | 200        | mA   |
|                                     | Pulse | $I_{DP}$       | 800        |      |
| Drain power dissipation (Ta = 25°C) |       | $P_D$ (Note 1) | 150        | mW   |
| Channel temperature                 |       | $T_{ch}$       | 150        | °C   |
| Storage temperature range           |       | $T_{stg}$      | -55 to 150 | °C   |

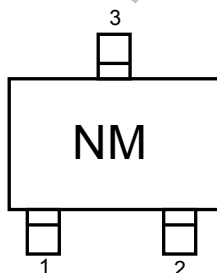
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

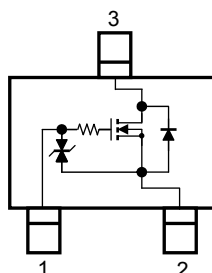
Note 1: mounted on FR4 board  
 (25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.6mm<sup>2</sup> × 3)



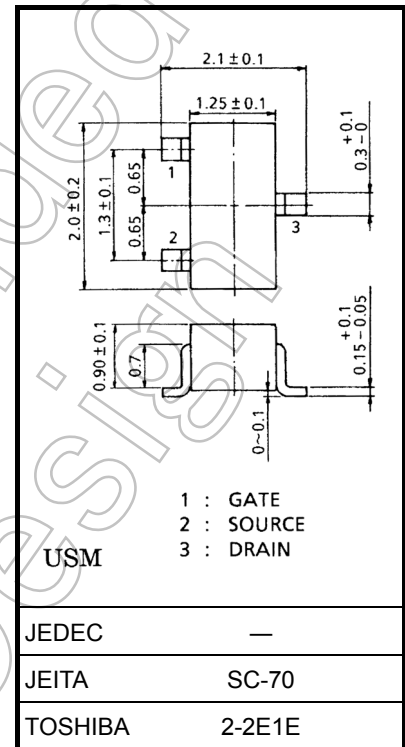
## Marking



## Equivalent Circuit (top view)



Unit: mm



Weight: 6.0 mg (typ.)

Start of commercial production  
 2009-07

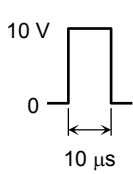
**Electrical Characteristics (Ta = 25°C)**

| Characteristics                | Symbol              | Test Condition  | Min | Typ   | Max      | Unit          |
|--------------------------------|---------------------|---|-----|-------|----------|---------------|
| Gate leakage current           | $I_{GSS}$           | $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$                               | —   | —     | $\pm 10$ | $\mu\text{A}$ |
| Drain-source breakdown voltage | $V_{(BR)DSS}$       | $I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$                                     | 60  | —     | —        | V             |
|                                | $V_{(BR)DSX}$       | $I_D = 10\text{ mA}, V_{GS} = -10\text{ V}$                                   | 45  | —     | —        |               |
| Drain cutoff current           | $I_{DSS}$           | $V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$                                   | —   | —     | 1        | $\mu\text{A}$ |
| Gate threshold voltage         | $V_{th}$            | $V_{DS} = 10\text{ V}, I_D = 0.25\text{ mA}$                                  | 1.5 | —     | 3.1      | V             |
| Forward transfer admittance    | $ Y_{fs} $          | $V_{DS} = 10\text{ V}, I_D = 200\text{ mA}$ (Note 2)                          | 225 | —     | —        | mS            |
| Drain-source ON-resistance     | $R_{DS(ON)}$        | $I_D = 500\text{ mA}, V_{GS} = 10\text{ V}$ (Note 2)                          | —   | 1.62  | 2.1      | $\Omega$      |
|                                |                     | $I_D = 100\text{ mA}, V_{GS} = 5\text{ V}$ (Note 2)                           | —   | 1.90  | 2.6      |               |
|                                |                     | $I_D = 100\text{ mA}, V_{GS} = 4.5\text{ V}$ (Note 2)                         | —   | 2.10  | 3.3      |               |
| Input capacitance              | $C_{iss}$           | $V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$                 | —   | 17.0  | —        | pF            |
| Reverse transfer capacitance   | $C_{rss}$           |   | —   | 1.9   | —        |               |
| Output capacitance             | $C_{oss}$           |   | —   | 3.6   | —        |               |
| Switching time                 | Turn-on delay time  | $V_{DD} = 30\text{ V}, I_D = 200\text{ mA}, V_{GS} = 0\text{ to }10\text{ V}$ | —   | 3.3   | 6.6      | ns            |
|                                | Turn-off delay time |   | —   | 14.5  | 40       |               |
| Drain-source forward voltage   | $V_{DSF}$           | $I_D = -200\text{ mA}, V_{GS} = 0\text{ V}$ (Note 2)                          | —   | -0.84 | -1.2     | V             |

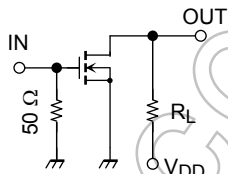
Note2: Pulse test

**Switching Time Test Circuit**

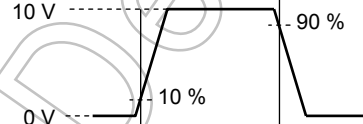
**(a) Test circuit**



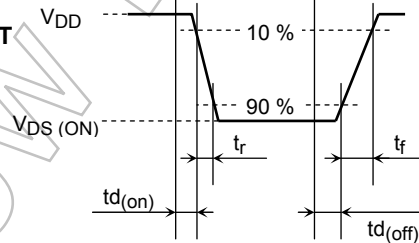
$V_{DD} = 30\text{ V}$   
 Duty  $\leq 1\%$   
 $V_{IN}$ :  $t_r, t_f < 2\text{ ns}$   
 ( $Z_{out} = 50\ \Omega$ )  
 Common Source  
 $T_a = 25\text{ }^\circ\text{C}$



**(b)  $V_{IN}$**



**(c)  $V_{OUT}$**

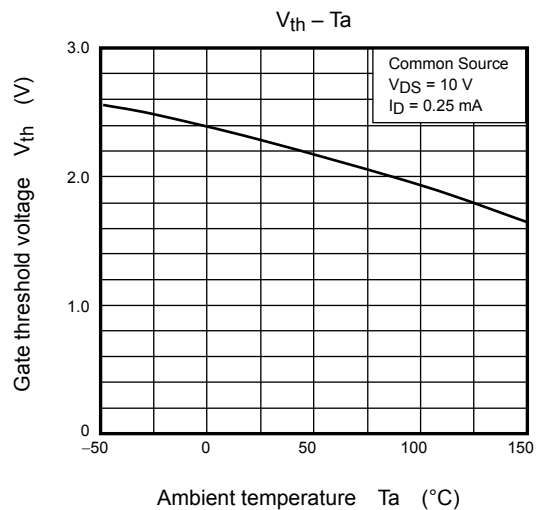
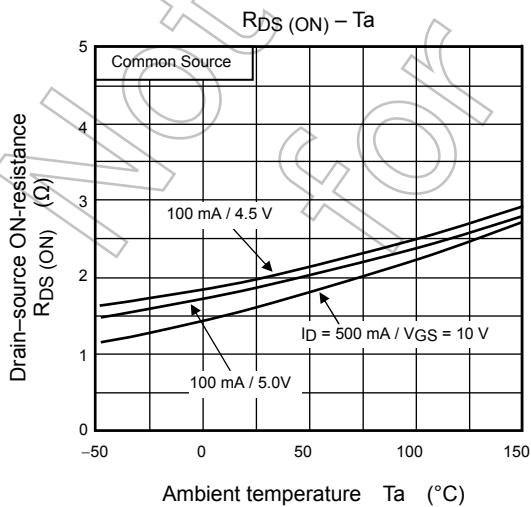
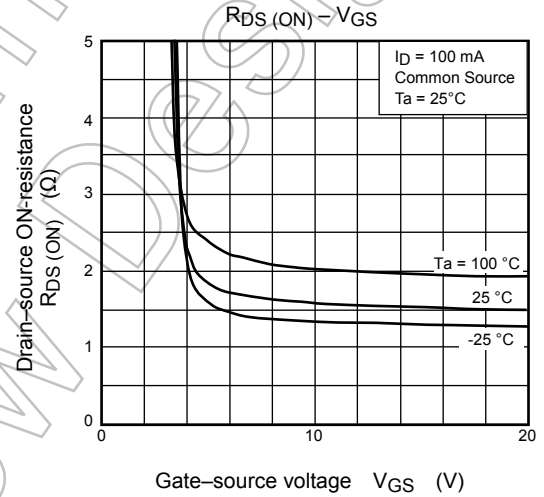
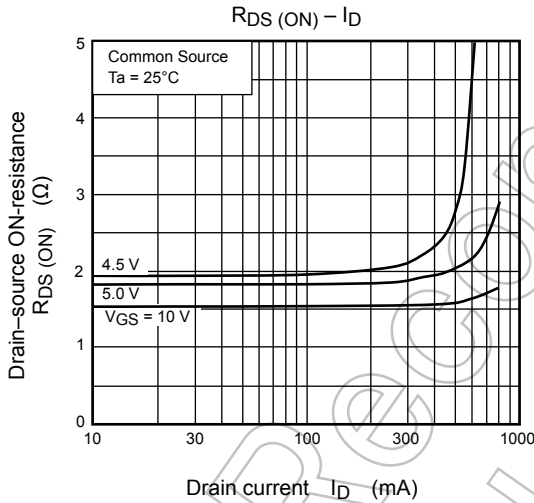
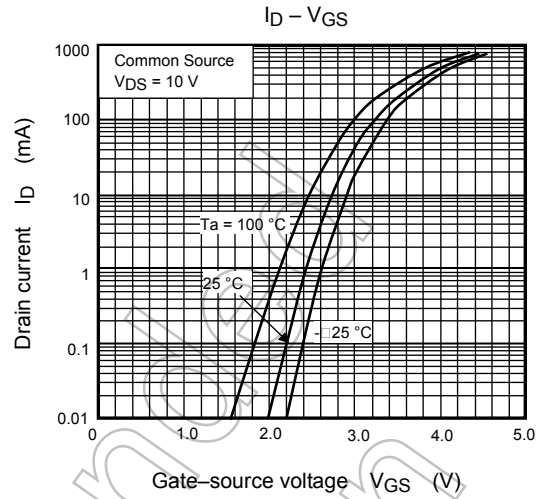
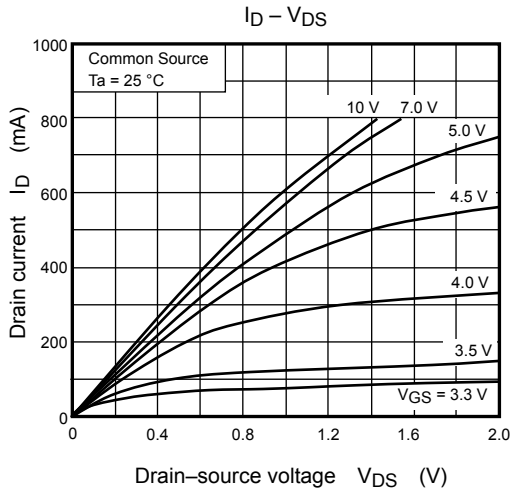


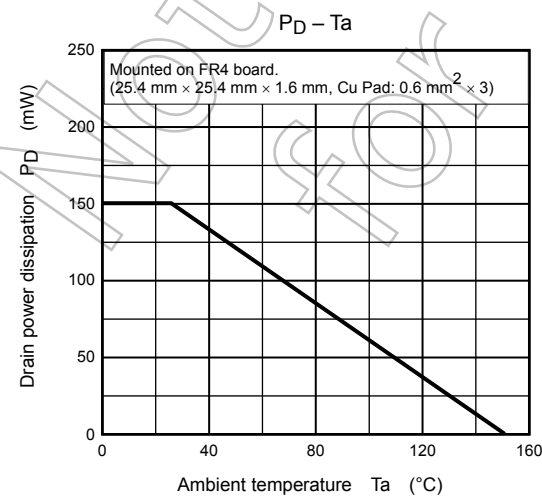
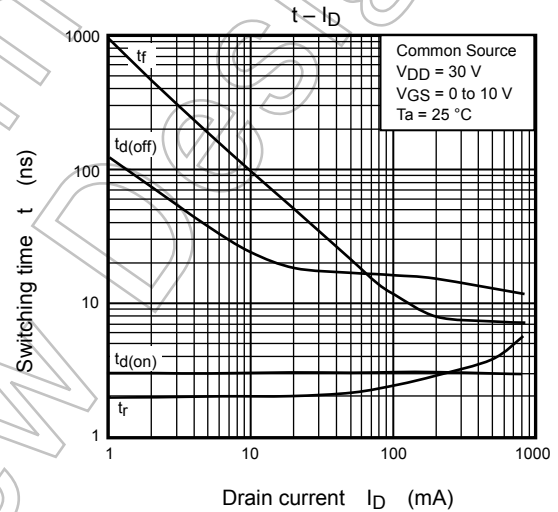
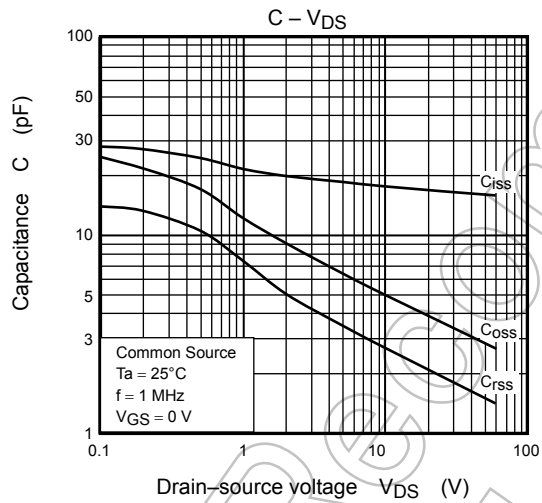
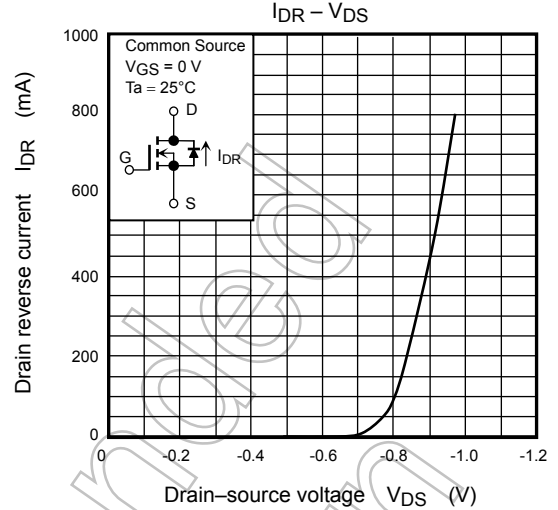
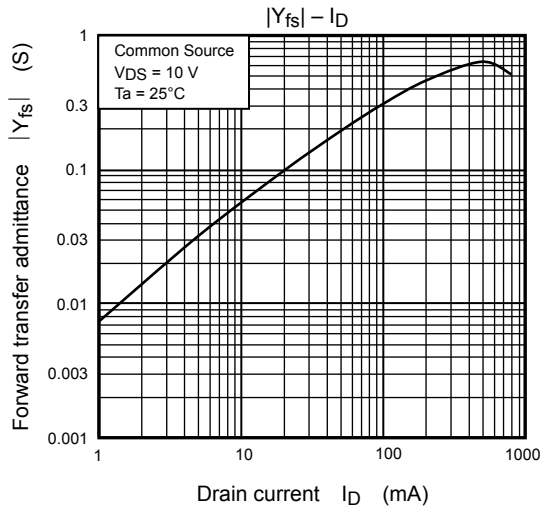
**Precaution**

Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to be low (0.25 mA for the SSM3K7002BFU). Then, for normal switching operation,  $V_{GS(on)}$  must be higher than  $V_{th}$ , and  $V_{GS(off)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(off)} < V_{th} < V_{GS(on)}$ . Take this into consideration when using the device

**Handling Precaution**

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.





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