PESD3V3L4BHC

4-fold bidirectional ESD protection array

7 June 2019 **Product data sheet**

1. General description

4-fold bidirectional ElectroStatic Discharge (ESD) protection array designed to protect up to four lines from the damage caused by ESD and other transients.

The device is housed in a leadless extremely thin small DFN1308-6 (SOT8006) Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- Bidirectional ESD protection of up to 4 lines
- Very high surge robustness; I_{PP} = 6 A for 8/20 µs pulse
- Very low clamping voltage: V_{CL} = 7.3 V typ. for 6 A 8/20 µs pulse
- ESD protection up to 20 kV
- Very low dynamic resistance R_{dyn} = 0.2 Ω (TLP)

3. Applications

ESD protection for low-speed lines in portable communication, consumer devices and computing devices.

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	3.3	V
I_{PPM}	rated peak pulse current	t_p = 8/20 µs; T_{amb} = 25 °C	[1]	-	-	6	A
V_{t1}	trigger voltage	T_{amb} = 25 °C		-	6.7	-	V

[1] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.

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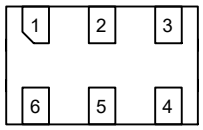
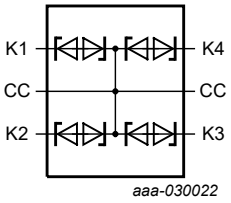
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 DFN1308-6 (SOT8006)	
2	CC	common cathode		
3	K2	cathode (diode 2)		
4	K3	cathode (diode 3)		
5	CC	common cathode		
6	K4	cathode (diode 4)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD3V3L4BHC	DFN1308-6	DFN1308-6, plastic, leadless extremely thin small package; 6 terminals; body 1.3 x 0.8 x 0.38 mm	SOT8006

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD3V3L4BHC	L4

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134)

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	rated peak pulse current	t_p = 8/20 µs; T_{amb} = 25 °C	[1]	-	6	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[2]	-	20	kV
		IEC 61000-4-2 (air discharge)	[2]	-	20	kV

[1] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[2] Device stressed with ten non-repetitive ESD pulses.

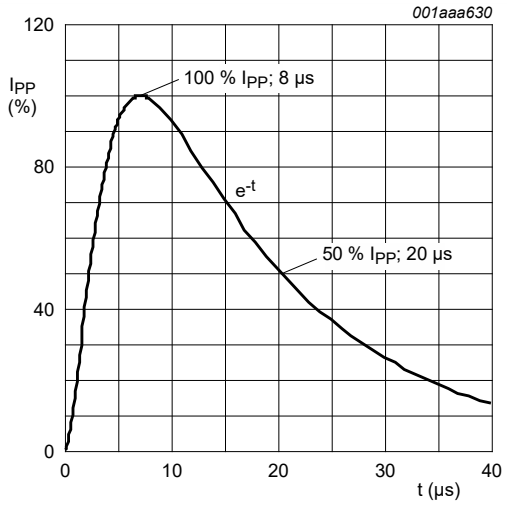


Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5

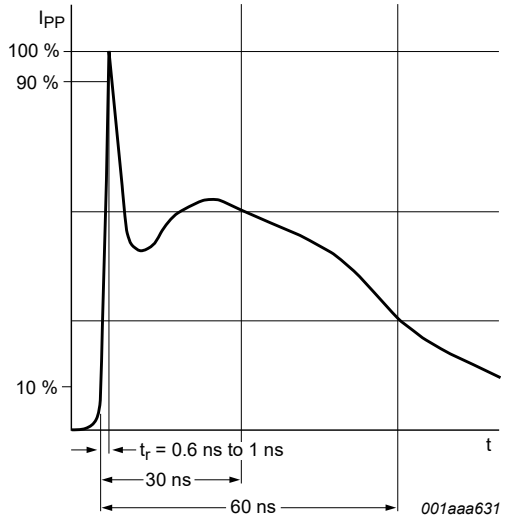


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	3.3	V
I_{RM}	reverse leakage current	V_{RWM} = 3.3 V; T_{amb} = 25 °C		-	3	100	nA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	7.2	9	pF
V_{CL}	clamping voltage	I_{PPM} = 1 A; t_p = 8/20 µs; T_{amb} = 25 °C	[1]	-	5.9	-	V
		I_{PPM} = 6 A; t_p = 8/20 µs; T_{amb} = 25 °C	[1]	-	7.3	8.5	V
R_{dyn}	dynamic resistance	I_R = 10 A; T_{amb} = 25 °C	[2]	-	0.2	-	Ω
V_{t1}	trigger voltage	T_{amb} = 25 °C		-	6.7	-	V
V_h	holding voltage			4	-	-	V

[1] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[2] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI/ESD STM5.5.1-2008.

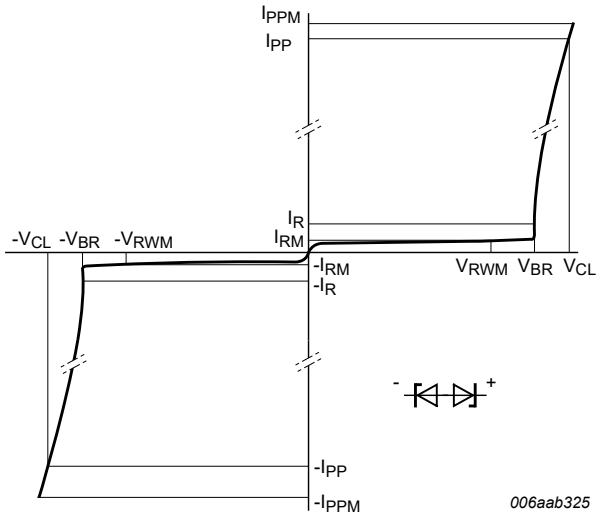
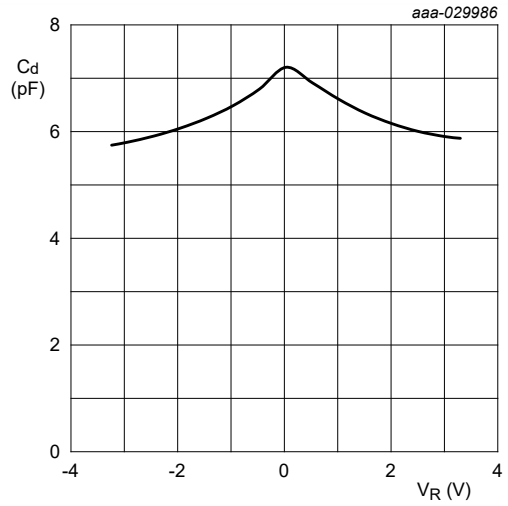
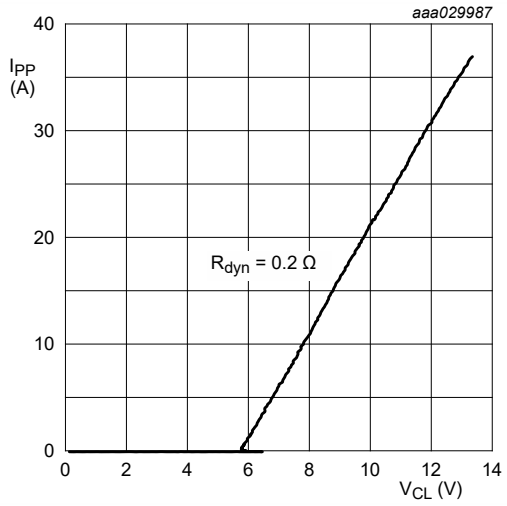


Fig. 3. V-I characteristics for a bidirectional ESD protection diode



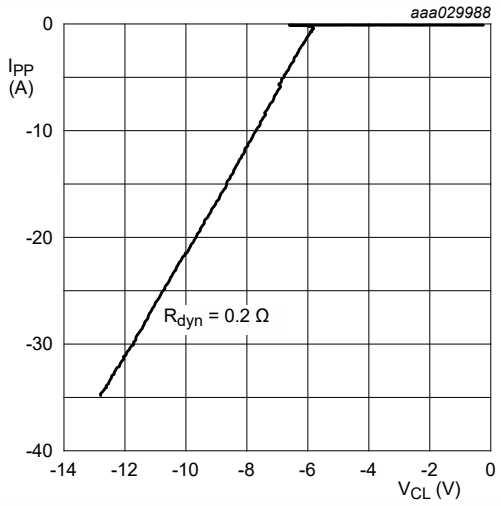
f = 1 MHz; T_{amb} = 25 °C

Fig. 4. Diode capacitance as a function of reverse voltage; typical values



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 5. Positive clamping voltage (TLP); typical values



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 6. Negative clamping voltage (TLP); typical values

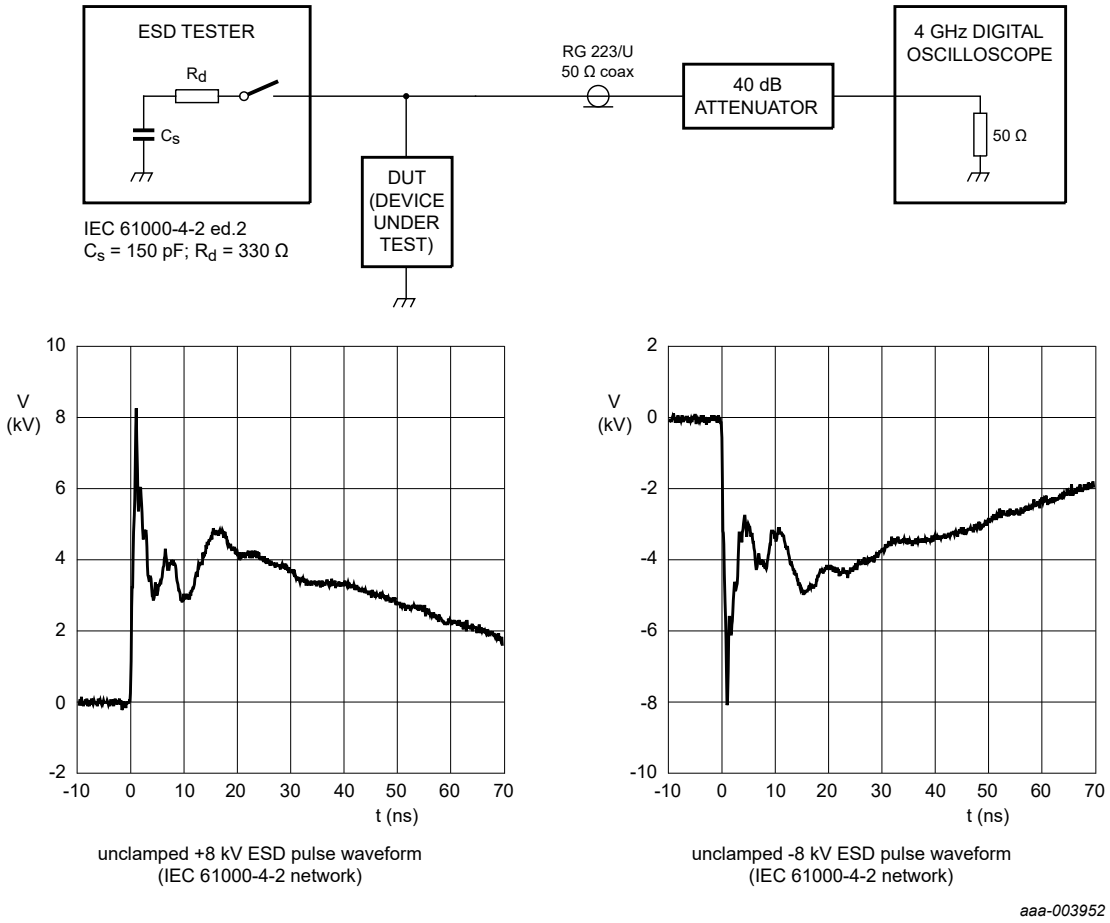


Fig. 7. ESD clamping test setup and waveforms

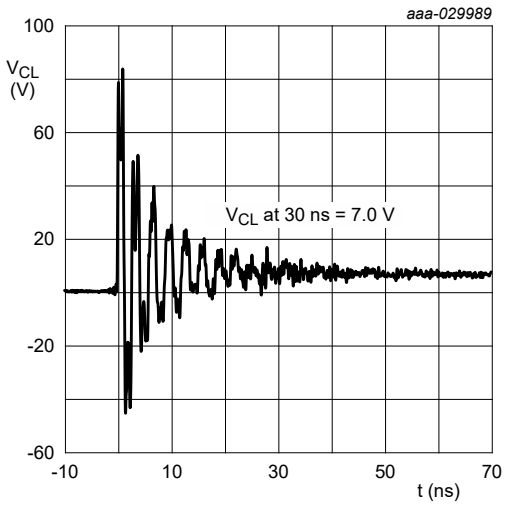


Fig. 8. Clamped +8 kV pulse waveform (IEC 61000-4-2 network)

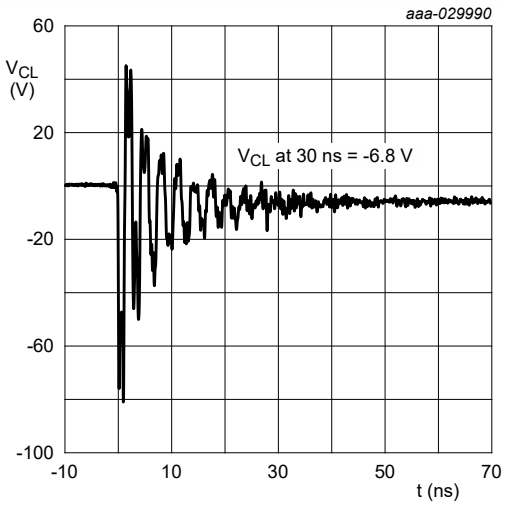


Fig. 9. Clamped -8 kV pulse waveform (IEC 61000-4-2 network)

10. Application information

The device is designed for protection of up to 4 bidirectional data lines from the damage caused by ESD and surge pulses. The device is suitable on lines where the signal polarities are above or below ground.

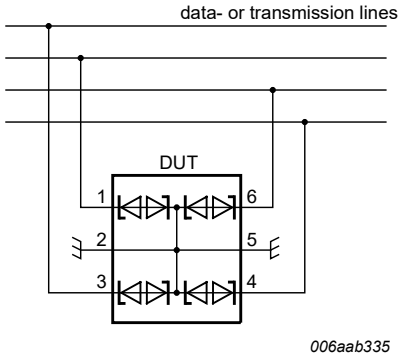


Fig. 10. Application diagram

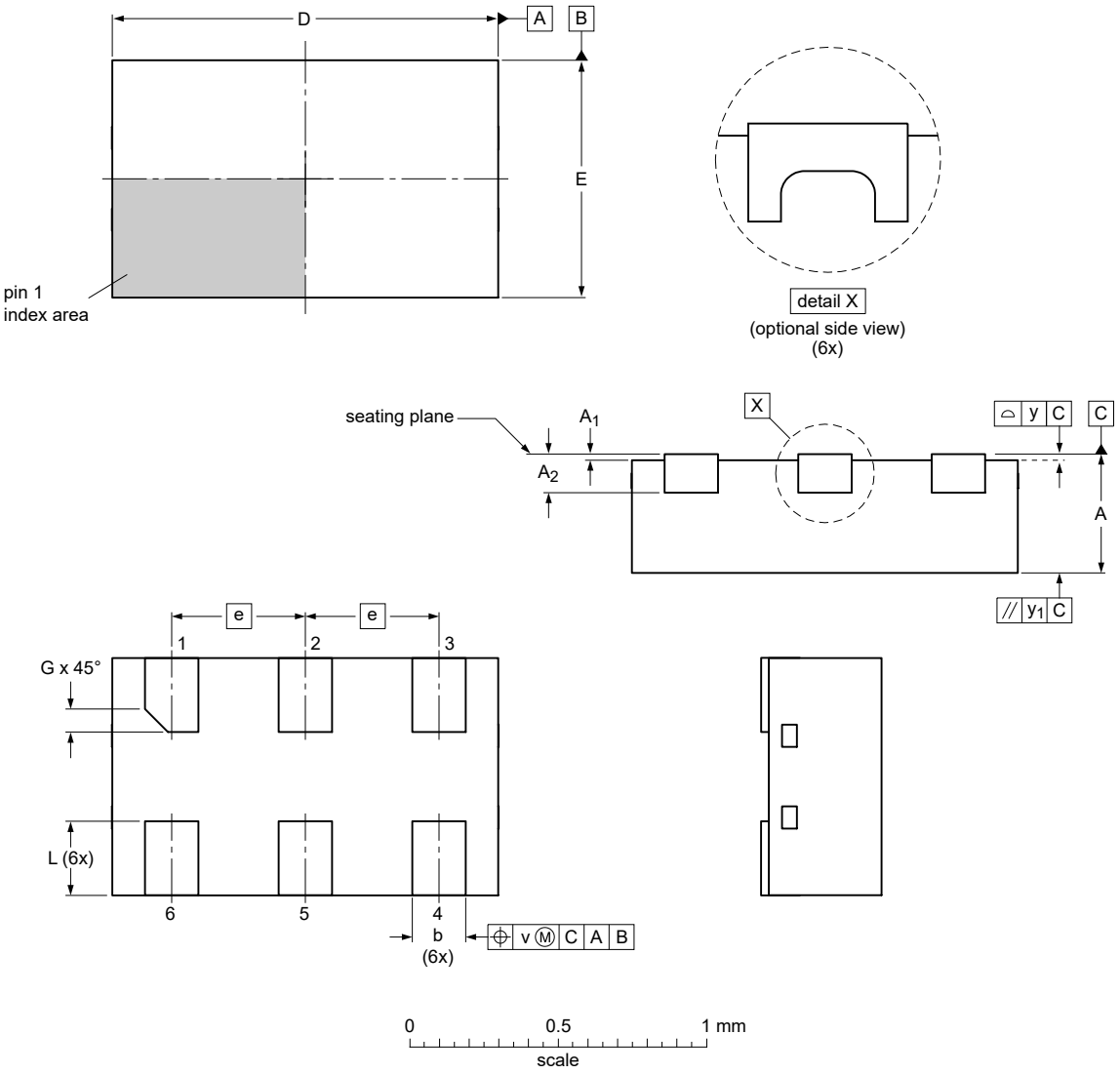
Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

- Place the device as close to the input terminal or connector as possible
- Minimize the path length between the device and the protected line.
- Keep parallel signal paths to a minimum.
- Avoid running protected conductors in parallel with unprotected conductors.
- Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- Minimize the length of the transient return path to ground.
- Avoid using shared transient return paths to a common ground point.
- Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

DFN1308-6, plastic, leadless extremely thin small package; 6 terminals; body 1.3 x 0.8 x 0.38 mm **SOT8006**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	G	L	u	v	y	y_1
mm	max	0.43	0.05	0.18	0.23	1.40	0.90		0.11	0.30				
	nom	0.38	0.02	0.13	0.18	1.30	0.80	0.45	0.08	0.25	0.1	0.1	0.05	0.05
	min	0.33	0.00	0.08	0.13	1.20	0.70		0.05	0.20				

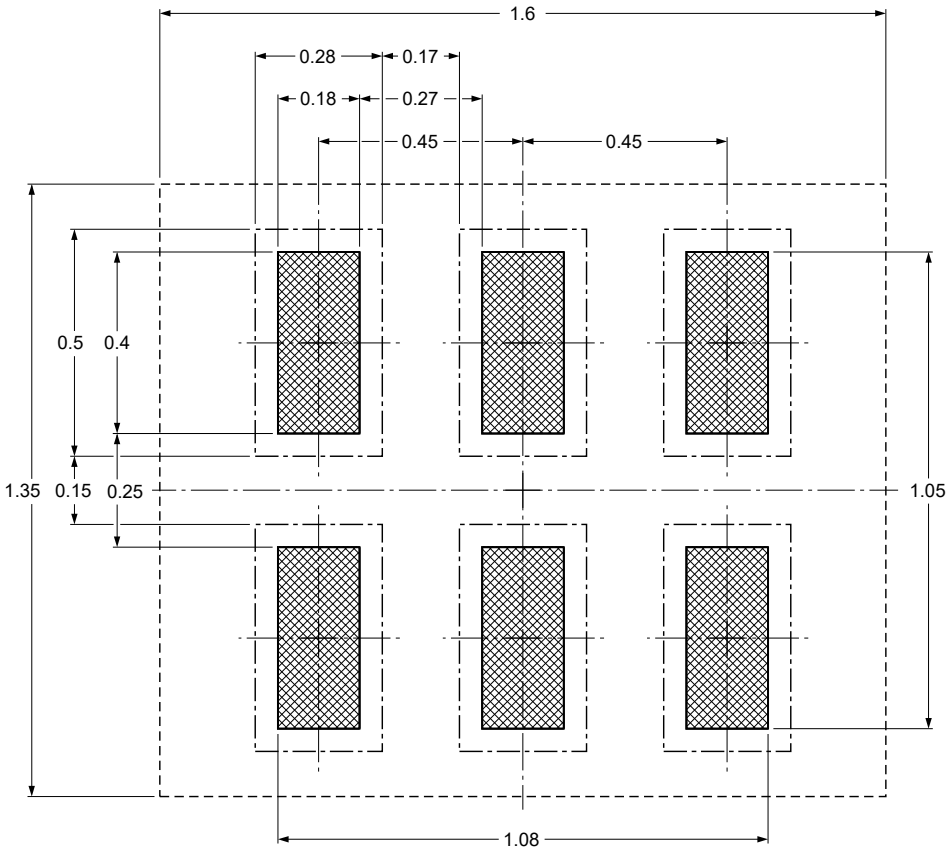
sot8006_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8006		---				19-05-06

Fig. 11. Package outline DFN1308-6 (SOT8006)

12. Soldering

Footprint information for reflow soldering of DFN1308-6 package **SOT8006**



recommend stencil thickness: 0.1 mm

occupied area

solder resist

solder lands

solder paste

Dimensions in mm

Issue date 19-05-06

sot8006_fr

Fig. 12. Reflow soldering footprint for DFN1308-6 (SOT8006)

13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD3V3L4BHC v.1	20190607	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 7 June 2019

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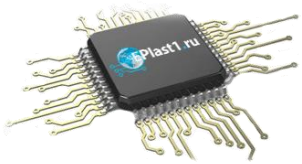

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