

High Speed, Integrated Ultrasound Driver IC

Features

- ▶ Drives two ultrasound transducer channels
- ▶ Generates five-level waveform
- ▶ Drives 12 high voltage MOSFETs
- ▶ $\pm 2.0A$ source and sink peak current
- ▶ Up to 20MHz output frequency
- ▶ 12V/ns slew rate
- ▶ $\pm 3.0ns$ matched delay times
- ▶ Second harmonic is less than -40dB
- ▶ Two separate gate drive voltages
- ▶ 1.8 to 3.3V CMOS logic interface

Applications

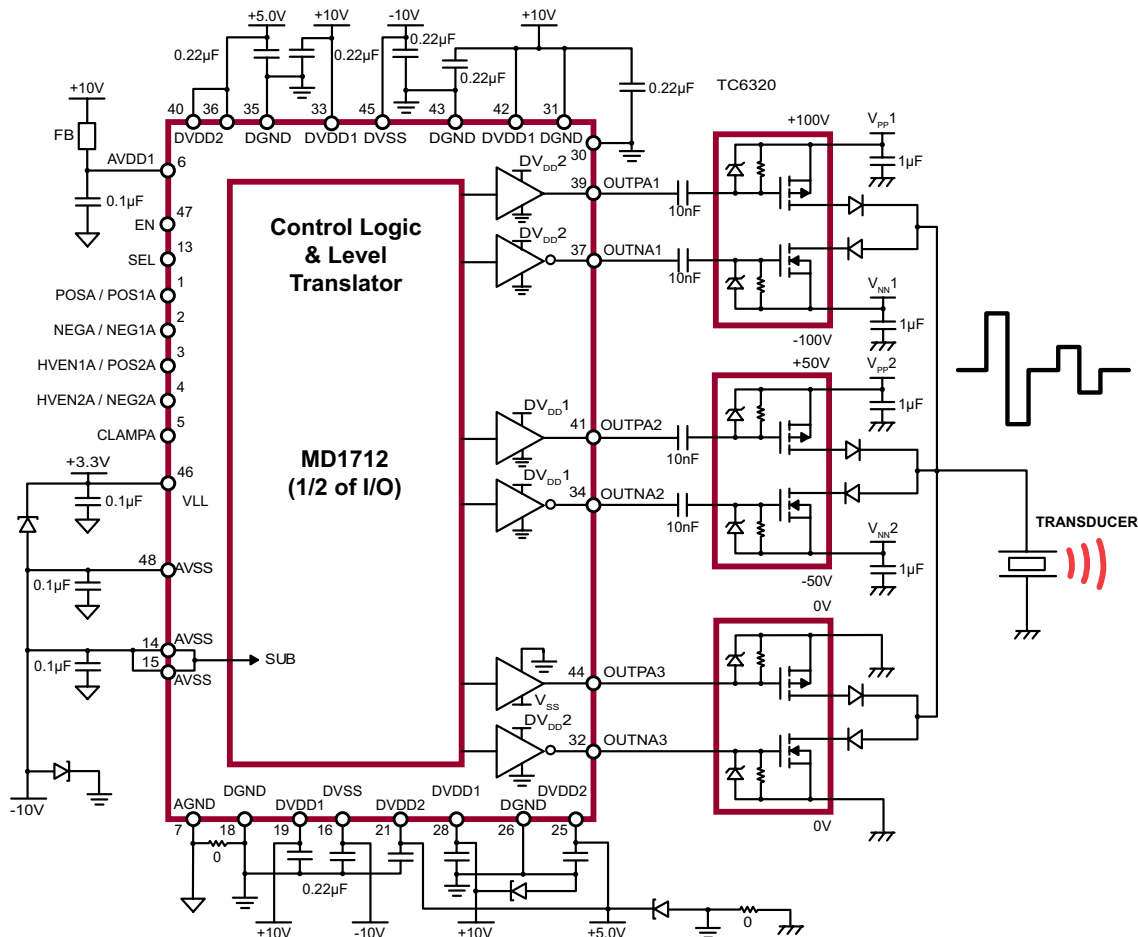
- ▶ Medical ultrasound imaging
- ▶ Piezoelectric transducer drivers
- ▶ Non-Destructive Testing (NDT)
- ▶ Metal flaw detection
- ▶ Sonar transmitter

General Description

The Supertex MD1712 is a two-channel, five-level, high voltage and high speed transmitter driver IC. It is designed for medical ultrasound imaging applications, but can also be used for metal flaw detection, Non-Destructive Testing (NDT), and for driving piezoelectric transducers.

The MD1712 is a two-channel logic controller circuit with low impedance MOSFET gate drivers. There are two sets of control logic inputs, one for channel A and one for channel B. Each channel consists of three pairs of MOSFET gate drivers. These drivers are designed to match the drive requirements of the Supertex TC6320. The MD1712 drives six TC6320s. Each pair consists of an N-channel and a P-channel MOSFET. They are designed to have the same impedance and can provide peak currents of over 2.0 amps.

Typical Application Circuit



Ordering Information

| Device | Package Options | |
|--------|---|--|
| | 48-Lead LQFP 7.00x7.00mm body 1.60mm height (max) 0.50mm pitch | 48-Lead QFN 7.00x7.00mm body 1.00mm height (max) 0.50mm pitch |
| MD1712 | MD1712FG-G | MD1712K6-G |

-G indicates package is RoHS compliant ('Green')



Absolute Maximum Ratings

| Parameter | Value |
|--|----------------|
| V _{LL} logic supply voltage | -0.5V to +5.5V |
| AV _{DD1} , DV _{DD1} , positive gate drive supply | -0.5V to +15V |
| DV _{DD2} , positive gate drive supply | -0.5V to +15V |
| AV _{SS} , DV _{SS} , negative gate drive supply | -15V to +0.5V |
| Thermal resistance (θ_{JA}): | |
| 48-Lead LQFP* | 50°C/W |
| 48-Lead QFN* | 29°C/W |
| Maximum junction temperature | +125C |
| Storage temperature | -65°C to 150°C |
| Power dissipation | 1.2W |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

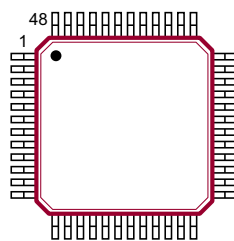
* 1.0oz 4-layer 3x4" PCB

Operating Supply Voltages and Currents

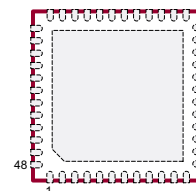
(Over operating conditions unless otherwise specified, AV_{DD1} = DV_{DD1} = DV_{DD2} = 10V, AV_{SS} = DV_{SS} = -10V, V_{LL} = 3.3V, T_A = 25°C)

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|---------------------------------------|--|-------|------|-------|-------|------------------------------------|
| V _{LL} | Logic supply | +1.8 | +3.3 | +5.0 | V | --- |
| AV _{DD1} | Positive drive bias supply | +8.0 | +10 | +12.6 | V | --- |
| DV _{DD1} | Positive gate drive supply | +4.75 | - | +12.6 | V | --- |
| DV _{DD2} | Positive gate drive supply | +4.75 | - | +12.6 | V | --- |
| AV _{SS} , DV _{SS} | Negative gate drive and bias supply | -12.0 | -10 | -8.0 | V | --- |
| I _{VLL} | Logic supply current | - | 2.0 | - | mA | All channels on at 5.0Mhz, no load |
| I _{AVDD1} | Positive bias current | - | 5.0 | - | | |
| I _{AVSS} & I _{DVSS} | Negative drive and bias supply current | - | 20 | - | | |
| I _{DVDD1} | Positive drive current 1 | - | 55 | - | | |

Pin Configurations



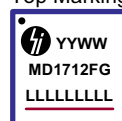
48-Lead LQFP (FG)
(top view)



48-Lead QFN (K6)
(top view)

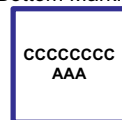
Package Marking

Top Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*

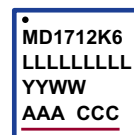
Bottom Marking



A = Assembler ID*
— = "Green" Packaging
*May be part of top marking

Package may or may not include the following marks: Si or

48-Lead LQFP (FG)



L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
— = "Green" Packaging

Package may or may not include the following marks: Si or

48-Lead QFN (K6)

Operating Supply Voltages and Currents (cont.)

(Over operating conditions unless otherwise specified, $AV_{DD1} = DV_{DD1} = DV_{DD2} = 10V$, $AV_{SS} = DV_{SS} = -10V$, $V_{LL} = 3.3V$, $T_A = 25^\circ C$)

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|--------------|--------------------------------|-----|------|-----|---------|---|
| I_{DVDD2} | Positive drive current 2 | - | 13 | - | mA | All channels on at 5.0Mhz, $D_{VDD2} = 5.0$, no load |
| I_{AVDD1Q} | V_{AVDD} 1 quiescent current | - | 2.0 | - | mA | EN = low, All inputs low or high. |
| I_{AVSSQ} | V_{AVSS} quiescent current | - | 0.75 | - | mA | |
| I_{DVDD1Q} | V_{DVDD} 1 quiescent current | - | - | 10 | μA | |
| I_{DVDD2Q} | V_{DVDD} 2 quiescent current | - | - | 10 | μA | |
| I_{VLLQ} | Logic supply current | - | 1.0 | - | mA | |

DC Electrical Characteristics

(Over operating conditions unless otherwise specified, $AV_{DD1} = DV_{DD1} = DV_{DD2} = 10V$, $AV_{SS} = DV_{SS} = -10V$, $V_{LL} = 3.3V$, $T_A = 0$ to $70^\circ C$)

P-Channel Gate Driver Outputs

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|--------------|----------------------------|-----|-----|-----|----------|----------------------|
| R_{SINK} | Output sink resistance | - | - | 6.0 | Ω | $I_{SINK} = 100mA$ |
| R_{SOURCE} | Output source resistance | - | - | 6.0 | Ω | $I_{SOURCE} = 100mA$ |
| I_{SINK} | Peak output sink current | - | 2.0 | - | A | --- |
| I_{SOURCE} | Peak output source current | - | 2.0 | - | A | --- |

N-Channel Gate Driver Outputs

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|--------------|----------------------------|-----|-----|-----|----------|----------------------|
| R_{SINK} | Output sink resistance | - | - | 10 | Ω | $I_{SINK} = 100mA$ |
| R_{SOURCE} | Output source resistance | - | - | 10 | Ω | $I_{SOURCE} = 100mA$ |
| I_{SINK} | Peak output sink current | - | 1.5 | - | A | --- |
| I_{SOURCE} | Peak output source current | - | 1.5 | - | A | --- |

Logic Inputs

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|----------|--------------------------|-------------|-----|-------------|---------|------------|
| V_{IH} | Input logic high voltage | $0.8V_{LL}$ | - | V_{LL} | V | --- |
| V_{IL} | Input logic low voltage | 0 | - | $0.2V_{LL}$ | V | --- |
| I_{IH} | Input logic high current | - | - | 1.0 | μA | --- |
| I_{IL} | Input logic low current | -1.0 | - | - | μA | --- |

AC Electrical Characteristics

(Over operating conditions unless otherwise specified, $AV_{DD1} = DV_{DD1} = DV_{DD2} = 10V$, $AV_{SS} = DV_{SS} = -10V$, $V_{LL} = 3.3V$, $T_A = 0$ to $70^\circ C$)

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|--------------------|---|-----|-----|-----------|-------|--|
| f_{OUT} | Output frequency range | - | - | 20 | MHz | --- |
| t_{PH} | Propagation delay when output is from low to high | - | 19 | - | ns | No load, see timing diagram |
| t_{PL} | Propagation delay when output is from high to low | - | 19 | - | ns | No load, see timing diagram |
| t_r | Output rise time | - | 8.0 | - | ns | 1000pF load, see timing diagram |
| t_f | Output fall time | - | 8.0 | - | ns | 1000pF load, see timing diagram |
| Δt_{DM} | Delay time matching | - | - | ± 3.0 | ns | No load, from device to device |
| Δt_{DELAY} | Output jitter | - | 30 | - | ps | Standard deviation of t_d samples (1k) |
| SR | Output slew rate | - | 12 | - | V/ns | Measured at TC6320 output with 100 Ω load |
| HD2 | 2 nd harmonic distortion | - | -40 | - | dB | |

Power-Up Sequence

| Step | Connection | Description |
|------|---|---|
| 1 | AV_{SS} , DV_{SS} | Negative gate drive supply and substrate bias |
| 2 | V_{LL} , AV_{DD1} , DV_{DD1} & DV_{DD2} | Logic supply, positive gate drive supply and bias |

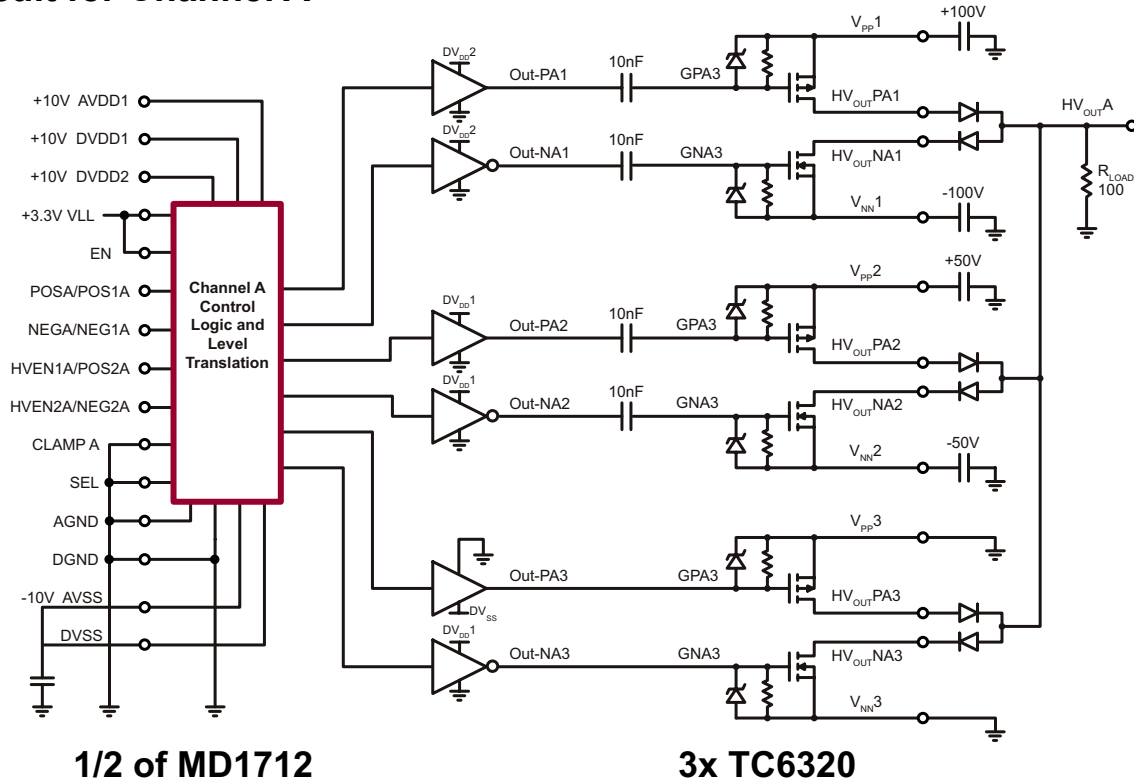
Truth Table for Channels A and B (For SEL = L)

| Logic Control Inputs | | | | | | | V _{PP1} to V _{NN1} Output | | V _{PP2} to V _{NN2} Output | | V _{PP3} to V _{NN3} Output | |
|----------------------|----|----------------|----------------|-------|--------------|--------------|---|----------------------|---|----------------------|---|----------------------|
| SEL | EN | HVEN1/ POS2 | HVEN2/ NEG2 | Clamp | POS/ POS1 | NEG/ NEG1 | HV _{OUT} P1 | HV _{OUT} N1 | HV _{OUT} P2 | HV _{OUT} N2 | HV _{OUT} P3 | HV _{OUT} N3 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | OFF | | OFF | | ON | ON |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | | | | | ON | ON |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | | | | | ON | ON |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | | | | | OFF | OFF |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | OFF | | OFF | | OFF | |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | | | | | | |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | | | | | | |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | | | | | | |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | OFF | | OFF | OFF | ON | ON |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | | | OFF | ON | OFF | OFF |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | | | ON | OFF | OFF | OFF |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | | | OFF | OFF | OFF | OFF |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | OFF | | OFF | | OFF | |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | | | | | | |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | | | | | | |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | | | | | | |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | OFF | OFF | OFF | | ON | ON |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | OFF | ON | | | OFF | OFF |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | ON | OFF | | | OFF | OFF |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | OFF | OFF | | | OFF | OFF |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | OFF | | OFF | | OFF | |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | | | | | | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | | | | | | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | | | | | | |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | OFF | | OFF | | OFF | |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | | | | | | |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | | | | | | |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | | | | | | |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | OFF | | OFF | | OFF | |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | | | | | | |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | | | | | | |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | | | | | | |
| 0 | 0 | X | X | X | X | X | OFF | | OFF | | OFF | |

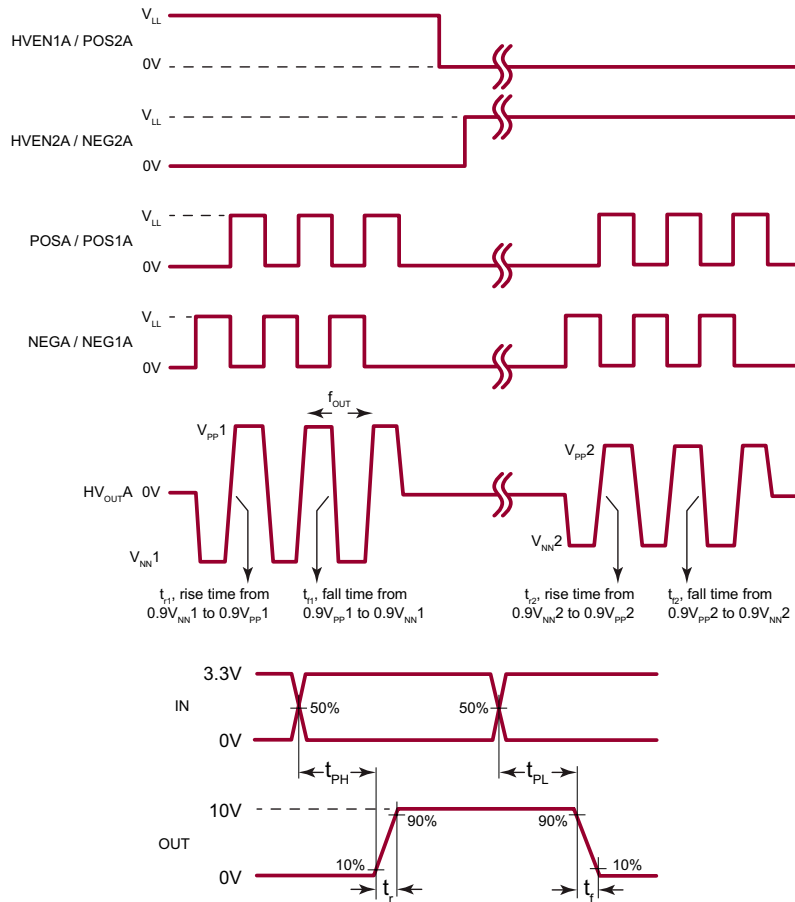
Truth Table for Channels A and B (For SEL = H)

| Logic Control Inputs | | | | | | | V _{PP1} to V _{NN1} Output | | V _{PP2} to V _{NN2} Output | | V _{PP3} to V _{NN3} Output | |
|----------------------|----|-------|----------------|----------------|--------------|--------------|---|----------------------|---|----------------------|---|----------------------|
| SEL | EN | Clamp | HVEN1/ POS2 | HVEN2/ NEG2 | POS/ POS1 | NEG/ NEG1 | HV _{OUT} P1 | HV _{OUT} N1 | HV _{OUT} P2 | HV _{OUT} N2 | HV _{OUT} P3 | HV _{OUT} N3 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | OFF | OFF | OFF | OFF | OFF | OFF |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | OFF | ON | | | | |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | ON | OFF | | | | |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | ON | ON | | | | |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | OFF | OFF | OFF | ON | OFF | OFF |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | OFF | ON | | | | |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | ON | OFF | | | | |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | ON | ON | | | | |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | OFF | OFF | ON | OFF | OFF | OFF |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | OFF | ON | | | | |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | ON | OFF | | | | |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | ON | ON | | | | |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | OFF | OFF | ON | ON | OFF | OFF |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | OFF | ON | | | | |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | ON | OFF | | | | |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | ON | ON | | | | |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | OFF | OFF | OFF | OFF | ON | ON |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | OFF | ON | | | | |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | ON | OFF | | | | |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | ON | ON | | | | |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | OFF | OFF | OFF | ON | ON | ON |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | OFF | ON | | | | |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | ON | OFF | | | | |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | ON | ON | | | | |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | OFF | OFF | ON | OFF | ON | ON |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | OFF | ON | | | | |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | ON | OFF | | | | |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | ON | ON | | | | |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | OFF | OFF | ON | ON | ON | ON |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | OFF | ON | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | ON | OFF | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | ON | ON | | | | |
| 1 | 0 | X | X | X | X | X | OFF | OFF | OFF | OFF | OFF | OFF |

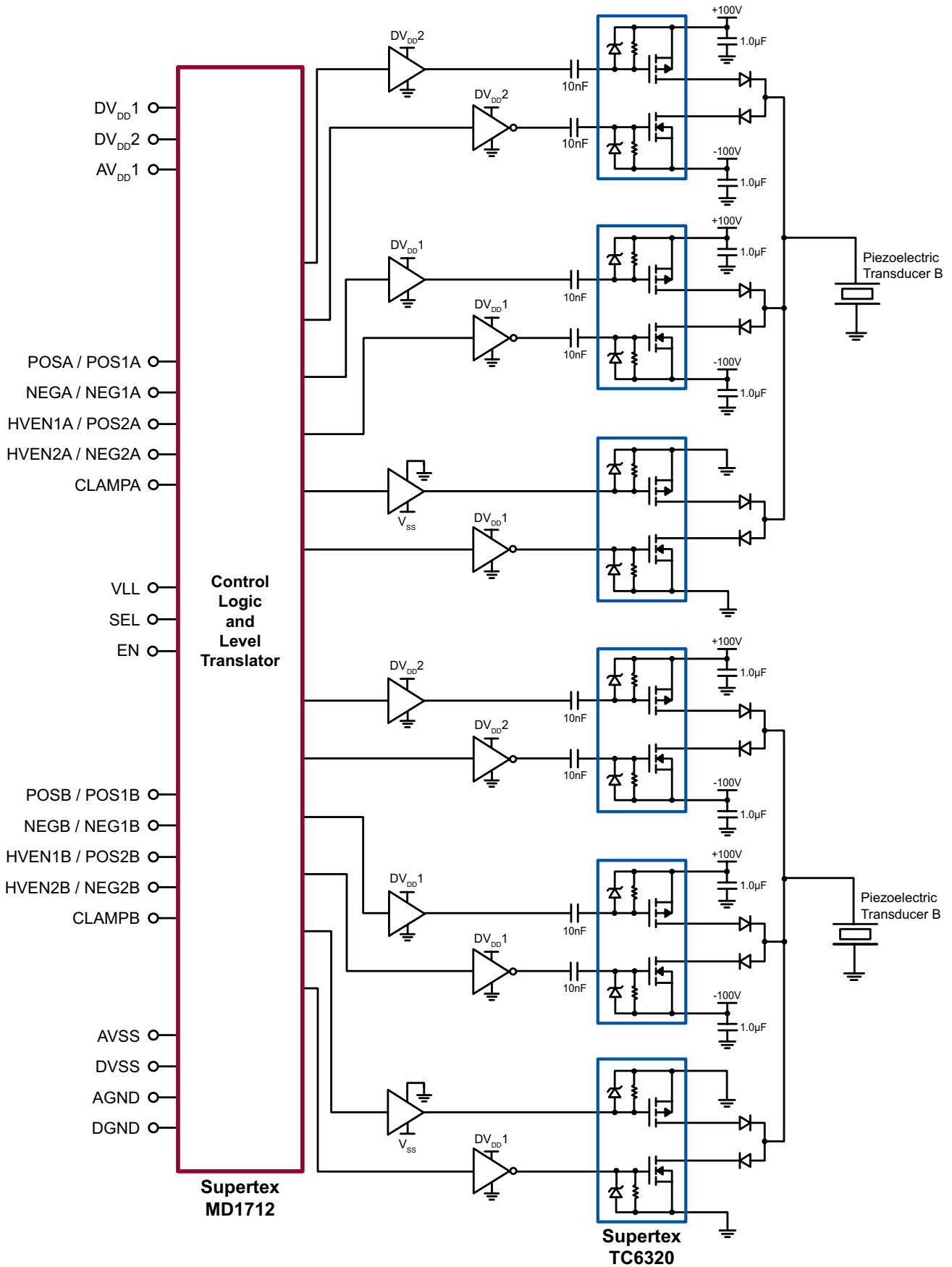
Test Circuit for Channel A



Timing Diagram



Block Diagram



Pin Description (48-Lead LQFP & 48-Lead QFN)

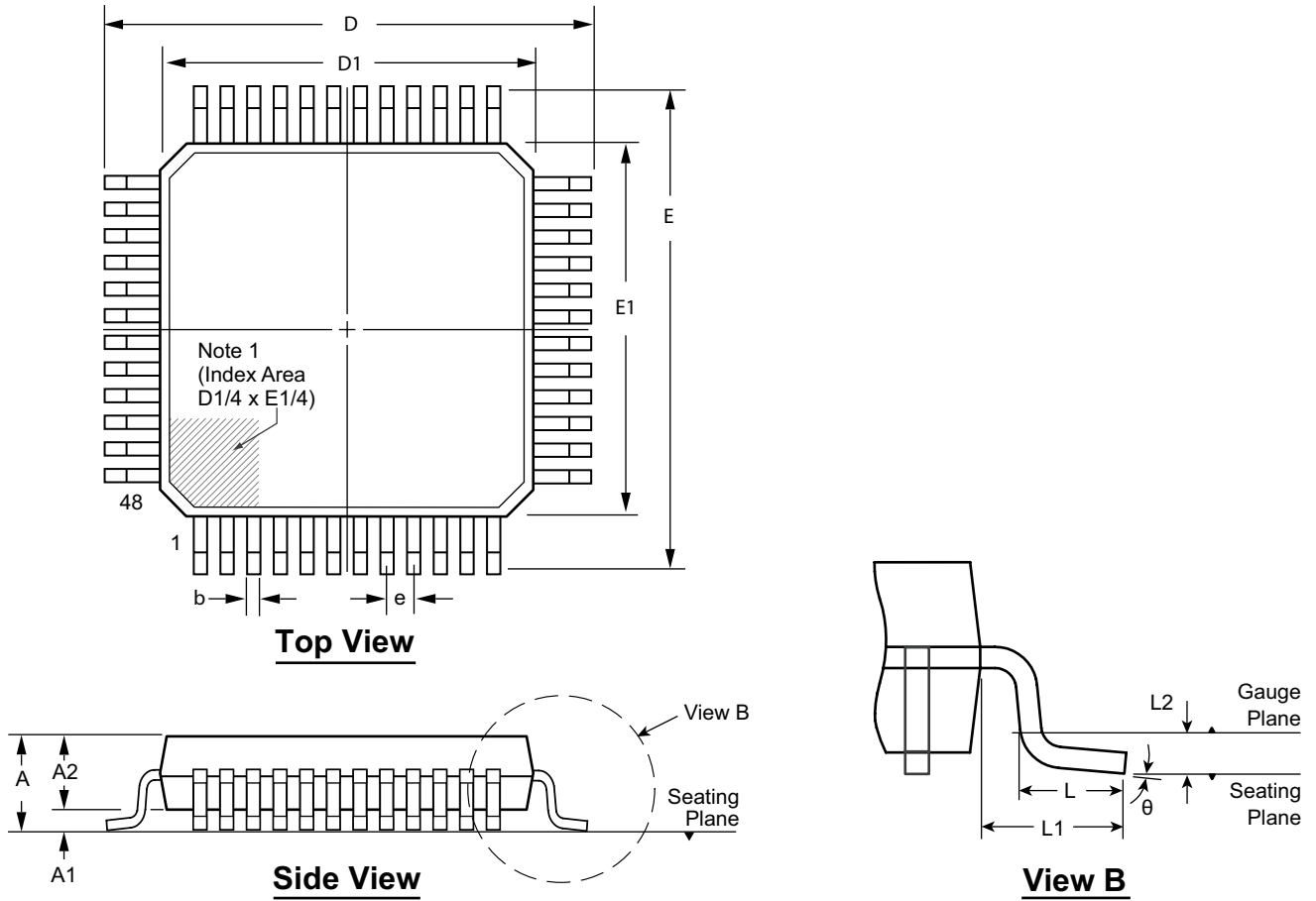
| Pin # | Name | Description |
|-------|--------------------|---|
| 1 | POSA / POS1A | Logic input control for channel A. When SEL = L, the pin is POSA. When SEL = H, the pin is POS1A. |
| 2 | NEGA / NEG1A | Logic input control for channel A. When SEL = L, the pin is NEGA. When SEL = H, the pin is NEG1A. |
| 3 | HVEN1A / POS2A | Logic input control for channel A. When SEL = L, the pin is HVEN1A. When SEL = H, the pin is POS2A. |
| 4 | HVEN2A / NEG2A | Logic input control for channel A. When SEL = L, the pin is HVEN2A. When SEL = H, the pin is NEG2A. |
| 5 | CLAMPA | Used with SEL = H. Logic input control for OUT-PA3 and OUT-NA3. Connect to ground when SEL = L. |
| 6 | AV _{DD} 1 | Supplies analog circuitry portion of the gate driver. Should be at the same potential as DV _{DD} 1. |
| 7 | AGND | Analog Ground. |
| 8 | CLAMPB | Used with SEL = H. Logic input control for OUT-PB3 and OUT-NB3. Connect to ground when SEL = L. |
| 9 | HVEN2B / NEG2B | Logic input control for channel B. When SEL = L, the pin is HVEN2B. When SEL = H, the pin is NEG2B. |
| 10 | HVEN1B / POS2B | Logic input control for channel B. When SEL = L, the pin is HVEN1B. When SEL = H, the pin is POS2B. |
| 11 | NEGB / NEG1B | Logic input control for channel B. When SEL = L, the pin is NEGB. When SEL = H, the pin is NEG1B. |
| 12 | POSB / POS1B | Logic input control for channel B. When SEL = L, the pin is POSB. When SEL = H, the pin is POS1B. |
| 13 | SEL | Logic input select. See truth tables for SEL = L and SEL = H. |
| 14 | AVSS | Negative driver supply for OUT-PA3, OUT-PB3 and bias circuits. They are also connected to the IC substrate. They are required to connect to the most negative potential of voltage supplies. |
| 15 | | |
| 16 | DVSS | Gate drive supply voltage for OUT-PA3 and OUT-PB3. Supplies digital circuitry portion and the main Output stage. Should be at the same potential as AVSS. |
| 17 | OUT-PB3 | Output P-Channel gate driver for channel B |
| 18 | DGND | Digital Ground. |
| 19 | DV _{DD} 1 | Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT-PA2, OUT-NA2, OUT-NA3, OUT-PB2, OUT-NB2, and OUT-NB3. Should be at the same potential as AV _{DD} 1. |
| 20 | OUT-PB2 | Output P-Channel gate driver for channel B |
| 21 | DV _{DD} 2 | Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT-PA1, OUT-NA1, OUT-PB1, and OUT-NB1. Can be at a different potential than DV _{DD} 1. |
| 22 | OUT-PB1 | Output P-Channel gate driver for channel B |
| 23 | N/C | No connect. |
| 24 | OUT-NB1 | Output N-Channel gate driver for channel B |
| 25 | DV _{DD} 2 | Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT-PA1, OUT-NA1, OUT-PB1, and OUT-NB1. Can be at a different potential than DV _{DD} 1. |

Pin Description (48-Lead LQFP & 48-Lead QFN) (cont.)

| Pin # | Name | Description |
|------------|--------------------|---|
| 26 | DGND | Digital Ground. |
| 27 | OUT-NB2 | Output N-Channel gate driver for channel B |
| 28 | DV _{DD} 1 | Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT-PA2, OUT-NA2, OUT-NA3, OUT-PB2, OUT-NB2, and OUT-NB3. Should be at the same potential as AV _{DD} 1. |
| 29 | OUT-NB3 | Output N-Channel gate driver for channel B |
| 30 | DGND | Digital Ground. |
| 31 | DV _{DD} 1 | Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT-PA2, OUT-NA2, OUT-NA3, OUT-PB2, OUT-NB2, and OUT-NB3. Should be at the same potential as AV _{DD} 1. |
| 32 | OUT-NA3 | Output N-Channel gate drivers for channel A. |
| 33 | DV _{DD} 1 | Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT-PA2, OUT-NA2, OUT-NA3, OUT-PB2, OUT-NB2, and OUT-NB3. Should be at the same potential as AV _{DD} 1. |
| 34 | OUT-NA2 | Output N-Channel gate drivers for channel A. |
| 35 | DGND | Digital Ground. |
| 36 | DV _{DD} 2 | Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT-PA1, OUT-NA1, OUT-PB1, and OUT-NB1. Can be at a different potential than DV _{DD} 1. |
| 37 | OUT-NA1 | Output N-Channel gate drivers for channel A. |
| 38 | N/C | No connect. |
| 39 | OUT-PA1 | Output P-Channel gate drivers for channel A |
| 40 | DV _{DD} 2 | Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT-PA1, OUT-NA1, OUT-PB1, and OUT-NB1. Can be at a different potential than DV _{DD} 1. |
| 41 | OUT-PA2 | Output P-Channel gate drivers for channel A |
| 42 | DV _{DD} 1 | Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for OUT-PA2, OUT-NA2, OUT-NA3, OUT-PB2, OUT-NB2, and OUT-NB3. Should be at the same potential as AV _{DD} 1. |
| 43 | DGND | Digital Ground. |
| 44 | OUT-PA3 | Output P-Channel gate drivers for channel A |
| 45 | DVSS | Gate drive supply voltage for OUT-PA3 and OUT-PB3. Supplies digital circuitry portion and the main output stage. Should be at the same potential as AVSS. |
| 46 | VLL | Logic supply voltage. |
| 47 | EN | Logic input enable control. When EN = L, all P-channel output drivers are high and all N-channel output drivers are low. |
| 48 | AVSS | Negative driver supply for OUT-PA3, OUT-PB3 and bias circuits. They are also connected to the IC substrate. They are required to connect to the most negative potential of voltage supplies. |
| Center Pad | AVSS | For the QFN package, the center pad is at AVSS potential. It should be externally connected to AVSS. |

48-Lead LQFP Package Outline (FG)

7.00x7.00mm body, 1.60mm height (max), 0.50mm pitch



Note:
 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol | A | A1 | A2 | b | D | D1 | E | E1 | e | L | L1 | L2 | θ |
|----------------|-----|-------|------|------|------|-------|-------|-------|-------|----------|----------|----------|------|
| Dimension (mm) | MIN | 1.40* | 0.05 | 1.35 | 0.17 | 8.80* | 6.80* | 8.80* | 6.80* | 0.50 BSC | 1.00 REF | 0.25 BSC | 0° |
| | NOM | - | - | 1.40 | 0.22 | 9.00 | 7.00 | 9.00 | 7.00 | | | | 3.5° |
| | MAX | 1.60 | 0.15 | 1.45 | 0.27 | 9.20* | 7.20* | 9.20* | 7.20* | | | | 7° |

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.

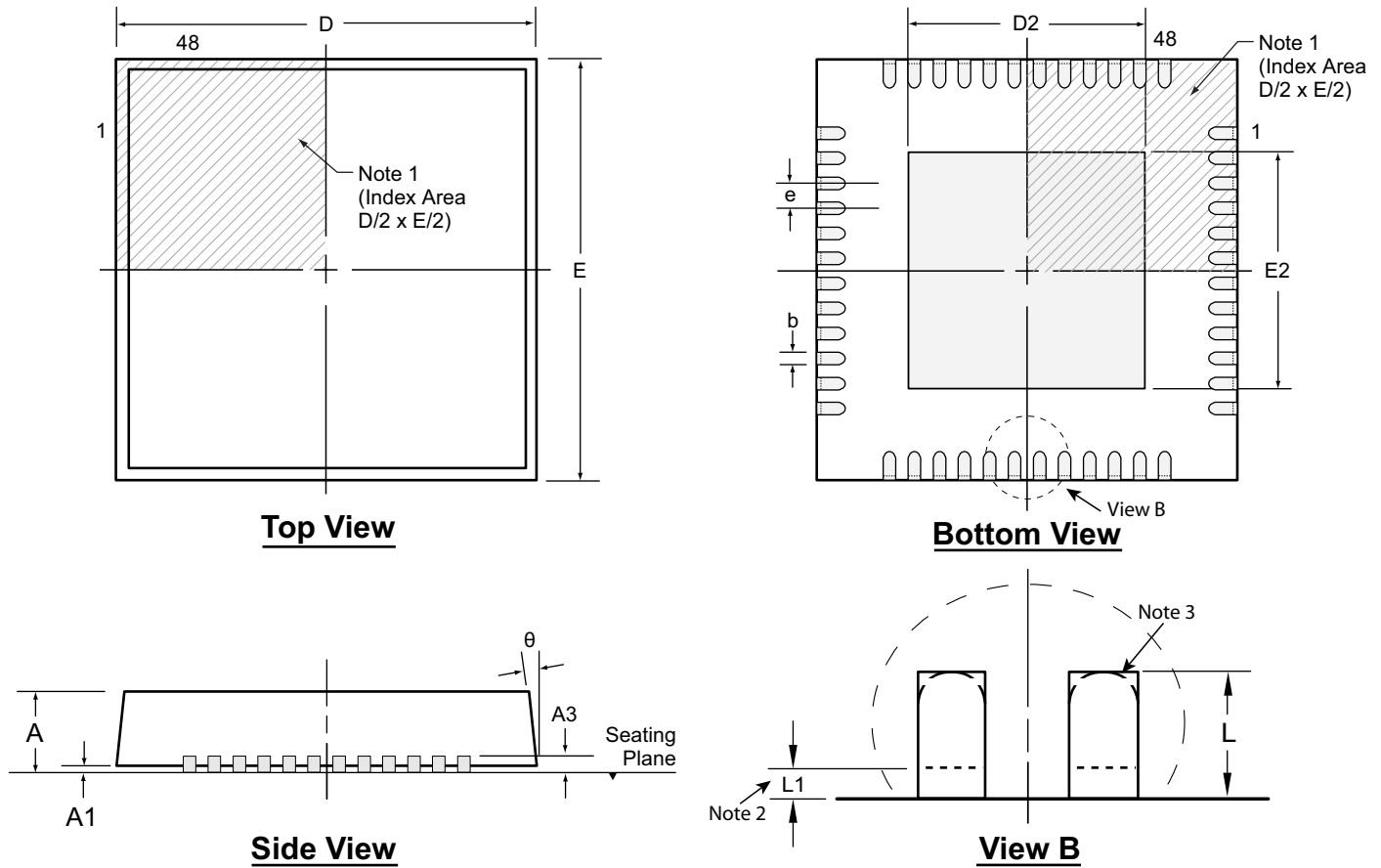
* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

Supertex Doc. #: DSPD-48LQFPFG Version, D041309.

48-Lead QFN Package Outline (K6)

7.00x7.00mm body, 1.00mm height (max), 0.50mm pitch



Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L_1) may be present.
3. The inner tip of the lead may be either rounded or square.

| Symbol | | A | A1 | A3 | b | D | D2 | E | E2 | e | L | L1 | θ |
|----------------|-----|------|------|----------|------|-------|------|-------|------|----------|-------------------|------|----------|
| Dimension (mm) | MIN | 0.80 | 0.00 | 0.20 REF | 0.18 | 6.85* | 1.25 | 6.85* | 1.25 | 0.50 BSC | 0.30 [†] | 0.00 | 0° |
| | NOM | 0.90 | 0.02 | | 0.25 | 7.00 | - | 7.00 | - | | 0.40 [†] | - | - |
| | MAX | 1.00 | 0.05 | | 0.30 | 7.15* | 5.45 | 7.15* | 5.45 | | 0.50 [†] | 0.15 | 14° |

JEDEC Registration MO-220, Variation VKKD-6, Issue K, June 2006.

* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings are not to scale.

Supertex Doc.#: DSPD-48QFNK67X7P050, Version C041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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Как с нами связаться

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