

SY89856U



2GHz, Low-Power, 1:6 LVPECL Fanout Buffer with 2:1 Input MUX and Internal Termination

General Description

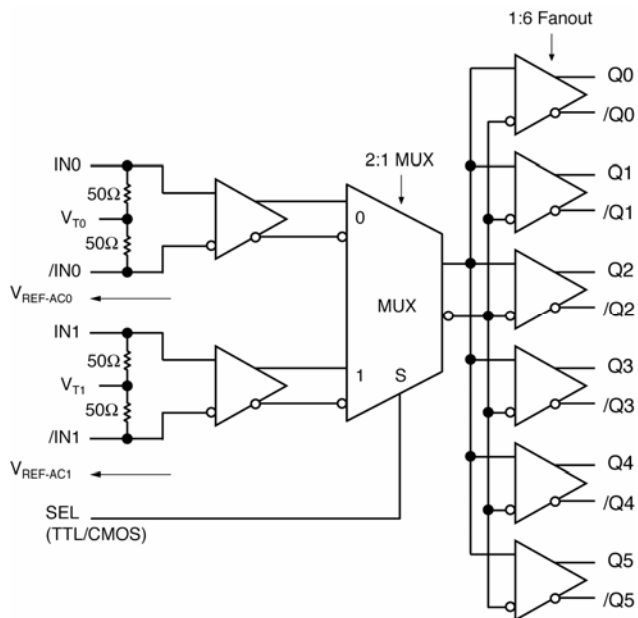
The SY89856U is a 2.5V/3.3V precision, high-speed, 1:6 fanout capable of handling clocks up to 2.0GHz. A differential 2:1 MUX input is included for redundant clock switchover applications.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows the device to interface to any differential signal (AC- or DC-coupled) as small as 100mV (200mV_{pp}) without any level shifting or termination resistor networks in the signal path. The outputs are LVPECL (100k, temperature compensated), with extremely fast rise/fall times guaranteed to be less than 200ps.

The SY89856U operates from a 2.5V ±5% supply or a 3.3V ±10% supply and is guaranteed over the full industrial temperature range of -40°C to +85°C. The SY89856U is part of Micrel's high-speed, Precision Edge[®] product line.

All support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Block Diagram



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MLF and MicroLeadFrame registered are trademarks of Amkor Technology.



Precision Edge[®]

Features

- 6 ultra-low skew copies of the selected input
- 2:1 MUX input included for clock switchover applications
- Low power: 225mW typical (2.5V)
- 2.5V to 3.3V supply voltage
- Unique input isolation design minimizes crosstalk
- Guaranteed AC performance over temperature and voltage:
 - Clock frequency range: DC to >2.0GHz
 - <400ps IN-to-OUT t_{pd}
 - <200ps t_r/t_f times
 - <30ps skew (output-to-output)
- Ultra-low jitter design:
 - <1ps_{RMS} random jitter
 - <10ps_{PP} total jitter (clock)
 - <1ps_{RMS} cycle-to-cycle jitter
 - <0.7ps_{RMS} crosstalk-induced jitter
- Unique input termination and VT pin accepts DC- and AC-coupled inputs (CML, PECL, LVDS)
- 100k LVPECL compatible output swing
- -40°C to +85°C industrial temperature range
- Available in 32-pin (5mm x 5mm) MLF[®] package

Applications

- Redundant clock distribution
- All SONET/SDH clock/data distribution
- All Fibre Channel distribution
- All Gigabit Ethernet clock distribution

Markets

- LAN/WAN
- Enterprise servers
- ATE
- Test and measurement

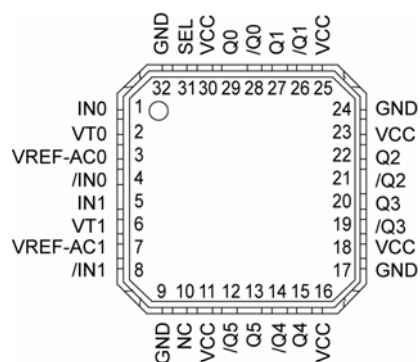
Ordering Information⁽¹⁾

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|-----------------------------|--------------|-----------------|--|-------------------|
| SY89856UMG | MLF-32 | Industrial | SY89856U with Pb-Free bar-line indicator | NiPdAu Pb-Free |
| SY89856UMGTR ⁽²⁾ | MLF-32 | Industrial | SY89856U with Pb-Free bar-line indicator | NiPdAu Pb-Free |

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



32-Pin MLF[®] (MLF-32)

Pin Description

| Pin Number | Pin Name | Pin Function |
|--|---|---|
| 1,4 5, 8 | IN0, /IN0 IN1, /IN1 | Differential Input: These input pairs are the differential signal inputs to the device. These inputs accept AC- or DC-coupled signals as small as 100mV (200mV _{p-p}). Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Please refer to the "Input Interface Applications" section for more details. |
| 2, 6 | VT0, VT1 | Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT0 and VT1 pins provide a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more details. |
| 31 | SEL | This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open. The MUX select switchover function is asynchronous. |
| 10 | NC | No connect. |
| 11, 16, 18, 23, 25, 30 | VCC | Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors as close to VCC pins as possible. |
| 29, 28 27, 26 22, 21 20, 19 15, 14 13, 12 | Q0, /Q0, Q1, /Q1, Q2, /Q2, Q3, /Q3, Q4, /Q4, Q5, /Q5 | Differential Outputs: These 100k (temperature compensated) LVPECL output pairs are low skew copies of the selected input. Unused output pins may be left floating. Please refer to the "LVPECL Output Interface Applications" for details. |
| 9, 17, 24, 32 | GND, Exposed Pad | Ground: Ground pins and exposed pad must be connected to the same ground plane. |
| 3, 7 | VREF-AC0 VREF-AC1 | Reference Voltage: This output biases to V _{CC} -1.2V. It is used for AC-coupling inputs (IN, /IN). Connect VREF_AC directly to the VT pin. Bypass with 0.01μF low ESR capacitor to V _{CC} . See "Input Interface Applications" section. Maximum sink/source current is ±1.5mA. Due to the limited drive capability use for input at the same package only. |

LVPECL Output Interface Applications

| SEL | Output |
|-----|--------------------|
| 0 | IN0 Input Selected |
| 1 | IN1 Input Selected |

Absolute Maximum Ratings⁽¹⁾

| | | |
|---------------------------------------|-------|-------------------|
| Supply Voltage (V_{CC}) | | -0.5V to +4.0V |
| Input Voltage (V_{IN}) | | -0.5V to V_{CC} |
| LVPECL Output Current (I_{OUT}) | | |
| Continuous | | 50mA |
| Surge | | 100mA |
| Termination Current | | |
| Source or sink current on V_T | | ± 100 mA |
| V_{REF-AC} Source or sink current | | ± 2.0 mA |
| Lead Temperature (soldering, 20 sec.) | | +260°C |
| Storage Temperature (T_s) | | -65°C to 150°C |

Operating Ratings⁽²⁾

| | | |
|---|-------|--------------------|
| Supply Voltage (V_{CC}) | | +2.375V to +2.625V |
| | | +3.0V to +3.6V |
| Ambient Temperature (T_A) | | -40°C to +85°C |
| Package Thermal Resistance ⁽³⁾ | | |
| MLF [®] (θ_{JA}) | | |
| Still-Air | | 35°C/W |
| MLF [®] (ψ_{JB}) | | |
| Junction-to-Board | | 16°C/W |

DC Electrical Characteristics⁽⁴⁾

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------------|--|-------------------------|--------------|--------------|--------------|----------|
| V_{CC} | Power Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| | | | 3.0 | 3.3 | 3.6 | V |
| I_{CC} | Power Supply Current | No load, max V_{CC} . | | 90 | 140 | mA |
| R_{IN} | Input Resistance (IN-to- V_T) | | 45 | 50 | 55 | Ω |
| R_{DIFF_IN} | Differential Input Resistance (IN-to- $/IN$) | | 90 | 100 | 110 | Ω |
| V_{IH} | Input High Voltage (IN, $/IN$) | | $V_{IH}-1.2$ | | V_{CC} | V |
| V_{IL} | Input Low Voltage (IN, $/IN$) | | 0 | | $V_{IH}-0.1$ | V |
| V_{IN} | Input Voltage Swing (IN, $/IN$) | See Figure 1a. | 0.1 | | 1.7 | V |
| V_{DIFF_IN} | Differential Input Voltage Swing $ IN- /IN $ | See Figure 1b. | 0.2 | | | V |
| V_{T_IN} | IN-to- V_T (IN, $/IN$) | | | | 1.28 | V |
| V_{REF-AC} | Output Reference Voltage | | $V_{CC}-1.3$ | $V_{CC}-1.2$ | $V_{CC}-1.1$ | V |

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to an absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and ψ_{JB} values are determined for a 4-layer board in still air, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

LVPECL Outputs DC Electrical Characteristics⁽⁶⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$; $R_L = 50\Omega$ to $V_{CC} - 2V$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------------|-----------------------------------|----------------|----------------|-----|----------------|-------|
| V_{OH} | Output HIGH Voltage | | $V_{CC}-1.145$ | | $V_{CC}-0.895$ | V |
| V_{OL} | Output LOW Voltage | | $V_{CC}-1.945$ | | $V_{CC}-1.695$ | V |
| V_{OUT} | Output Voltage Swing | See Figure 1a. | 550 | 800 | | mV |
| $V_{DIFF-OUT}$ | Differential Output Voltage Swing | See Figure 1b. | 1.1 | 1.6 | | V |

LVTTL/CMOS DC Electrical Characteristics⁽⁶⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------|--------------------|-----------|------|-----|-----|---------|
| V_{IH} | Input HIGH Voltage | | 2.0 | | | V |
| V_{IL} | Input LOW Voltage | | | | 0.8 | V |
| I_{IH} | Input HIGH Current | | -125 | | 30 | μA |
| I_{IL} | Input LOW Current | | -300 | | | μA |

Note:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics⁽⁷⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$, $R_L = 50\Omega$ to $V_{CC} - 2V$, unless otherwise stated.

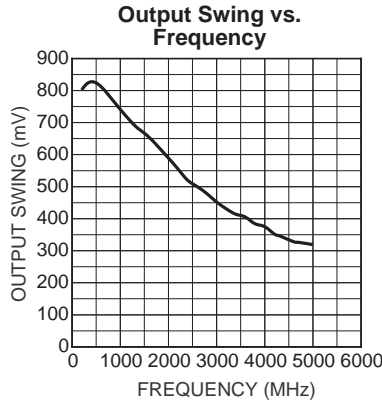
| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|------------------------|---|-------------------------|-----|-----|-----|---------------------|
| f_{MAX} | Maximum Operating Frequency | $V_{OUT} \geq 400mV$ | 2.0 | 3.0 | | GHz |
| t_{pd} | Differential Propagation Delay (IN0 or IN1-to-Q) (SEL-to-Q) | | 200 | 280 | 400 | ps |
| | | | 140 | | 460 | ps |
| Δt_{pd} Tempco | Differential Propagation Delay Temperature Coefficient | | | 65 | | fs/ $^\circ C$ |
| t_{SKEW} | Output-to-Output Part-to-Part | Note 8 | | 10 | 30 | ps |
| | | Note 9 | | | 150 | ps |
| t_{JITTER} | Clock Cycle-to-Cycle Jitter Deterministic Jitter (DJ) Random Jitter (RJ) Total Jitter (TJ) | Note 10 | | | 1 | ps _(rms) |
| | | Note 11 | | | 10 | ps _(rms) |
| | | Note 12 | | | 1 | ps _(pp) |
| | | Note 13 | | | 10 | ps _(pp) |
| | Adjacent Channel Crosstalk-Induced Jitter | Note 14 | | | 0.7 | ps _(rms) |
| t_r, t_f | Output Rise/Fall Time | Full swing, 20% to 80%. | 75 | 130 | 200 | ps |

Notes:

- High-frequency AC-parameters are guaranteed by design and characterization.
- Output-to-output skew is measured between outputs under identical input conditions.
- Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
- Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
- Deterministic Jitter is measured at 2.5Gbps/3.2Gbps, with both K28.5 and $2^{23}-1$ PRBS pattern.
- Random Jitter is measured with a K28.7 character pattern, measured at 2.5Gbps.
- Total Jitter definition: with an ideal clock input of frequency $< f_{MAX}$, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
- Crosstalk is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other at the inputs.

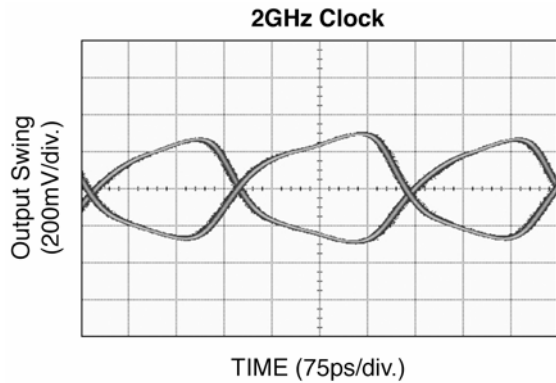
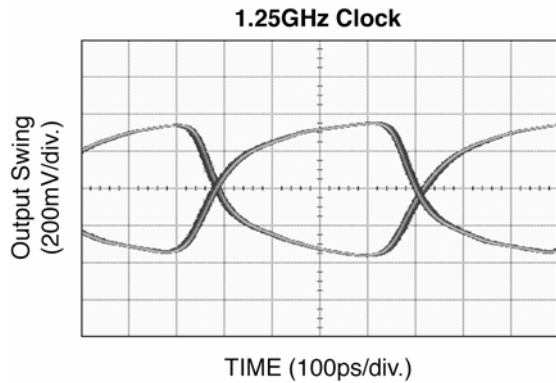
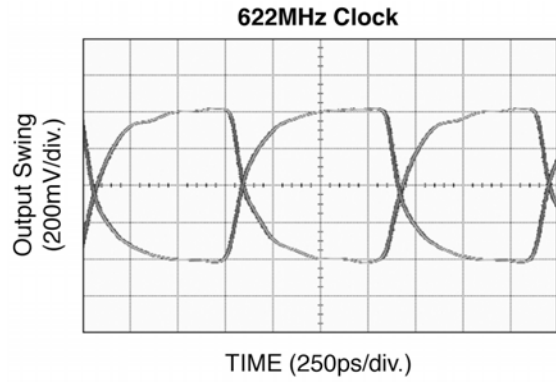
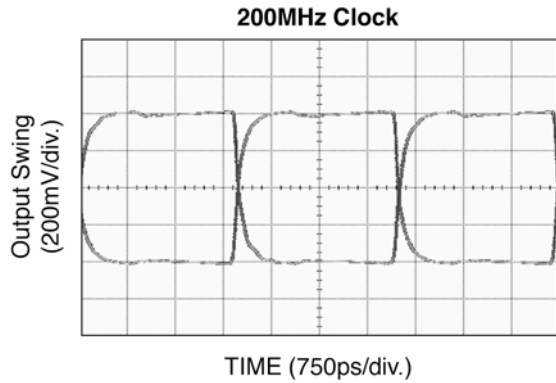
Typical Operating Characteristics

$V_{CC} = 3.3V$, $GND = 0V$, $V_{IN} \geq 400mV$, $t_r/t_f \leq 300ps$, $T_A = 25^\circ C$, unless otherwise stated.



Functional Characteristics

$V_{CC} = 3.3V$, $GND = 0V$, $V_{IN} \geq 400mV$, $t_r/t_f \leq 300ps$, $T_A = 25^\circ C$, unless otherwise stated.



Singled-Ended and Differential Swings



Figure 1a. Single-Ended Voltage Swing

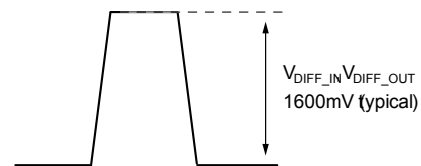
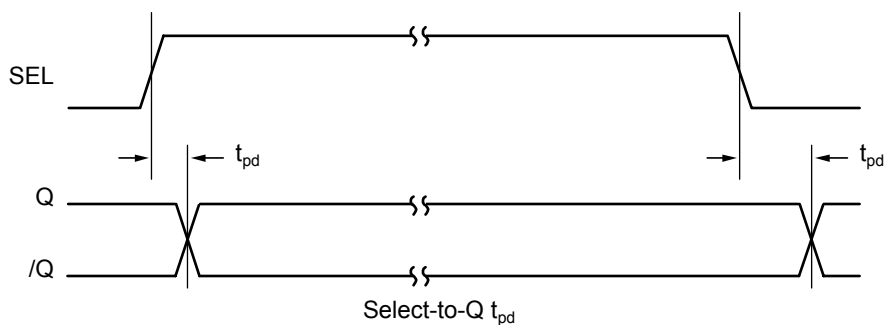
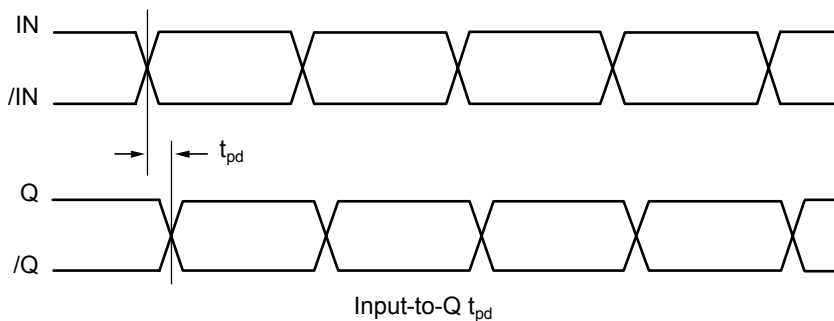


Figure 1b. Differential Voltage Swing

Timing Diagrams



Input and Output Stages

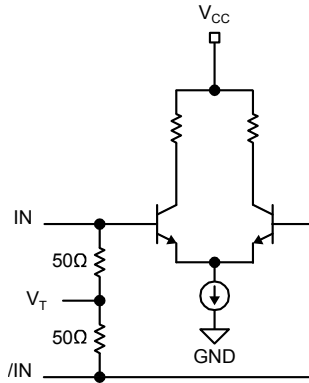


Figure 2a. Simplified Differential Input Stage

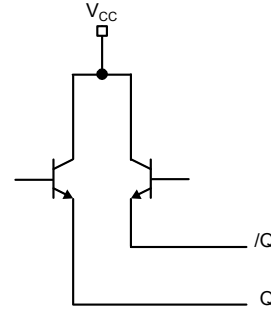


Figure 2b. Simplified LVPECL Output Stage

Input Interface Applications

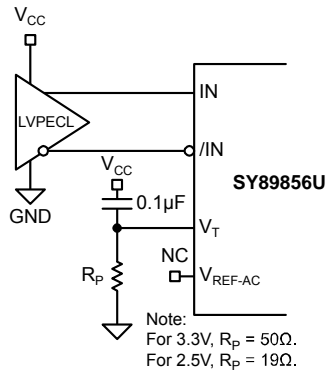


Figure 3a. LVPECL Interface (DC-Coupled)

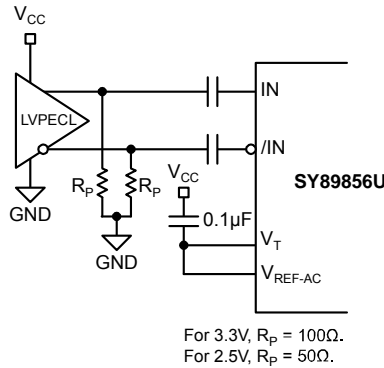


Figure 3b. LVPECL Interface (AC-Coupled)

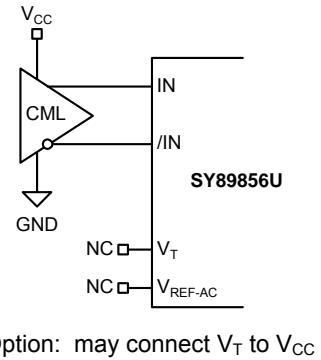


Figure 3c. CML Interface (DC-Coupled)

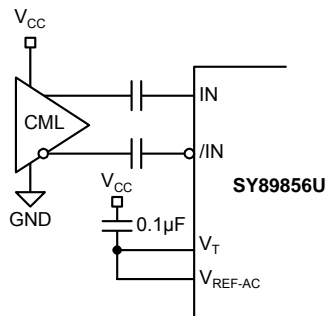


Figure 3d. CML Interface (AC-Coupled)

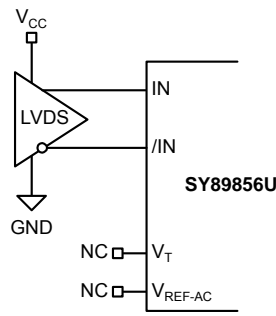
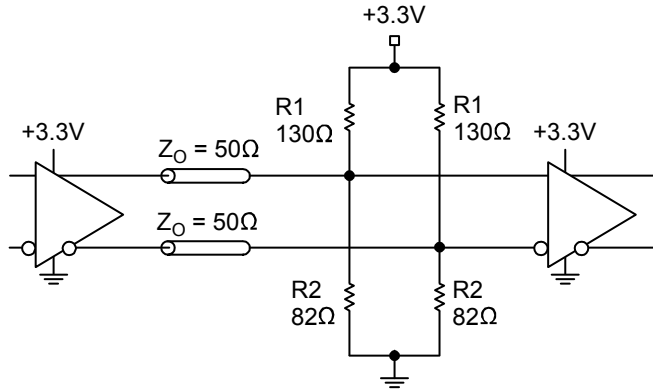


Figure 3e. LVDS Interface (DC-Coupled)

LVPECL Output Interface Applications

LVPECL has a high input impedance and a very low output impedance (open emitter), and a small signal swing which results in low EMI. LVPECL is ideal for driving 50Ω and 100Ω-controlled impedance transmission lines. There are several techniques for

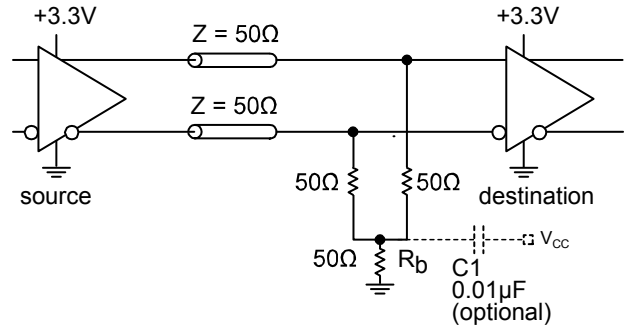
terminating the LVPECL output: Parallel Termination-Thevenin Equivalent, Parallel Termination (3-resistor), and AC-coupled Termination. Unused output pairs may be left floating. However, single-ended outputs must be terminated, or balanced.



Notes:

1. For 2.5V systems, R1 = 250Ω, R2 = 62.5Ω.

Figure 4a. Parallel Termination-Thevenin Equivalent



Notes:

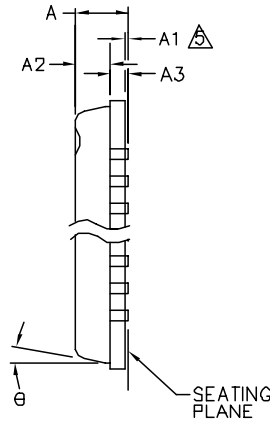
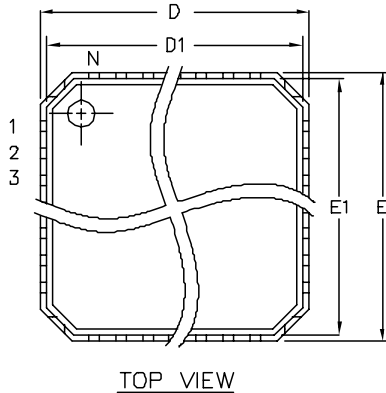
2. Power-saving alternative to Thevenin termination.
3. Place termination resistors as close to destination inputs as possible.
4. R_b resistor sets the DC bias voltage, equal to V_T.
5. For 2.5V systems, R_b = 19Ω.

Figure 4b. Parallel Termination (3-Resistors)

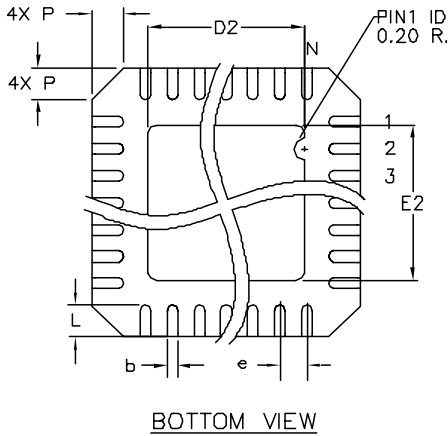
Related Documentation

| Part Number | Function | Data Sheet Link |
|---------------|--|--|
| SY58035U | 4.5GHz, 1:6 LVPECL Fanout Buffer with 2:1 MUX Input and Internal Termination | www.micrel.com/product-info/products/sy58035u.html |
| | MLF [®] Application Note | www.amkor.com/products/notes_papers/MLFappnote.pdf |
| HBW Solutions | New Products and Applications | www.micrel.com/product-info/products/solutions.shtml |

32-Pin MicroLeadFrame® (MLF-32)



| | DIMENSION (mm) | | |
|----|----------------|------|------|
| | MIN. | NOM. | MAX. |
| A | - | 0.85 | 1.00 |
| A1 | 0.00 | 0.01 | 0.05 |
| A2 | - | 0.65 | 0.80 |
| A3 | 0.20 REF. | | |
| D | 5.00 BSC | | |
| D1 | 4.75 BSC | | |
| D2 | 3.15 | 3.30 | 3.45 |
| E | 5.00 BSC | | |
| E1 | 4.75 BSC | | |
| E2 | 3.15 | 3.30 | 3.45 |
| Ø | 12° | | |
| P | 0.24 | 0.42 | 0.60 |
| e | 0.50 BSC | | |
| N | 32 | | |
| L | 0.30 | 0.40 | 0.50 |
| b | 0.18 | 0.23 | 0.30 |



- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. N IS THE NUMBER OF TERMINALS. THE NUMBER OF TERMINALS PER SIDE IS N/4.
 3. THE PIN#1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY.
 4. PACKAGE WARPAGE MAX 0.05mm.
- ⚠ APPLIED FOR EXPOSED PAD AND TERMINALS.

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