TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

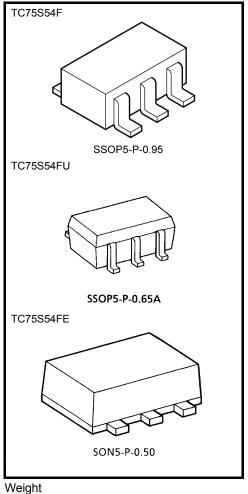
TC75S54F, TC75S54FU, TC75S54FE

Single Operational Amplifier

The TC75S54F/TC75S54FU/TC75S54FE is a CMOS singleoperation amplifier which incorporates a phase compensation circuit. It is designed for use with a low-voltage, low-current power supply; this differentiates this device from conventional general-purpose bipolar op-amps.

Features

- : $V_{DD} = \pm 0.9 \text{ to } \pm 3.5 \text{ V or } 1.8 \text{ to } 7 \text{ V}$ Low-voltage operation
- Low-current power supply : IDD (VDD = 3 V) = $100 \mu\text{A}$ (typ.)
- Built-in phase-compensated op-amp, obviating the need for any external device
- Ultra-compact package



SSOP5-P-0.95 : 0.014 g (typ.) SSOP5-P-0.65A: 0.006 g (typ.) SON5-P-0.50 : 0.003 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

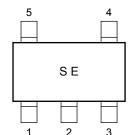
Characteristics		Symbol	Rating	Unit
Supply voltage		V _{DD} , V _{SS}	7	V
Differential input voltage		DV _{IN}	±7	V
Input voltage		V _{IN}	V _{DD} to V _{SS}	V
Power dissipation	TC75S54F/FU	PD	200	mW
	TC75S54FE	רט פי	100	IIIVV
Operating temperature		T _{opr}	-40 to 85	°C
Storage temperature		T _{stg}	-55 to 125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

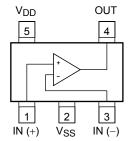
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

> Start of commercial production 1995-01

Marking (top view)



Pin Connection (top view)



Electrical Characteristics

DC Characteristics (V_{DD} = 3.0 V, V_{SS} = GND, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Input offset voltage	V _{IO}	1	$R_S = 1 k\Omega$	_	2	10	mV
Input offset current	I _{IO}	_	_	_	1	_	pA
Input bias current	lı	_	_	_	1	_	pA
Common mode input voltage	CMV _{IN}	2	_	0.0	_	2.1	V
Voltage gain (open loop)	G _V	_	_	60	70	_	dB
Maximum output voltage	V _{OH}	3	R _L ≥ 100 kΩ	2.9	_	_	V
Maximum output voltage	V _{OL}	4	R _L ≥ 100 kΩ	_	_	0.1	\ \ \
Common mode input signal rejection ratio	CMRR	2	V _{IN} = 0.0 to 2.1 V	60	70	_	dB
Supply voltage rejection ratio	SVRR	1	V _{DD} = 1.8 to 7.0 V	60	70	_	dB
Supply current	I _{DD}	5	_	_	100	200	μА
Source current	I _{source}	6	_	100	200	_	μА
Sink current	I _{sink}	7	_	200	700	_	μА

DC Characteristics (V_{DD} = 1.8 V, V_{SS} = GND, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Input offset voltage	V _{IO}	1	$R_S = 10 \text{ k}\Omega$	_	2	10	mV
Input offset current	I _{IO}	_	_	_	1	_	pА
Input bias current	II	_	_	_	1	_	pА
Common mode input voltage	CMV _{IN}	2	_	0.2	_	0.9	V
Voltage gain (open loop)	G _V	_	_	60	70	_	dB
Maximum output voltage	V _{OH}	3	R _L ≥ 100 kΩ	1.7	_	_	V
	V _{OL}	4	R _L ≥ 100 kΩ	_	_	0.1	V
Supply current	I _{DD}	5	_	_	80	160	μА
Source current	I _{source}	6	_	80	160	_	μА
Sink current	I _{sink}	7	_	200	600	_	μА

AC Characteristics ($V_{DD} = 3.0 \text{ V}, V_{SS} = GND, Ta = 25^{\circ}\text{C}$)

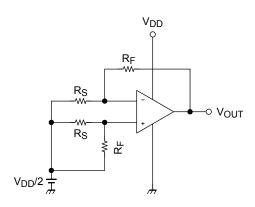
Characteristics	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Slew rate	SR	_	_	_	0.7	_	V/μs
Unity gain cross frequency	f _T	_	_	_	0.9		MHz

AC Characteristics (V_{DD} = 1.8 V, V_{SS} = GND, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Slew rate	SR	_	_	_	0.6	_	V/μs
Unity gain cross frequency	f _T	_	_	_	0.8	_	MHz

Test Circuit

1. SVRR, VIO



SVRR

For each of the two V_{DD} values, measure the V_{OUT} value, as indicated below, and calculate the value of SVRR using the equation shown.

When
$$V_{DD}$$
 = 1.8 V, V_{DD} = V_{DD} 1 and V_{OUT} = V_{OUT} 1 When V_{DD} = 7.0 V, V_{DD} = V_{DD} 2 and V_{OUT} = V_{OUT} 2

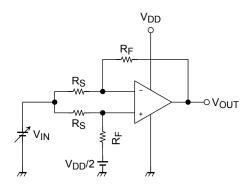
$$SVRR = 20 \ log \left(\left| \frac{V_{OUT}1 - V_{OUT}2}{V_{DD}1 - V_{DD}2} \right| \times \frac{R_S}{R_F + R_S} \right)$$

• V_{IO}

Measure the value of $V_{\mbox{\scriptsize OUT}}$ and calculate the value of $V_{\mbox{\scriptsize IO}}$ using the following equation.

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2}\right) \times \frac{R_S}{R_F + R_S}$$

2. CMRR, CMVIN



CMRR

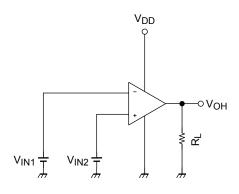
Measure the $V_{\mbox{\scriptsize OUT}}$ value, as indicated below, and calculate the value of the CMRR using the equation shown.

$$CMRR = 20 \log \left(\frac{|V_{OUT}1 - V_{OUT}2|}{|V_{IN}1 - V_{IN}2|} \times \frac{R_S}{R_F + R_S} \right)$$

CMV_{IN}

Input range within which the CMRR specification guarantees $V_{\mbox{OUT}}$ value (as varied by the $V_{\mbox{IN}}$ value).

3. V_{OH}

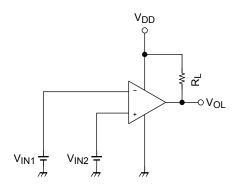


V_{OH}

$$V_{IN1} = \frac{V_{DD}}{2} - 0.05 \text{ V}$$

$$V_{IN2} = \frac{V_{DD}}{2} + 0.05 \text{ V}$$

4. V_{OL}



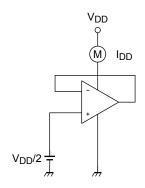
V_{OL}

$$V_{IN1} = \frac{V_{DD}}{2} + 0.05 \text{ V}$$

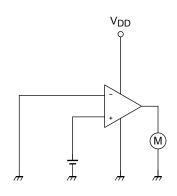
$$V_{IN2} = \frac{V_{DD}}{2} - 0.05 \text{ V}$$

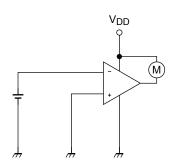
5. I_{DD}

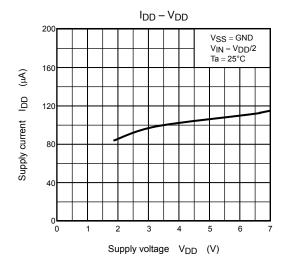
6. I_{source}

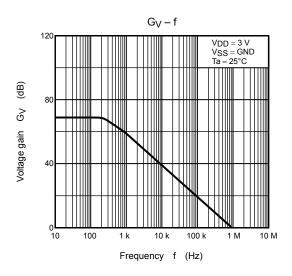


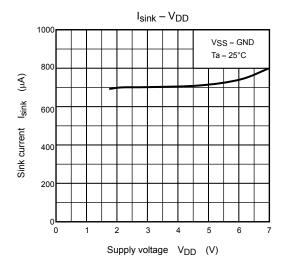
7. I_{sink}

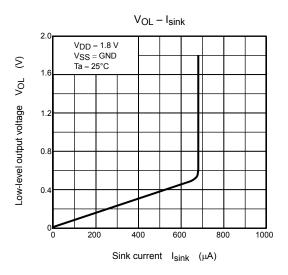


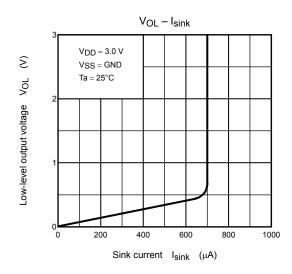


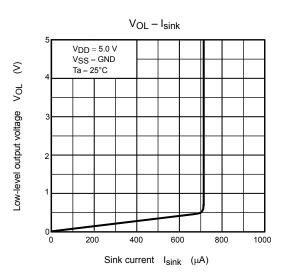


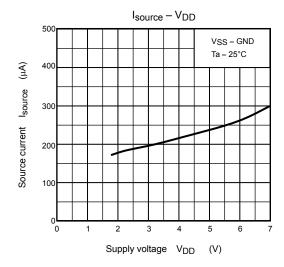


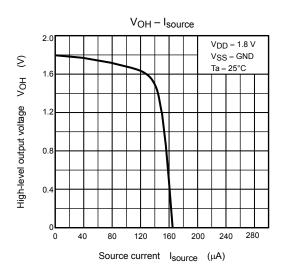


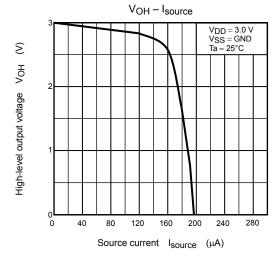


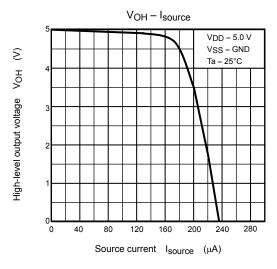


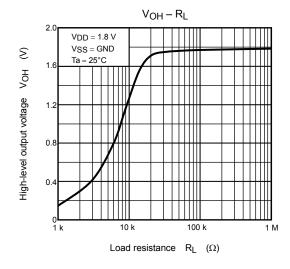


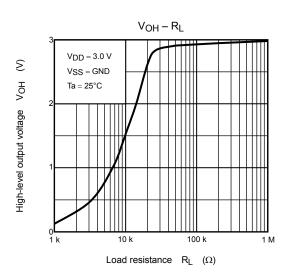


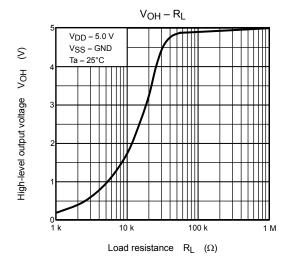


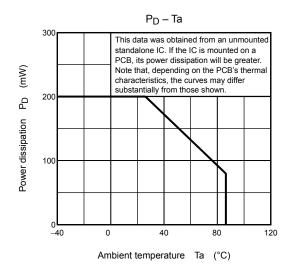








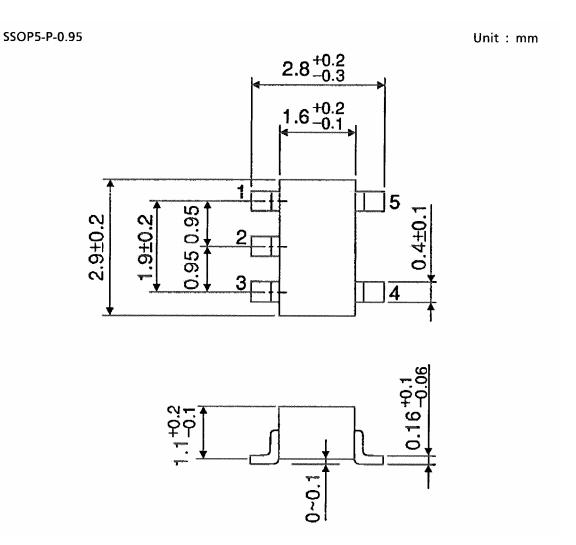




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Package Dimensions

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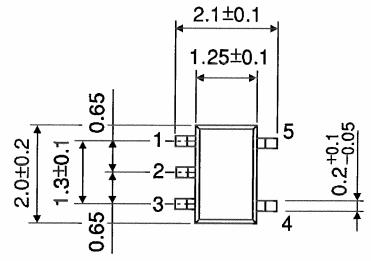
Weight: 0.014 g (typ.)

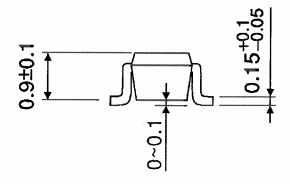
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Package Dimensions

SSOP5-P-0.65A Unit: mm





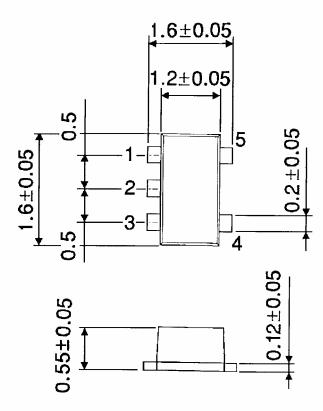
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Weight: 0.006 g (typ.)



Package Dimensions

SON5-P-0.50 Unit: mm



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Weight: 0.003 g (typ.)

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