Ordering number : ENA1228

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

LC88F83B0A — CMOS IC FROM 128K byte, RAM 4096K byte on-chip 16-bit 1-chip Microcontroller

Overview

The LC88F83B0A is a 16-bit microcontroller, centered around an Xstormy16 CPU, integrates on a single chip a number of hardware features such as 32-bit program counter, 16 bits × 16 general purpose register, 128K-byte flash ROM (onboard programmable), 4096-byte RAM, LCD display dedicated RAM, LCD dot matrix driver, on-chip debugging function, programmable timer, a base timer serving as a time-of-day clock, a synchronous SIO interface with automatic transmission capability, an asynchronous SIO (UART) interface, a 12-/8-bit resolution 4-channel AD converter, and a 12-source 11-vector interrupt feature.

Features

■Flash ROM
- 128K × 8bit (Table data reside in the same space.)

■RAM
- 4240 × 8bit
- For data 4096 × 8bit
- For display 72 × 16bit

■LCD Display
- 64 segment × 16 common/72 segment × 8 common (1/4 bias)

* This product is licensed from Silicon Storage Technology, Inc. (USA), and manufactured and sold by SANYO Semiconductor Co., Ltd.

■Instruction Execution Time (min)
- 31.0µs : 32.768kHz crystal used
- 15.6µs (typ) : Low speed RC oscillation (typ: 64kHz)
- 0.25µs : 4.0MHz ceramic filter oscillation
- 1.00µs (typ) : High speed RC oscillation (typ: 1MHz)

■Power Supply Voltage
- 2.3V to 5.5V (Ta =-20 to 75°C) : 32.768kHz crystal used
- 2.3V to 5.5V (Ta =0 to 60°C) : Low speed RC oscillation (typ: 64kHz)
- 2.4V to 5.5V (Ta =-20 to 75°C) : 4.0MHz ceramic filter oscillation
- 2.3V to 5.5V (Ta =0 to 60°C) : High-speed RC oscillation (typ: 1MHz)
- 2.4V to 5.5V (Ta =-20 to 75°C) : When LCD ON

■Consumption Current (3.0V):
- 10.5µA (typ)
  (Ta=25°C, crystal oscillation 32.768kHz, 1/1 dividing frequency, HALT, LCD: ON)
- 300µA (typ)
  (Ta=25°C, crystal oscillation 32.768kHz, CF 4MHz, 1/2 dividing frequency, HALT, LCD: ON)
- 2200µA (typ)
  (Ta=25°C, crystal oscillation 32.768kHz, CF 4MHz, 1/2 dividing frequency, continuous operation, LCD: ON)

■Ports
- Normal withstand voltage I/O ports 20 (P0n, P1n, P20 to P23)
- LCD (COM8/SEG0 to COM15/SEG7 pins are multiplexed with COMMON and SEGMENT)
  - LCD drive bias power supply port 4 ($V_{LCD}1$ to $V_{LCD}4$)
  - Step-up capacitor port 2 (CUP00, CUP01)
  - 16 common mode
    - Segment output 64 (SEG8 to SEG71)
    - Common output 16 (COM0 to COM15)
  - 8 common mode
    - Segment output 72 (SEG0 to SEG71)
    - Common output 8 (COM0 to COM7)
- Oscillation pins 4 (XT1, XT2, CF1, CF2)
- Reset pin 1 (RESB)
- Test pin 1 (TST)
- LCD port power pins 2 ($LCDV_{SS}0$, $LCDV_{SS}1$)
- Power pins 2 (V_{DD}, V_{SS})

■LCD
- LCD power supply : Capacitor step-up type
- Number of dots : 1024 (64 segments × 16 commons) / 576 (72 segments × 8 commons)
- Contrast : Adjustable in 16 steps
- LCD frame frequency : Selectable from 4 types

■Timers
- Timer 0: 16-bit timer that supports PWM/toggle outputs
  1) With 5-bit prescaler
  2) 8-bit PWM × 2/8-bit timer + 8-bit PWM mode selectable
  3) Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator
- Timer 1: 16-bit timer with capture registers
  1) With 5-bit prescaler
  2) May be divided into 2 channels of 8-bit timer
  3) Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator
- Timer 3: 16-bit timer that supports PWM/toggle outputs
  1) With 8-bit prescaler
  2) 8-bit timer × 2ch/8-bit timer + 8-bit PWM mode selectable
  3) Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator
- Timer 4: 16-bit timer that supports toggle outputs
  1) Clock source selectable from system clock and prescaler 0
- Timer 5: 16-bit timer that supports toggle outputs
  1) Clock source selectable from system clock and prescaler 0
- Base timer
  1) Clock may be selected from OSC0 (32.768kHz crystal oscillator) and frequency-divided output of system clock.
  2) Interrupts can be generated in 7 timing schemes.

■Watchdog Timer
1) Driven by the base timer + internal watchdog timer dedicated counter.
2) Interrupt or reset mode selectable

■SIO0: 8-bit synchronous SIO
1) LSB first/MSB first mode selectable
2) It is possible to communicate with 8 bits or less. (1 to 8 bits specifiable in 1-bit units)
3) Built-in 8-bit baudrate generator (transfer clock cycle 4 tCYC to 512 tCYC)
4) Automatic continuous data transmission (9 to 32768 bits specifiable in 1-bit units)
5) Interval function (interval time: 0 to 64 SIOCLKs specifiable in 1 SIOCLK units)
6) Wakeup function

■UART2: Asynchronous SIO
1) Full duplex transmission
2) Start bit 1, data bit 8 (LSB first), stop bit 1
3) Parity bit: None/even parity/odd parity
4) Transfer rate: 8 to 4096 tCYC
5) Baudrate source clock: systemclock/OSC0/OSC1
6) Wakeup function

■AD converter: 12bit × 4 channels
1) 12-/8-bit resolution selectable
2) Analog input: 4 channels
3) Comparator mode
4) Automatic reference voltage generation

■Interrupts

- 12 sources, 11 vector addresses

1) Provides three levels of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.

2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Interrupt Source
1	08000H	WATCHDOGTIMER
2	08004H	BASETIMER
3	08008H	TIMER0
4	08018H	SIO0
5	0801CH	TIMER1
6	08020H	UART2
7	08024H	TIMER3
8	08028H	TIMER4
9	0802CH	TIMER5
10	08030H	ADC
11	0803CH	P00 to P05 SEG71 to SEG64

- The priority level can be specified by three levels.
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels

- Max- whole RAM area (Stack is set in RAM)

■Oscillation Circuits

- OSC1: For system clock
  ceramic oscillation with external CGC, CDC or RC oscillation (external RCR1)
- OSC0: For low-speed system clock, base timer count, for LCD display
  32kHz crystal oscillation with external CGX, CDX or RC oscillation (external RCR0)
- Internal oscillation circuit: Internal RC

* Depends on control resister for each oscillator operation and stop.
  Initial setting - External oscillation stop, internal RC oscillation operation

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) Released by a system reset or occurrence of an interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) OSC1, internal RC and X'tal oscillators automatically stop operation.
  2) There are the following methods of resetting the HOLD.
    (1) Setting the reset pin to the low level
    (2) Having an interrupt source established in the SIO0
    (3) Having an interrupt source established in the UART2
    (4) Having an interrupt source established in the P00 to P05
    (5) Having an interrupt source established in the SEG71 to SEG64
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except using OSC0.
  1) The OSC1 and internal RC oscillators automatically stop operation.
  2) The state of OSC0 oscillation established when the X'tal HOLD mode is entered is retained.
  3) There are the following methods of resetting the X'tal HOLD mode.
    (1) Setting the reset pin to the low level
    (2) Having an interrupt source established in the base timer circuit
    (3) Having an interrupt source established in the timers 0, 1, 3, 4, 5
    (4) Having an interrupt source established in the SIO0
    (5) Having an interrupt source established in the UART2
    (6) Having an interrupt source established in the P00 to P05
    (7) Having an interrupt source established in the SEG71 to SEG64

■On-chip debugger

- Supports software debugging with the IC mounted on the target board.
- Supports tracing, realtime monitoring, and breakpoint setting.
- Single-wire communication

■Package Form

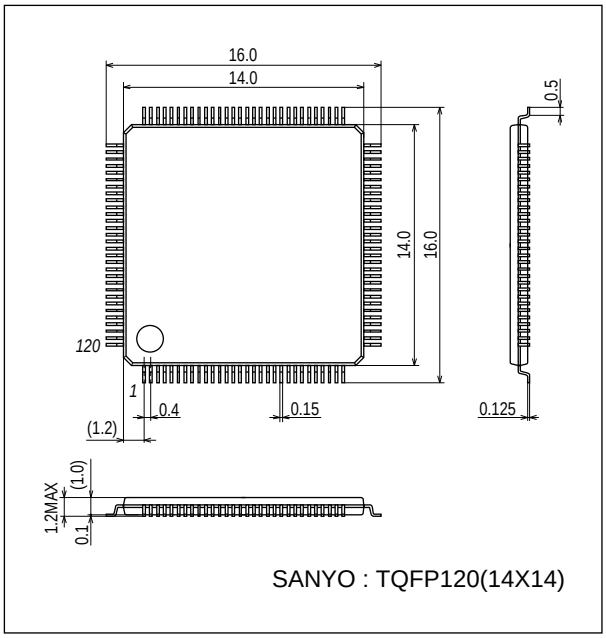
- TQFP120(14×14): Lead-free type

■Development Tools

- On-chip debugger : EOCUIF1 + LC88F83B0A
- Programming boards :

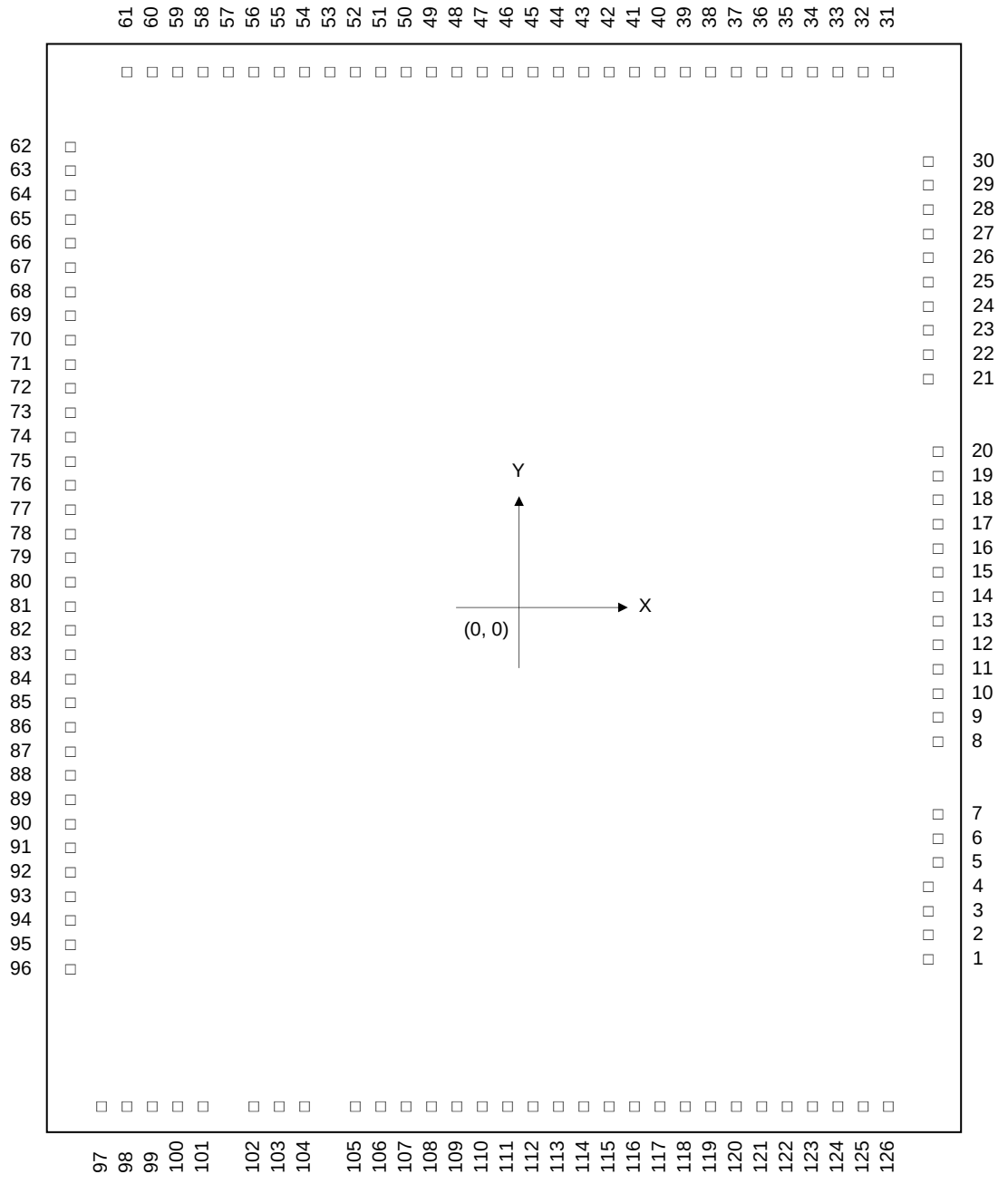
Package Dimensions

unit : mm (typ)
3257A



Pad Assignment

- Chip size (X × Y) : 3.40mm × 3.19mm
- Pad size : 59μm
- Pad pitch : 80μm
- Chip thickness : 280μm ± 20μm



Note: Pin numbers assigned to a package differ from pad numbers assigned to a chip.
Numbers in the above figure show the pad numbers of the chip.

Pad Coordinates Table

Pad No.	Pin Name	Coordinates		Pad No.	Pin Name	Coordinates	
		X μm	Y μm			X μm	Y μm
1	P20	1567.4	-1308	48	SEG29	-192	1462.4
2	P21	1567.4	-1228	49	SEG28	-272	1462.4
3	P22	1567.4	-1147	50	SEG27	-352	1462.4
4	P23	1567.4	-1067	51	SEG26	-432	1462.4
5	SEG71	1606.99	-951.8	52	SEG25	-512	1462.4
6	SEG70	1606.99	-863.6	53	SEG24	-592	1462.4
7	SEG69	1606.99	-775.4	54	SEG23	-672	1462.4
8	SEG68	1606.99	-606.8	55	SEG22	-752	1462.4
9	SEG67	1606.99	-518.6	56	SEG21	-832	1462.4
10	SEG66	1606.99	-430.4	57	SEG20	-912	1462.4
11	SEG65	1606.99	-342.2	58	SEG19	-992	1462.4
12	SEG64	1606.99	-254	59	SEG18	-1072	1462.4
13	SEG63	1606.99	-165.8	60	SEG17	-1152	1462.4
14	SEG62	1606.99	-77.6	61	SEG16	-1232	1462.4
15	SEG61	1606.99	10.6	62	SEG15	-1567.4	1335
16	SEG60	1606.99	98.8	63	SEG14	-1567.4	1255
17	SEG59	1606.99	187	64	SEG13	-1567.4	1175
18	SEG58	1606.99	275.2	65	SEG12	-1567.4	1095
19	SEG57	1606.99	363.4	66	SEG11	-1567.4	1015
20	SEG56	1606.99	451.6	67	SEG10	-1567.4	935
21	SEG55	1567.4	573	68	SEG9	-1567.4	855
22	SEG54	1567.4	653	69	SEG8	-1567.4	775
23	SEG53	1567.4	733	70	-	-	-
24	SEG52	1567.4	813	71	COM15/SEG7	-1567.4	615
25	SEG51	1567.4	893	72	-	-	-
26	SEG50	1567.4	973	73	COM14/SEG6	-1567.4	455
27	SEG49	1567.4	1053	74	-	-	-
28	SEG48	1567.4	1133	75	COM13/SEG5	-1567.4	295
29	SEG47	1567.4	1213	76	-	-	-
30	SEG46	1567.4	1293	77	COM12/SEG4	-1567.4	135
31	$LCDV_{SS}1$	1190	1462.4	78	-	-	-
32	SEG45	1088	1462.4	79	COM11/SEG3	-1567.4	-25
33	SEG44	1008	1462.4	80	-	-	-
34	SEG43	928	1462.4	81	COM10/SEG2	-1567.4	-185
35	SEG42	848	1462.4	82	-	-	-
36	SEG41	768	1462.4	83	COM9/SEG1	-1567.4	-345
37	SEG40	688	1462.4	84	-	-	-
38	SEG39	608	1462.4	85	COM8/SEG0	-1567.4	-505
39	SEG38	528	1462.4	86	COM7	-1567.4	-585
40	SEG37	448	1462.4	87	COM6	-1567.4	-665
41	SEG36	368	1462.4	88	COM5	-1567.4	-745
42	SEG35	288	1462.4	89	COM4	-1567.4	-825
43	SEG34	208	1462.4	90	COM3	-1567.4	-905
44	SEG33	128	1462.4	91	COM2	-1567.4	-985
45	SEG32	48	1462.4	92	COM1	-1567.4	-1065
46	SEG31	-32	1462.4	93	COM0	-1567.4	-1145
47	SEG30	-112	1462.4	94	$LCDV_{SS}0$	-1567.4	-1240

Continued on next page.

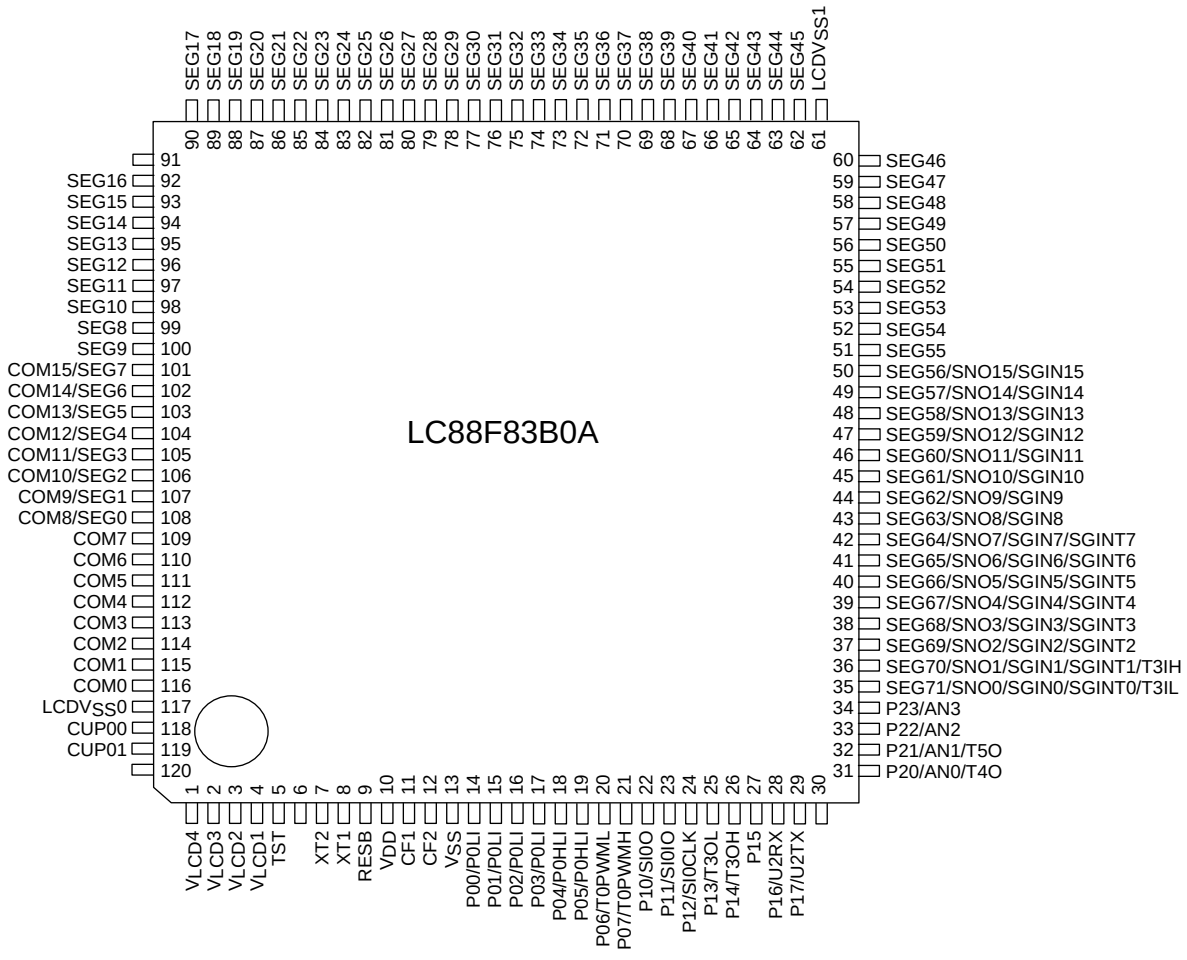
Continued from preceding page.

Pad No.	Pin Name	Coordinates		Pad No.	Pin Name	Coordinates	
		X μm	Y μm			X μm	Y μm
95	CUP00	-1567.4	-1335.8	111	P00	205	-1462.4
96	CUP01	-1567.4	-1415.8	112	P01	285	-1462.4
97	$V_{LCD}4$	-1295.45	-1462.4	113	P02	365	-1462.4
98	$V_{LCD}3$	-1215.45	-1462.4	114	P03	445	-1462.4
99	$V_{LCD}2$	-1130.8	-1462.4	115	P04	525	-1462.4
100	$V_{LCD}1$	-1050.8	-1462.4	116	P05	605	-1462.4
101	TST	-965	-1462.4	117	P06	685	-1462.4
102	XT2	-723	-1462.4	118	P07	765	-1462.4
103	XT1	-643	-1462.4	119	P10	845	-1462.4
104	RESB	-563	-1462.4	120	P11	925	-1462.4
105	V_{DD}	-383.5	-1462.4	121	P12	1005	-1462.4
106		-272.5	-1462.4	122	P13	1085	-1462.4
107	CF1	-172	-1462.4	123	P14	1165	-1462.4
108	CF2	-92	-1462.4	124	P15	1245	-1462.4
109	V_{SS}	3	-1462.4	125	P16	1325	-1462.4
110		108	-1462.4	126	P17	1405	-1462.4

Note:

- Pad coordinates shown in above table are referenced at the center of the IC-chip as an origin.
- There are two pads for each V_{DD} and V_{SS}, and each set of pads needs double-bonding.

Pin Assignment

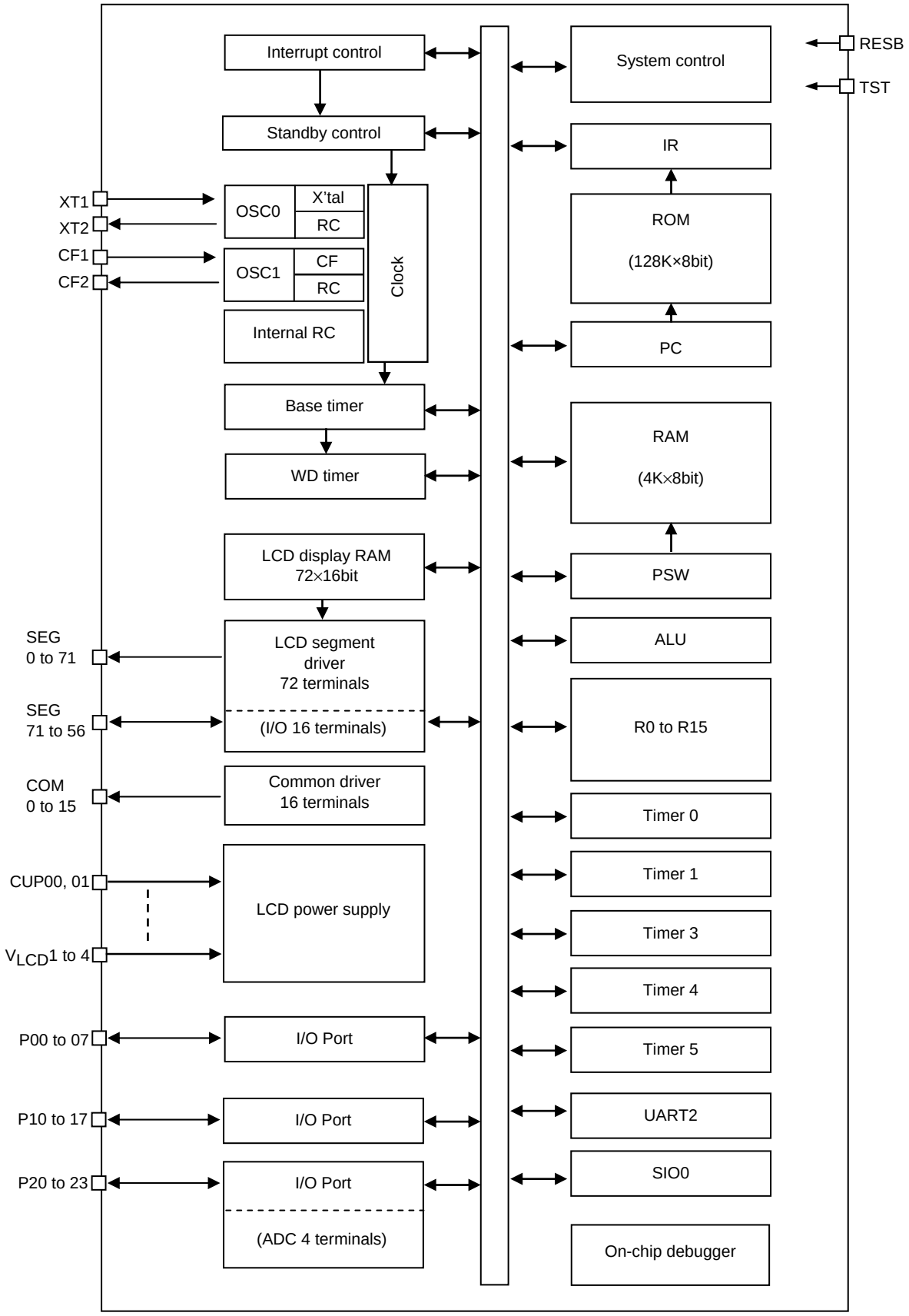


Top view

SANYO: TQFP120(14×14) "Lead-free Type"

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	$V_{LCD}4$	31	P20/AN0/T4O	61	$LCDV_{SS}1$	91	
2	$V_{LCD}3$	32	P21/AN1/T5O	62	SEG45	92	SEG16
3	$V_{LCD}2$	33	P22/AN2	63	SEG44	93	SEG15
4	$V_{LCD}1$	34	P23/AN3	64	SEG43	94	SEG14
5	TST	35	SEG71/SNO0 /SGIN0/SGINT0 /T3IL	65	SEG42	95	SEG13
6		36	SEG70/SNO1 /SGIN1/SGINT1 /T3IH	66	SEG41	96	SEG12
7	XT2	37	SEG69/SNO2 /SGIN2/SGINT2	67	SEG40	97	SEG11
8	XT1	38	SEG68/SNO3 /SGIN3/SGINT3	68	SEG39	98	SEG10
9	RESB	39	SEG67/SNO4 /SGIN4/SGINT4	69	SEG38	99	SEG9
10	V_{DD}	40	SEG66/SNO5 /SGIN5/SGINT5	70	SEG37	100	SEG8
11	CF1	41	SEG65/SNO6 /SGIN6/SGINT6	71	SEG36	101	COM15/SEG7
12	CF2	42	SEG64/SNO7 /SGIN7/SGINT7	72	SEG35	102	COM14/SEG6
13	V_{SS}	43	SEG63/SNO8 /SGIN8	73	SEG34	103	COM13/SEG5
14	P00/P0LI	44	SEG62/SNO9 /SGIN9	74	SEG33	104	COM12/SEG4
15	P01/P0LI	45	SEG61/SNO10 /SGIN10	75	SEG32	105	COM11/SEG3
16	P02/P0LI	46	SEG60/SNO11 /SGIN11	76	SEG31	106	COM10/SEG2
17	P03/P0LI	47	SEG59/SNO12 /SGIN12	77	SEG30	107	COM9/SEG1
18	P04/P0HLI	48	SEG58/SNO13 /SGIN13	78	SEG29	108	COM8/SEG0
19	P05/P0HLI	49	SEG57/SNO14 /SGIN14	79	SEG28	109	COM7
20	P06/T0PWML	50	SEG56/SNO15 /SGIN15	80	SEG27	110	COM6
21	P07/T0PWMH	51	SEG55	81	SEG26	111	COM5
22	P10/SI0O	52	SEG54	82	SEG25	112	COM4
23	P11/SI0IO	53	SEG53	83	SEG24	113	COM3
24	P12/SI0CLK	54	SEG52	84	SEG23	114	COM2
25	P13/T3OL	55	SEG51	85	SEG22	115	COM1
26	P14/T3OH	56	SEG50	86	SEG21	116	COM0
27	P15	57	SEG49	87	SEG20	117	$LCDV_{SS}0$
28	P16/U2RX	58	SEG48	88	SEG19	118	CUP00
29	P17/U2TX	59	SEG47	89	SEG18	119	CUP01
30		60	SEG46	90	SEG17	120	

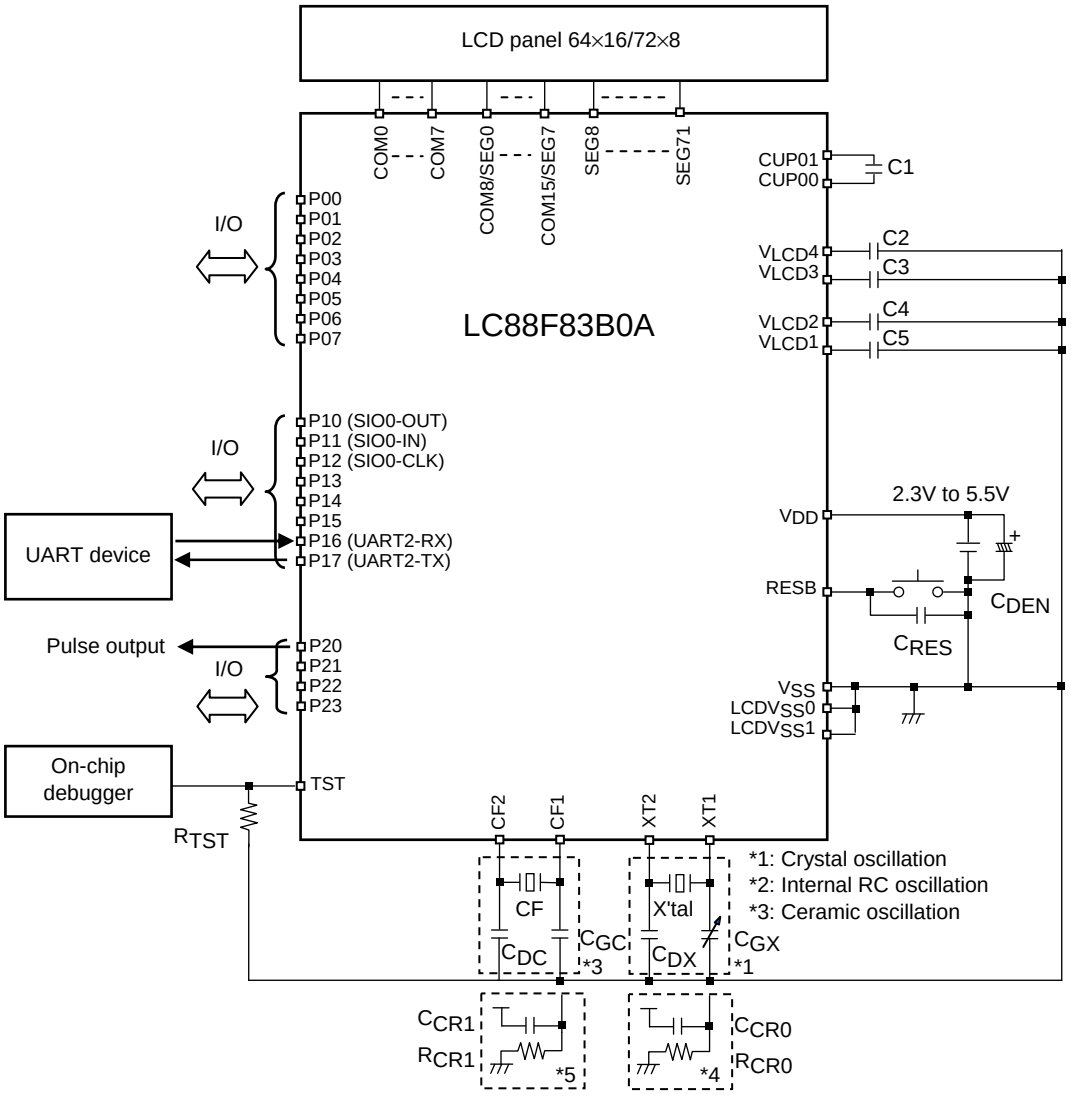
System Block Diagram



Pin Description

Pin Name		I/O	Description
V_{DD}		-	+ power supply pin
V_{SS}		-	- power supply pin
$V_{LCD}1$ to 4		-	LCD bias power port (capacitor connection port)
$LCDV_{SS}0$, $LCDV_{SS}1$		-	LCD power supply pin
CUP00, 01		-	Switching pin for generating LCD driving voltage Connect capacitor between both ports.
OSC0	XT1	I	Oscillator circuit for system clock (low speed) • 32.768kHz crystal oscillator and capacitor for oscillation connection • XT1: Resistor connection for RC oscillation (RC model)
	XT2	O	
OSC1	CF1	I	Oscillator circuit for system clock (high speed) • Ceramic oscillator and capacitor for oscillator connection • CF1: Resistance connection for RC oscillator (RC model)
	CF2	O	
PORT 0 P00 to P07		I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Shared pins P00 to P05 : Interrupt function P06: Timer 0 PWML output P07: Timer 0 PWMH output
PORT 1 P10 to P17		I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Shared pins P10: SIO0 data output P11: SIO0 data input/Bus I/O P12: SIO0 Clock I/O P13: Timer 3 PWML output P14: Timer 3 PWMH output P16: UART 2 receive P17: UART 2 send
PORT 2 P20 to P23		I/O	• 4-bit I/O port • I/O specifiable in 1-bit units P20 to P23: AD converter input ports (AN0 to AN3) • Shared pins P20: Timer 4 output P21: Timer 5 output
COM0 to COM7		O	• LCD common output port
COM8/SEG0 to COM15/SEG7		O	• LCD common output port/segment output port common output/segment output is switched according to the register.
SEG8 to SEG55		O	• LCD segment output port
SEG56 to SEG71		I/O	• LCD segment output port • SEG71 to SEG56: General purpose Nch OD output/General purpose input SEG71 to SEG56 can switch LCD output, a general-purpose Nch OD output, and a general-purpose input (every 4 bits). • SEG71 to SEG64: Interrupt function (every 4 bits) Selecting sampling frequency for chattering removal (every 4 bits) Level/edge selection (every 4 bits) Hi/Low level or rise/fall selection (every 1 bit) • SEG71 to SEG70: Timer 3 external input
RESB		I	• Input terminal for system initialization It operates reset by the “LOW” input. with pull-up resistor
TST		I/O	• TEST pin • On-chip debugger communication terminal Used with pull-down or V_{SS} *Connect 100kΩ between this pin and V_{SS} when on-chip debugger is used.

Application circuit



X'tal	Crystal oscillator
C_{GX}	Trimmer capacitor
C_{DX}	Capacitance for X'tal
R_{CR0}	Resistor for low-speed oscillation *4: RC oscillation specification
C_{CR0}	Capacitor for low-speed oscillation *4: RC oscillation specification (**1)
(**1)	0.1µF capacitor is recommended when using XT1/XT2 as a system clock.
CF	Ceramic oscillator
C_{GC}	Capacitance for CF
C_{DC}	Capacitance for CF
R_{CR1}	Resistor for high-speed oscillation *5: RC oscillation specification
C_{CR1}	Capacitor for high-speed oscillation *5: RC oscillation specification
C1 to C5	Capacitor
C_{DEN}	Electrolytic capacitor
C_{RES}	Capacitance for RESB
R_{TST}	Resister when on-chip debugger is used

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = $LCDV_{SS}0$ = $LCDV_{SS}1$ = 0V

Parameter		Symbol	Pin/Remarks	Conditions		Specification			
					V_{DD}[V]	min	typ	max	unit
Maximum supply voltage		V_{DD} max	V_{DD}	V_{DD}		-0.3		+6.5	V
LCD supply voltage		V_{LCD} max	$V_{LCD}2$ to $V_{LCD}4$	V_{DD}		-0.3		+6.5	
LCD maximum supply voltage		LCD max	SEG0 to SEG71 COM0 to COM15	V_{DD}, $V_{LCD}4$		-0.3		+6.5	
Input voltage		V_I(1)	RESB, XT1, CF1			-0.3		V_{DD}+0.3	
Input/output voltage		V_{IO}(1)	PORT 0, 1, 2 SEG71 to SEG56			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	PORT0, 2	CMOS output selected Current at each pin		-5			mA
		IOPH(2)	PORT1	CMOS output selected Current at each pin		-14			
	Mean output current (Note 1-1)	IOMH(1)	PORT0, 2	CMOS output selected Current at each pin		-3			
		IOMH(2)	PORT1	CMOS output selected Current at each pin		-9			
	Total output current	ΣIOAH(1)	PORT0, 2	Total of all pins		22.5			
		ΣIOAH(2)	PORT1	Total of all pins		25			
		ΣIOAH(3)	PORT 0, 1, 2	Total of all pins		47.5			
Low level output current	Peak output current	IOPL(1)	PORT0, 2	Current at each pin				13	
		IOPL(2)	PORT1	Current at each pin				17	
	Mean output current (Note 1-1)	IOML(1)	PORT0, 2	Current at each pin				7.5	
		IOML(2)	PORT1	Current at each pin				10.5	
	Total output current	ΣIOAL(1)	PORT0, 2	Total of all pins				35	
		ΣIOAL(2)	PORT1	Total of all pins				60	
		ΣIOAL(3)	PORT 0, 1, 2	Total of all pins				80	
Allowable power dissipation		Pd max	TQFP120(14×14)	Ta=-20 to +75°C				250	mW
Operating ambient temperature		Topg				-20		75	°C
Storage ambient temperature		Tstg				-65		125	

Note 1-1: The mean output current is a mean value measured over 100ms.

Note: We assume that the measurements for the allowable operating ranges and electrical characteristics described in this document are performed with the chip mounted in a package.
Although this product is shipped in chip form, the characteristic values listed in this document are measured with this IC mounted on a SANYO-designated package at operating ambient temperature range of -20°C to +70°C.
The specifications of this product in package form or in chip forms are basically identical, however, the characteristics of the product in chip form may vary depending on the board on which the product is mounted, the bonding pressure, and the type of mold resin used.

Allowable Operating Conditions at Ta = -20°C to +75°C, V_{SS} = $LCDV_{SS}0$ = $LCDV_{SS}1$ = 0V

Parameter	Symbol	Pin /Remarks	Conditions		Ratings			
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage (Note2-1)	V_{DD}(1)	V_{DD}	0.238µs≤tCYC≤100µs		2.6		5.5	V
			0.476µs≤tCYC≤100µs		2.4		5.5	
			0.909µs≤tCYC≤100µs		2.3		5.5	
LCD drive voltage	V_{LCD}(1)	V_{LCD}2 to V_{LCD}4					5.5	
Memory sustaining supply voltage	VHD	V_{DD}	RAM and register contents sustained in HOLD mode.		2.0		5.5	
High level input voltage	V_{IH}(1)	Port 0, 1	Output disabled		0.30V_{DD} +0.70		V_{DD}	
	V_{IH}(2)	RESB			0.75V_{DD}		V_{DD}	
Low level input voltage	V_{IL}(1)	Port 0, 1	Output disabled		V_{SS}		0.10V_{DD} +0.40	
	V_{IL}(2)	RESB			V_{SS}		0.25V_{DD}	
Oscillating frequency range (Note2-3)	FOSC0	XT1, XT2	Crystal oscillation	2.3 to 5.5		32.768		kHz
			Low speed RC oscillation (Note2-2)	2.3 to 5.5	30		80	
	FOSC1	CF1, CF2	Ceramic oscillation	2.4 to 5.5	400		4200	
			High-speed RC oscillation (Note2-2)	2.4 to 5.5	400		4200	
				2.3 to 5.5	400		1100	
	FINTRC		Internal RC oscillation			1000		

Note2-1: V_{DD} must be held greater than or equal to 2.7V in the flash ROM onboard programming mode.
Note2-2: Ta=0°C to 60°C
Note2-3: The parts value of oscillation circuit is shown in table 1 and table 2.

Electrical Characteristics at Ta = -20°C to +75°C, V_{SS} = LCDV_{SS}0 = LCDV_{SS}1 = 0V

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
High level input current	I_{IH}(1)	PORT 0, 1, 2	Output disabled Pull-up resister OFF V_{IN}=V_{DD} (including OFF state leak current of the output Tr.)	2.7 to 5.5			1	μA
	I_{IH}(2)	RESB	V_{IN}=V_{DD}	2.7 to 5.5			1	
Low level input current	I_{IL}(1)	PORT 0, 1, 2	Output disabled Pull-up resister OFF V_{IN}=V_{SS} (including OFF state leak current of the output Tr.)	2.7 to 5.5	-1			
	I_{IL}(2)	PORT 0, 1, 2	Output disabled Pull-up resister ON V_{IN}=V_{SS} (including OFF state leak current of the output Tr.)	4.5 to 5.5	-117		-25	
	I_{IL}(3)			2.7 to 3.0	-31		-5.8	
	I_{IL}(4)	RESB		4.5 to 5.5	-10.2		-3.7	
	I_{IL}(5)			2.7 to 3.0	-6.3		-2.4	
High level output current	I_{OH}(1)	CMOS output mode PORT0, 2	V_{OH}(1)=V_{DD}-1.0V	4.5 to 5.5			-3.7	mA
	I_{OH}(2)			2.7 to 3.0			-1.6	
	I_{OH}(3)	CMOS output mode PORT1		4.5 to 5.5			-10	
	I_{OH}(4)			2.7 to 3.0			-4.5	
Low level output current	I_{OL}(1)	PORT0, 2	V_{OL}(1)=V_{SS}+1.0V	4.5 to 5.5	10			
	I_{OL}(2)			2.7 to 3.0	4.4			
	I_{OL}(3)	PORT1		4.5 to 5.5	14.5			
	I_{OL}(4)			2.7 to 3.0	6.5			
	I_{OL}(5)	SEG71 to SEG56		4.5 to 5.5	0.5			
	I_{OL}(6)			2.7 to 3.0	0.5			
Common output current	I_{OH}(5)	COM0 to COM15	V_{OH}(2)=V_{LCD}4-0.05V	2.7 to 5.5			-25	μA
	I_{OL}(7)		V_{OL}(2)=V_{SS}+0.05V		25			
Segment output current	I_{OH}(6)	SEG0 to SEG71	V_{OH}(2)=V_{LCD}4-0.05V	2.7 to 5.5			-10	
	I_{OL}(8)		V_{OL}(2)=V_{SS}+0.05V		10			
Hysterisis voltage	VHYS(1)	PORT 0, 1, 2 RESB		2.7 to 5.5		0.1V_{DD}		V
Pin capacitance	CP	All pins	For pins other than that under test: V_{IN}=V_{SS} f=1MHz Ta=25°C	2.7 to 5.5		10		pF

LCD Drive Voltage at Ta = -20°C to +75°C, V_{SS} = $LCDV_{SS}0$ = $LCDV_{SS}1$ = 0V

Special notes: 0.1µF capacitor must be connected to $V_{LCD}1$, $V_{LCD}2$, $V_{LCD}3$, and $V_{LCD}4$. (with no panel load)

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
LCD drive voltage	$V_{LCD}1$	V_{DD} $V_{LCD}1$	Contrast “00”	2.4 to 5.5	Typ ×0.88	1.030	Typ ×1.10	V
			Contrast “01”			1.045		
			Contrast “02”			1.060		
			Contrast “03”			1.075		
			Contrast “04”			1.090		
			Contrast “05”			1.105		
			Contrast “06”			1.120		
			Contrast “07”			1.135		
			Contrast “08”			1.150		
			Contrast “09”			1.165		
			Contrast “10”			1.180		
			Contrast “11”			1.195		
			Contrast “12”			1.210		
			Contrast “13”			1.225		
			Contrast “14”			1.240		
			Contrast “15”			1.255		
	$V_{LCD}2$					$2×V_{LCD}1$		
	$V_{LCD}3$					$3×V_{LCD}1$		
	$V_{LCD}4$					$4×V_{LCD}1$		

Serial I/O Characteristics at Ta = -20°C to +75°C, V_{SS} = LCDV_{SS}0 = LCDV_{SS}1 = 0V

1. SIO0 Serial I/O Characteristics (Wake-up function is not in use) (Note 4-1-1)

Parameter			Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	See Fig. 6.	2.3 to 5.5	4			tCYC
		Low level pulse width	tSCKL(1)				2			
		High level pulse width	tSCKH(1)				2			
			tSCKHA(1)		Automatic communication mode See Fig. 6.		6			
			tSCKHBSY(1a)		Automatic communication mode See Fig. 6.		23			
			tSCKHBSY(1b)		Excluding Automatic communication mode See Fig. 6.		4			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	CMOS output selected See Fig. 6.	2.3 to 5.5	4			tCYC
		Low level pulse width	tSCKL(2)				1/2			tSCK
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2)		Automatic communication mode CMOS output selected See Fig. 6.		6			tCYC
			tSCKHBSY(2a)		Automatic communication mode CMOS output selected See Fig. 6.		4		23	
			tSCKHBSY(2b)		Excluding automatic communication mode See Fig. 6.		4			
Serial input	Data setup time		tsDI(1)	SI0(P11), SB0(P11)	Must be specified with respect to rising edge of SIOCLK. See Fig. 6.	2.3 to 5.5	0.03			µs
	Data hold time		thDI(1)				0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	(Note4-1-2)	2.3 to 5.5			1tCYC +0.05	
	Output clock		tdDO(2)		(Note4-1-2)				1tCYC +0.05	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig.6.

2. SIO1 Serial I/O Characteristics (Wake-up function is not in use) (Note 4-2-1)

Parameter			Symbol	Pin/Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK0(P12)	See Fig. 6.	2.3 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
			tSCKHBSY(3)				2			
Serial input	Data setup time		tsDI(2)	SI0(P11), SB0(P11)	Must be specified with respect to rising edge of SIOCLK. See Fig. 6.	2.3 to 5.5	0.03			µs
	Data hold time		thDI(2)				0.03			
Serial output	Input clock	Output delay time	tdD0(3)	SO0(P10), SB0(P11)	(Note4-2-2)	2.3 to 5.5			1tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-2-2: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig.6.

UART2 Operating Conditions at Ta = -20 to +75°C, V_{SS} = $LCDV_{SS}0$ = $LCDV_{SS}1$ = 0V

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Transfer rate	UBR2	URX2(P16), UTX2(P17)		2.3 to 5.5	8		4096	tCYC

Pulse Input Conditions at Ta = -20 to +75°C, V_{SS} = $LCDV_{SS}0$ = $LCDV_{SS}1$ = 0V

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tPIL(1)	RESB	Resetting is enabled.	2.3 to 5.5	50			µs

AD Converter Characteristics at V_{SS} = $LCDV_{SS}0$ = $LCDV_{SS}1$ = 0V

<12-bits AD Converter Mode/Ta= -10°C to +75°C>

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(SEG71) to AN3(SEG68)		2.9 to 5.5		12		bit
Absolute accuracy	ET		(Note7-1)	2.9 to 5.5			±16	LSB
Conversion time	TCAD		See Conversion time calculation formulas. (Note7-2)	2.9 to 5.5	90		130	µs
Analog input voltage range	VAIN			2.9 to 5.5	V_{SS}		V_{DD}	V
Analog ports input current	IAINH		VAIN=V_{DD}	2.9 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	2.9 to 5.5	-1			

<8-bits AD Converter Mode/Ta= -10°C to +75°C >

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(SEG71) to AN3(SEG68)		2.9 to 5.5		8		bit
Absolute accuracy	ET		(Note7-1)	2.9 to 5.5			±1.5	LSB
Conversion time	TCAD		See Conversion time calculation formulas. (Note7-2)	2.9 to 5.5	55		75	µs
Analog input voltage range	VAIN			2.9 to 5.5	V_{SS}		V_{DD}	V
Analog ports input current	IAINH		VAIN=V_{DD}	2.9 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	2.9 to 5.5	-1			

<Conversion Time Calculation Formulas>

12-bits AD Converter Mode: TCAD (Conversion time) = ((52/(Division ratio))+2) × tCYC

8-bits AD Converter Mode: TCAD (Conversion time) = ((32/(Division ratio))+2) × tCYC

<Recommended Operating Conditions>

External Oscillator FmCF[MHz]	Operating Supply Voltage Range V_{DD}[V]	System Division Ratio (SYSDIV)	Cycle Time tCYC [ns]	AD Division Ratio (ADDIV)	AD Conversion Time (TCAD)[µs]	
					12-bit AD	8-bit AD
CF-4	2.9 to 4.0	1/1	250	1/8	104.5	64.5
		1/2	500	1/4	105.0	65.0

Note 7-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 7-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:

- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

Consumption Current Characteristics at Ta = -20 to +75°C, V_{SS} = $LCDV_{SS}0$ = $LCDV_{SS}1$ = 0V

Parameter	Symbol	Pin/ Remarks	Conditions		Specification				
					V_{DD}[V]	min	typ	max	unit
Consumption current during normal operation (Note 8-1)	IDDOP(1)	V_{DD}	Crystal oscillation mode • FOSC0=32.768kHz • System clock: FOSC0 • Internal RC oscillation stopped • FOSC1=0Hz (Oscillation stop) • 1/1frequency division ratio. [No panel load]	LCD Display ON	2.4 to 5.5		70	150	µA
	IDDOP(2)				2.4 to 3.6		50	80	
	IDDOP(3)			LCD Display OFF	2.3 to 5.5		70	120	
	IDDOP(4)				2.3 to 3.6		40	70	
	IDDOP(5)		Ceramic oscillation mode • FOSC1=4MHz • System clock: FOSC1 • Internal RC oscillation stopped • FOSC0=0Hz (Oscillation stop) • 1/2 frequency division ratio.		2.4 to5.5		3000	4100	
	IDDOP(6)				2.4 to 3.6		2200	2900	
	IDDOP(7)		Internal RC oscillation mode • System clock: Internal RC • Internal RC oscillates • FOSC0=0Hz (Oscillation stop) • FOSC1=0Hz (Oscillation stop) • 1/1 frequency division ratio		2.3 to 5.5		1900	3000	
	IDDOP(8)				2.3 to3.6		1200	2000	
	IDDOP(9)		High-speed RC oscillation mode *Ta=0 to 60°C • FOSC1=1MHz RCR1=470kΩ • System clock: FOSC1 • Internal RC oscillation stopped • FOSC0=0Hz (Oscillation stop) • 1/1 frequency division ratio.		2.3 to 5.5		1700	2300	
	IDDOP(10)				2.3 to 3.6		1200	1700	
	IDDOP(11)		Low-speed RC oscillation mode *Ta=0 to 60°C • FOSC0=64kHz RCR0=910kΩ • System clock: FOSC0 • Internal RC oscillation stopped • FOSC1=0Hz (Oscillation stop) • 1/1 frequency division ratio.		2.3 to 5.5		110	170	
	IDDOP(12)				2.3 to 3.6		70	110	

Note 8-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Pin/ Remarks	Condition		Specification				
					V_{DD}[V]	min	typ	max	unit
Consumption current during HALT mode (Note 8-1)	IDDHALT(1)	V_{DD}	HALT mode Crystal oscillation mode • FOSC0=32.768kHz • System clock: FOSC0 • Internal RC oscillation stopped • FOSC1=0Hz (Oscillation stop) • 1/1frequency division ratio. [No panel load]	LCD Display ON	2.4 to 5.5		32	93	µA
	IDDHALT(2)				2.4 to 3.6		15	35	
	IDDHALT(3)			LCD Display OFF	2.3 to 5.5		22	59	
	IDDHALT(4)				2.3 to 3.6		6	21	
	IDDHALT(5)		HALT mode Ceramic oscillation mode • FOSC1=4MHz • System clock: FOSC1 • Internal RC oscillation stopped • FOSC0=0Hz (Oscillation stop) • 1/2 frequency division ratio.		2.4 to 5.5		700	1100	
	IDDHALT(6)				2.4 to 3.6		300	500	
	IDDHALT(7)		HALT mode Internal RC oscillation mode • System clock: Internal RC • Internal RC oscillates • FOSC0=0Hz (Oscillation stop) • FOSC1=0Hz (Oscillation stop) • 1/1 frequency division ratio.		2.3 to 5.5		400	700	
	IDDHALT(8)				2.3 to 3.6		200	300	
	IDDHALT(9)		HALT mode High-speed RC oscillation mode *Ta=0 to 60°C • FOSC1=1MHz RCR1=470kΩ • System clock: FOSC1 • Internal RC oscillation stopped • FOSC0=0Hz (Oscillation stop) • 1/1 frequency division ratio.		2.3 to 5.5		200	400	
	IDDHALT(10)				2.3 to 3.6		100	200	
	IDDHALT(11)		HALT mode Low-speed RC oscillation mode *Ta=0 to 60°C • FOSC0=64kHz RCR0=910kΩ • System clock: FOSC0 • Internal RC oscillation stopped • FOSC1=0Hz (Oscillation stop) • 1/1 frequency division ratio.		2.3 to 5.5		20	50	
	IDDHALT(12)				2.3 to 3.6		10	30	
Consumption current during HOLD mode	IDDHOLD(1)	V_{DD}	HOLD mode • CF1=V_{DD} or OPEN (External clock mode)		2.3 to 5.5			12	
	IDDHOLD(2)				2.3 to 3.6			5	
Consumption current during clock HOLD mode	IDDHOLD(3)	V_{DD}	Clock HOLD mode • CF1=V_{DD} or OPEN (External clock mode) • FmX'tal=32.768kHz crystal oscillation mode		2.3 to 5.5		16	55	
	IDDHOLD(4)				2.3 to 3.6		3	16	

Note 8-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

F-ROM Programming Characteristics at Ta = +10°C to +55°C, V_{SS} = LCDV_{SS}0 = LCDV_{SS}1 = 0V

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	V_{DD}	The consumption current of the microcomputer is excluded.	2.7 to 5.5		5	10	mA
Programming time	tFW(1)		Erasing time: 128 bytes	2.7 to 5.5		20	30	ms
	tFW(2)		Programming time: 2 bytes	2.7 to 5.5		40	60	µs

Characteristics of a Sample OSC1 System Clock Oscillation Circuit

Given below are the characteristics of a sample OSC1 system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample OSC1 System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf1 [Ω]	Rd1 [Ω]		typ [ms]	max [ms]	
4.194MHz	MURATA	CSTCR4M00G53-R0	(15)	(15)	OPEN	0	2.4 to 5.5	0.1	0.5	Internal C1,C2
		CSTLS4M00G53-B0	(15)	(15)	OPEN	0	2.4 to 5.5	0.1	0.5	
4.000MHz	MURATA	CSTCR4M00G53-R0	(15)	(15)	OPEN	0	2.4 to 5.5	0.1	0.5	Internal C1,C2
		CSTLS4M00G53-B0	(15)	(15)	OPEN	0	2.4 to 5.5	0.1	0.5	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the following reference timing points: (See Figure 4)

- V_{DD} goes above the operating voltage lower limit.
- An instruction for starting the OSC1 clock oscillator circuit is executed.
- Oscillation starts after the microcontroller exits the X'tal HOLD mode with the ENOSC1 bit (OCR0 register, bit 1) set to 1.

Characteristics of a Sample OSC0 System Clock Oscillator Circuit

Given below are the characteristics of a sample OSC0 system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample OSC0 System Clock Oscillator Circuit with a CF Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	18	18	OPEN	390k	2.3 to 5.5	1.3	3.0	Applicable CL value=12.5pF SMD-type

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the OSC0 clock oscillation circuit is executed. (See Figure 4)

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

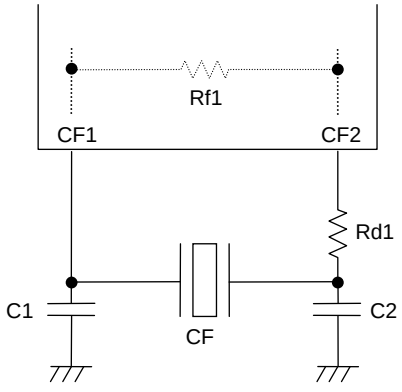


Figure 1 CF Oscillator Circuit

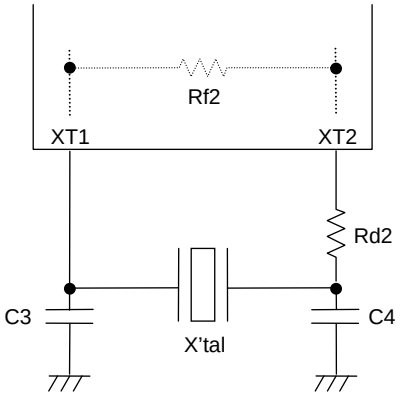


Figure 2 XT Oscillator Circuit

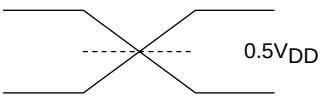
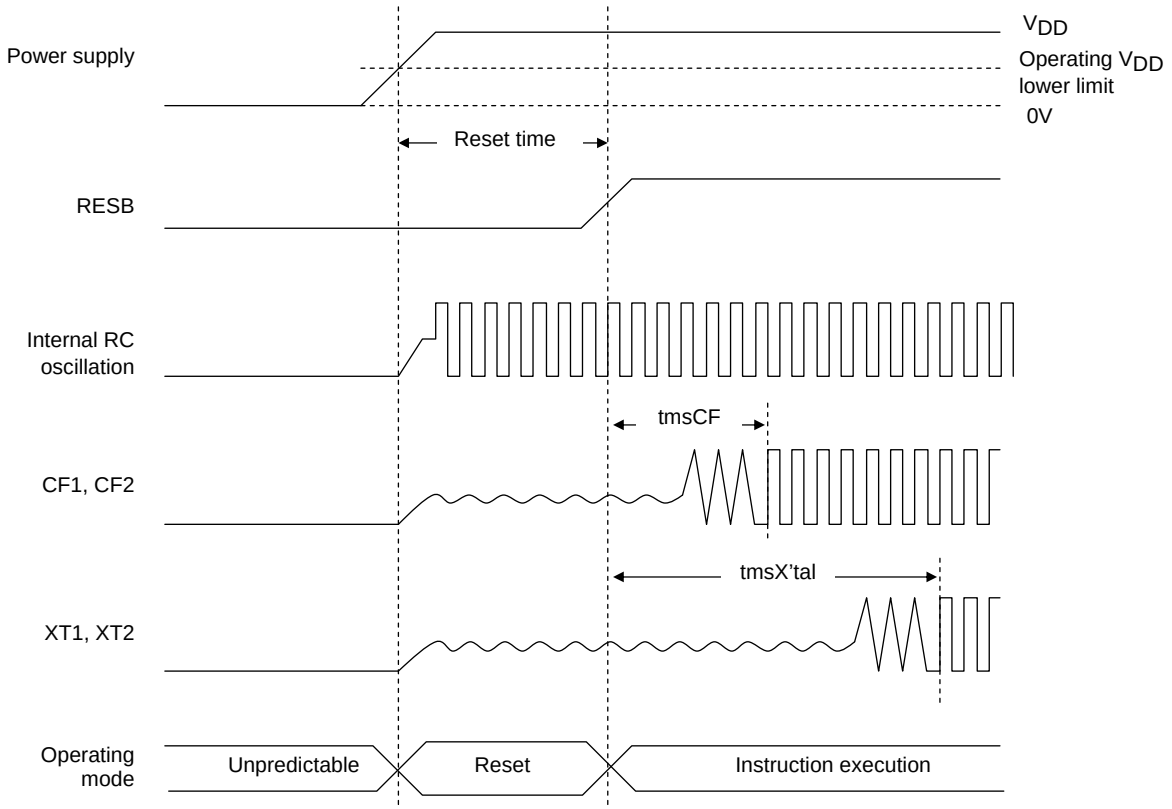
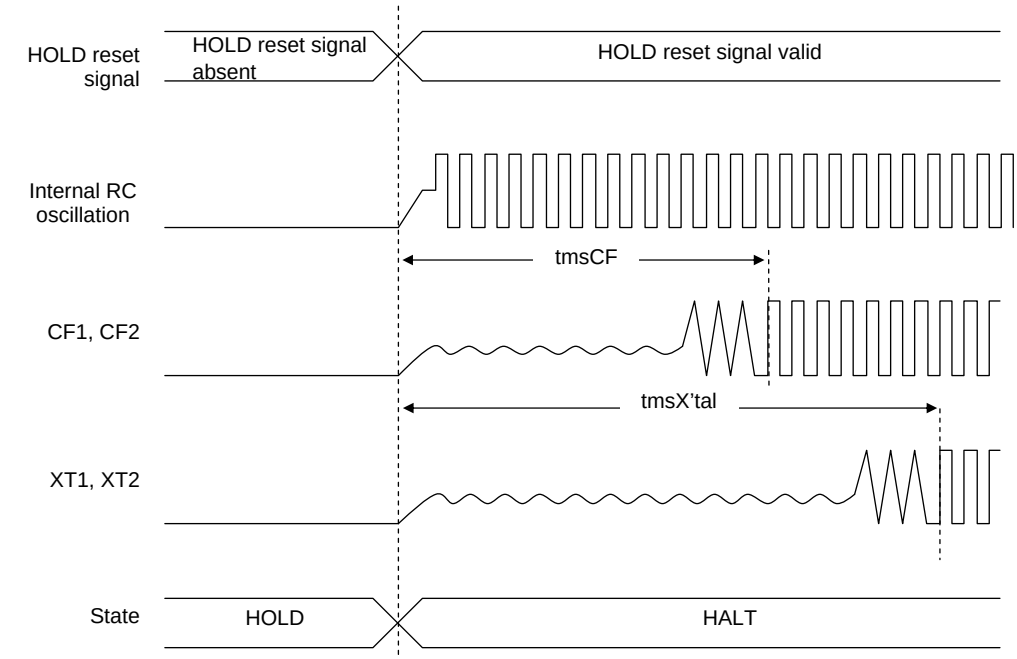


Figure 3 AC Timing Measurement Point

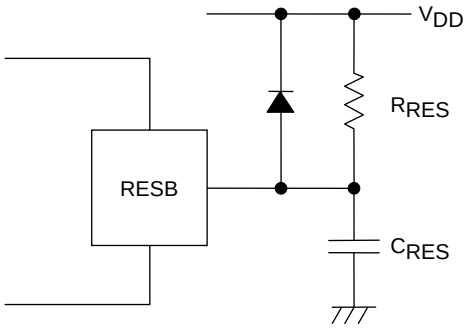


Reset Time and Oscillation Stabilization Time



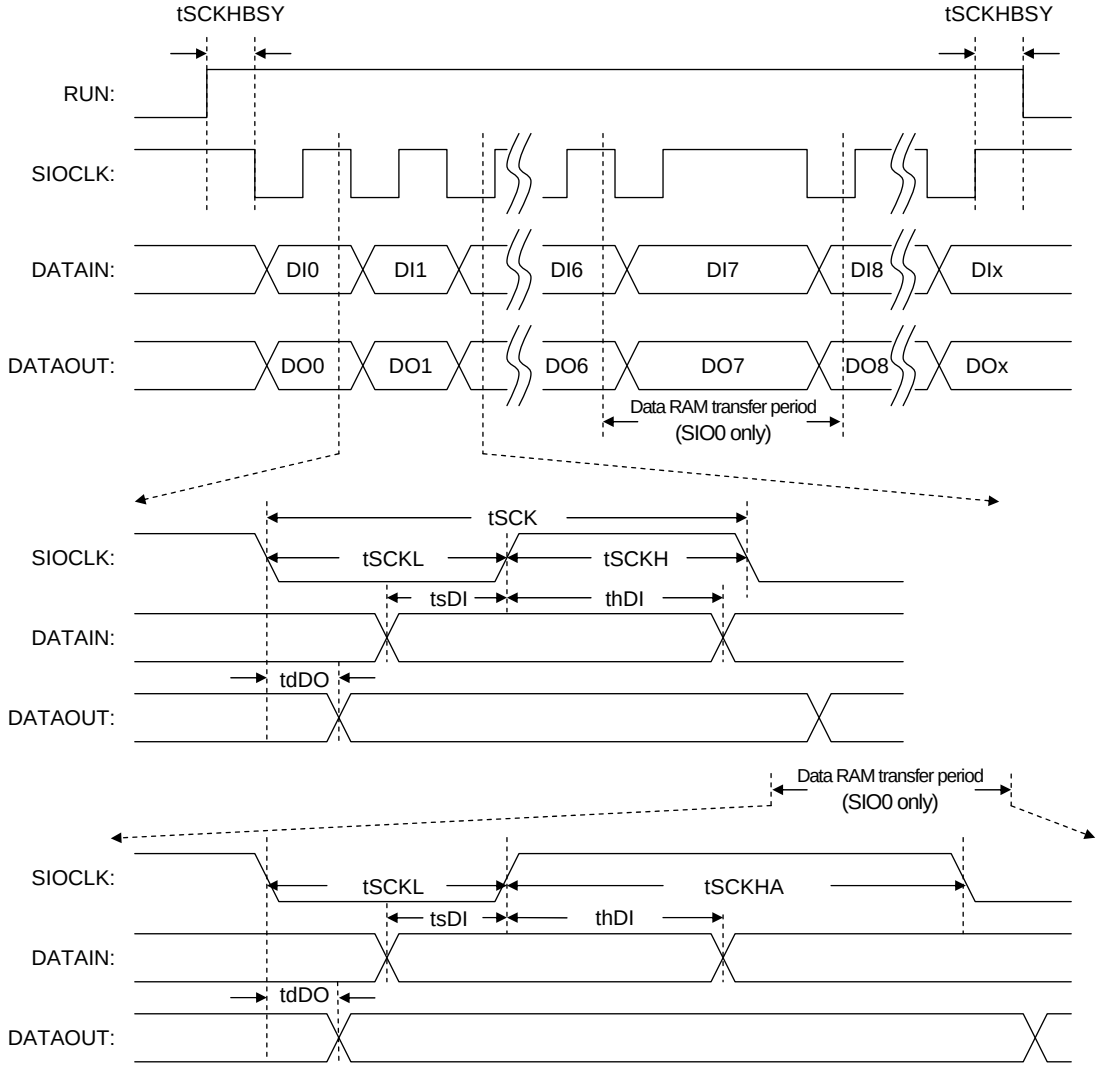
HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Time



Note:
Select C_{RES} and R_{RES} values to assure that at least 50µs reset time is provided after the V_{DD} becomes higher than the minimum operating voltage.

Figure 5 Reset Circuit



*: Remarks: DIx and DOx are the final communication bits. X = 0 to 32768

Figure 6 Serial I/O Waveforms

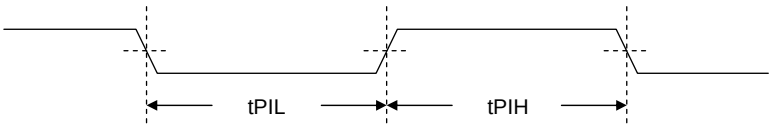


Figure 7 Pulse Input Timing Signal Waveform

Note: The oscillation frequency changes with the board pattern and used parts when OSC1 and OSC0 are used as the RC oscillation. It also greatly depends on the product shape (chip and plastic package) and the board capacitance, and it is recommended to evaluate the resistor value with an actual product. Use the following characteristics as only for a reference.

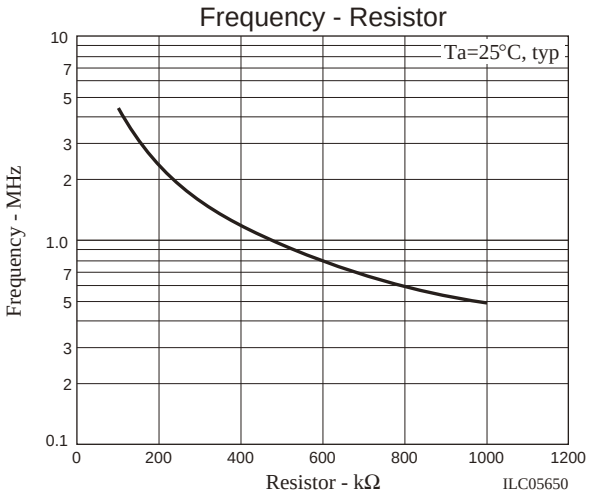


Figure 8 Characteristics of Resistor v.s. Frequency of OSC1

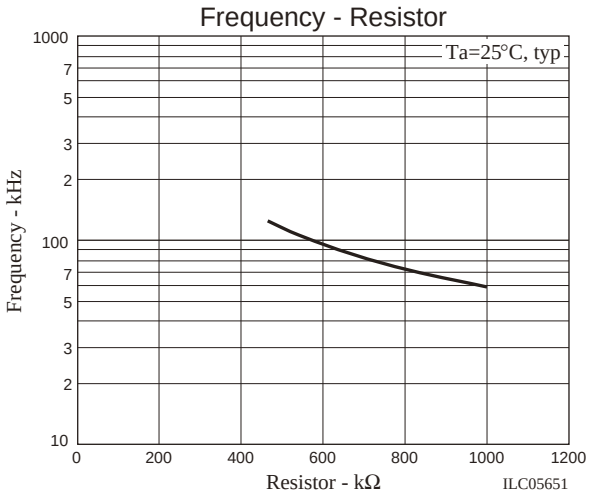


Figure 9 Characteristics of Resistor v.s. Frequency of OSC0

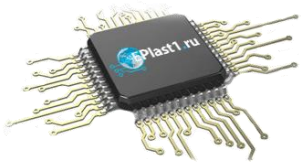
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.