

## LED Display Modules

128 x 32 Graphics Display with Drive Electronics and + 5 V HC CMOS Level Video Interface  
Orange 0603 Chip LEDs, High Brightness



The LED-128G032 is an LED replacement for the popular APD-128G032 plasma display module. It is designed to offer high brightness and superior viewing characteristics in a slim package. This display is ideal for low to medium level information content and is ideal for applications such as arcade games, process control, POS terminals, medical equipment, message centers and ATM machines.

The LED-128G032 LED display offers high contrast, wide viewing angle, and long distance readability. It emits a brilliant orange color which catches the attention of the viewer, but is yet comfortable to the eye.

The LED-128G032 LED display has a video type interface and is driven in a standard row/column refresh method. Pixel data is clocked for a row, and rows are scanned sequentially. Signals are presented for *serial data*, *dot clock*, *column latch*, *row data*, *row clock* and *display enable*. The *serial data* is entered with the *dot clock* up to frequencies as high as 8 MHz. After a row of 128 pixels is clocked in, the *column latch* signal is toggled and the data is latched. At the time the data is latched, the display is briefly disabled using the *display enable* signal, then the row pointer is advanced with the *row clock* signal. Once each frame the *row data* must be asserted to synchronize the column serial data with the beginning row. The recommended scanning frequency is approximately 70 Hz, but may be as high as 200 Hz.

### STANDARD ELECTRICAL SPECIFICATIONS <sup>(1)</sup>

| DESCRIPTION                             | SYMBOL   | MIN.         | TYP.  | MAX.         | UNITS    |
|-----------------------------------------|----------|--------------|-------|--------------|----------|
| Logic and LED Drive Voltage             | $V_{CC}$ | + 4.5        | + 5.0 | + 5.5        | $V_{DC}$ |
| Logic and LED Drive Current (Fully Lit) | $I_{CC}$ | -            | 2.5   | 3.0          | $A_{DC}$ |
| Logic 1 Input                           | $V_{ih}$ | 0.7 $V_{CC}$ | -     | -            | $V_{DC}$ |
| Logic 0 Input                           | $V_{il}$ | -            | -     | 0.2 $V_{CC}$ | $V_{DC}$ |

#### Note

<sup>(1)</sup> Recommended operating voltages, all maximums are absolute maximum

### FEATURES

- LED replacement for the popular APD-128G032 plasma display module
- + 5 V HC CMOS level video interface
- Large characters
- Highly visible for long distance viewing
- > 30:1 contrast ratio
- Brilliant neon orange color
- Slim profile

### ELECTRICAL SPECIFICATIONS

**Voltage(s) Required:** + 5  $V_{DC}$  ( $V_{CC}$ )

**Power Required (Fully Lit):** Typical = 12.5 W  
Maximum = 15 W

### OPTICAL SPECIFICATIONS

**Viewing Area:** 12.75" [323.8 mm] W x 3.15" [80.01 mm] L

**Character Size (5 x 7):** 0.65" [16.51 mm] H x 0.45" [11.43 mm] W

**Pixel Size:** 0.063" [1.6 mm] H x 0.031" [0.8 mm] W

**Pixel Pitch:** 0.100" [2.54 mm]

**Luminance:** 100 ft-L minimum

**Color:** Neon orange

**Viewing Angle:** > 150°

### ENVIRONMENTAL SPECIFICATIONS

**Operating Temperature:** - 40 °C to + 85 °C

**Storage Temperature:** - 40 °C to + 85 °C

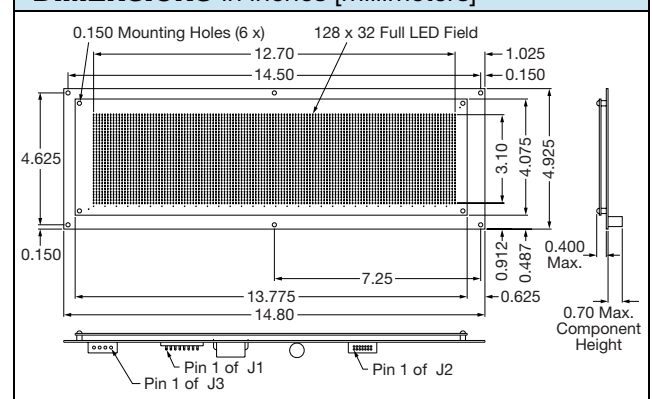
**Relative Operating Humidity:** To 95 % non-condensing

**Mechanical Shock:** 30 G

**Vibration:** 3 G

**Operating Altitude:** 10 000 ft

### DIMENSIONS in inches [millimeters]



**PIN DESCRIPTION****J1 - POWER CONNECTOR**

Tyco AMP #640445-8 or equivalent.  
Mates with Tyco AMP 640428-8, Molex 09-50-3081 or equivalent

| PIN | SIGNAL          | DESCRIPTION                |
|-----|-----------------|----------------------------|
| 1   | N/C             | No connection              |
| 2   | N/C             | No connection              |
| 3   | KEY             | Used to key connector      |
| 4   | GND             | Ground                     |
| 5   | GND             | Ground                     |
| 6   | V <sub>CC</sub> | Logic and LED drive supply |
| 7   | RESERVED        | No connection              |
| 8   | N/C             | No connection              |

**J2 - DATA CONNECTOR**

Tyco AMP#103309-2 or equivalent.  
Mates with Tyco AMP 746195-2, Molex 39-27-1146 or equivalent

| PIN | DESCRIPTION    | PIN | DESCRIPTION |
|-----|----------------|-----|-------------|
| 1   | Display enable | 2   | Ground      |
| 3   | Row data       | 4   | Ground      |
| 5   | Row clock      | 6   | Ground      |
| 7   | Column latch   | 8   | Ground      |
| 9   | Dot clock      | 10  | Ground      |
| 11  | Serial data    | 12  | Ground      |
| 13  | No connection  | 14  | Ground      |

**J3 - POWER CONNECTOR**

Tyco AMP #641737-1 or equivalent.  
Mates with Tyco AMP 1-480424-0 housing, 60617-4 socket terminals

| PIN | SIGNAL          | DESCRIPTION                |
|-----|-----------------|----------------------------|
| 1   | RESERVED        | No connection              |
| 2   | GND             | Ground                     |
| 3   | GND             | Ground                     |
| 4   | V <sub>CC</sub> | Logic and LED drive supply |

**INTERFACE SIGNAL DESCRIPTION**

**Dot clock** - This signal enters the *serial data* on each low to high transition. A total of 128 *dot clock* transitions must be present for each line of column/anode data.

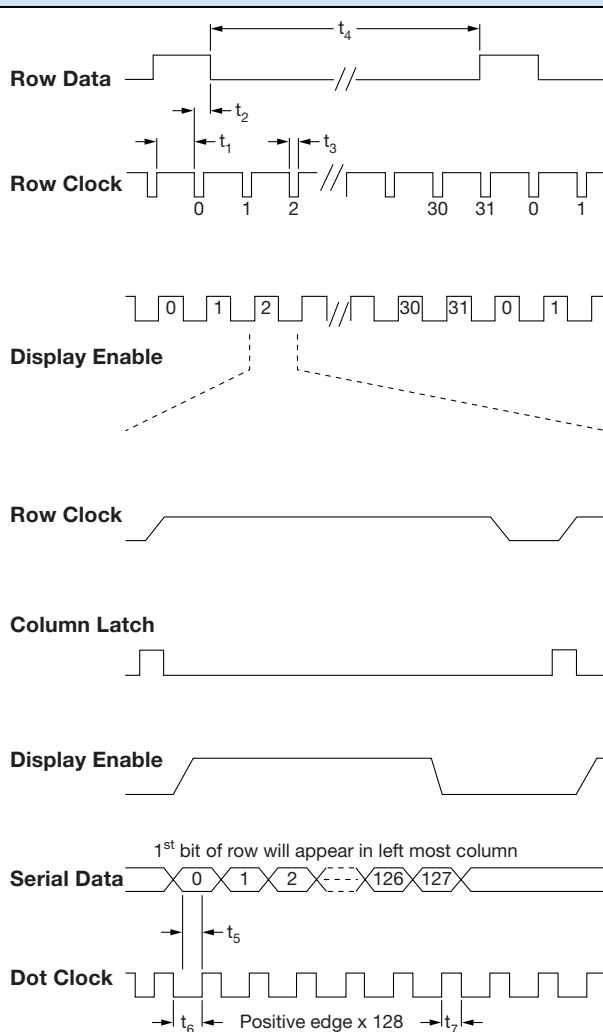
**Serial data** - This signal presents the pixel data in positive logic format. A logic one represents a lit pixel and a logic zero represents an extinguished pixel. Data is entered from right to left. The first pixel data entered will represent the left most pixel in the row.

**Column latch** - This signal latches the pixel data into the driver outputs. When the *column latch* signal goes to logic one the data entered previously will fall through to the driver outputs. When the signal returns to a logic zero the data is latched and the shift register is now ready to accept the next row of data. Must be held low while entering new *serial data*.

**Display enable** - This signal enables the output drivers. Using a duty cycle control, this signal may also be used for intensity control. The *display enable* must be at logic zero before the *column latch* signal transitions. To avoid display blurring, the *row clock* signal should also transition while *display enable* is a logic zero.

**Row data** - This signal is the first line marker for the scan. This input should be held high to correspond to the first row of pixel data.

**Row clock** - This signal clocks *row data* on the falling edge. The *row clock* signal is repetitive and must be present for proper scanning of the display module. The LED-128G032 has an unique input protection circuit that assures the column drivers stay blanked on power up. The protection circuit unblanks the column drivers when the *row clock* signal begins (i.e the display begins scanning).

**LOGIC AND DATA TIMING**

| PARAMETER | MIN. | TYP. | MAX. | UNITS   |
|-----------|------|------|------|---------|
| $t_1$     | 100  | -    | -    | ns      |
| $t_2$     | 5    | -    | -    | $\mu$ s |
| $t_3$     | 1    | -    | -    | $\mu$ s |
| $t_4$     | -    | 70   | 200  | Hz      |
| $t_5$     | 25   | -    | -    | ns      |
| $t_6$     | 75   | -    | -    | ns      |
| $t_7$     | 75   | -    | -    | ns      |

**ORDERING INFORMATION**

| DESCRIPTION                                             | PART NUMBER |
|---------------------------------------------------------|-------------|
| Display, Driver Electronics and + 5 V HC CMOS Interface | LED-128G032 |
| J2 Data Connector Kit (2 pcs. recommended)              | 280105-05   |
| J1 Power Connector Kit                                  | 280108-12   |
| J3 Power Connector Kit                                  | 280108-05   |



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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
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