

NVBLS0D5N04M8

Product Preview

Power MOSFET

40 V, 300 A, 0.57 mΩ, Single N-Channel

Features

- Typical $R_{DS(on)}$ = 0.46 mΩ at V_{GS} = 10 V, I_D = 80 A
- Typical $Q_{g(tot)}$ = 220 nC at V_{GS} = 10 V, I_D = 80 A
- UIS Capability
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS T_J = 25°C unless otherwise noted

Parameter	Symbol	Ratings	Units
Drain-to-Source Voltage	V_{DSS}	40	V
Gate-to-Source Voltage	V_{GS}	±20	V
Drain Current – Continuous (V_{GS} = 10) (Note 1)	I_D	300	A
Pulsed Drain Current T_C = 25°C		See Figure 4	
Single Pulse Avalanche Energy (Note 2)	E_{AS}	1064	mJ
Power Dissipation	P_D	429	W
Derate Above 25°C		2.86	W/°C
Operating and Storage Temperature	T_J, T_{STG}	–55 to +175	°C
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.35	°C/W
Maximum Thermal Resistance, Junction-to-Ambient (Note 3)	$R_{\theta JA}$	43	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.
2. Starting T_J = 25°C, L = 0.3 mH, I_{AS} = 84 A, V_{DD} = 40 V during inductor charging and V_{DD} = 0 V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2 oz copper.

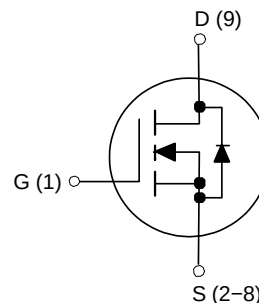


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MO-299A
CASE 100CU



ORDERING INFORMATION

Device	Package	Marking
NVBLS0D5N04M8TXG	MO-299A (Pb-Free)	0D5N04M8

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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Table 1. ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
B _{VDSS}	Drain-to-Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V		40	–	–	V
I _{DSS}	Drain-to-Source Leakage Current	V _{DS} = 40 V, V _{GS} = 0 V	T _J = 25°C	–	–	1	μA
			T _J = 175°C (Note 4)	–	–	1	mA
I _{GSS}	Gate-to-Source Leakage Current	V _{GS} = ±20 V		–	–	±100	nA
ON CHARACTERISTICS							
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA		2.0	3.0	4.0	V
R _{DS(on)}	Drain-to-Source On Resistance	I _D = 80 A, V _{GS} = 10 V	T _J = 25°C	–	0.46	0.57	mΩ
DYNAMIC CHARACTERISTICS							
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz		–	15900	–	pF
C _{oss}	Output Capacitance			–	4000	–	pF
C _{rss}	Reverse Transfer Capacitance			–	600	–	pF
R _g	Gate Resistance	f = 1 MHz		–	2.6	–	Ω
Q _{g(ToT)}	Total Gate Charge at 10 V	V _{GS} = 0 to 10 V	V _{DD} = 20 V I _D = 80 A	–	220	296	nC
Q _{g(th)}	Threshold Gate Charge	V _{GS} = 0 to 2 V		–	29	39	nC
Q _{gs}	Gate-to-Source Gate Charge			–	73	–	nC
Q _{gd}	Gate-to-Drain “Miller” Charge			–	41	–	nC
SWITCHING CHARACTERISTICS							
t _{on}	Turn-On Time	V _{DD} = 20 V, I _D = 80 A, V _{GS} = 10 V, R _{GEN} = 6 Ω		–	–	221	ns
t _{d(on)}	Turn-On Delay			–	54	–	ns
t _r	Rise Time			–	82	–	ns
t _{d(off)}	Turn-Off Delay			–	106	–	ns
t _f	Fall Time			–	52	–	ns
t _{off}	Turn-Off Time			–	–	215	ns
DRAIN-SOURCE DIODE CHARACTERISTICS							
V _{SD}	Source-to-Drain Diode Voltage	I _{SD} = 80 A, V _{GS} = 0 V		–	–	1.25	V
		I _{SD} = 40 A, V _{GS} = 0 V		–	–	1.2	V
t _{rr}	Reverse-Recovery Time	I _F = 80 A, dI _{SD} /dt = 100 A/μs, V _{DD} = 32 V		–	119	133	ns
Q _{rr}	Reverse-Recovery Charge			–	228	274	nC

4. The maximum value is specified by design at $T_J = 175^\circ\text{C}$. Product is not tested to this condition in production. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Typical Characteristics

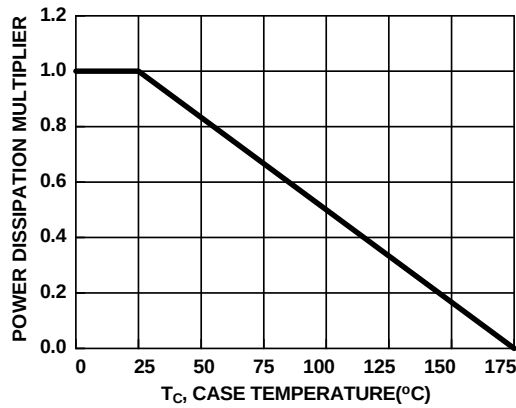


Figure 1. Normalized Power Dissipation vs. Case Temperature

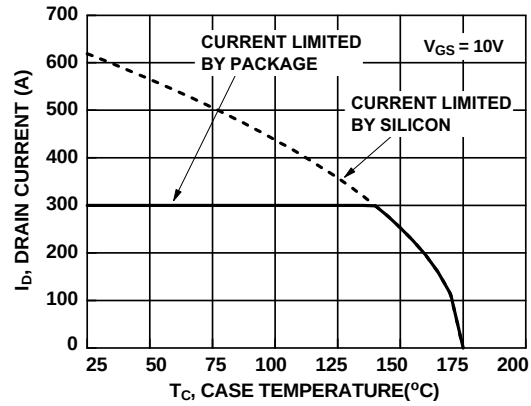


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

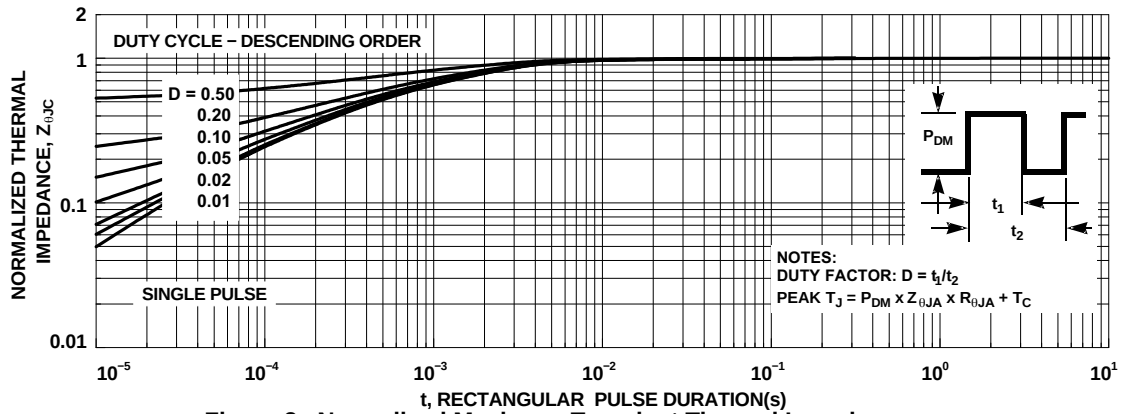


Figure 3. Normalized Maximum Transient Thermal Impedance

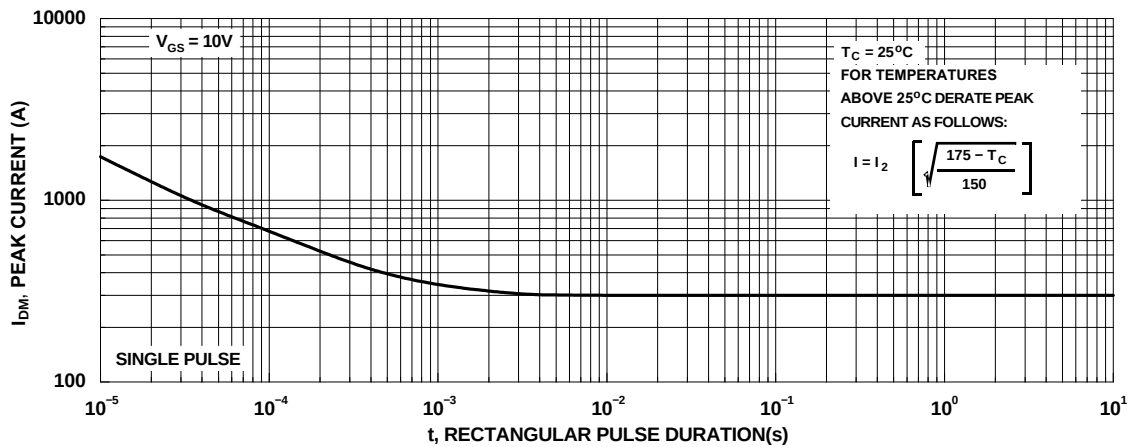


Figure 4. Peak Current Capability

Typical Characteristics

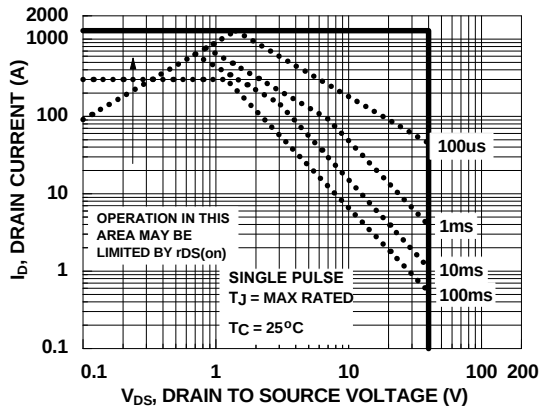
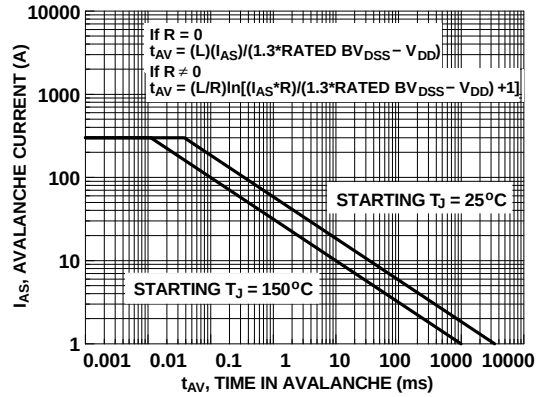


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

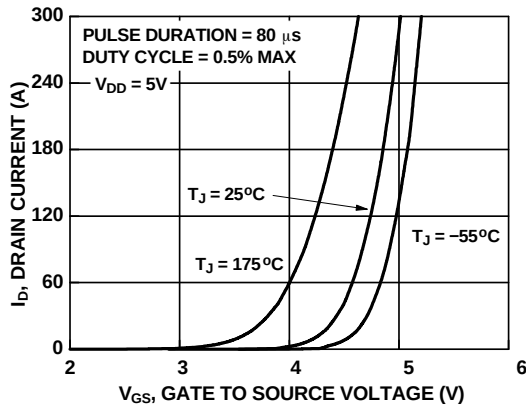


Figure 7. Transfer Characteristics

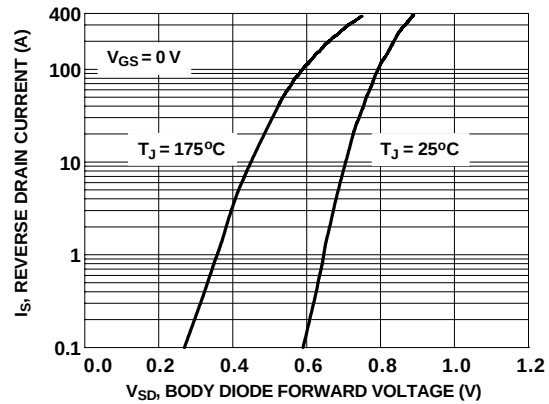


Figure 8. Forward Diode Characteristics

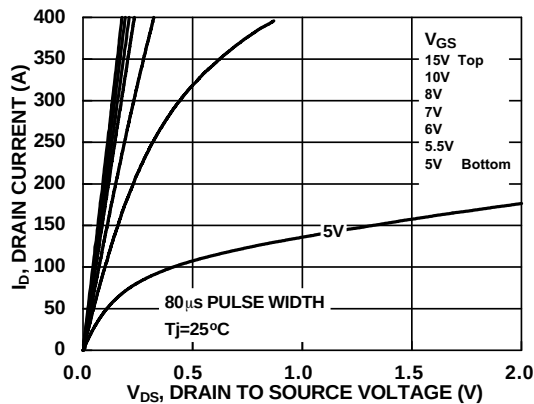


Figure 9. Saturation Characteristics

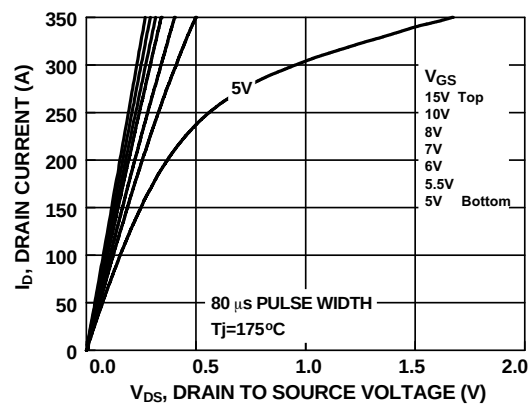


Figure 10. Saturation Characteristics

Typical Characteristics

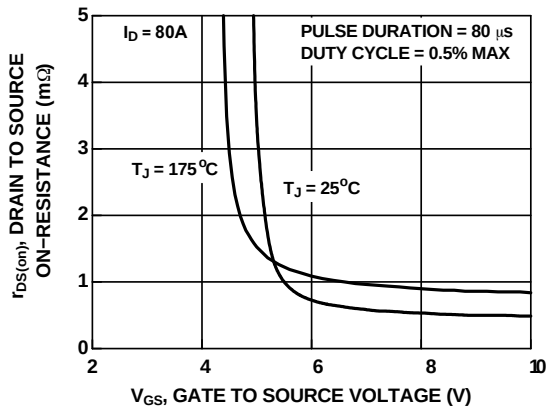


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

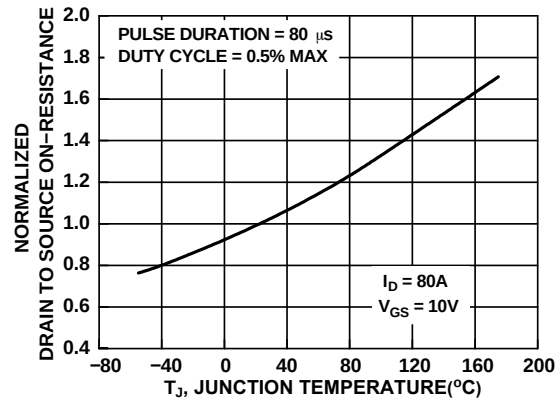


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

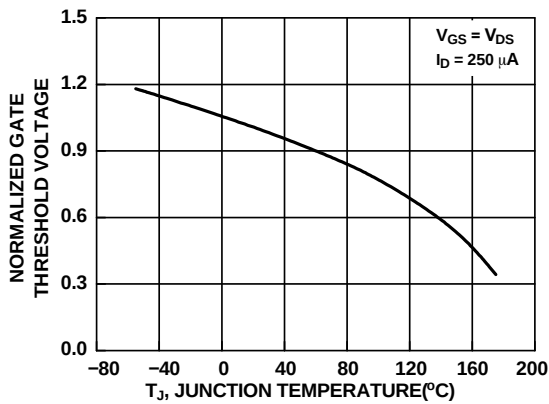


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

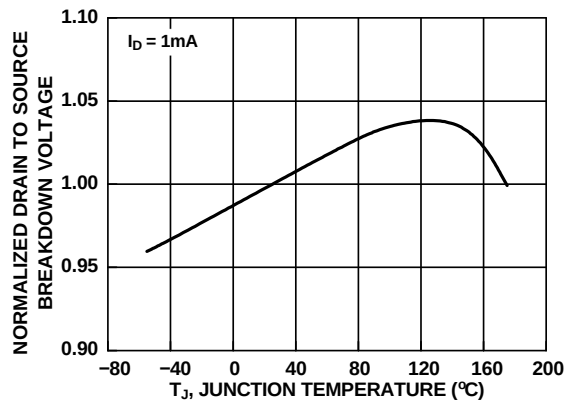


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

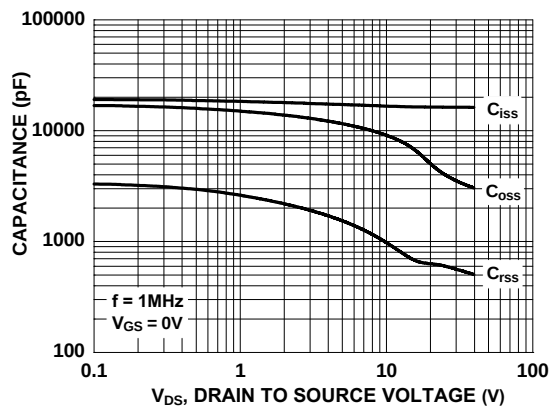


Figure 15. Capacitance vs. Drain to Source Voltage

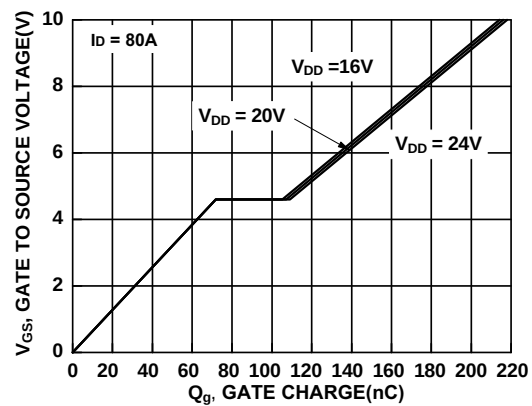
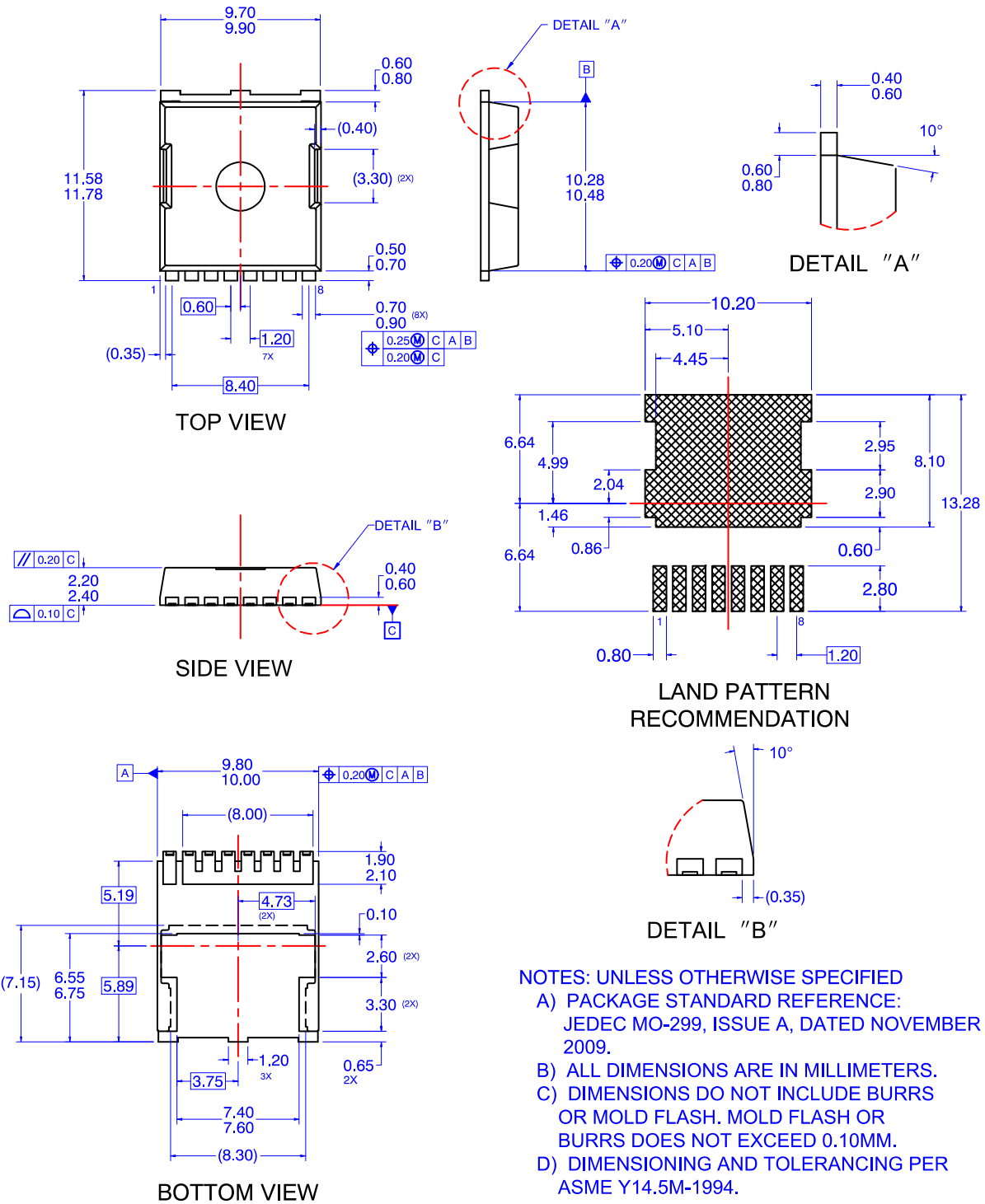


Figure 16. Gate Charge vs. Gate to Source Voltage

NVBLS0D5N04M8

PACKAGE DIMENSIONS

H-PSOF8L 11.68x9.80
CASE 100CU
ISSUE O



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) PACKAGE STANDARD REFERENCE:
JEDEC MO-299, ISSUE A, DATED NOVEMBER 2009.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
 - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

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