Datasheet

DS000522

CMV50000

47.5MP CMOS Machine Vision Image Sensor

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Content Guide

1 General Description

The CMV50000 is a high speed CMOS image sensor with 7920 × 6004 effective pixels (47.5Mp) developed for machine vision and video applications. The image array consists of 4.6µm pipelined 8T global shutter pixels which allow exposure during read out, while performing true CDS (Correlated Double Sampling) operation. The image sensor also integrates a programmable analog gain amplifier and offset regulation. The image sensor has 22 digital sub-LVDS data output channels. Each output channel runs up to 830 Mbit/s, which results in a frame rate of 30 fps at full resolution. Higher frame rates can be achieved in row-windowing mode or row-subsampling mode. These modes are all programmable using the SPI interface. All internal exposure and read out timings are generated by a programmable on-chip sequencer. External triggering and exposure programming is also possible. Extended optical dynamic range can be achieved by a dual exposure HDR mode.

1.1 Key Benefits & Features

The benefits and features of CMV50000, 47.5MP CMOS Machine Vision Image Sensor, are listed below:

Figure 1:
Added Value of Using CMV50000

Benefits	Features
Designed for high performance applications	Resolution of 7920x6004 at 30 frames per second
Capture fast moving objects	8T global shutter pixel with true Correlated Double Sampling (true-CDS)
Use in low light conditions	Low noise (8.8e) and high sensitivity (QE=60%), with on-chip noise reduction.
Use in bright light conditions	In binning mode the full well capacity reaches 58000e^- with an SNR of 47.6dB and DR=68dB
Standard optics can be used	35mm Full Frame optical format
Easy to operate	On-chip digital sequencer which handles all the sensor controls, over SPI

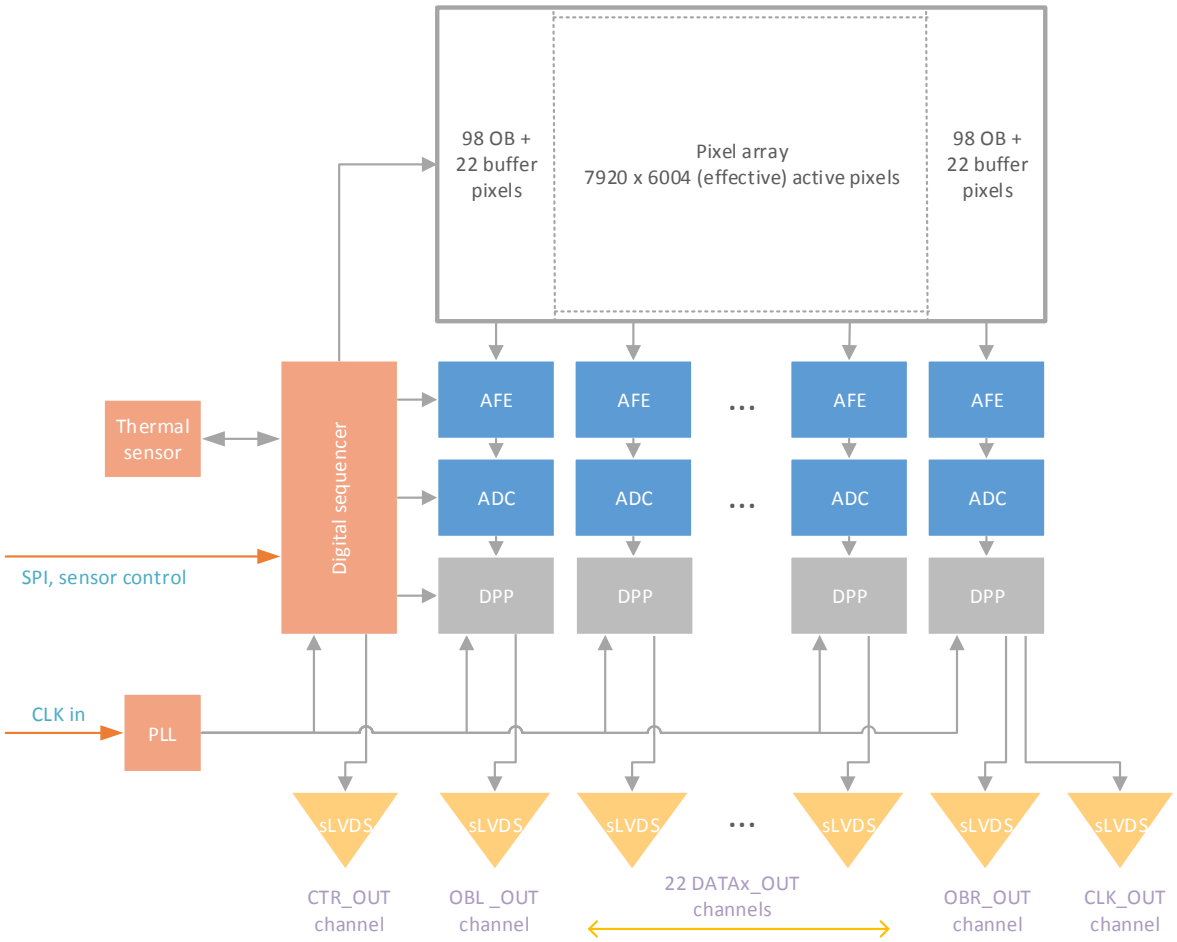
1.2 Applications

- Machine vision
- Video/Broadcast
- Security
- High-end inspection
- Aerial mapping
- Document scanning
- ITS
- Scientific
- 3D imaging

1.3 Block Diagram

The functional blocks of this device are shown below:

Figure 2 :
Functional Blocks of CMV50000



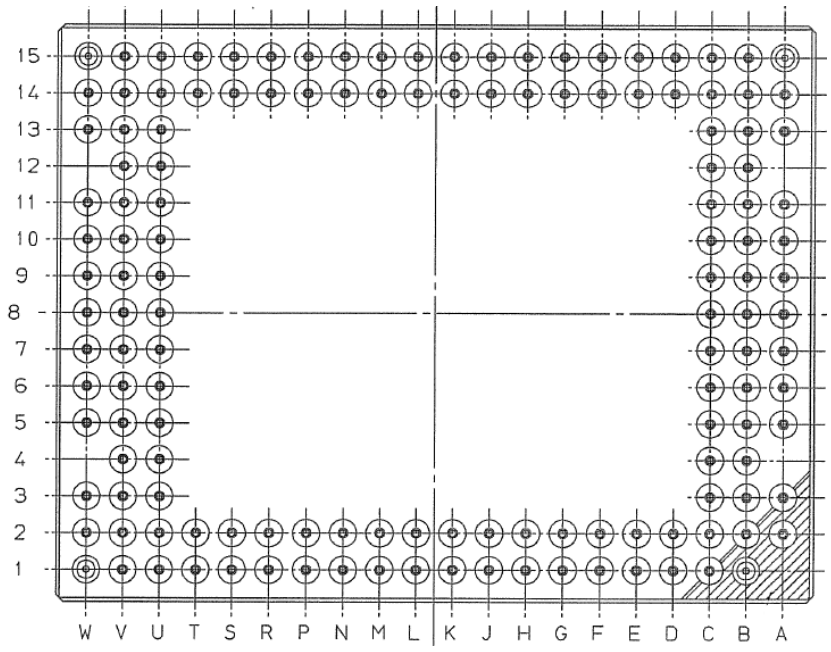
2 Ordering Information

Ordering Code	Package	Chroma	Options	Delivery Quantity
CMV50000ES-1E3M1PA	PGA	Mono		10 Pcs / Tray
CMV50000ES-1E3C1PA	PGA	Color		10 Pcs / Tray

3 Pin Assignment

3.1 Pin Diagram

Figure 3 :
Pin Numbering (bottom view)



3.2 Pin Description

Figure 4:
Pin Description of CMV50000

Pin Number	Pin Name	Pin Type	Description
A2	SPI_CSN	Digital input	SPI Chip Select
A3	VSSA	Analog ground	Analog ground
A5	REQ_FRAME	Digital input	Request frame (stop exposure)
A6	VDDARRAY	Analog supply	Pixel array supply
A7	VDDARRAY	Analog supply	Pixel array supply
A8	NC1	Analog	Do Not Connect
A9	NC2	Analog	Do Not Connect

Pin Number	Pin Name	Pin Type	Description
A10	CTRL_P	sub-LVDS	Control channel output
A11	CTRL_N	sub-LVDS	Control channel output
A13	VSSA	Analog ground	Main analog ground
A14	DOBL_P	sub-LVDS	Left Optical Black output
A15	DOBL_N	sub-LVDS	Left Optical Black output
B1	SPI_MISO	Digital output	SPI Master In/Slave Out data
B2	SPI_MOSI	Digital input	SPI Master Out/Slave In data
B3	SPI_CLK	Digital input	SPI clock
B4	CLK_IN	Digital input	Sensor input clock
B5	RST_N	Digital input	Asynchronous hard reset input pin
B6	VDD33	Analog supply	On-chip regulators supply
B7	VSELHREG	Analog	On-chip regulator output
B8	VS2HREG	Analog	On-chip regulator output
B9	VS1HREG	Analog	On-chip regulator output
B10	VTXHREG	Analog	On-chip regulator output
B11	VRESHREG	Analog	On-chip regulator output
B12	VDD27	Analog supply	Main analog supply
B13	D00_P	sub-LVDS	Channel 0 output
B14	D00_N	sub-LVDS	Channel 0 output
B15	D02_P	sub-LVDS	Channel 2 output
C1	VDDD12PLL1	Digital supply	Digital supply for PLL1
C2	VDDD12PLL2	Digital supply	Digital supply for PLL2
C3	REQ_EXP	Digital input	Request exposure (start exposure)
C4	VDD27	Analog supply	Main analog supply
C5	VSSD	Digital ground	Digital ground
C6	VSSD	Digital ground	Digital ground
C7	VSELH	Analog	Bias
C8	VS2H	Analog	Bias
C9	VS1H	Analog	Bias
C10	VTXH	Analog	Bias
C11	VRESH	Analog	Bias
C12	D01_P	sub-LVDS	Channel 1 output
C13	D01_N	sub-LVDS	Channel 1 output
C14	D03_P	sub-LVDS	Channel 3 output
C15	D02_N	sub-LVDS	Channel 2 output

Pin Number	Pin Name	Pin Type	Description
D1	VDD12C	Digital supply	Logic supply for ADC
D2	VSSD	Digital ground	Main digital ground
D14	D03_N	sub-LVDS	Channel 3 output
D15	D04_P	sub-LVDS	Channel 4 output
E1	VSSDPLL1	Digital ground	Digital ground for PLL1
E2	VSSDPLL2	Digital ground	Digital ground for PLL2
E14	D05_P	sub-LVDS	Channel 0 output
E15	D04_N	sub-LVDS	Channel 0 output
F1	VSSAPLL1	Analog ground	Analog ground for PLL1
F2	VSSAPLL2	Analog ground	Analog ground for PLL2
F14	D05_N	sub-LVDS	Channel 5 output
F15	D06_P	sub-LVDS	Channel 6 output
G1	VDDA12PLL1	Analog supply	Analog supply for PLL1
G2	VDDA12PLL2	Analog supply	Analog supply for PLL2
G14	D07_P	sub-LVDS	Channel 7 output
G15	D06_N	sub-LVDS	Channel 6 output
H1	VDD12	Digital supply	Logic supply for core logic
H2	VSSD	Digital ground	Main digital ground
H14	D07_N	sub-LVDS	Channel 7 output
H15	D08_P	sub-LVDS	Channel 8 output
J1	VDD12	Digital supply	Logic supply for core logic
J2	VSSA	Analog ground	Main analog ground
J14	D09_P	sub-LVDS	Channel 9 output
J15	D08_N	sub-LVDS	Channel 8 output
K1	VDD12C	Digital supply	Logic supply for ADC
K2	VSSA	Analog ground	Main analog ground
K14	D09_N	sub-LVDS	Channel 9 output
K15	D10_P	sub-LVDS	Channel 10 output
L1	VSSDC	Digital ground	Digital ground for ADC
L2	VDDARRAY	Analog supply	Pixel array supply
L14	D11_P	sub-LVDS	Channel 11 output
L15	D10_N	sub-LVDS	Channel 10 output
M1	VSSDC	Digital ground	Digital ground for ADC
M2	VDDARRAY	Analog supply	Pixel array supply
M14	D11_N	sub-LVDS	Channel 11 output

Pin Number	Pin Name	Pin Type	Description
M15	D12_P	sub-LVDS	Channel 12 output
N1	VSSDC	Digital ground	Digital ground
N2	VSSD	Digital ground	Digital ground
N14	D13_P	sub-LVDS	Channel 13 output
N15	D12_N	sub-LVDS	Channel 12 output
P1	VDD18	Digital supply	I/O supply for CMOS and I/O's
P2	VDD27	Analog supply	Main analog supply
P14	D13_N	sub-LVDS	Channel 13 output
P15	D14_P	sub-LVDS	Channel 14 output
R1	VDD18	Digital supply	I/O supply for CMOS and I/O's
R2	VDD27	Analog supply	Main analog supply
R14	D15_P	sub-LVDS	Channel 15 output
R15	D14_N	sub-LVDS	Channel 14 output
S1	VDD27CP	Analog supply	Connect to VDD27
S2	VSSACP	Analog ground	Analog ground
S14	D15_N	sub-LVDS	Channel 15 output
S15	D16_P	sub-LVDS	Channel 16 output
T1	VDD12C	Digital supply	Logic supply for ADC
T2	VSSD	Digital ground	Main digital ground
T14	D17_P	sub-LVDS	Channel 17 output
T15	D16_N	sub-LVDS	Channel 16 output
U1	EXTRA1	Analog ground	Connect to analog ground
U2	TDIGO1	Digital output	Digital test output
U3	TANAI1	Analog	Do Not Connect
U4	TANAI2	Analog	Do Not Connect
U5	VSELLNEG12	Analog	On-chip regulator output
U6	VS2LNEG12	Analog	On-chip regulator output
U7	VPCLNEG12	Analog	On-chip regulator output
U8	VS1LNEG12	Analog	On-chip regulator output
U9	VABNEG12	Analog	On-chip regulator output
U10	VRESLNEG12	Analog	On-chip regulator output
U11	VRESL	Analog	Bias
U12	D19_N	sub-LVDS	Channel 19 output
U13	D19_P	sub-LVDS	Channel 19 output
U14	D17_N	sub-LVDS	Channel 17 output

Pin Number	Pin Name	Pin Type	Description
U15	D18_P	sub-LVDS	Channel 18 output
V1	REF2	Analog	Do Not Connect
V2	JTAG_MODE	Digital input	JTAG Mode select. Connect to VSSD if JTAG is not used.
V3	REF3	Analog	Bias
V4	TANAO	Analog	Do Not Connect
V5	VSELL	Analog	Bias
V6	VS2L	Analog	Bias
V7	VPCL	Analog	Bias
V8	VS1L	Analog	Bias
V9	VABREG	Analog	On-chip regulator output
V10	VRESLREG	Analog	On-chip regulator output
V11	DOBR_P	sub-LVDS	Right Optical Black output
V12	DOBR_N	sub-LVDS	Right Optical Black output
V13	D20_N	sub-LVDS	Channel 20 output
V14	D20_P	sub-LVDS	Channel 20 output
V15	D18_N	sub-LVDS	Channel 18 output
W1	REF1	Analog	Do Not Connect
W2	REF0	Analog	Bias
W3	VSSA	Analog ground	Analog ground
W5	VSELLREG	Analog	On-chip regulator output
W6	VS2LREG	Analog	On-chip regulator output
W7	VPCLREG	Analog	On-chip regulator output
W8	VS1LREG	Analog	On-chip regulator output
W9	VAB	Analog	Bias
W10	CLK_N	sub-LVDS	Clock output
W11	CLK_P	sub-LVDS	Clock output
W13	VSSA	Analog ground	Main analog ground
W14	D21_N	sub-LVDS	Channel 21 output
W15	D21_P	sub-LVDS	Channel 21 output

4 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings of CMV50000

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
I_{SCR}	Input Current (latch-up immunity)		±100	mA	JEDEC JESD78D Nov 2011
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM		±2000	V	JEDEC JS-001-2014
ESD_{CDM}	Electrostatic Discharge CDM		±250	V	JEDEC JS-002-2014
Temperature Ranges and Storage Conditions					
T_J	Operating Junction Temperature	-30	70	°C	
T_{STRG}	Storage Temperature Range	-30	70	°C	
R_{HNC}	Relative Humidity (non-condensing)	30	60	%	Storage condition

5 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Electrical Characteristics of CMV50000

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supplies						
VDD12	Logic Supply Voltage of digital core, PLL		1.10	1.20	1.30	V
VDD12C	Logic Supply Voltage of ADC		1.10	1.20	1.30	V
VDD18	I/O Supply Voltage for sub-LVDS, CMOS I/O's		1.70	1.80	1.90	V
VDD27	Main Analog Supply Voltage; Supply Voltage for negative regulators		2.60	2.70	2.80	V
VDDARRAY	Pixel Array Supply Voltage		2.60	2.70	2.80	V
VDD33	Internal Regulator Supply Voltage		3.20	3.30	3.40	V
IDD12	Supply Current	Idle Running		350 375		mA
IDD12C	Supply Current	Idle Running		10 410		mA
IDD18	Supply Current	Idle Running		130 115		mA
IDD27	Supply Current	Idle Running		550 550		mA
IDDARRAY	Supply Current	Idle Running		130 130 (1)		mA
IDD33	Supply Current	Idle Running		20 20		mA
Ptot	Total Power Consumption	Idle Running		2.5 3.0		W
Digital I/O						
V_{IH}	High level input voltage		0.7 × VDD18		VDD18 +0.5	V
V_{IL}	Low level input voltage		-0.5		0.3 × VDD18	V
V_{OH}	High level output voltage	I_{OH}=4mA	VDD18 -0.15		-	V
V_{OL}	Low level output voltage	I_{OL}=4mA	-		0.15	V
C_I	Input load		-		10	pF
C_O	Output load		-		20	pF
T_{tran}	Input transition time		0.1		5.0	ns
f_{CLK_IN}	CLK_IN frequency		6		96	MHz
DC_{CLK_IN}	CLK_IN duty cycle		40		60	%

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SPI_CLK}	SPI input clock frequency		-		10	MHz
t_{setup}	SPI setup time		0.25 × T_{SPI_CLK}		-	ns
t_{hold}	SPI hold time		0		-	ns
t_{REQ}	REQ_FRAME/EXP pulse width		2 × T_{CLK_PIX}		-	ns
Sub-LVDS Interface						
V_{CM}	Common mode voltage		0.8	0.9	1.0	V
V_{OD}	Differential voltage swing		100	150	200	mV
R_O	Output impedance (2)		40		240	Ohm
D_{R0}	Impedance mismatch				10	%
DC	Clock duty cycle		45	50	55	%
f	Operating frequency		60		415	MHz
I_{OD}	Drive current		1	1.5	2	mA
ΔIOD	IOD variation over Temp.				15	%
I_{DC}	DC current consumption			3.7		mA
I_{AC}	AC current consumption			7.2		µA/MHz

(1) VDDARRAY draws high peak currents (>1A) during GLOB. Enough decoupling is needed to suppress these peaks.
(2) Unused sub-LVDS channels must be terminated the same way as the used channels.

6 Typical Operating Characteristics

6.1 Electro-Optical Characteristics

Below are the typical electro-optical specifications of the CMV50000. These are typical values for the whole operating temperature range.

Figure 7:
Electro-Optical Characteristics of CMV50000

Parameter	Value	Remark
Effective pixels	7920 × 6004	
Pixel pitch	4.6 × 4.6 µm^2	
Optical format	35mm full frame	
Pixel type	Global shutter with true CDS	Allows fixed pattern noise correction and reset (kTC) noise canceling by true correlated double sampling (true-CDS).
Shutter type	Pipelined global shutter	Exposure of next image during readout of the previous image.
Full well charge	14500 e$^-$ 58000 e$^-$	Normal mode Binning mode
Conversion gain	0.27 DN/e$^-$ 0.068 DN/ e$^-$	Normal mode, unity gain Binning mode, unity gain
Responsivity	0.16 DN/photon 0.25 A/W	@ 510nm (with micro-lenses)
Temporal noise	8.8 e$^-$ 22 e$^-$	Normal mode Binning mode
Dynamic range	64 dB 68 dB	Normal mode Binning mode
SNR_{MAX}	41.6 dB 47.6dB	Normal mode Binning mode
Shutter efficiency 1/PLS	1/18000	At 520nm, f/8.
DC	0.24 e$^-$/s 66.2 e$^-$/s	@ 20°C sensor temperature @ 60°C sensor temperature Dark Current doubles every 5.1°C increase
DCNU	0.72 e$^-$/s 14.2 e$^-$/s	@ 20°C sensor temperature @ 60°C sensor temperature DC Non-Uniformity doubles every 10°C increase
DSNU	24.5 e$^-$	Dark Signal Non Uniformity (FPN) <0.2%rms of saturation
PRNU	< 1.0% RMS	Photo Response Non Uniformity RMS of signal

Parameter	Value	Remark
Color filters	Optional	RGB Bayer pattern
QE	58 / 61 / 53 / 14.5 % 49 / 55 / 45 %	Quantum Efficiency (with micro-lenses) @ 450 / 510 / 600 / 850nm (mono device) @ 450 / 510 / 600nm (color device)
Sub-LVDS outputs	22 Data 1 Control 1 Clock	Each data output running @ 830 Mbit/s. Less outputs selectable at reduced frame rate
Frame rate	30 fps	Using 830 Mbit/s sub-LVDS in pixel-based output Higher frame rate possible in row windowing mode.
Timing generation	On-chip	Possibility to control exposure time through external pin.
PGA	Yes	x1, x1.33, x2, x4 analog gain settings
Programmable registers	Sensor parameters	Window coordinates, Timing parameters, Gain & offset, Exposure time,
HDR mode	Interleaved	2 exposure times for odd/even columns
ADC	12 bit	Column ADC
Interface	sub-LVDS; 830 Mbit/s	Serial output data + synchronization signals
I/O logic levels	sub-LVDS = 1.2 V Dig. I/O = 1.8 V	
Cover glass	D263T eco	Double sided AR coating R<1.5 % abs, 400 - 900nm, per surface, AOI=15°
Mass	20gr	

6.2 Spectral Characteristics

Figure 8 :
Quantum Efficiency

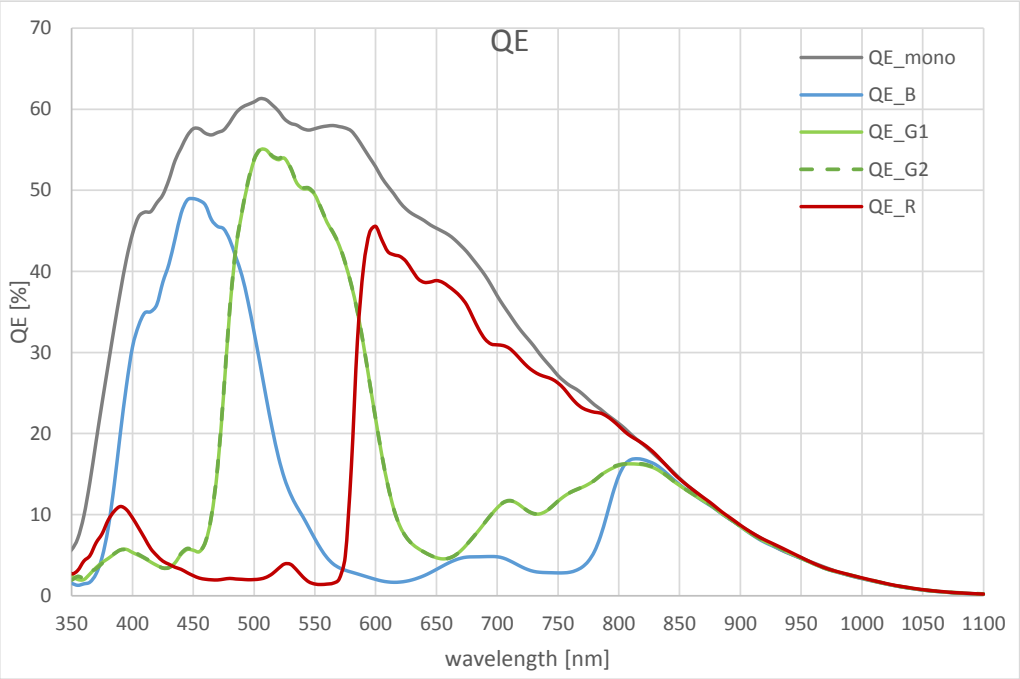


Figure 9 :
Responsivity (Analog Gain x4)

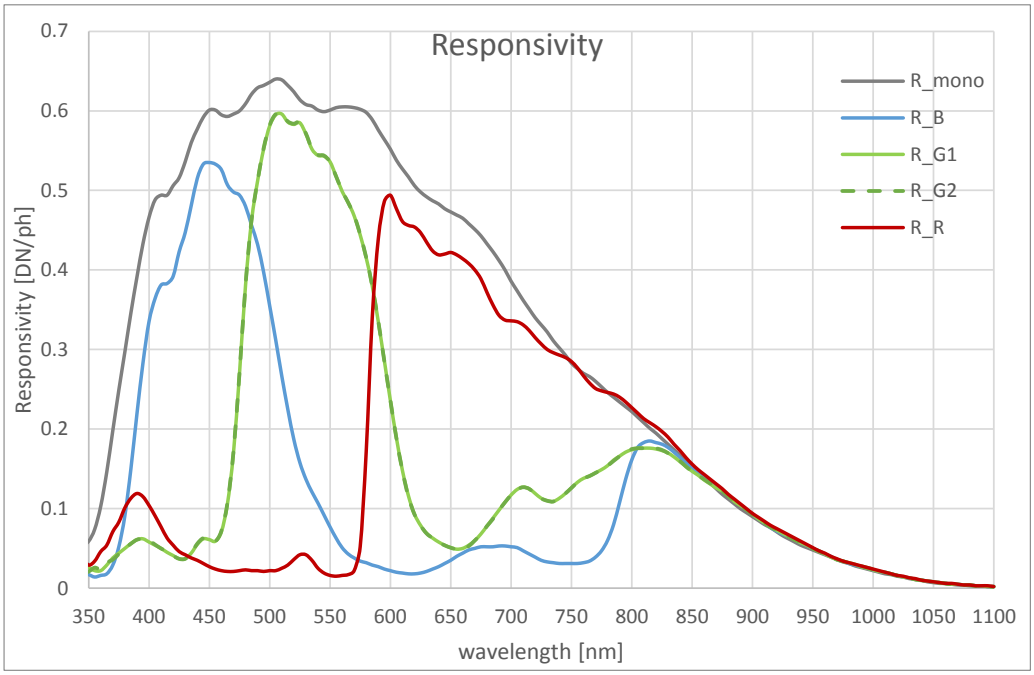


Figure 10 :
Spectral Response

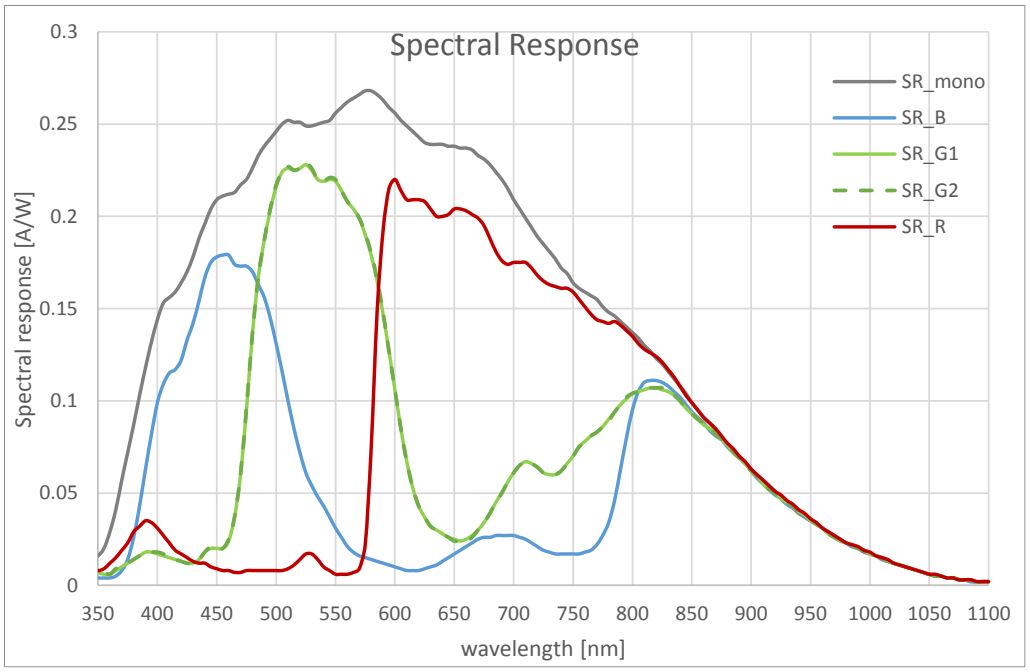


Figure 11 :
Responsivity (Analog Gain x4)

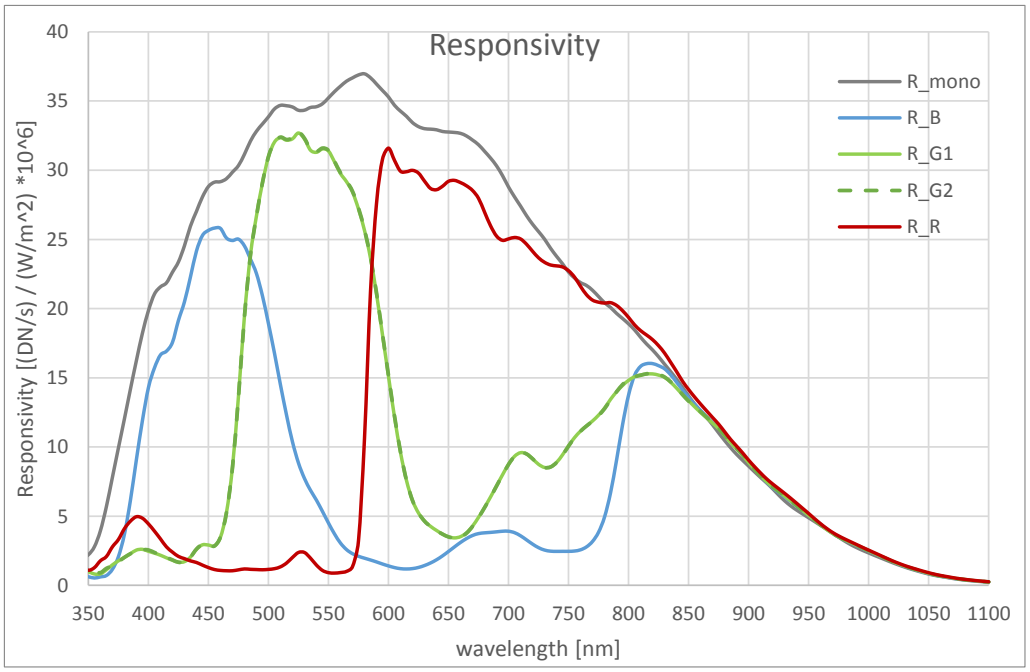


Figure 12 :
MTF

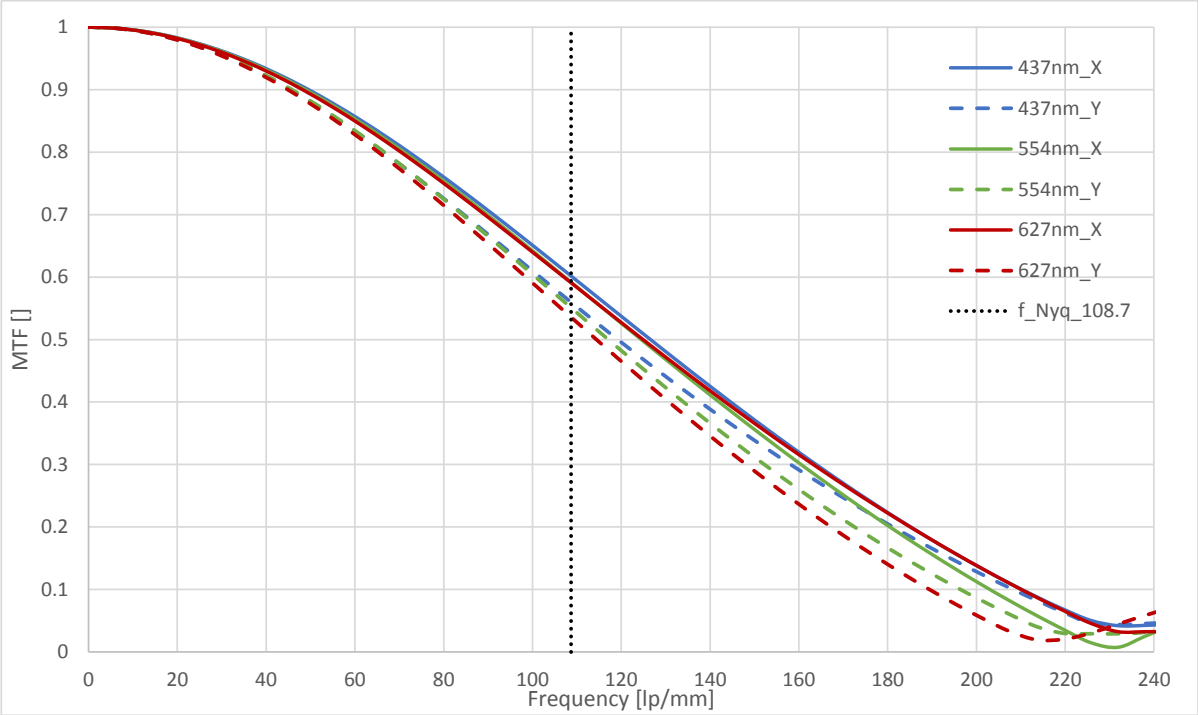
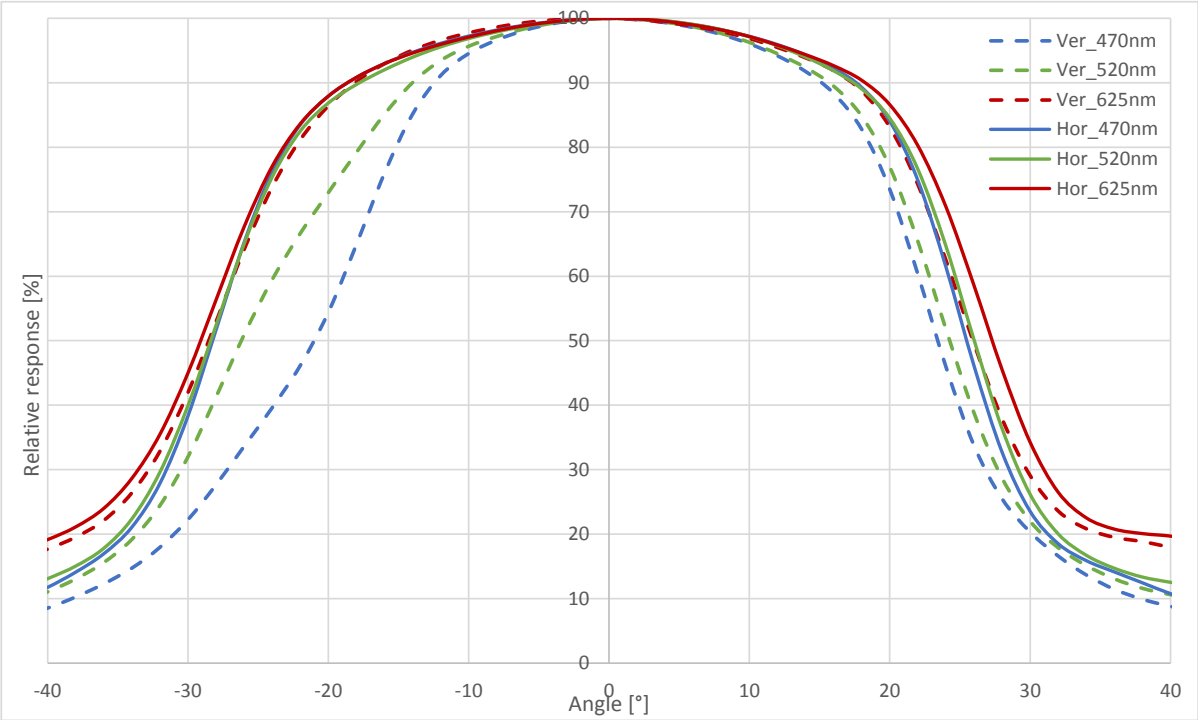


Figure 13 :
Angular Response



7 Functional Description

7.1 Sensor Architecture

Figure 2 shows a high-level representation of the chip architecture for the CMV50000 sensor. The drawing shows the active pixel array and the periphery around it that enables the control and readout of the pixels.

The core of the image sensor is made up from the pixel array, which is driven from two sides by 2 instances of the row logic and drivers. The pixel control signals are created globally by the global drivers and distributed to the sides of the sensor. The pixel data is read out row by row using a data path consisting of an analog front-end (AFE), analog-to-digital converter (ADC) and a digital data post-processing (DPP) block.

The converted data is sent, pixel by pixel, to a set of sub-LVDS drivers. An additional control (CTR) channel provides synchronization information about the data on the data channels, while a specific CLK channel can be used to sample the data channels.

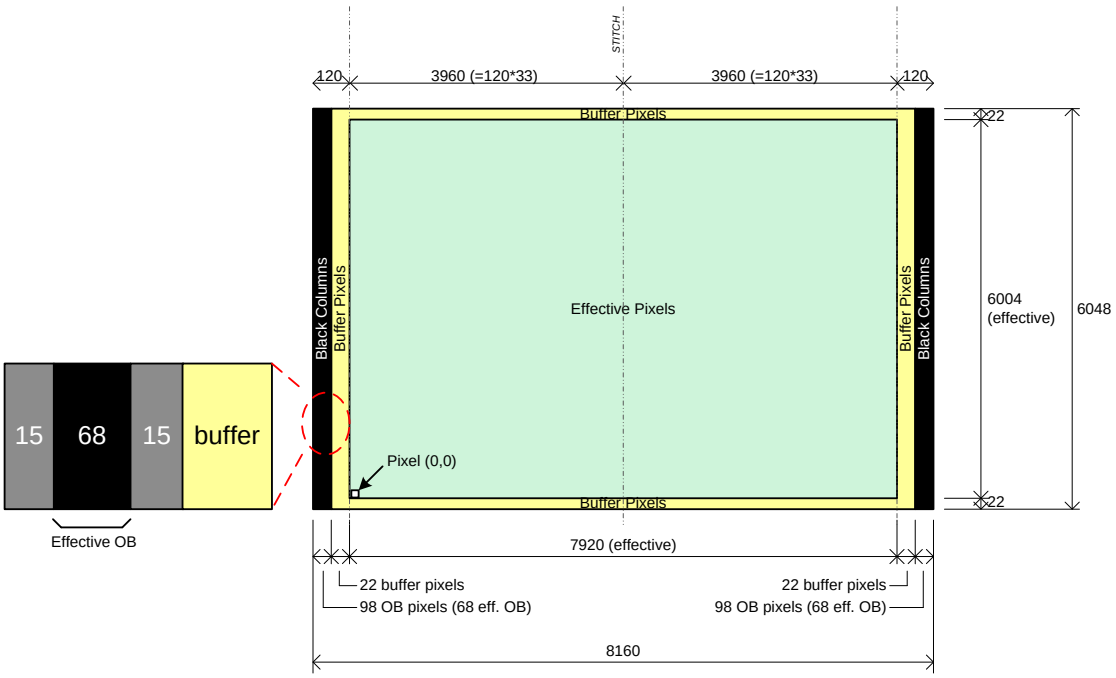
The data path is organized in kernels of 360 columns. Between kernels, control signals are repeated. There is one sub-LVDS driver for every kernel. At the left and right side of the pixel array, an additional kernel of OB pixels is added.

An on-chip sequencer controls the sensor operation and contains a register bank that is programmable over an SPI interface. There is also an on-chip temperature sensor available. A low-frequency CMOS input clock is transformed using an on-chip PLL to a set of high-frequency signals used in the sensor.

7.1.1 Pixel Array

Figure 14 shows the complete pixel array.

Figure 14:
Pixel Array



The pixel array can be split up in 3 parts: Optical black (OB) pixels (left and right side), buffer pixels (around effective array perimeter) and effective pixels. Only the 68 effective OB pixels are used for internal row clamping, which improves row noise and allows setting a pre-defined black level. The buffer pixels form a guard ring around the effective pixels. The buffer pixels are optically active, but are not guaranteed to meet the optical specifications. The 98 OB and 22 buffer pixels are read out via the sub-LVDS OB-L/R outputs.

The full resolution of the pixel array is 8160 × 6048 pixels. This results in an effective resolution of 7920 × 6004 pixels or 47.5Mpixels. The effective array is 36.4mm × 27.6mm which is slightly larger than the 35mm full frame optical format (= 36mm × 24mm; which would correspond to a window of 7826 × 5217).

Because of the large sensor area, a wafer process called mask stitching is done. The vertical stitch line is located exactly in the middle of the array. Therefor a small offset between the pixels left and right of the stitch line might be present.

Micro-lenses are placed on the pixels for improved quantum efficiency and fill factor.

7.1.2 Analog Front End

The analog front end consists of the PGA (programmable gain amplifier) and circuitry to prepare the signal for ADC conversion

7.1.3 ADC

The column ADC converts the analog pixel value to a 12-bit value.

7.1.4 DPP

The DPP blocks perform digital operations on the visible pixel data: digital offset, digital gain, row noise correction.

7.1.5 Sub-LVDS Outputs

The sensor has 22 sub-LVDS data channels to output the processed data. Each data channel outputs the data of 360 columns. Readout modes using less parallel channels at reduced framerate are supported as well.

7.1.6 Sequencer

The on-chip sequencer will generate all required control signals to operate the sensor from only a few external control clocks. This sequencer can be activated and programmed through the SPI interface.

- Among the different features that the sequencer has implemented are the following:
- SPI protocol and register banks management.
- Exposure and frame timing generation based on external inputs or internal settings.
- Dual exposure HDR mode.
- Y-windowing, subsampling and binning

7.1.7 SPI Interface

The SPI interface is used to load the sequencer registers with settings to configure the image sensor. Features like windowing, subsampling, gain and offset are programmed using this interface. The settings in the on-chip registers can also be read back for test and debug of the surrounding system.

7.1.8 Temperature Sensor

An on-chip thermal sensor is included. The temperature data is read out through the SPI interface.

7.1.9 PLL

Various clock frequencies are required internally to operate the sensor. These are derived from a single input frequency using an on-chip PLL. Through configuration over SPI, a range of input clock frequencies is supported.

The 3 main internal clocks are CLK_ADC, CLK_SER and CLK_PIX:

- CLK_ADC is the PLL output clock and is equal to the data rate (830MHz for 830Mbit/s).
- CLK_SER is 1:2 of CLK_ADC and equal to the sub-LVDS output clock.
- CLK_PIX is the pixel clock and has a ratio of 1:12 of CLK_ADC.

7.1.10 OTP Memory

A non-volatile, one time programmable memory is included on-chip. This is programmed with unique device ID and temperature sensor calibration data which the user can use.

7.2 Operating the Sensor

This section explains how to connect and power the sensor, as well as basic recipes of how to configure the sensor in a certain operation mode.

7.2.1 Power Supplies

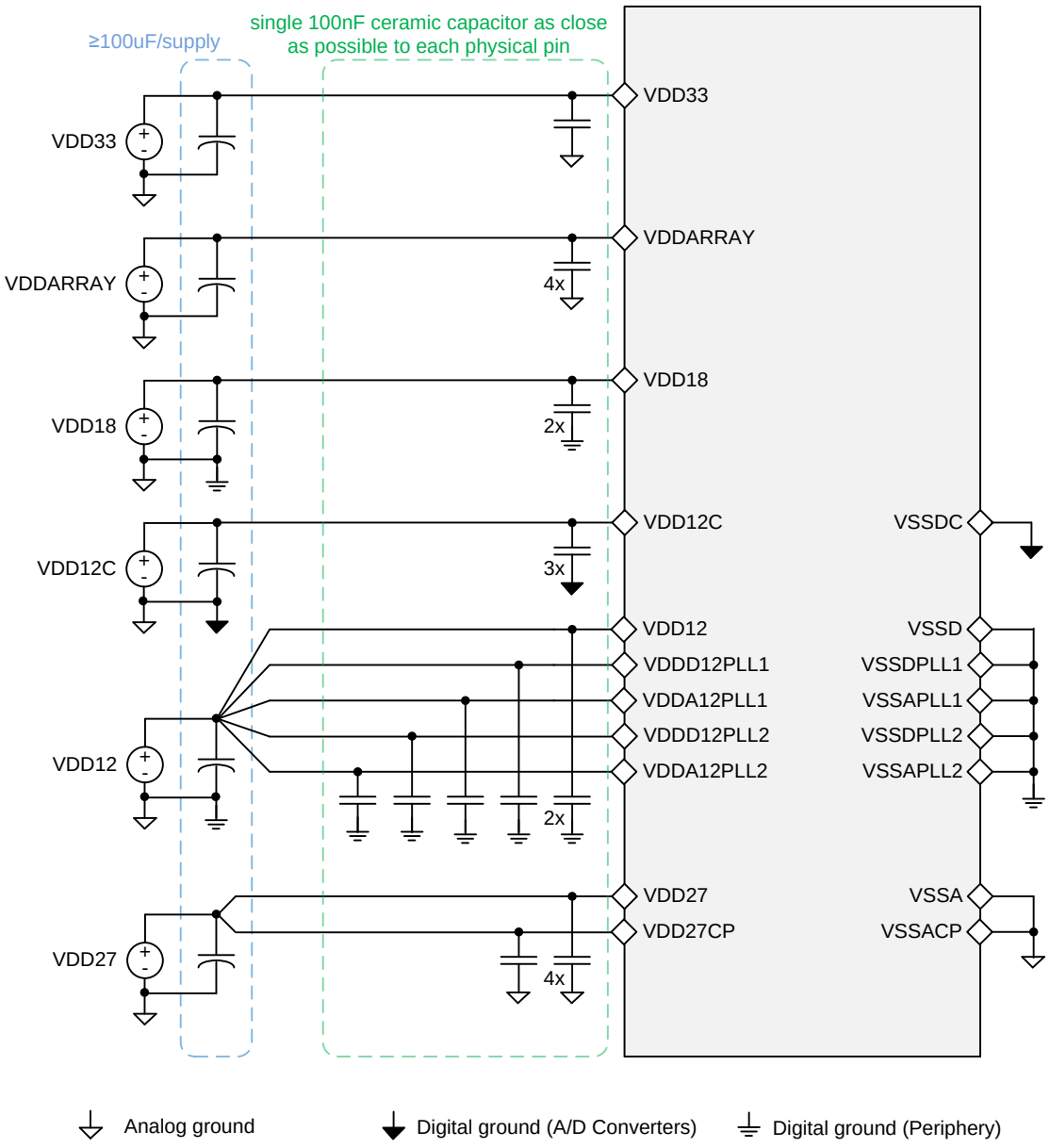
External Power Supplies

To power the sensor, six externally generated supplies are required as listed in Figure 6. A distinction is made between digital supplies (VDD12, VDD12C, VDD18) and analog supplies (VDD27, VDDARRAY, VDD33). Avoid using switching power supplies when possible, especially for the analog supplies.

Sufficient bulk (at the regulators) and local (at the sensor pins) decoupling is needed. In case of multiple pins for the same supply, local decoupling must be foreseen for each pin (e.g. four capacitors for the four VDDARRAY pins). Separate ground planes must be provided to minimize coupling.

For optimal noise performance, it is advised to keep the analog and digital ground nets separated and connect them together as close as possible to the external supply regulators.

Figure 15:
Power Supply Decoupling and Grounding Diagram



Biasing (on-chip regulators)

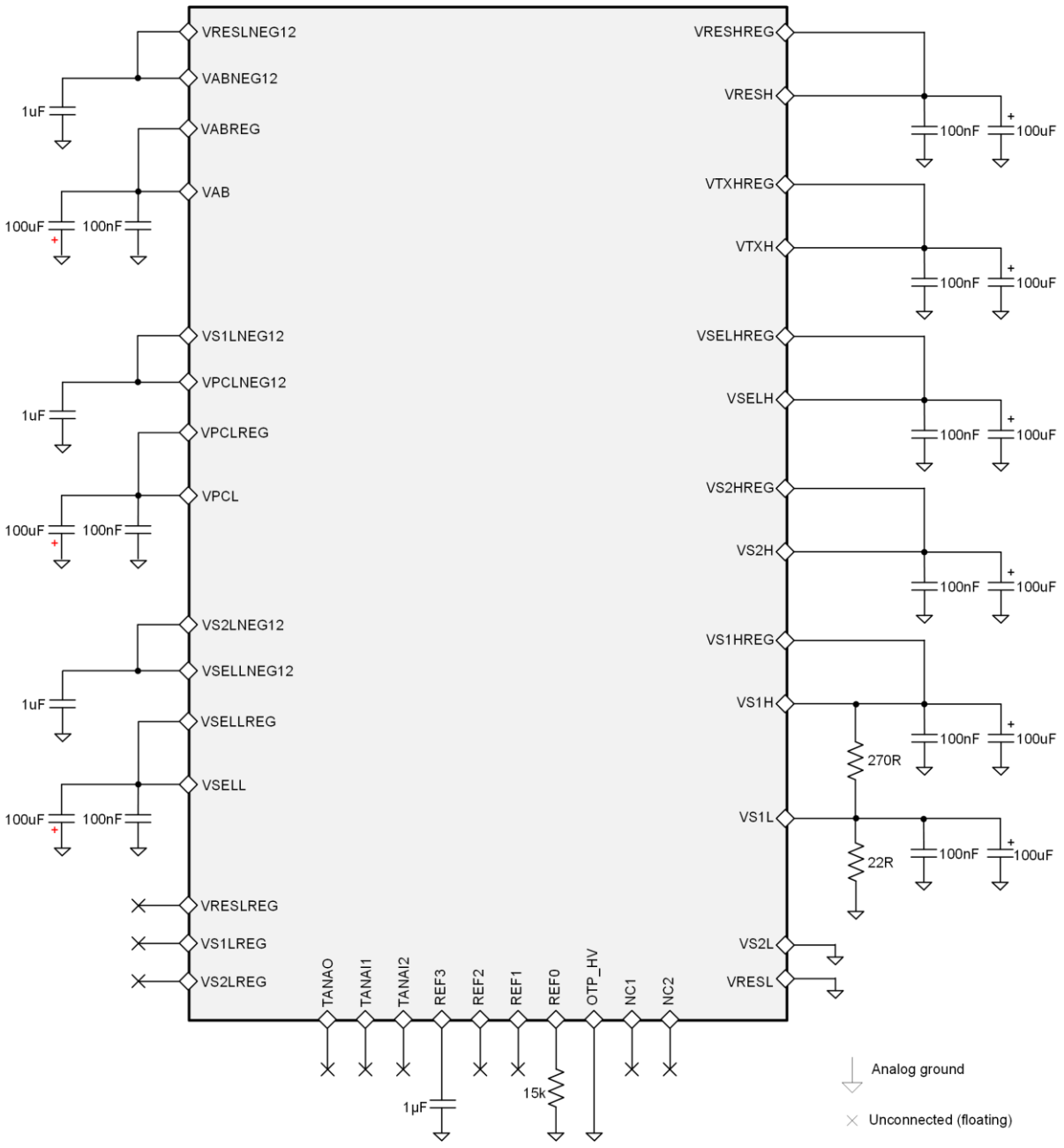
Operating the pixel array requires multiple different biasing supply levels. These supply levels can be generated using on-chip regulators. The chip contains 2 types of regulators, for positive supply levels and negative supply levels. The regulator output voltages are controlled using the SPI interface.

The supply regulators are internally not connected to the actual image sensor. Connections have to be made on PCB level (from a VxxREG pin to a Vyy pin). Also, each supply regulator requires to be

decoupled by a 100µF and 100nF capacitor. The negative supply regulators also require a decoupling of 1µF on a separate output pin (which will settle to -1.2V).

Next figure shows the positive and negative voltage regulator as well as the bias connections.

Figure 16:
On-Chip Regulators Connection Diagram



For the 100nF and 1µF capacitors, ceramic types can be used. Capacitances of 100µF can be electrolytic types (beware of the polarity on the negative supplies!). The maximal specified ESR and ESL of these 100µF capacitors are 0.1Ω and 10nH respectively.

A resistor network is necessary between VS1H and VS1L (±5% tolerance).

To obtain an accurate current bias reference in the sensor, an external bias resistor of 15kOhm (±5%) must be placed between REF0 and ground. No decoupling is required in parallel with this resistor. A maximal capacitance of 1nF on this node is allowed.

After power-up of the sensor, the recommended register settings will set the correct supply levels for these regulators (see section 7.4). Next table gives an overview of the available supply regulators, the connection to the bias pin and the required voltage on that pin.

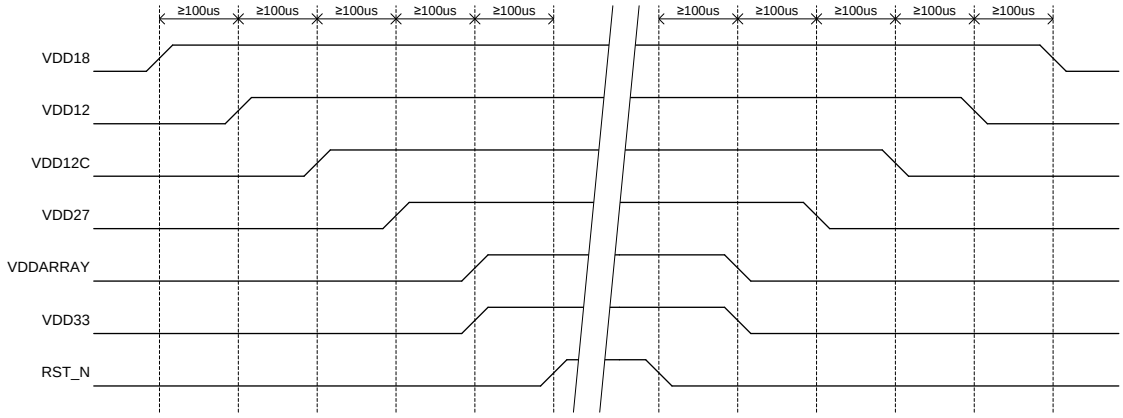
Figure 17:
Bias Voltages

Regulator Pin	Type	Bias Pin	Voltage (V)
VRESHREG	Positive	VRESH	3.2
VTXHREG	Positive	VTXH	3.0
VS1HREG	Positive	VS1H	3.0
VS2HREG	Positive	VS2H	3.0
VSELHREG	Positive	VSELH	3.0
VABREG	Negative	VAB	-0.8
VPCLREG	Negative	VPCL	-0.3
VSELLREG	Negative	VSELL	-0.6
-	Positive	VS1L	0.25
-	Ground	VS2L	0
-	Ground	VRESL	0
VRESLREG	Negative	-	0
VS1LREG	Negative	-	0
VS2LREG	Negative	-	0
VRESLNEG12	Negative	VABNEG12	-1.2
VS1LNEG12	Negative	VPCLNEG12	-1.2
VS2LNEG12	Negative	VSELLNEG12	-1.2

7.2.2 Power-Up/Down Sequence

To avoid peak currents and guarantee a proper power-up/down of the sensor, following supply order and timing must be applied.

Figure 18:
Supply Power-Up and Power-Down Sequences



7.2.3 Startup Sequence

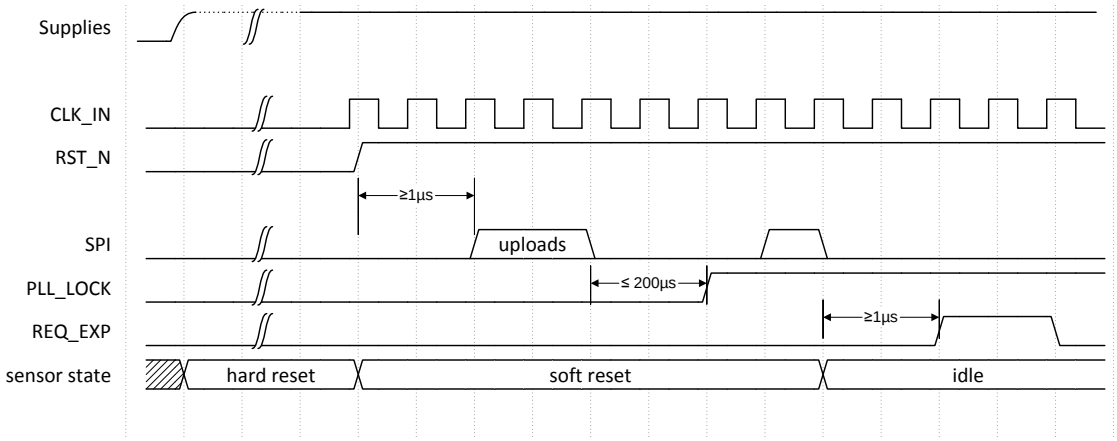
After the supply power-up sequence, the general sequence below must be followed to configure and start operating the sensor. Deviating from the order or timing can lead to the sensor being in an unknown or unstable state.

The sensor hard reset pin, RST_N, must be asserted (‘0’) during the supply ramp-up to initialize the sensor in the hard reset state. By releasing RST_N (‘1’), the sensor moves to soft reset state. CLK_IN can be started during either the hard reset or during soft reset state. During the soft reset state, the recommended SPI uploads must be executed (see section 7.4). One of them enables the PLL. After maximally 200µs, the PLL will lock. After the PLL has locked the sensor can be moved from soft reset state to idle state through a short SPI upload.

In idle state, the sensor waits for an exposure request to begin grabbing, for example with REQ_EXP pin (depending on the configured sensor control mode).

As indicated in the figure, a non-overlap of 1 µs must be respected between each sensor state change and the next action.

Figure 19:
Power-Up Sequence (not to scale)



7.2.4 Clocking

The sensor has two CMOS clock inputs: SPI_CLK and CLK_IN. SPI_CLK is part of the SPI interface used to configure the sensor. All other internal sensor clocks are derived from two PLLs running on CLK_IN.

Refer to section 5 for the electrical specifications of the input clocks and to section 7.1.9 for the configuration procedure of the PLL.

7.2.5 SPI and Register Access

The sensor operation must be configured by uploading register settings. These static register values control the behavior of the sequencer on the chip, but also of all the analog and mixed-signal blocks. To write and read register settings the SPI interface is used.

The SPI (Serial Peripheral Interface) consists of four wires, as shown in Figure 21. The CMV50000 image sensor always operates as the SPI slave. A single SPI access always consists of:

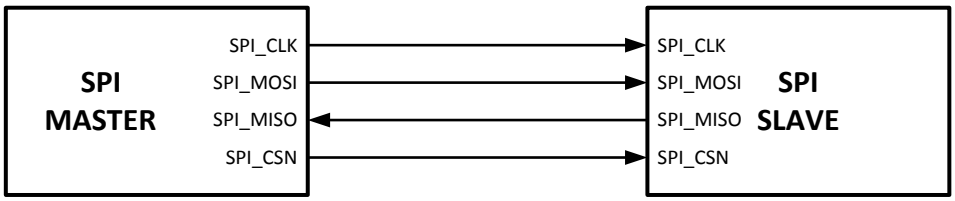
- Transfer of a control bit from master to slave to specify transfer direction (read or write)
- Transfer of 7-bit register address from master to slave
- Transfer of 8-bit data from master to slave (write operation) or from slave to master (read operation)

Figure 20:
SPI Signal Overview

Pin Name	Direction	Purpose
SPI_CSN	Sensor Input	Active-low chip select
SPI_CLK	Sensor Input	Rising-edge triggered clock for SPI protocol
SPI_MOSI	Sensor Input	Data moving from master to slave
SPI_MISO	Sensor Output	Data moving from slave to master

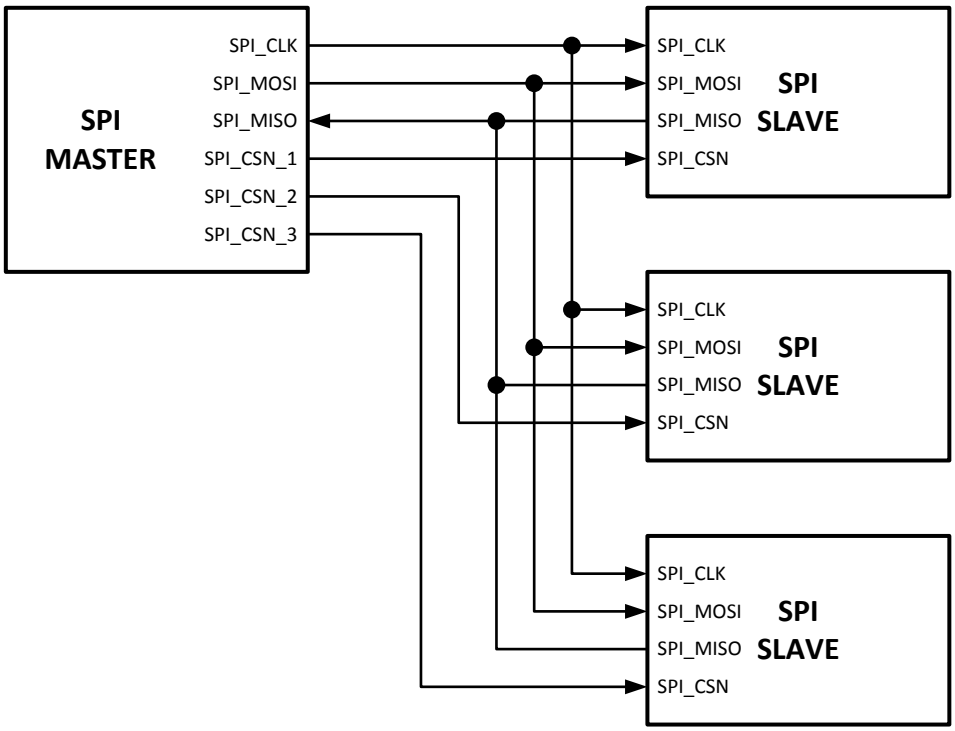
Data is written to the registers of the SPI slave over the SPI_MOSI wire. The data written to the programming registers can also be read out over this same SPI interface, using the SPI_MISO wire. SPI_CSN is an active-low chip select that enables the SPI slave. The details of the timing and data format are described below.

Figure 21:
SPI Connection Diagram



When using multiple CMV image sensors, the SPI_CLK and SPI_MOSI can be shared among them. The SPI_CSN operates as a chip select for each of the slaves. The SPI_MISO can also be shared on a bus because it is tri-stated when it is not used. This configuration of one master and multiple slaves is shown in Figure 22.

Figure 22:
SPI with 1 Master and 3 Slaves



An SPI access always consists of the transfer of the following bits (in this order), as given in Figure 23:

Figure 23:
SPI Bits Transfer Sequence

Phase	# Bits	Via	Purpose
CTRL	1	SPI_MISO	Control bit indicating SPI access direction (1 for write, 0 for read)
ADDR	7	SPI_MISO	Address (0-127) of register to be accessed
DATA	N*8	SPI_MISO	Data written to N consecutive register addresses, starting at ADDR
		SPI_MOSI	Data read from N consecutive register addresses, starting at ADDR

Via a burst mode, it's possible to write/read multiple consecutive register addresses with a single address upload.

The state of SPI_CLK whenever SPI_CSN is high is ignored, though it is advised to stop the clock to save unnecessary power consumption.

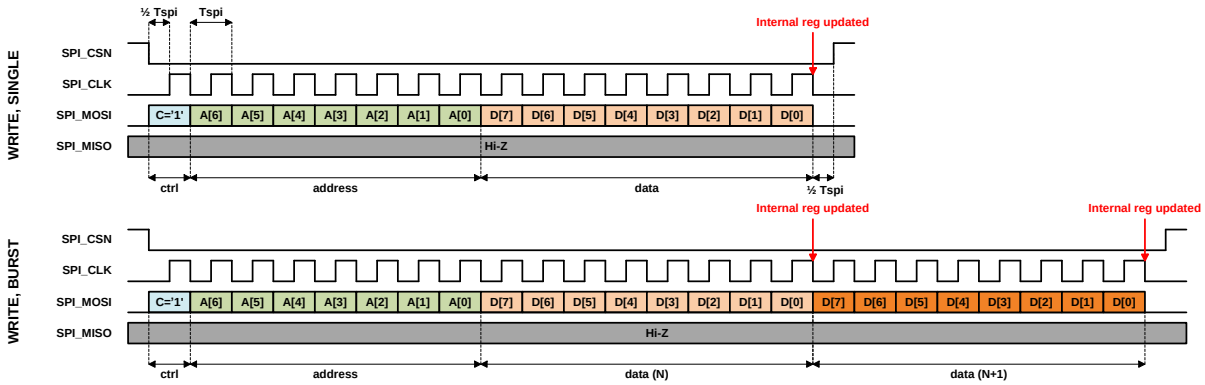
SPI Write

The SPI_MOSI data is sampled by the CMV image sensor on the rising edge of the SPI_CLK. The SPI_CSN signal shall be low for ½ a SPI_CLK period before the first data bit is sampled. SPI_CSN shall remain low for ½ a SPI_CLK period after the last falling edge of SPI_CLK. The first bit transferred is a control bit indicating a write operation (‘1’). Both the subsequent address (A<6:0>) and data (D<7:0>) are sent MSB-first.

When writing multiple sequential registers (e.g. 100, 101, 102 ...), the write burst mode can be used. The address is that of the 1st register to be written to and the sequencer will automatically shift to the next register after 8 data bits. SPI_CSN shall stay low the entire time.

The actual register value is updated with the new value on the falling edge of SPI_CLK on every D[0] bit. I.e. SPI_CLK shall go low at the end of D[0] for the write sequence to be completed. The timing of both write modes is illustrated below.

Figure 24:
SPI Write Timing

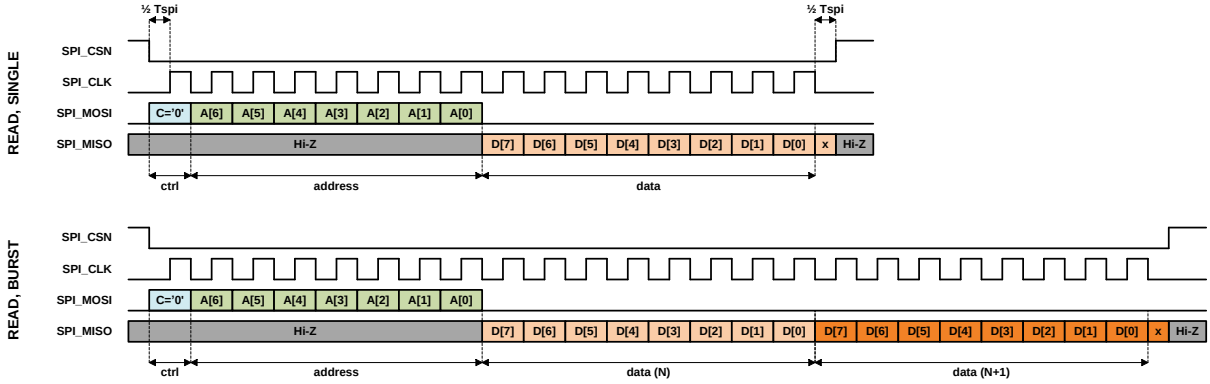


SPI Read

The timing of the SPI read sequence is similar to the SPI write sequence. The main differences are the control bit and the use of SPI_MISO. An SPI read is indicated by setting the control bit to ‘0’. After the control bit, the address of the register to read shall be transmitted MSB first. At the end of the LSB of the address, the data is launched on the SPI_MISO pin on the falling edge of the SPI_CLK. This means that the data can be sampled by the SPI master on the rising edge of the SPI_CLK. The data D<7:0> is transmitted MSB first on SPI_MISO. When not transmitting data, the SPI_MISO output is in high-Z state.

Sequential SPI register addresses can also be read out in burst mode by keeping SPI_CSN low and clocking out additional bytes. The timing of both read modes is illustrated below.

Figure 25:
SPI Read Timing



Register Banks

The sensor's configuration registers are organized in four banks. Each bank contains 127 8-bit registers.

To select a certain register bank, the register at address 0 is used. This register is accessible regardless of the currently selected register bank, of course.

Figure 26:
Bank Selection Register

Register Name	Bit Name	Bank	Addr	Pos	Description
BANK_SEL	BANK_SEL	N/A	0	[1:0]	0: Bank 0 1: Bank 1 2: Bank 2 3: Bank 3

The value of BANK_SEL selects which register bank the current SPI access will have an effect on. An example is given below. 'Addr' is the address of the register being written to or read from and 'D' is the data being written.

Figure 27:
Bank Selection Example Sequence

#	Action	Effect
1	WRITE(Addr=0, D=0)	Set BANK_SEL to 0 (Point to BANK 0)
2	WRITE(Addr=12, D=3)	BANK_SEL points to bank 0 Write value 3 to NROF_FRAMES register
3	WRITE(Addr=79,D=1)	BANK_SEL points to bank 0 Write value of 1 to 8 lowest bits of TRAINING_WORD

#	Action	Effect
4	WRITE(Addr=80,D=2)	BANK_SEL points to bank 0 Write value of 2 to highest bits of TRAINING_WORD Completes full 14-bit register: TRAINING_WORD = 513
5	WRITE(Addr=79, D=8;1;3) burst upload	BANK_SEL points to bank 0 Write 8 to LSBs of TRAINING_WORD Write 1 to MSBs of TRAINING_WORD Write 3 to TEST_LVDS
6	WRITE(Addr=0, D=0)	Set BANK_SEL to 0 (Point to BANK 0)
7	READ(Addr=81)	Reads TEST_LVDS (result = 3)

Register Categories

The registers are grouped into various categories, based on when they may or may not be updated. The category for every individual register can be found in section 8. The table below explains the details of the various categories.

Figure 28:
Register Categories

Category	Description
-	Registers without category can be changed at any time, but might directly influence the sensor execution.
SYNC	Registers are internally synchronized to start of frame (at the start of the GLOB state), so an entire frame is always read with the same SYNC configuration. This means that the registers may be updated at any time.
FRAME	Registers controlling the frame and exposure timing. These are only checked at the rising edge of REQ_EXP and may be updated at any time during operation.
DC	Can only be changed when sensor is in IDLE state, or in soft reset state.
RST	Only to be changed when sensor is in soft reset state.
RO	Read-only register. All write operations are ignored.

Reading from a register is always allowed. When reading registers of category 'SYNC', the last previously uploaded value is read. This is NOT necessarily the same as the active frame-synchronized value.

Figure 29:
Frame Sync

Reg. Name	Bank	Addr	Bits	Def.	Description
DISABLE_FRAMESYNC	0	1	[0]	0	0: Enable 1: Disable
PARAM_HOLD	0	2	[0]	0	0: Frame sync 1: During SPI upload

The upload of 'SYNC' type registers can be constrained with the following registers:

If **DISABLE_FRAMESYNC** is set to '1', frame synchronization is disabled. Any uploads will take effect immediately.

Frame synchronization only happens if **PARAM_HOLD** is '0'. When uploading a bunch of SYNC-type registers together (for example, change a number of different YWIN settings), it's advised to set **PARAM_HOLD** to '1' during the entire upload. This prevents a frame from being started with only half of the required updates in case the frame start happened when the entire upload had not completed.

7.2.6 Soft Reset

Figure 30:
Soft Reset Register

Reg. name	B	Addr	Bits	Description
CMD_REGS. CMD_RST_SOFT_N	0	3	[0]	Use calculated value

The sensor has an asynchronous reset input pin (**RST_N**) and an asynchronous reset register (**CMD_RST_SOFT_N**). Both are active-low.

When combined, they have the following function:

- **RST_N**: Reset the entire sensor when low. This is considered a hard reset.
- **CMD_RST_SOFT_N:** Reset the entire sensor, except the SPI interface and register bank when low. This is considered a soft reset.

As long as RST_N is high, all registers retain their value when CMD_RST_SOFT_N is low.

The procedures to assert and release soft reset are described in detail in section 7.4.2.

7.2.7 Controlling Exposure and Readout

This section explains the different ways the exposure of a frame can be started and ended. First some important concepts of the frame timing model are explained.

Basic Frame Timing

During operation, the sensor can be in any of the following states:

- **RESET:** asynchronous sensor reset is low, disabling the sensor entirely
- **IDLE:** sensor is not doing anything while waiting for external requests
- **EXPOSURE:** light is being integrated in the pixels
- **GLOB:** closing global shutter by sampling all integrated pixel values
- **READOUT:** reading out the acquired frame plus meta data and mandatory overhead

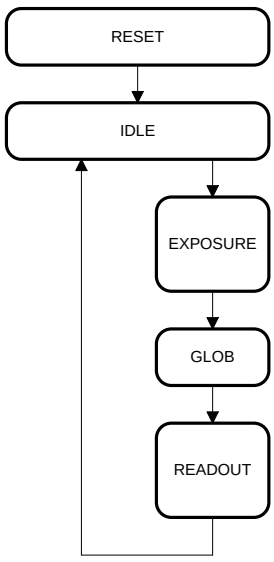
The sensor always exits a general sensor RESET condition in the IDLE state. This means that the sensor always acts as a slave, responding to external controls.

A distinction can be made between two basic frame timing operations (sequential and pipelined operation), as detailed in the following two sections.

Sequential Operation

In sequential operation, the sensor goes through a sequential succession of EXPOSURE - GLOB - READOUT to grab a single image, as indicated in the figure below. When a cycle like this has been completed, the sensor is again in an IDLE state, waiting for new commands.

Figure 31:
State Chart: Sequential Operation

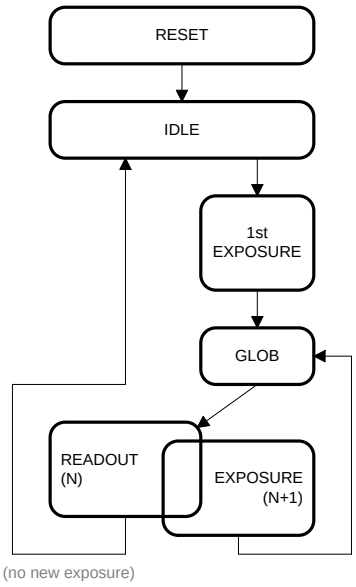


Pipelined Operation

The main property of pipelined operation is that the sensor can be in the EXPOSURE state and READOUT state at the same time. This basically means that the readout of frame N can be busy while

the EXPOSURE state of frame N+1 has already started. The EXPOSURE can fully or partially overlap with a READOUT state.

Figure 32:
State Chart: Pipelined Operation



When exiting IDLE state, the first EXPOSURE period starts. Just like in the sequential operation, this flows into a GLOB state, which in its turn starts the READOUT of a frame. Depending on the sensor control or configuration (see 7.2.7 and 7.2.8 for details and options), a new EXPOSURE may start when the READOUT is still busy.

At the end of the READOUT period, there are two options:

- **No new EXPOSURE got started**. The sensor will return to IDLE.
- **A new EXPOSURE did get started**. The sensor will wait until this new EXPOSURE finishes, before moving back to GLOB, which will always trigger a new READOUT.

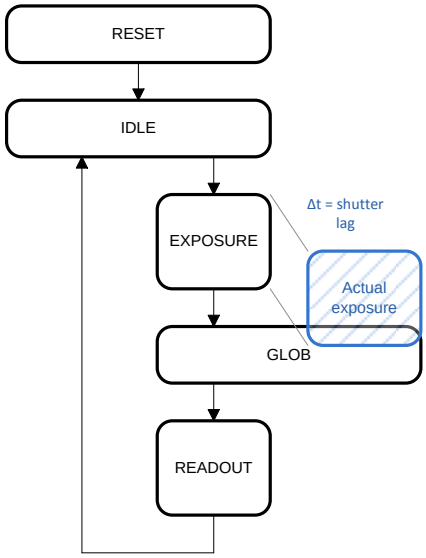
Shutter Lag

Figure 33:
No Shutter Lag Register

Reg. Name	B	Addr	Bits	Def.	Description
NO_SHUTTER_LAG	0	117	[0]	0	0: Shutter lag 1: No shutter lag

By default, the sensor always has a shutter lag. This effectively means that there is a delay between the start and end of **EXPOSURE state** and the start and end of the **actual exposure** (actual exposure = time where sensor is actually capturing and integrating light). This is illustrated in the figure below.

Figure 34:
State Diagram: Sequential Operation with Shutter Lag



The distinction is important because:

- The EXPOSURE state is the direct response of external control (through sensor I/O requests or register settings),
- Yet it is the actual exposure that really matters to the user

In the remainder of the document, when the concept of exposure or exposure time is mentioned, it will always be about the **EXPOSURE state**, unless stated otherwise. The reader should always bear in mind that the **actual exposure** is delayed in time with respect to this EXPOSURE state due to the shutter lag mechanism.

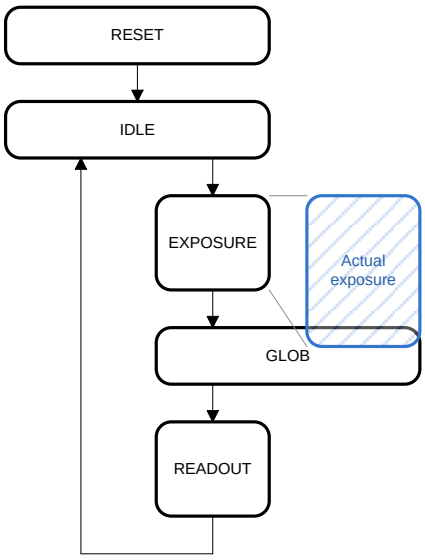
In Figure 34 the shutter lag is shown under sequential operating conditions only, but note however that the shutter lag is present in all operation modes.

The shutter lag is always present at the end of the EXPOSURE period: part of the actual exposure time will always extend into the GLOB state (sometimes called "exposure overlap"). The shutter lag at the beginning of the EXPOSURE periods is introduced artificially to compensate for this exposure overlap.

If the shutter lag at the start of EXPOSURE is not allowed in certain applications, it can be disabled by setting register **NO_SHUTTER_LAG** high. This means that the actual exposure will start together with the start of the EXPOSURE state (practically: "immediately after an exposure request"). The

disadvantage of this is obviously that the length of the actual exposure time is not the same as the length of the EXPOSURE state (the "exposure overlap" needs to be added).

Figure 35:
State Diagram: Sequential Operation, no Shutter Lag at Start



7.2.8 Sensor Control Modes

Figure 36:
Control Mode Register

Reg. Name	Bank	Addr	Bits	Def.	Description
CTRL_MODE	0	9	[2:0]	0	0: Full external 1: Programmed external 2: Triggered internal 3: Streaming

The travel through the state diagrams of Figure 34 and Figure 35 can be externally controlled with the sensor inputs REQ_EXP and REQ_FRAME and a bunch of register settings (which will be detailed in further sections). This can be done in a number of different modes (each varying slightly in behavior and level of dependency on I/O control versus register configuration).

The control mode is set with the **CTRL_MODE** register, as listed in Figure 37.

Figure 37:
Control Modes

CTRL MODE	Name	External Control	Internal Control
0	Full external	Start of exposure. End of exposure (starting readout).	Readout details.
1	Programmed external	Start of exposure.	Length of exposure. Readout details.
2	Triggered internal	A finite sequence of 1 or more consecutive frames.	Length of exposure. Frame rate. Sequence length. Readout details.
3	Streaming	An infinite sequence of consecutive frames.	Length of exposure. Frame rate. Readout details.

Each of these control modes is introduced in one of the following sections.

Control Mode 0: Full External

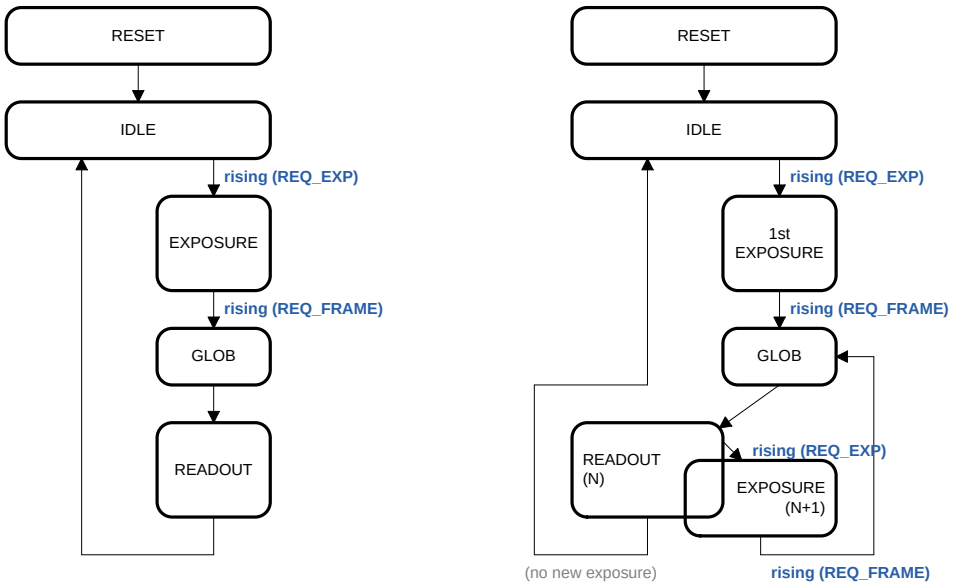
In the *Full External* control mode, the exposure timing is fully controlled with the sensor input pins:

- A rising edge on **REQ_EXP** moves the sensor to the EXPOSURE state
- A rising edge on **REQ_FRAME** moves the sensor to the GLOB state, which will be automatically followed by READOUT.

The length of the EXPOSURE state will exactly match the time between the rising edges of both triggers.

In the figure below, the state diagrams of sequential and pipelined operation are annotated with the external control events.

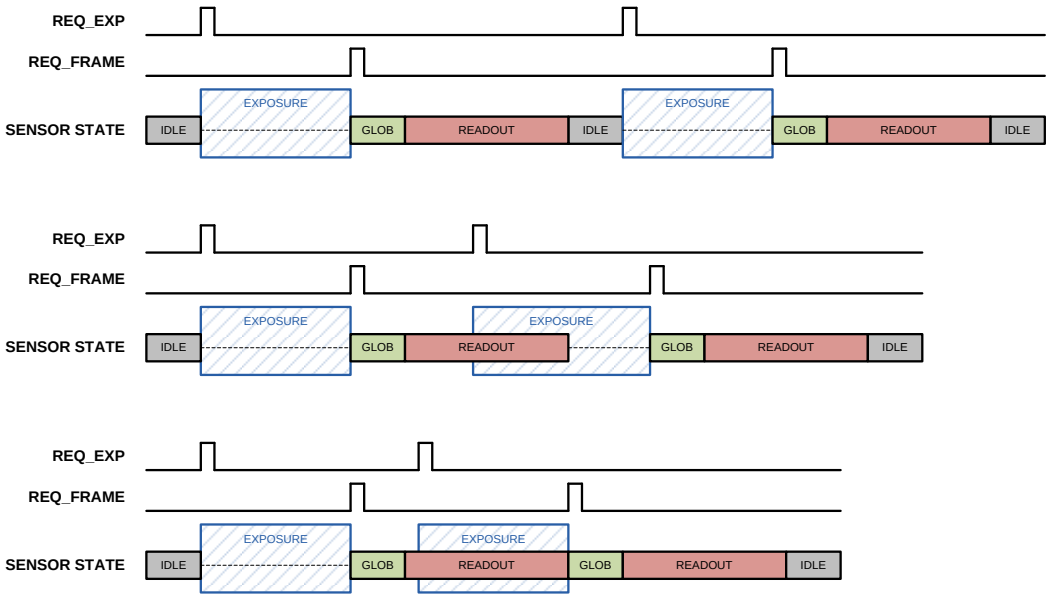
Figure 38:
State Diagram: Full External Mode



The length of the GLOB state, as well as the length of the READOUT period depends on a number of register settings.

The state diagram is expanded into a timing diagram for a few situations in the figure below.

Figure 39 :
Timing Diagram: Full External Mode



The figure shows how the *Full External* control mode can be used to (from top to bottom):

- Operate the sensor in *Sequential Operation* mode.
- Operate the sensor in *Pipelined Operation* mode, with the parallel exposure extending beyond the readout phase.
- Operate the sensor in *Pipelined Operation* mode, with the parallel exposure ending together with the readout phase (gives maximum frame rate).

Except for the invalid timings listed in Figure 40, the requests on REQ_EXP and REQ_FRAME can be freely placed anywhere by the external controller. This will result in the most flexible external control possible with this sensor (start and end exposure at any possible time, freely vary exposure time from frame to frame, interrupt frames being read to start a new readout…).

Figure 40:
Full External Mode: Invalid Control Timing

#	Invalid Control Timing	Sensor Response
FE_i0	REQ_EXP during GLOB	Will disrupt the GLOB execution, causing the READOUT that naturally follows the GLOB phase to contain corrupted data.
FE_i1	REQ_FRAME during GLOB	Will initiate a new GLOB, followed by READOUT. Image data in this READOUT will be corrupt.
FE_i2	2 consecutive REQ_FRAME, without REQ_EXP in between	Second REQ_FRAME will initiate GLOB followed by READOUT. Since there has not been EXPOSURE, the image data in the second frame will be corrupt.
FE_i3	REQ_FRAME when sensor is IDLE	Same as above: READOUT without EXPOSURE results in corrupted image.

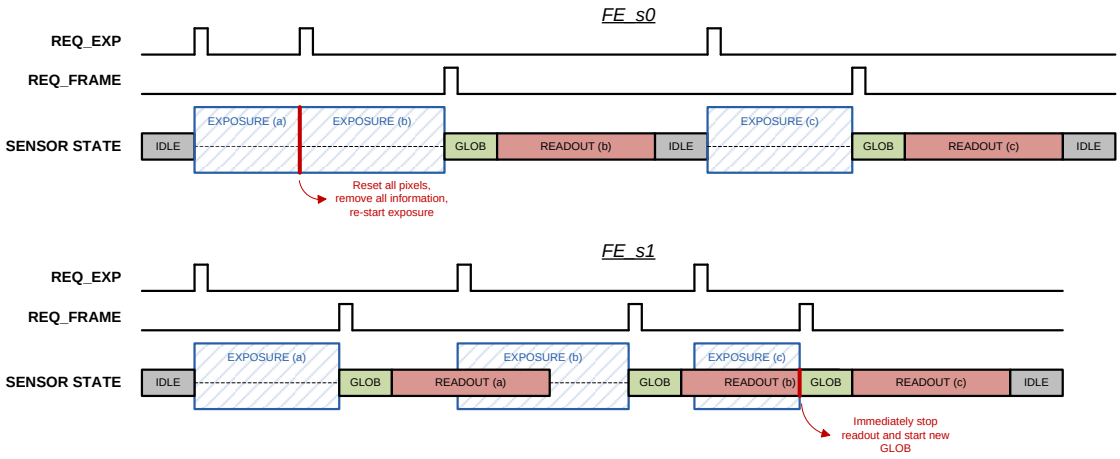
The table below lists some special cases that are not part of the table above and are therefore not illegal (though they each do have some consequences)

Figure 41:
Full External Mode: Special Control Timing

#	Special Control Timing	Sensor Response
FE_s0	REQ_EXP during EXPOSURE	Will initiate a new EXPOSURE, erasing all previously integrated information. The next REQ_FRAME will initiate a GLOB+READOUT that will contain image data of only the second EXPOSURE.
FE_s1	REQ_FRAME during READOUT	Will immediately interrupt the active READOUT to start a new GLOB, followed by a new READOUT. The image information of the first READOUT which had not been read will be forever lost. The new READOUT will be complete and correct (if not violating FE_i2, Figure 40).

The figure below shows an example of the cases listed in Figure 41.

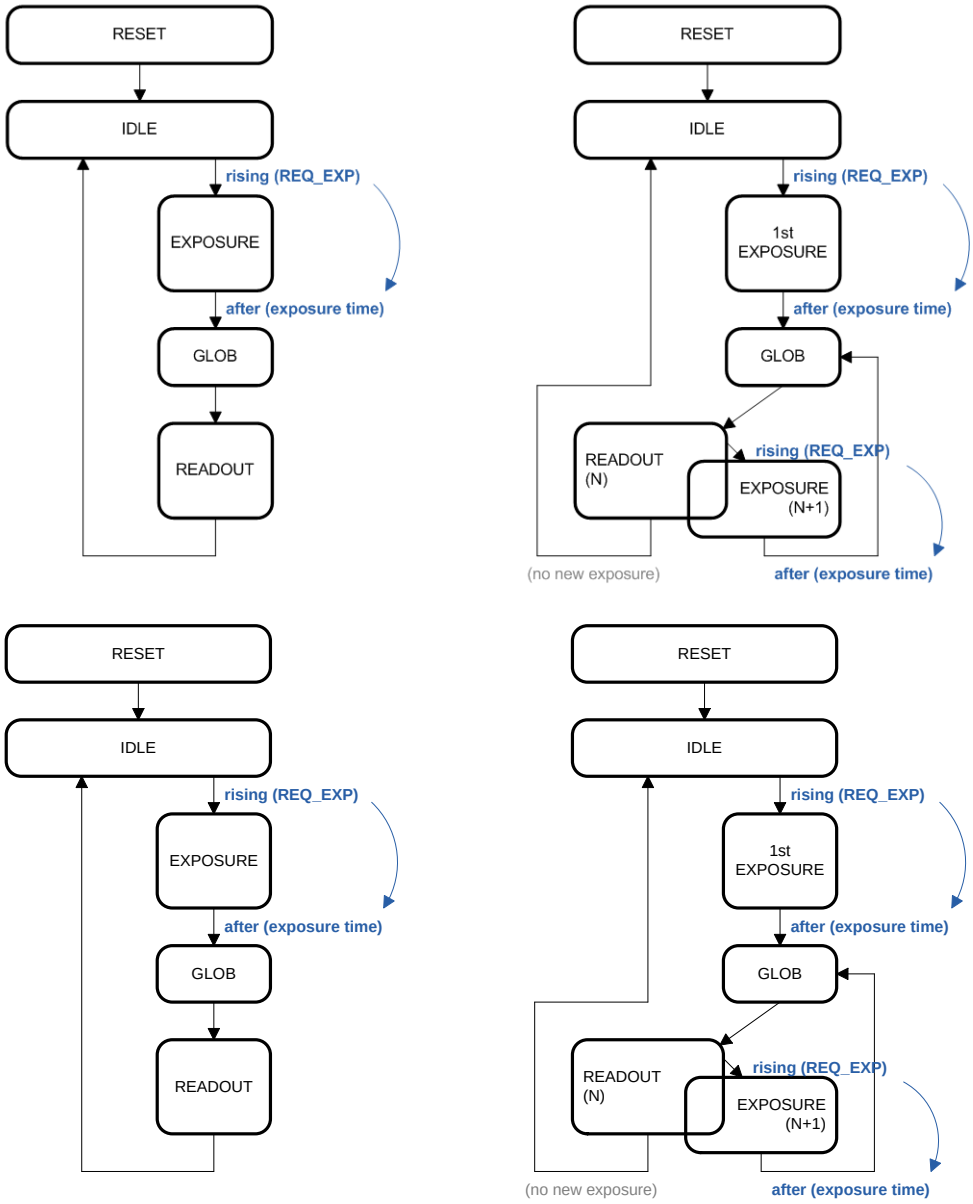
Figure 42 :
Timing Diagram: Special Control Timing in Full External Mode



Control Mode 1: Programmed External

This control mode is quite similar to the *Full External* mode, with the exception that the transition from EXPOSURE to GLOB state is not triggered by a pulse on REQ_FRAME sensor input. Instead the sensor ends the EXPOSURE period and moves to GLOB after a programmable time, set by register upload. This behavior is illustrated in the figure below.

Figure 43 :
State Diagram: Programmed External Mode



Expanding this to a timing diagram gives similar timings to the ones shown in Figure 39 with REQ_FRAME continuously low.

Since this mode is so similar to the *Full External* mode, also the lists of invalid and special control timing are quite similar.

Figure 44:
Programmed External Mode: Invalid and Special Control Timing

#	Invalid Control Timing	Sensor Response
PE_i0	REQ_EXP during GLOB	Same response as FE_i0
PE_i1	EXPOSURE time expires during GLOB	Same response as FE_i1

#	Special Control Timing	Sensor Response
PE_s0	REQ_EXP during EXPOSURE	Same response as FE_s0
PE_s1	EXPOSURE time expires during READOUT	Same response as FE_s1
PE_s2	Any pulse on REQ_FRAME	Will be ignored

Control Mode 2: Triggered Internal

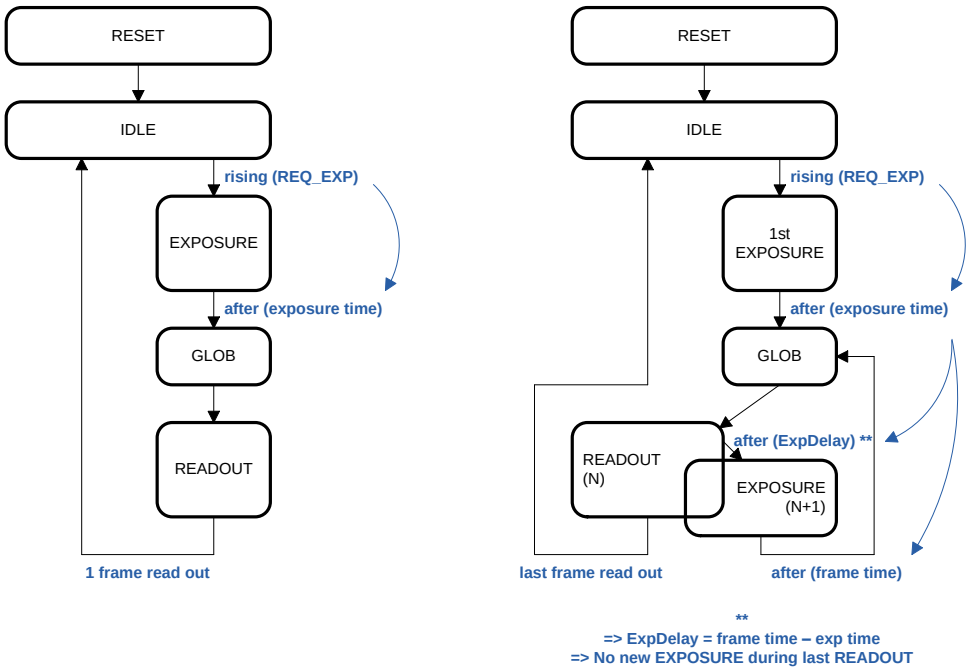
Both external control modes have in common that every external request results in exactly one sensor response:

- In Full External mode:
  - Each REQ_EXP initiates 1 EXPOSURE period
  - Each REQ_FRAME initiates 1 GLOB period, followed by READOUT
- In Programmed External mode:
  - Each REQ_EXP initiates the complete readout of 1 frame (EXPOSURE, GLOB and READOUT).

This means that in those two modes, the frame rate is fully controlled externally by timing the requests.

In the *Triggered Internal* mode, a single request is followed by a programmable number of frames, at a frame rate also set by register upload.

Figure 45 :
State Diagram: Triggered Internal Mode



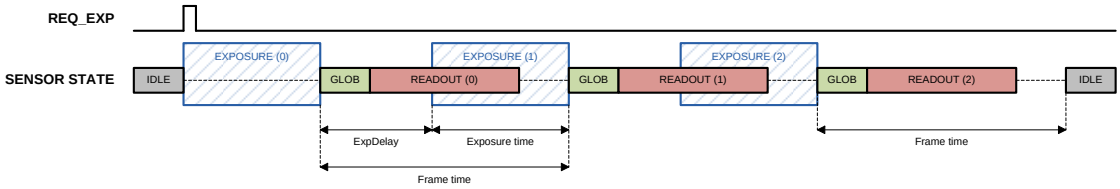
When exiting IDLE mode, the behavior is identical to Programmed External mode: a rising edge on REQ_EXP will initiate the EXPOSURE state, which ends after a register defined exposure time. When the exposure time expires, a GLOB state is started, followed by READOUT.

The behavior during the READOUT phase depends on the number of frames that were requested (also set by register) and the amount of frames that have already been read during the active sequence:

- Last READOUT of requested sequence:
  - Finish active READOUT and move back to IDLE state
- All other READOUT:
  - Restart EXPOSURE for the next frame. EXPOSURE is started at the correct moment to make it finish exactly 'frame time' later than the GLOB period was started.
  - The end of this EXPOSURE will initiate a new GLOB phase.
  - Because a GLOB period immediately follows the EXPOSURE period, there will be exactly 'frame time' delay between two consecutive frames.

An example (with 3 frames requested) is shown in the figure below.

Figure 46 :
Timing Diagram: Triggered Internal Mode



In the example, the programmed 'frame time' is longer than the sum of GLOB length and READOUT length. This situation is allowed and provides an easy mechanism to fine-tune frame rate.

In the most extreme case, the programmed frame time exactly matches the minimum length of the GLOB and READOUT phases together. This will start a new GLOB period as soon as the previous READOUT is finished, which results in the maximum frame rate for given GLOB and READOUT settings.

Because this mode is internally controlled based on register settings, there are no invalid control timing conditions. Invalid register settings do exist (for example: frame time shorter than GLOB+READOUT length), but these are specified in the relevant sections describing those registers later in this document.

The table below lists the special timing conditions of this mode.

Figure 47:
Triggered Internal Mode: Special Control Timing

#	Special Control Timing	Sensor Response
TI_s0	REQ_EXP ***before*** last READOUT of sequence has started	Will do nothing else than increase the sequence length (add the number of frames of the new request to the total length of this sequence, with a maximum total of 255 frames).
TI_s1	REQ_EXP ***after*** last READOUT of sequence has started	Will initiate a new 'first' EXPOSURE, followed by a complete new sequence. Depending on the timing of the new request, the frame rate may be temporally change. See below.
TI_s2	Any pulse on REQ_FRAME	Will be ignored

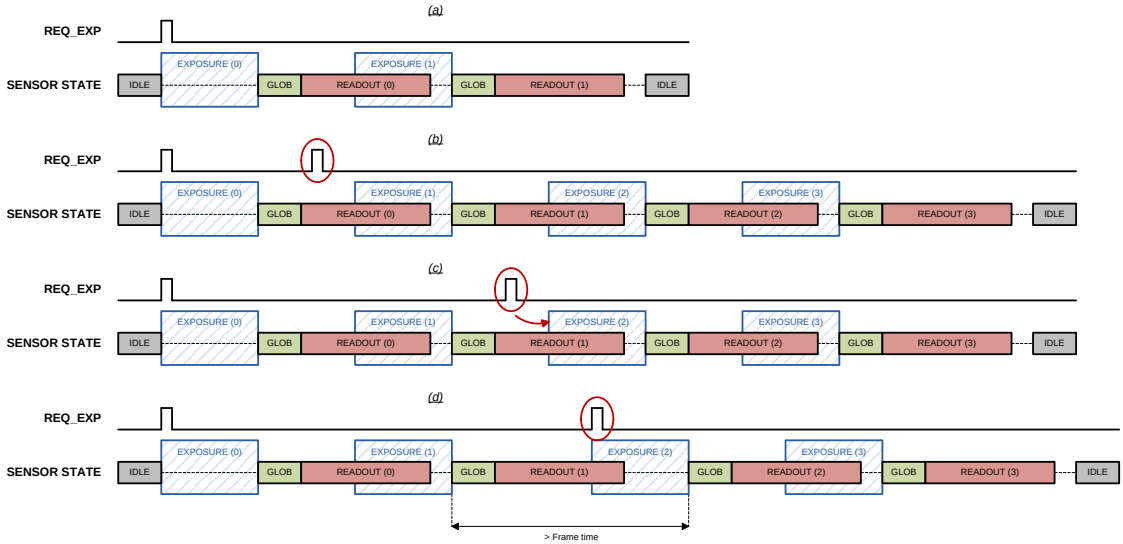
The behavior in case of TI_s1 depends on the relation between (1) the programmed exposure time of the new request and (2) the time remaining to complete the active frame (see last 'Frame time' in Figure 46).

- If (1) < (2):
  - The start of the new EXPOSURE will be delayed.
  - It will be started at the correct moment so its end will coincide with the end of the active frame.
  - The frame rate will not change: the first GLOB of the new sequence will be exactly 'frame time' after the last GLOB of the active sequence.

- If (1) > (2)
  - The new EXPOSURE will start immediately.
  - Because (1) is larger than (2), this EXPOSURE will end after the last frame would have finished.
  - This causes a temporary drop in frame rate.

The figure below shows the following cases (in all cases, the requested sequence is 2 frames long):

Figure 48 :
Timing Diagram: Special Control Timing in Triggered Internal Mode



(a) Normal timing → Capture 2 frames and go back to idle when done
(b) TI_s0 → New request before last frame is active; extend sequence length to 4
(c) TI_s1, (1) < (2) → New EXPOSURE delayed to guarantee programmed frame rate
(d) TI_s1, (1) > (2) → Temporary frame rate decrease to guarantee complete exposure time

Programmed External vs Triggered Internal

The attentive reader may have noticed that the *Triggered Internal* mode with a sequence length of 1 is quite similar to the *Programmed External* mode. This is mainly true, yet both differ in the way they handle new REQ_EXP requests if the sensor is **not IDLE**.

Figure 49:
Special Control Timing: PE and TI Comparison

#	Special Timing	Programmed External Response	Triggered Internal Response
PE_i0	REQ_EXP during GLOB	Will corrupt next frame	= TI_s0 Sequence length extended by 1 frame with every new request

#	Special Timing	Programmed External Response	Triggered Internal Response
PE_s0	REQ_EXP during EXPOSURE	Will stop EXPOSURE and start new one	Impossible situation: EXPOSURE by construction never finishes during READOUT or GLOB
PE_i1	EXPOSURE time expires during GLOB	Will corrupt next frame	
PE_s1	EXPOSURE time expires during READOUT	Will stop READOUT and start new GLOB	
TI_s0	REQ_EXP ***before*** last READOUT of sequence has started	= PE_i0 or PE_s0	Extend sequence length
TI_s1	REQ_EXP ***after*** last READOUT of sequence has started	Will start new exposure immediately, resulting in default behavior or PE_s1	Will start new exposure (directly or after delay, see Figure 48)

In summary:

- *Triggered Internal* is the more forgiving mode. It adjusts the actual timing and scheduling of events as needed to always yield complete and correct images.
- *Programmed External* mode (and by extend also *Full External* mode) however directly responds to external requests at the cost of possibly corrupting or interrupting images but no missing higher priority exposures.

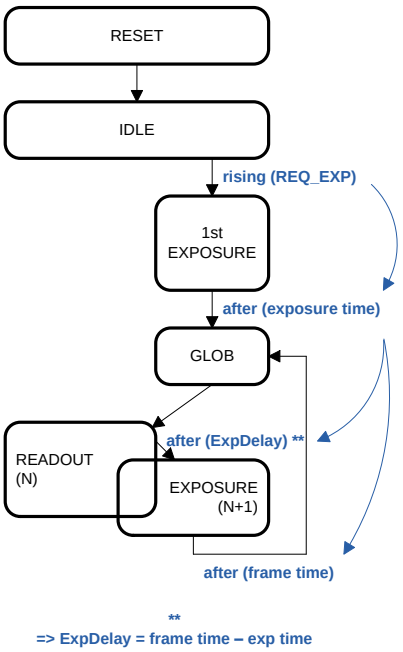
Control Mode 3: Streaming

Streaming mode is nothing else than *Triggered Internal* mode with an infinite sequence length.

After starting the *Streaming* mode with a rising edge on REQ_EXP, it will keep on generating a continuous stream of frames forever until stopped explicitly (via sensor reset or HALT command; see section 7.2.9). As in Triggered Internal mode, the entire frame configuration is done by register upload.

Next figure shows the state diagram of the *Streaming* mode.

Figure 50:
State Diagram: Streaming Mode



Because of the nature of the streaming mode, there is no such thing as invalid or special control timing. Once started, it will be forever looping and all further REQ_EXP and REQ_FRAME pulses are ignored.

7.2.9 Software Commands

Figure 51:
Software Command Registers

Reg. Name	Bank	Addr	Bits
CMD_REGS.CMD_RST_SOFT_N	0	3	[0]
CMD_REGS.CMD_REQ_EXP	0	3	[1]
CMD_REGS.CMD_REQ_FRAME	0	3	[2]
CMD_REGS.CMD_HALT_BLOCK	0	3	[3]
CMD_REGS.CMD_HALT_NBLOCK	0	3	[4]

The register bits **CMD_REQ_EXP** and **CMD_REQ_FRAME** are equivalent to their sensor input counterparts REQ_EXP and REQ_FRAME. The sensor REQ_EXP and REQ_FRAME inputs can therefore be tied low to use the register uploads for frame timing control. Just like with the sensor inputs, the rising edges of the register bits are considered.

By using the three registers defined above, the sensor can in theory be controlled with just the SPI interface plus 2 timing inputs (RST_N and CLK_IN) at the cost of a slightly reduced timing accuracy (because the registers are loaded via the SPI interface).

The two HALT commands can be used to stop any active sensor operation and return the sensor to the IDLE state, waiting for new requests. The difference between the two is:

- **CMD_HALT_BLOCK**: When asserted, the active READOUT is finished before moving to IDLE state
- **CMD_HALT_NBLOCK**: when asserted, all operation is immediately stopped and the sensor directly moves to IDLE state.

The HALT commands are a good way to get the sensor out of the *Streaming* control mode without asserting any reset.

7.3 Sensor Readout Format

7.3.1 Sub-LVDS Outputs

The CMV50000 has sub-LVDS (low voltage differential signaling) outputs to transport the image data to the surrounding system. In total, the sensor has 26 sub-LVDS output pairs (2 pins for each sub-LVDS channel):

- 22 Data channels
- 2 OB data channels
- 1 Control channel
- 1 Clock channel

This means that a total of 52 pins of the CMV50000 are used for the sub-LVDS outputs. See the pin list for the exact pin numbers of the sub-LVDS outputs.

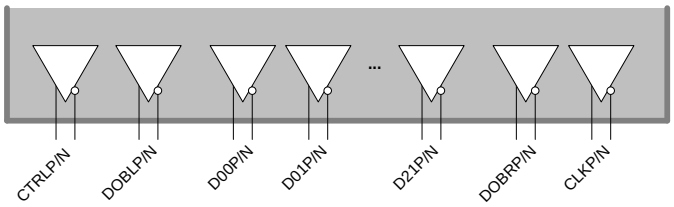
The data channels are used to transfer the pixel data from the sensor to the receiver in the surrounding system.

The output clock channel transports a clock, synchronous to the data on the other sub-LVDS channels. This clock should be used at the receiving end to sample the data. This clock is a DDR clock which means that the frequency will be half of the output data rate. When 830 Mbit/s output data rate is used, the sub-LVDS output clock will be 415MHz.

The data on the control channel contains status information on the validity of the data on the data channels. Information on the control channel is grouped in 12-bit words that are transferred synchronous to the data channels.

The figure below shows the data output interface.

Figure 52 :
Data Output Interface



Each pair of differential output pins transports data on one sub-LVDS channel.

For easier reading and writing, the channels will be called CTR_OUT, OBL_OUT, DATAx_OUT, OBR_OUT and CLK_OUT in the remainder of the document. The output channels have the following functionality:

Figure 53:
Output Channels Functionality

Name	Function
CLK_OUT	Can be used as sampling clock.
CTR_OUT	Serially transmit status word. (Capturing sensor status in various status bits)
DATAx_OUT	Serially transmit pixel data. (every channel transmits the data of 1 pixel, so up to 22 pixels are transmitted at the same time from the sensor)
OBL_OUT	Serially transmit pixel data of pixels in left-hand side OB columns
OBR_OUT	Serially transmit pixel data of pixels in right-hand side OB columns

At the output of the sensor, all channels are bit and word aligned with minimal skew. The phase of the sampling clock can be programmed with respect to the other channels as described in section 7.3.2.

Using the OBx_OUT channels is optional, because by default the row OB corrections (using the OB columns) are done on-chip.

Reading out a frame is done row-by-row. The pixels of a row are evenly distributed along all enabled outputs. Almost any number between 1 and 22 DATAx_OUT channels can be used, depending on the horizontal multiplexing settings (see section 7.6.4). DATA0_OUT is always active. If more than 1 channel is used, additional channels are enabled from left to right.

Two completely different readout formats are supported. The next sections provide an introduction to both of them.

7.3.2 Pixel-Based Readout Format

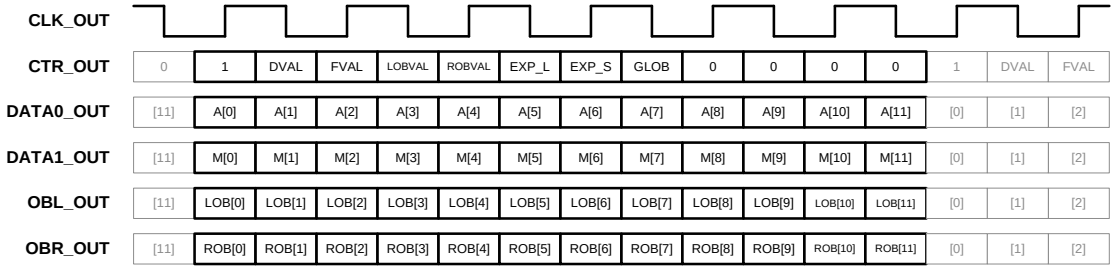
Similar to other products in the CMV family, the data readout can be organized in pixels aligned using a side-band control channel. This mode is also referred to as CMV-like readout.

Low-Level Pixel Timing

- Data is transferred serially over each channel, one complete word at a time.
- Data is transferred LSB first.
- All channels are word aligned (LSB of all channels sent during same CLK_OUT cycle).

This results in the timing diagram in the figure below. In the figure, the output clock is set to 90° phase, which is the default case.

Figure 54 :
Low-Level Pixel Timing



Control Channel

Like all other data channels, the CTR_OUT channel transmits its data word-based. A word being transmitted on the CTR channel consists of a number of bits, each reflecting the status of a certain aspect of the sensor behavior. The table below lists the function of each bit.

Figure 55:
Control Word

#	Name	Function
[0]	SYNC	Always '1'
[1]	DVAL	High when there is valid pixel data on DATAx_OUT. (Stays high for entire row of valid data)
[2]	FVAL	Goes high together with first DVAL of frame. Goes low together with last DVAL of frame. (Frames valid frame)
[3]	LOBVAL	High when there is valid OB pixel data on OBL_OUT
[4]	ROBVAL	High when there is valid OB pixel data on OBR_OUT
[5]	EXP_L	High when exposure group 'L' is integrating light
[6]	EXP_S	High when exposure group 'S' is integrating light

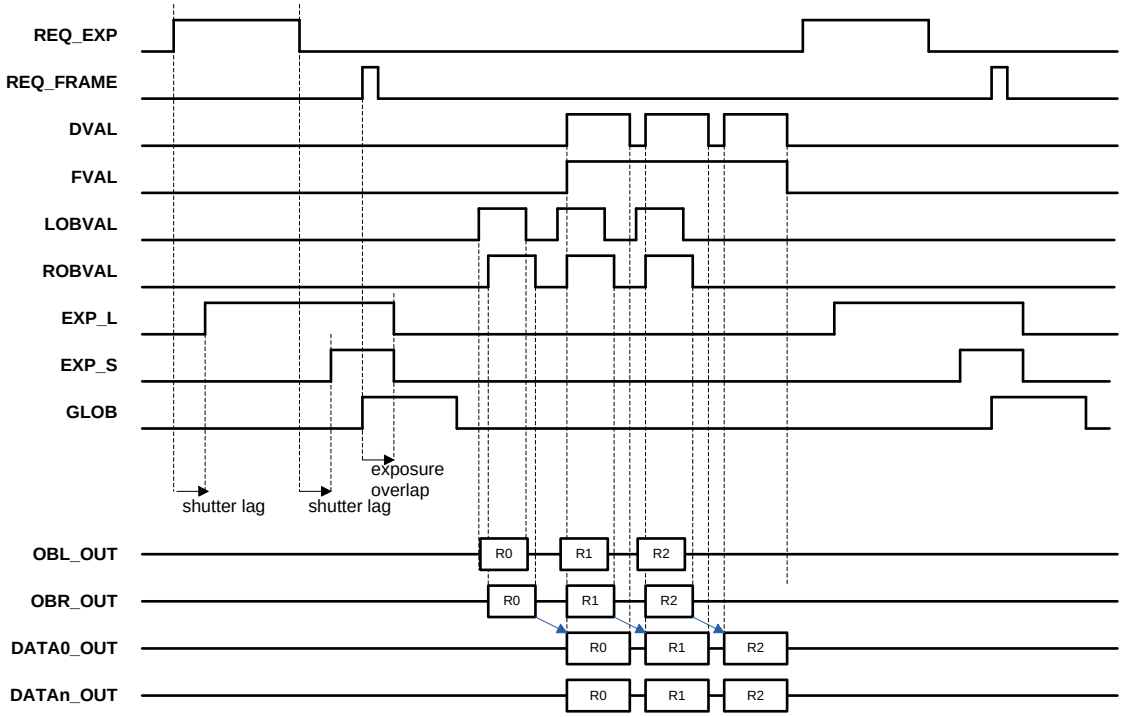
#	Name	Function
[7]	GLOB	High when sensor is in GLOB state
[8:13]	UNUSED	Always '0'

Figure 54 illustrates how the control word is transferred in line with pixel data. At the controller side, the data on CTR_OUT should be de-serialized like any other data channel. In the parallel domain, the various bits of the word can be used to extract status information on the sensor.

The figure below shows the timing of the various bits of the control word in an example frame. The timing of the bits is shown in the parallel domain. Some remarks concerning the figure:

- Sensor is in Full External control mode
- Dual exposure time is active (EXP_L is different from EXP_S)
- The frame size (y-window settings) is 3 rows.

Figure 56 :
CTR_OUT Channel Bits Timing



Some notes concerning the figure:

- EXP_L and EXP_S indicate the actual exposure time (so taking shutter lag and exposure overlap into account)
- The READOUT phase of the sensor (as used in section 7.2.7) is more than only FVAL. There certainly is some overhead time between the end of GLOB and the start of FVAL.

- Two DVAL periods are separated by an overhead time (OT). The length of this overhead time depends on the channel multiplexing and row time settings, but will be at least 1 word.
- The OB data of a row of pixels appears on OBx_OUT one row time before the valid pixel data of the same row appears on DATAx_OUT. This allows external grabbing and evaluation of the OB data before the pixels of the same row are being read. This way, corrections can be done without the need for an additional row buffer.

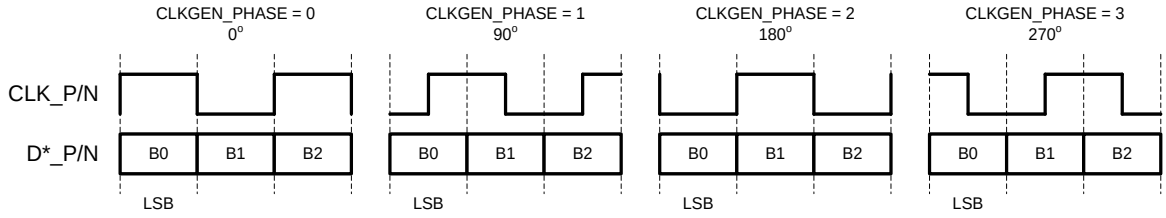
Output Clock Phase

Figure 57:
Output Clock Phase Register

Reg. Name	B	Addr	Bits	Def.	Description
CLKGEN_CFG. CLKGEN_PHASE	1	6	[2:1]	1	0: 0° 1: 90° 2: 180° 3: 270°

The sensor has an output clock channel (CLK_P/N) that is running synchronous to the output data. This clock can be used to sample the data at the receiver side. The phase of this clock (with respect to the data) can be programmed with **CLKGEN_CFG.CLKGEN_PHASE** as shown in the figure below depending on the receiver needs.

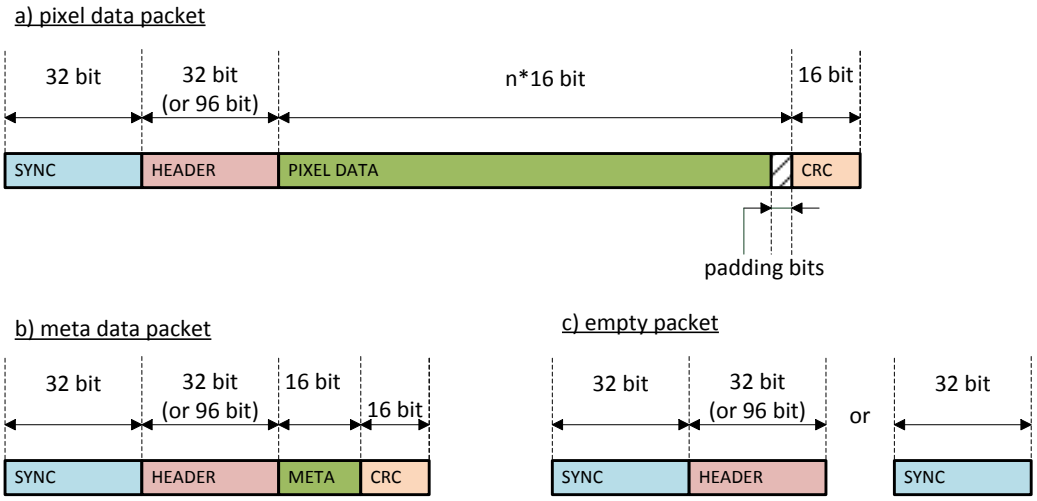
Figure 58 :
Output Clock: Phase Programmability



7.3.3 Packet-Based Readout Format

The data on DATAx_OUT, OBx_OUT and CTR_OUT can be re-formatted in byte-aligned packets. Three different packet types are used, as illustrated in Figure 59.

Figure 59 :
Packet Types



Data packets generally consist of:

- SYNC: synchronization code
- HEADER: information on the data that will follow
- PAYLOAD: the actual pixel or meta data
- Optional padding bits to keep 16-bit alignment
- CRC: checksum on the payload to detect bit errors

Every channel continuously sends packets. The CTR_OUT channel only sends meta-data packets. DATAx_OUT and OBx_OUT channels send pixel data packets during sensor READOUT state and empty packets during GLOB, EXPOSURE or IDLE states. The sensor may also insert empty packets in the middle of a frame readout, for example in multiplexing scenarios.

The packet header of an empty packet is optional (controlled via register upload), since it doesn't contain any information.

The possible padding bits in the pixel data are random.

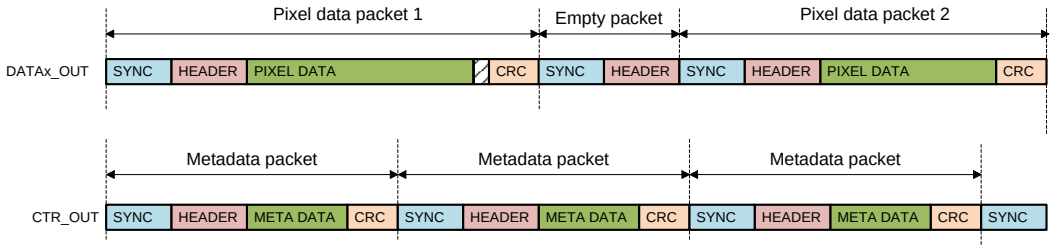
Low-Level Packet Timing

- The data output interface operates in 8-bit mode.
- Data is transferred serially over each channel in packets.
- Every packet field is transferred LSB/lsb first.
- Channels are not necessarily word aligned (LSB of different channels may be sent during different CLK_OUT cycle).
- A fixed serial sequence synchronizes the start of a packet.

Data is always sent in (even) byte multiples. The start of a new packet is given by a synchronization code, which forms a fixed known sequence on the serial output.

All packets start with an in-line sync word. Word-alignment can be fine-tuned at every packet start for every output channel. Due to the difference in packet lengths, not every channel will have its packet start aligned. So every channel needs its own packet/word-alignment. The CLK_OUT channel is still used as bit-clock reference as in CMV-like readout format.

Figure 60 :
Low-Level Packet Timing



SYNC Code

The SYNC code is a 4-byte long fixed sequence. The code is described in the table below (lsb first).

Figure 61:
SYNC Code Bits

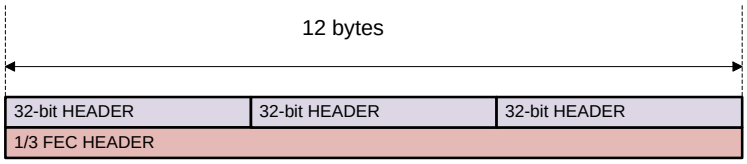
#	Value
[0]	Always '0'
[1]	Always '1'
[2]	Always '0'
[3]	Always '1'
[4:31]	Always '0'

The SYNC sequence is not unique and can occur elsewhere in the data stream. However, the header code contains information on packet length that allows making the distinction.

HEADER Code

The HEADER code is a 32-bit code that is optionally repeated 3 times (1/3 FEC protection). The repetition is not at bit or even byte level, but at 32-bit. This is illustrated in the figure below.

Figure 62 :
1/3 FEC Header



When the 1/3 FEC is disabled, the HEADER code will only be 4 bytes long.

The 32-bit header format is described in the table below. It is transmitted LSB/lsb first.

Figure 63:
HEADER Code

#	Nr of Bits	Name	Description/Coding
[1:0]	2	HeaderVersion	Always 0
[4:2]	3	PacketType	0 = Empty packet 2 = Visible Pixel packet 3 = Metadata packet 4 = OB Pixel packet (1, 5, 6 and 7 are reserved)
[12:5]	8	PacketNumber	Packet sequence number. Per line from left to right.
[14:13]	2	PixelDepth	(0 and 1 are reserved) 2 = 12 bit
[15]	1	FirstLineInFrame	'1' when the pixel data is for the first line in a frame.
[16]	1	LastLineInFrame	'1' when the pixel data is for the last line in a frame.
[18:17]	2	SequenceLine	Line number mod 4 (relative row address)
[19]	1	PayloadIsPadded	'1' when padding bits are added to the payload.
[31:20]	12	PayloadLength	Packet payload length in number of pixels. Not applicable to empty or metadata packet types, as these do not transmit any pixels.

Information

Only HeaderVersion and PacketType are useful for a metadata packet. Most of the other header fields have no meaning for a metadata packet and default to zero.

Meta-Data Code

Most of the validity information that is on CTR_OUT channel in CMV-like mode is included in the pixel data packet header. A few bits that do not directly relate to the pixel data validity can be signaled on CTR_OUT using meta-data packets.

The meta-data transmitted (LSB-first) on the control channel is organized according to Figure 64.

Figure 64:
CTR_OUT Channel Meta-Data Bits

#	Name	Function
[0]	EXP_L	High when pixel of dual exposure group 'L' are integrating
[1]	EXP_S	High when pixel of dual exposure group 'S' are integrating
[2]	GLOB	High when global sampling period is active
[3-15]	-	always 0

CRC Code

For all packets with a Payload, a CRC is calculated over the payload, including padding bits, using the CRC-16-CCITT polynomial (0x1021).

The CRC register is initialized to all ones (65535) at the start of each packet. Header and sync code are not included in the CRC. The highest order coefficient is transmitted least significant bit first.

7.4 Configuring the Sensor

This section provides detailed recipes for configuring the sensor in a certain operation mode. Refer to sections 7.5 and 7.6 for details on sensor exposure control and reading out images.

7.4.1 Operation Modes

The sensor supports different operation modes, listed per category in the table below, allowing for a large number of possible combinations.

Figure 65:
Operation Modes

Output Format Modes	
INT.1	Pixel-based Readout Format
INT.2	Packet-based Readout Format

Data Multiplexing Modes	
MUX.1	Use all 22 output channels
MUX.2	Multiplex image data to 11 output channels
MUX.3	Multiplex image data to 8 output channels
MUX.4	Multiplex image data to 6 output channels
MUX.5	Multiplex image data to 5 output channels
MUX.6	Multiplex image data to 4 output channels
MUX.7	Multiplex image data to 3 output channels
MUX.8	Multiplex image data to 2 output channels
MUX.9	Multiplex image data to 1 output channel

Sensor Control Modes	
SEN.1	Full External
SEN.2	Programmed External
SEN.3	Triggered Internal
SEN.4	Streaming
SEN.1	Full External
SEN.2	Programmed External
SEN.3	Triggered Internal
SEN.4	Streaming

Image Modes	
IMG.1	Full array readout
IMG.2.1	Color; sub-sampling in X and Y
IMG.2.2	Color; binning
IMG.3.1	Mono; sub-sampling in X and Y
IMG.3.2	Mono; binning

Gain Modes	
GAIN.1	Analog gain: ×1
GAIN.2	Analog gain: ×2
GAIN.3	Analog gain: ×4

OB Clamping Modes	
OBC.1	Optical black clamping ON
OBC.2	Optical black clamping OFF

7.4.2 Flow Chart

Using the flow chart below, all steps necessary to configure or reconfigure the sensor can be determined, as well as their correct and recommended order of execution.

Each step is elaborated in the next sections as a small recipe or procedure to follow. Where applicable, a reference to additional background information will be provided.

The configuration is split in a static and a dynamic part. The static part must be executed once after every power-up or upon a static mode change. The dynamic part must be executed once after every power-up and can then be executed (partially) when changing the operation mode on the fly. Subsequent steps cannot be skipped, e.g. GAIN mode can be changed without changing IMG mode, but not the other way around.

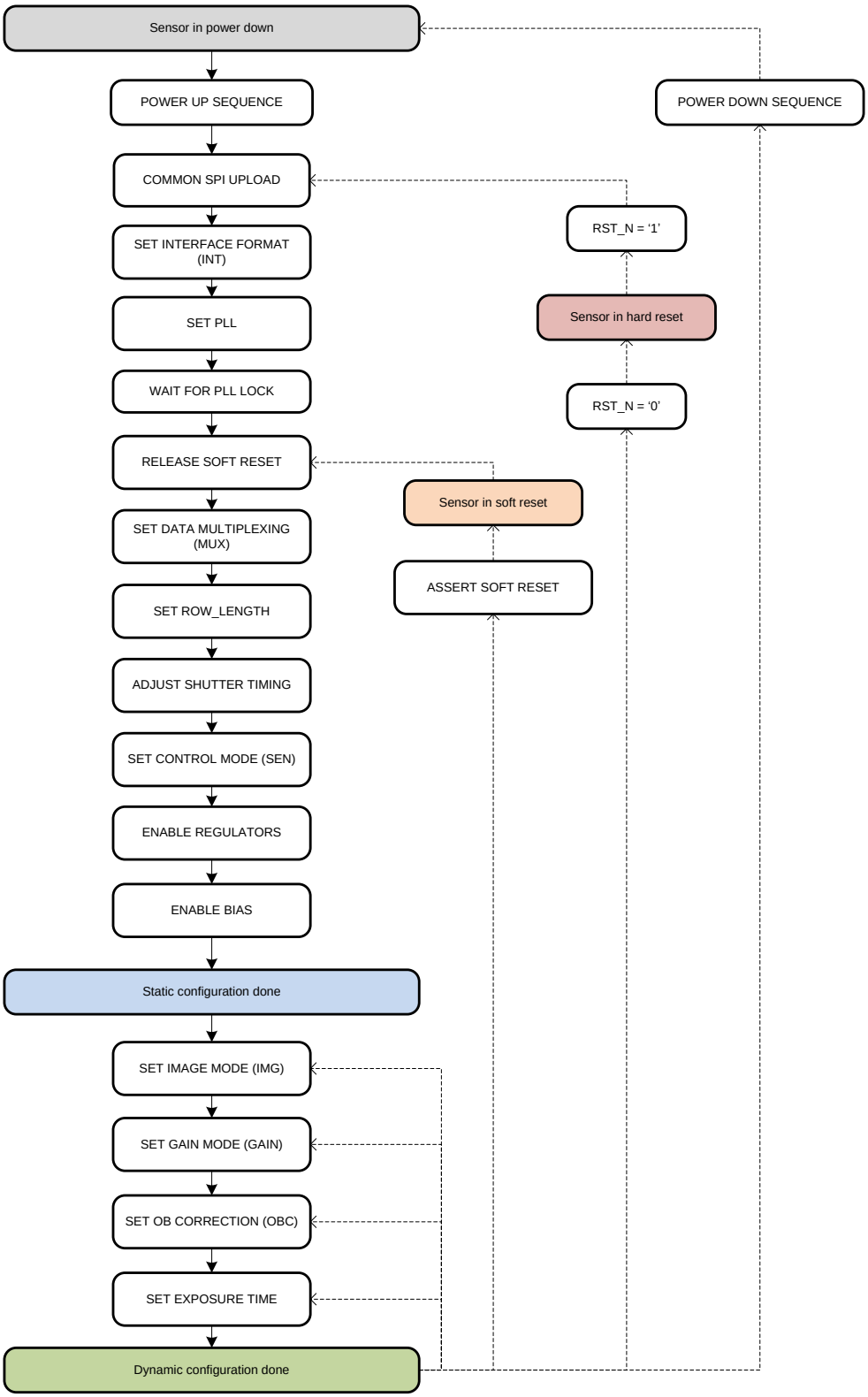
Information

Useful are the optional paths to return to either the soft reset state or the hard reset state, which can be taken to temporarily put the sensor in a lower consumption state without having to do a full power-down/power-up cycle.

Attention

Not following these recommendations can lead to the sensor being in an unknown state with unpredictable behavior.

Figure 66 :
Flow Chart



Power-Up Sequence

The power-up and reset release sequence is described in section 7.2.2.

Power-Down Sequence

The power-down and reset assert sequence is described in section 7.2.2.

Common SPI Upload

Independent of the sensor operation mode or use-case, these settings must be uploaded in the specified order. Each line is a single 8-bit SPI data write access. The bank selection uploads are not stated here but must be done when changing banks.

Figure 67:
Common SPI Upload Sequence

#	Bank	Address	Value (decimal)	#	Bank	Address	Value (decimal)
1	3	49	1	81	2	80	206
2	2	1	215	82	2	81	245
3	2	2	12	83	2	82	1
4	2	3	162	84	2	83	130
5	2	4	133	85	2	84	255
6	2	5	1	86	3	54	105
7	2	6	206	87	3	55	1
8	2	7	1	88	3	56	14
9	2	8	5	89	3	57	3
10	2	9	50	90	3	51	20
11	2	10	11	91	3	52	0
12	2	11	2	92	3	53	38
13	2	12	6	93	0	82	2
14	2	13	1	94	0	83	2
15	2	14	242	95	0	84	2
16	2	15	242	96	0	87	4
17	2	16	207	97	1	119	0
18	2	17	1	98	1	109	0
19	2	18	134	99	1	101	1
20	2	19	154	100	1	117	2
21	2	20	255	101	1	59	4
22	2	21	219	102	1	112	1
23	2	22	2	103	1	113	0

#	Bank	Address	Value (decimal)	#	Bank	Address	Value (decimal)
24	2	23	140	104	1	47	16
25	2	24	231	105	1	48	0
26	2	25	32	106	1	26	2
27	2	26	245	107	1	41	36
28	2	27	12	108	1	61	23
29	2	28	145	109	1	62	2
30	2	29	208	110	1	63	2
31	2	30	123	111	1	66	150
32	2	31	206	112	1	68	85
33	2	32	141	113	1	69	95
34	2	33	221	114	1	72	75
35	2	34	245	115	1	77	13
36	2	35	13	116	1	78	13
37	2	36	129	117	1	79	10
38	2	37	3	118	1	80	13
39	2	38	255	119	1	81	13
40	2	39	154	120	1	82	13
41	2	40	100	121	1	83	13
42	2	41	90	122	1	84	13
43	2	42	160	123	1	85	13
44	2	43	192	124	1	86	13
45	2	44	24	125	1	87	13
46	2	45	49	126	1	88	13
47	2	46	122	127	1	89	13
48	2	47	199	128	1	90	13
49	2	48	26	129	1	91	13
50	2	49	91	130	1	92	13
51	2	50	190	131	1	93	13
52	2	51	149	132	1	94	13
53	2	52	206	133	1	95	13
54	2	53	6	134	1	96	13
55	2	54	127	135	3	8	5
56	2	55	125	136	3	10	2
57	2	56	90	137	3	12	7
58	2	57	65	138	3	15	6
59	2	58	255	139	3	16	6
60	2	59	204	140	3	17	6
61	2	60	130	141	3	18	6

#	Bank	Address	Value (decimal)		#	Bank	Address	Value (decimal)
62	2	61	242		142	3	19	8
63	2	62	205		143	3	47	1
64	2	63	245		144	0	5	1
65	2	64	194		145	0	84	2
66	2	65	113		146	1	28	200
67	2	66	9		147	1	29	50
68	2	67	242		148	1	20	128
69	2	68	206		149	1	21	1
70	2	69	245		150	1	22	236
71	2	70	130		151	1	23	10
72	2	71	255		152	1	24	56
73	2	72	204		153	1	25	1
74	2	73	130		154	1	58	3
75	2	74	242		155	0	76	128
76	2	75	205		156	0	77	0
77	2	76	245		157	3	50	71
78	2	77	194		158	1	70	190
79	2	78	121		159	1	71	130
80	2	79	242					

Set Output Format

Next table lists the required register upload to set the sensor output format (see 7.3).

Figure 68:
Output Format Register

Register	Bank	Address	INT.1	INT.2
OUTP_FORMAT	0	6	0	1

Set PLL

Starting from the input clock frequency and the targeted output data rate, 4 parameters must be calculated to correctly configure the PLL. Then the PLL must be configured using the upload sequence below.

Figure 69:
Set PLL Sequence

#	Bank	Address	Value
#	Bank	Address	Value
1	0	106	0
2	0	110	0
3	0	114	0
4	0	107	pll1_pre_div (see calculation below)
5	0	109	pll1_clkout_sel (see calculation below)
6	0	108	pll1_ndiv (see calculation below)
7	0	112	pll2_ndiv (see calculation below)
8	0	114	1
9	0	106	1
10	0	110	1

The parameter pll1_pre_div depends only on the frequency of the sensor input clock CLK_IN (between 6 MHz and 96 MHz).

Figure 70:
CLK_IN Divider Selection

CLK_IN	pll1_pre_div
6 MHz – 12 MHz	0
12 MHz – 24 MHz	1
24 MHz – 48 MHz	2
48 MHz – 96 MHz	3

The parameter pll1_clkout_sel depends only on the targeted output data rate.

Figure 71:
Data Rate Selection

Target Output Data Rate	pll1_clkout_sel
460 – 830 Mbit/s	0
230 – 460 Mbit/s	1
120 – 230 Mbit/s	2

The parameter pll1_ndiv depends on the frequency of the sensor input clock CLK_IN as well as the desired output data rate.

Equation 1:

$$pll1\_ndiv = floor\left[\frac{2^{pll1\_pre\_div} * 2^{pll1\_clkout\_sel} * f(CLK\_ADC)}{f(CLK\_IN)}\right]$$

With f(CLK_ADC) (in MHz) corresponding to the target data rate (in Mbit/s), and the *floor* operation being a round down to an integer.

The parameter pll2_ndiv depends only on the frequency of the sensor input clock CLK_IN.

Equation 2:

$$pll2\_ndiv = floor\left[\frac{2^{pll1\_pre\_div} * 640}{f(CLK\_IN)}\right]$$

The resulting effective data rate can be calculated with the equation:

Equation 3:

$$effective\ data\ rate = pll1\_ndiv * \left(\frac{f(CLK\_IN)}{2^{pll1\_pre\_div} * 2^{pll1\_clkout\_sel}}\right)$$

Attention

Due to the flooring operation in calculating the parameters, the targeted data cannot be reached exactly for every possible input clock frequency (see example 3 below).

Figure 72:
PLL Settings Examples

Parameters	Example 1	Example 2	Example 3
f(CLK_IN)	20 MHz	96 MHz	6 MHz
Targeted data rate	830 Mbit/s	120 Mbit/s	415 Mbit/s
pll1_pre_div	1	3	0
pll1_clkout_sel	0	2	1
pll1_ndiv	83	40	138
pll2_ndiv	64	53	107
Effective data rate	830 Mbit/s	120 Mbit/s	414 Mbit/s

Wait for PLL Lock

As described in section7.2.3, a PLL lock time of maximum 200 µs needs to be respected.

The lock status of a PLL can be checked by polling the read-only **PLL_LOCK** register.

Figure 73:
PLL Lock Register

Register Name	Bank	Addr	Read Value
PLL_LOCK	0	115	0, 1 or 2: PLLs out of lock 3: PLLs locked

Alternatively, the lock status for each PLL can be monitored via the sensor output pin TDIGO1 using the register **DMUX1_SEL** as detailed in section 7.8.1.

Release Soft Reset

Once the PLLs are locked, the sensor can be released from soft reset and the main clock can be enabled, by applying the following register write sequence.

Figure 74:
Release Soft Reset Sequence

#	Bank	Address	Value (decimal)
1	3	49	1
2	0	3	1
3	3	49	0

Assert Soft Reset

To optionally return the sensor to the soft reset state, the following register uploads need to be applied.

Figure 75:
Assert Soft Reset Sequence

#	Bank	Address	Value (decimal)
1	0	3	0
2	3	49	1

Asserting the soft reset will not affect the PLL. Internal clock generation and distribution however are disabled by asserting the soft reset. So before you can start grabbing frames, the soft reset has to be released again.

Set Data Multiplexing

The data can be output on a reduced number of outputs, as described in section 7.6.4. The settings for the multiplexing modes are listed below.

Figure 76:
Data Multiplexing Options

Mode	NR_OUTP (bank 0, address 26)
MUX.1	22
MUX.2	11
MUX.3	8
MUX.4	6
MUX.5	5
MUX.6	4
MUX.7	3
MUX.8	2
MUX.9	1

Some additional registers need to be set, depending on the previously selected output interface.

Figure 77:
Output Format - Additional Registers

Bank	Address	Write Value
If pixel-based output format [INT.1]		
3	1	5
3	2	2
3	3	7
If packet-based output format [INT.2]		
3	1	1
3	2	7
3	3	20

Set Row_Length

The ‘row length’ parameter sets the row rate of the sensor. The required setting of this parameter is dependent on different sensor operation modes – which are known at this stage of the configuration procedure.

The equations below can be used to calculate the minimum setting for ROW_LENGTH needed to achieve a maximum frame rate.

Equation 4:

$$mult = ceiling\left[\frac{22}{NR\_OUTP}\right]$$

Figure 78:
ROW_LENGTH Calculation

Selected Output Format	NR_OUTP	ROW_LENGTH (bank 0, address 22-23)
Pixel-based [INT.1]	-	370 * mult
Packet-based [INT.2]	< 22	400 * mult
Packet-based [INT.2]	22	383

Ceiling must be interpreted as round up to the next integer. For example, for the packet-based readout mode with 5 output channels, mult = ceiling(22/5) = ceiling(4.4) = 5 and ROW_LENGTH should be set to 2000 or higher.

Adjust Shutter Timing

To keep the same pixel array timing independent of the PLL frequency, following parameters need to be adjusted.

Figure 79:
Shutter Timings Registers

Reg. Name	Bank	Address	Bits	Description
GRAN_GLOB	1	5	[7:0]	Use calculated value
TG_LENGTH	1	110-111	[13:0]	Use calculated value
SHUTTER_LAG	1	114-115	[13:0]	Use calculated value
NR_DUMMIES	1	46	[3:0]	Use calculated value

Use the following equations to calculate the required values:

Equation 5:

$$GRAN\_GLOB = floor\left\lfloor 69 * \frac{CLK\_ADC}{830} \right\rfloor$$

Equation 6:

$$TG\_LENGTH = GRAN\_GLOB * 17 + ROW\_LENGTH - ((GRAN\_GLOB * 17 + 1)\ mod\ ROW\_LENGTH)$$

Equation 7:

$$SHUTTER\_LAG = GRAN\_GLOB * 96$$

Equation 8:

$$NR\_DUMMIES\ = ceiling\left\lceil 17 * \frac{GRAN\_GLOB}{ROW\_LENGTH} \right\rceil + 1$$

CLK_ADC is the same as the PLL1 frequency, which nominally is 830MHz (at 830Mbit/s) and *mod* in the TG_LENGTH equation is the modulo operator (remainder after division).

Some example values are shown below for different data rates.

Figure 80:
Shutter Timings Examples

Reg. Name	830MHz	600MHz	415MHz
ROW_LENGTH	370	370	370
GRAN_GLOB	69	49	34
TG_LENGTH	1479	1109	739
SHUTTER_LAG	6624	4704	3264
NR_DUMMIES	5	4	3

Set Sensor Control Mode

Depending on the selected sensor control mode (see 7.4.1), the following SPI register settings must be written. Refer to section 7.2.8 for a detailed description of the control modes.

Figure 81:
Control Mode Register

Register	Bank	Address	SEN.1	SEN.2	SEN.3	SEN.4
CTRL_MODE	0	9	0	1	2	3

Enable Regulators

Next table lists the procedure to enable the on-chip regulators (see section 7.2.1). Both positive and negative regulators need to be enabled.

Figure 82:
Enable Regulators Sequence

#	Bank	Address	Value (decimal)
1	3	14	31
2	3	7	63
3	3	4	63
4	3	5	42
5	Wait ≥ 10ms (Settling)		
6	3	6	21
7	Wait ≥ 10ms (Settling)		

Enable Bias

To enable the internal biases, the following upload sequence (8-bit register writes and settling times) has to be followed:

Figure 83:
Enable Biasing Sequence

#	Bank	Address	Value (decimal)
1	1	60	4
2	Wait ≥ 1ms (settling)		
3	1	74	255
4	1	75	255
5	1	76	15
6	Wait ≥ 1ms (settling)		
7	1	65	127
8	Wait ≥ 1ms (settling)		
9	1	60	15
10	1	59	5
11	1	116	1
12	3	48	1
13	3	21	1
14	3	22	1
15	3	35	255
16	3	36	255

#	Bank	Address	Value (decimal)
17	3	37	255
18	3	38	255
19	3	39	255
20	3	40	255
21	3	41	255
22	3	42	255
23	3	43	3
24	3	44	3
25	3	23	255
26	3	24	255
27	3	25	255
28	3	26	255
29	3	27	255
30	3	28	255
31	3	29	255
32	3	30	255
33	3	31	3
34	3	32	3
35	Wait ≥ 1ms (settling)		

Set Image Mode

Depending on the selected image mode (see 7.4.1), the following SPI register settings must be written. Refer to sections 7.5.3, 7.5.5 and 7.5.7 for details.

Figure 84:
Image Mode Registers

Register	Bank	Address	IMG.1 (full)	IMG.2.1 (color subs)	IMG2.2 (color bin)	IMG3.1 (mono subs)	IMG3.2 (mono bin)
COLOR_MODE	0	4	0	1	1	0	0
XSUBS	0	24	0	1	0	1	0
BIN_MODE	0	25	0	0	1	0	1
YWIN0	0	32	116	186	116	186	116
	0	33	215	203	215	203	215
	0	34	2	2	2	2	2

Set Gain Mode

Next table lists the required uploads per available gain mode (see 7.4.1). The settings are depending on the selected image mode.

Figure 85:
Analog Gain Register

Register	Bank	Address	Gain 1x [GAIN.1]	Gain 2x [GAIN.2]	Gain 4x [GAIN.3]
If (bin_mode == 0) [IMG.1 or IMG.x.1]					
GANA	0	78	255	243	241
If (bin_mode == 1) [IMG.x.2]					
GANA	0	78	223	211	209

The optical black (OB) pixels can have an offset compared with the effective pixels in dark conditions. Register EOB_OFFSET_FINE can compensate for this offset. Next table gives an overview of the settings to be written, depending on the selected analog gain mode.

Figure 86:
OB Offset Register

Register	Bank	Address	Gain 1x [GAIN.1]	Gain 2x [GAIN.2]	Gain 4x [GAIN.3]
EOB_OFFSET_FINE	1	38	152	59	138
EOB_OFFSET_FINE	1	39	128	129	130

Set OB Correction

Next table lists the required uploads per available OB clamping mode. Refer to section 7.7.1 for details.

Figure 87:
OB Bypass Registers

Register	Bank	Address	[OBC.1]	[OBC.2]
EOB_BYPASS	1	42	0	1
EOB_BYPASS_VALUE	1	43	N/A	Estimate of minimal black level @ ADC output

Set Exposure Time

Please refer to section 7.5.1.

7.5 Configuring Readout and Exposure

7.5.1 Frame Time and Exposure Time

Figure 88:
Frame and Exposure Time Registers

Reg. Name	Bank	Addr	Bits	Description
CTRL_MODE	0	9	[2:0]	Sets the sensor control mode
TIME_UNIT	0	10-11	[13:0]	Unit for frame and exposure time
FRAME_TIME	0	13-14	[15:0]	Sets the frame time in TIME_UNITs
EXP_TIME_L	0	16-17	[15:0]	Sets the exposure time in TIME_UNITs

The table below briefly recaps the exposure and frame time configurability in the various sensor control modes (see section 7.2.8).

Figure 89:
Sensor Control Modes

CTRL_MODE	Mode	Frame Time	Exposure Time
0	Full External	Via external timing	Via external timing
1	Programmed External	Via external timing	Via registers
2	Triggered Internal	Via registers	Via registers
3	Streaming Internal	Via registers	Via registers

Both Frame time and Exposure time are specified via registers in number of Time Units (TU). The length of a Time Unit (TU) is itself register-programmable in 'number of CLK_PIX cycles'. The period of CLK_PIX equals the length of one complete (pixel-based) word at the output interface.

The nominal CLK_PIX frequency in 12-bit mode is 69.167 MHz (≈415MHz / 6). By setting the **TIME_UNIT** register to 69, the time unit becomes ~1µs. The frame and exposure time, as set with the **FRAME_TIME** and **EXP_TIME_*** registers now represent multiples of 1µs. A CLK_ADC of 828MHz, yields a time unit (TU) of exactly 1µs.

As an example, the default settings for these registers give:

Figure 90:
Default Times

Register	Setting	Equation	Effective
TIME_UNIT	69	69/ f(CLK_PIX)	1.0024 µs
FRAME_TIME	50 000	50 000 TU	50 ms (=20 fps)

Register	Setting	Equation	Effective
EXP_TIME_L	10 000	10 000 TU	10 ms

Frame and exposure time registers are both 16-bit wide, which means that the exposure time can be specified with a resolution of up to 1/65536 with respect to the frame time.

A too short FRAME_TIME will lead to unpredictable behavior.

Dual Exposure HDR

Figure 91:
HDR Registers

Reg. Name	Bank	Addr	Bits	Description
DUAL_EXPOSURE	0	15	[0]	0: Dual Exposure off 1: Dual exposure on
DUAL_EXP_GROUPING	0	118	[0]	0: Default grouping (mono) 1: Paired grouping (color)
EXP_TIME_L	0	16-17	[15:0]	Exposure Time of group L
EXP_TIME_S	0	18-19	[15:0]	Exposure Time of group S

In dual exposure mode, one image can have 2 different exposure times, divided in 2 column groups. In the camera system this image can then translated to an HDR image containing both details in dark and bright areas.

In the effective pixel array, the pixels are split into two exposure groups. When **DUAL_EXP_GROUPING** is set low:

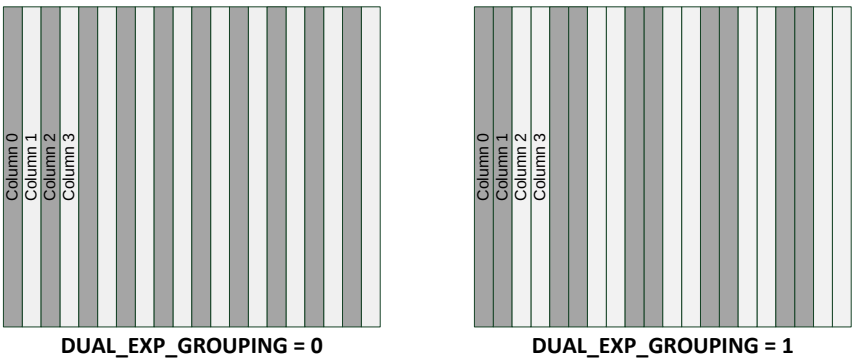
- **Exposure group S**: all pixels of columns 0+4i and 2+4i
- **Exposure group L**: all pixels of columns 1+4i and 3+4i

When **DUAL_EXP_GROUPING** is set high, the exposure groups use adjacent column pairs:

- **Exposure group S**: all pixels of columns 0+4i and 1+4i
- **Exposure group L**: all pixels of columns 2+4i and 3+4i

The latter should be used on color sensors, keeping the Bayer pattern complete.

Figure 92 :
Dual Exposure Grouping



When **DUAL_EXPOSURE** is set low, the exposure time of all pixels is set with **EXP_TIME_L**. When the register is set high, the exposure time of the two groups can be set independently with **EXP_TIME_S** and **EXP_TIME_L**.

Despite the naming of the L(ong) and S(hort) groups, it is allowed to have a shorter exposure time for the L group than for the S group.

Dual exposure mode is also supported in *Full External* control mode. In this control mode, the rising edge of REQ_EXP starts the exposure of the L group and the falling edge of REQ_EXP starts the exposure of S. If **DUAL_EXPOSURE** is low, both groups are started with the rising edge of REQ_EXP. This behavior is illustrated in Figure 56.

Frame Time Constraint

The frame time has a minimum value requirement to guarantee the entire frame readout and exposure is completed successfully before a new frame starts. This minimum requirement is captured in the equation:

Equation 9:

$$T_{frame} > T_{\text{glob}} + \max\{T_{\text{exp\_*}}, T_{read}\} \qquad with: T_{read} = T_{row} \times (T_{fval} + T_{dummy})$$

The components of this equation are:

Figure 93:
Minimum Frame Time Dependencies

Component	Description	Equation
T_{frame}	Frame time (= 1 / frame rate)	**FRAME_TIME** × TU
T_{glob}	Length GLOB state	See equation below (≈150µs)
T_{exp_L}	Exposure time, group L	**EXP_TIME_L** × TU

Component	Description	Equation
T_{exp_S}	Exposure time, group S (when **DUAL_EXPOSURE** = 1)	**EXP_TIME_S** × TU
T_{row}	Row length (= 1 / DVAL rate)	**ROW_LENGTH** × T_{CLK_PIX}
T_{fval}	Number of valid rows in frame	sum($\mathbf{YWIN}_{enabled}$.**SIZE**)
T_{dummy}	Number of dummy rows in frame	5 + (2 × **NR_DUMMIES)**

TU is time unit expressed in seconds, not to be confused with contents of register TIME_UNIT. The T_{read} component corresponds to the length of the READOUT state used in section 7.2.7.

In the external control modes, the same frame time equation should be respected to not interrupt the readout of active frames.

The T_{dummy} calculation is only valid in pipelined operation (starting a new exposure during read out). Five dummy rows are always inserted between GLOB and read out, the **NR_DUMMIES** dummy rows are inserted in the read out when a new exposure starts. The factor 2 is required for dual exposure mode.

If the above equation is not respected, the sensor behavior is undefined and no warning or error message is generated. It's the responsibility of the external controller to apply compliant register settings.

The equation above specifies a minimum frame time. On the upper side, the frame time may be set to any possible value within the limits of the relevant registers to fine-tune the frame rate.

The sensor has an absolute minimal exposure time of 100µs!

Maximum Frame Rate Calculation

If the frame time is set at its minimum and the exposure time is smaller than the read out time, the frame rate will be maximum and can be calculated with the following equation:

Equation 10:

$$Frame\ rate = \frac{1}{Frame\ time} = \frac{1}{T_{glob} + T_{read}}$$

With T_{glob} the overhead time between read outs, needed to close the global shutter and sample the pixel charges in the sampling capacitors.

Equation 11:

$$T_{glob} = \frac{150 * \mathrm{GRAN\_GLOB} * 12}{CLK\_ADC}$$

Data rate is the sub-LVDS output data rate. With the standard settings at the maximum data rate of 830Mbit/s, T_{glob} will be 149.64µs.

The read out time T_{read} consists of the time actual data is read out (FVAL is high) and some dummy rows. 5 of these dummy rows are between the end of GLOB and start of FVAL and the other are injected when the exposure of the next frame starts (defined by 2 * **NR_DUMMIES**). So the total read out time is:

Equation 12:

$$T_{(read)} = \boldsymbol{ROW\_LENGTH} * (\ \mathrm{sum}[\mathbf{YWIN}_{\mathrm{enabled}}.\boldsymbol{SIZE}] + \#\mathrm{dummy\_rows\_total}) * \frac{12}{CLK\_ADC}$$

With **ROW_LENGTH** being the value of register as set in section 7.4.2, sum(**YWIN$_{enabled}$.SIZE**), the sum of the rows in all enabled windows and #dummy_rows_total the total amount of dummy rows.

With the full array being read out, the total read out time is 370*(6004+15)*12/830 = 32.198ms.

The total frame time then becomes 32.35ms which is a maximum frame rate of 30.9fps in pixel-based output interface mode.

Sequence Length

Figure 94:
Number of Frames Register

Register Name	Bank	Addr	Bits	Description
NROF_FRAMES	0	12	[7:0]	See below

In triggered internal mode (**CTRL_MODE** = 2), every rising edge on REQ_EXP (through external pin or register) will initiate the capture of a sequence of frames. The value in the **NROF_FRAMES** register at the moment of the rising edge on REQ_EXP will determine the sequence length.

NROF_FRAMES may be set to any value between 1 and 255. In all other control modes, the register is ignored.

When a sequence is still active, a new rising edge on REQ_EXP will increment the remaining number of frames by the value set in **NROF_FRAMES**. The total number of remaining frames may not be higher than 255.

7.5.2 Row Length

Figure 95:
Row Length Register

Register Name	Bank	Addr	Bits	Description
ROW_LENGTH	0	22-23	[13:0]	Use equations below

The row length T_{row} defines the DVAL frequency during readout; it can be programmed in number of CLK_PIX cycles with the **ROW_LENGTH** register.

The row length has a minimum value because a number of parallel processes in the sensor need to be completed within one row time. The minimal row length depends on the number of outputs used and the read out mode (see equations in section 7.4.2).

The maximal row length value is only constrained by the 14 bits size of register.

Fine frame rate adjustments are done through external timing or with the **FRAME_TIME** register. Changing the row length only influences the DVAL frequency within a readout sequence. This can be useful when smaller or slower row buffers are used in the FPGA.

7.5.3 Windowing

The sensor supports multiple windows in the vertical direction to create regions of interest (ROI).

Row Addressing

As introduced in section 7.1.1, the sensor has buffer pixels rows above and below the effective pixels.

Every row in the array is paired with a physical row address. This row address is used to specify vertical ROI positions as described in next section.

Row addresses are assigned in ascending order starting from 0 for the row closest to the package pin row 1.

Figure 96:
Valid Row Addresses

Region	Address Range
Effective pixels	22 -> 6025
Bottom buffer rows	0 -> 21
Top buffer rows	6026 -> 6047

Vertical ROI Settings

The sensor allows up to 10 vertical windows to be concatenated in one single frame readout.

Each of these windows is enabled by setting their bit in **YWIN_ENA** to '1' (bit [0] = **YWIN0**, [1] = **YWIN1** …).

Each of these windows is configured with an **YWINi** register that defines the position, size and sub-sampling of the window. The 29 bits of each YWINi register span 4 physical SPI addresses. In the table below, only the start address is given (the upper address being 35+4×j).

Figure 97:
Vertical Windows Registers

Register Name	Bank	Addr	Bits	Description
YWIN_ENA	0	28-29	[9:0]	One bit per window 0: Disable 1: Enable
YWIN_BLACK	0	30	[9:0]	One bit per window to control the 'Electrical Black' mode 0: Disable 1: Enable
YWINi.SIZE	0	32+4×i	[12:0]	Number of read out rows in window i
YWINi.START	0	32+4×i	[25:13]	Physical address of first row in window i
YWINi.SUBS	0	32+4×i	[28:26]	Row subsampling in window i Ratio = $1/(2^{SUBS})$

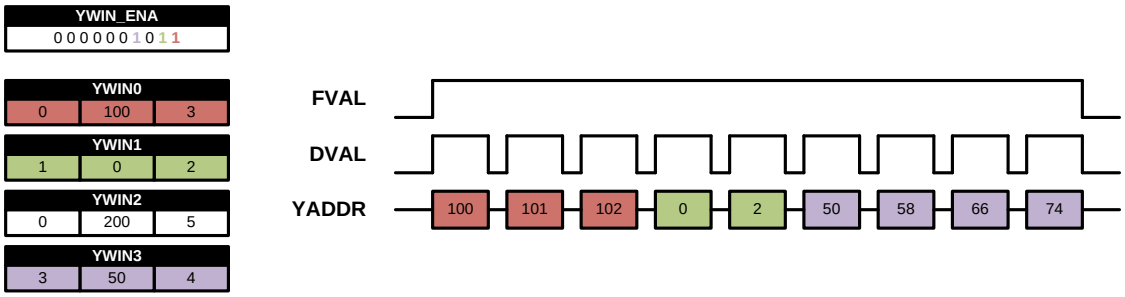
The **START** address of a window should comply with the values in Figure 96.

Only windows for which the respective bit in **YWIN_ENA** is set high are actually read out. This way multiple relevant Y-window specifications can be stored in the register map at the same time, enabling only the relevant ones.

All enabled windows are concatenated together (the first row of a new window is read immediately after the last row of the previous). The number of rows actually read in one frame (= # of DVAL within one FVAL) is the sum of the SIZE fields of all windows enabled by **YWIN_ENA**.

The figure below shows an example of using multiple windows.

Figure 98 :
Vertical ROI Example (monochrome)



Electrical Black Windows

With the **YWIN_BLACK** register, windows can be made 'electrical black' (setting a fixed voltage at the read out path instead of the pixel voltage). If the respective bit of the YWIN_BLACK register is set high (same mapping as YWIN_ENA), then all signal information in the window is suppressed. This results in a black window containing only readout FPN information. This feature could be used for column FPN correction.

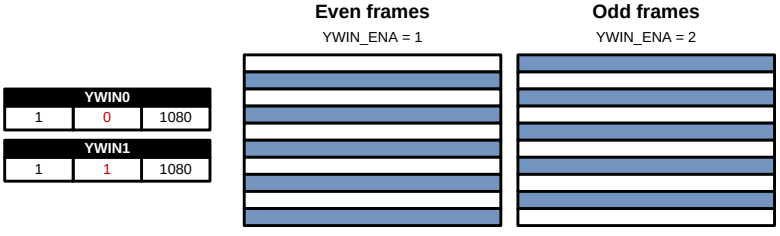
Window Overlap

Several vertical windows may overlap, although this is only useful in subsampling mode. If the same row is read multiple times within one frame, it will only contain valid data the first time (destructive read out).

One possibility is to create an interleaved readout scheme by:

1. Defining two vertical windows with identical size and SUBS set to 1
2. Giving START of the second window an offset so it starts at a row skipped by the sub sampling scheme of the first window
3. Alternating the respective YWIN_ENA bits between every frame.

Figure 99 :
Interleaved Readout



7.5.4 Vertical Subsampling

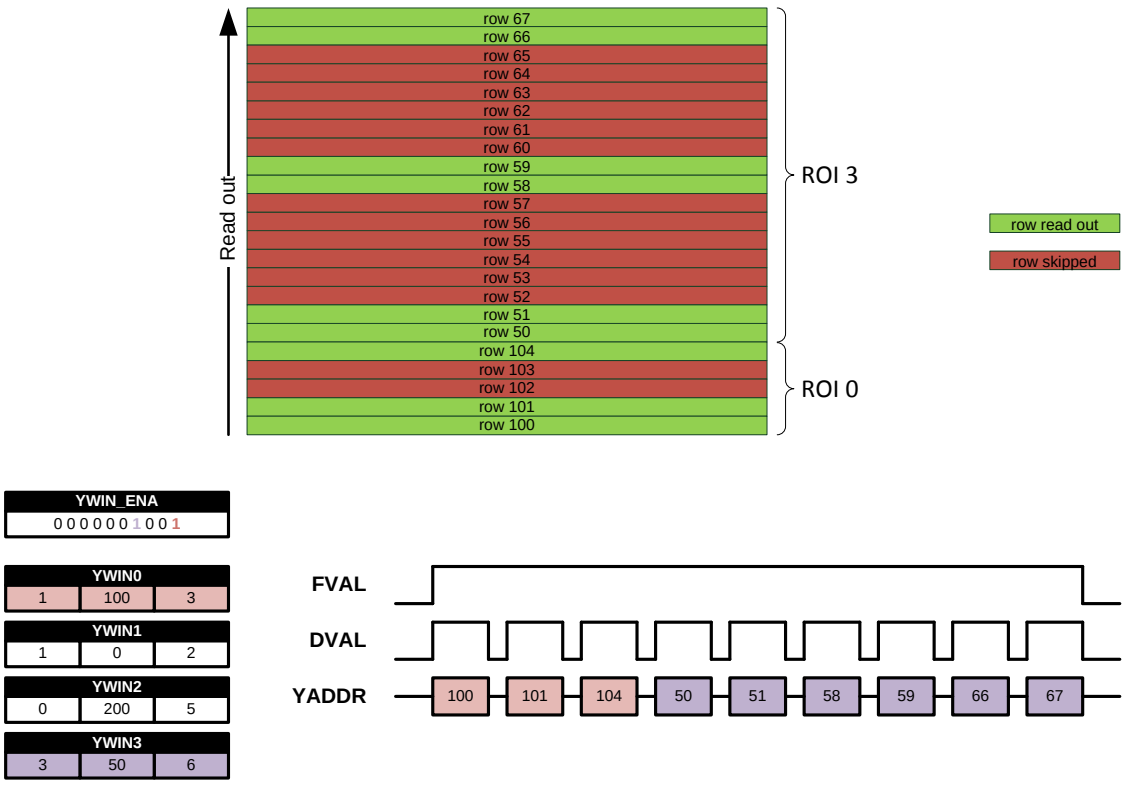
Figure 100:
Vertical Subsampling Registers

Register Name	Bank	Addr	Bits	Description
YWINi.SUBS	0	32+4×i	[28:26]	Row subsampling in window i
COLOR_MODE	0	4	[0]	0: Monochrome 1: Color

The sensor supports vertical subsampling (skipping rows), which can be set per window. The register **YWINi.SUBS** defines the ratio of the accessed rows in window *i* as 1 out of every 2^{SUBS} rows.

When **COLOR_MODE** register is set to 1, the rows are grouped per 2 to follow the Bayer pattern, as illustrated in Figure 101. It is recommended to only use even window sizes in color mode to keep the Bayer filter pattern intact. ROI0 in the example below demonstrates the effect of an odd window size.

Figure 101 :
Vertical ROI Example (color mode)



7.5.5 Horizontal Subsampling

Figure 102:
Horizontal Subsampling Registers

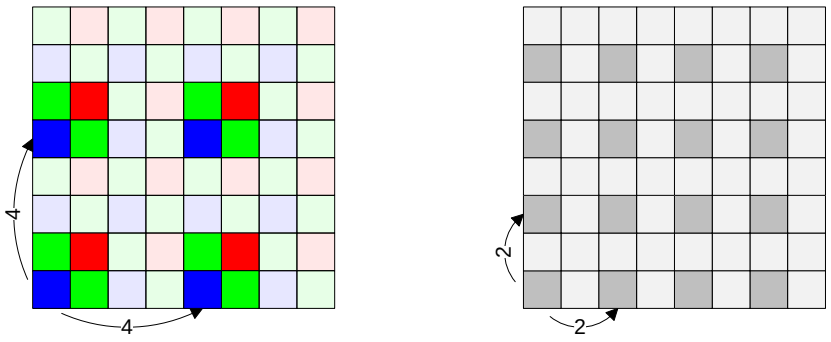
Register Name	Bank	Addr	Bits	Description
XSUBS	0	24	[1:0]	Horizontal subsampling setting Ratio = $1/(2^{XSUBS})$
COLOR_MODE	0	4	[0]	0: Mono 1: Color

The sensor supports horizontal subsampling, reducing the amount of pixels per line to $1:2^{XSUBS}$. This horizontal subsampling is applied to the whole array and not per ROI like vertical subsampling. Depending on COLOR_MODE, pixel grouping is done to preserve the Bayer pattern.

7.5.6 Subsampling Mode

Combining both horizontal and vertical subsampling will divide the resolution of the image by 2 in both dimensions as illustrated in Figure 103.

Figure 103 :
XY-Subsampling for Color and Mono Sensors



In color mode, only 4 out of 4x4 neighboring pixels are read out. The output data is still Bayer patterned.

In monochrome mode, only 1 out of 2x2 neighboring pixels is read out.

The amount of pixels per channel mentioned in Figure 111 scales accordingly when combining horizontal subsampling with the readout over a reduced number of data channels.

7.5.7 Binning Mode

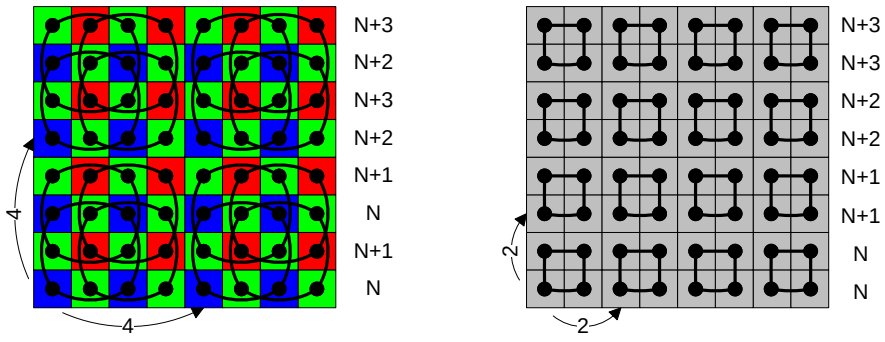
Figure 104:
Binning Mode Registers

Register Name	Bank	Addr	Bits	Description
BIN_MODE	0	25	[0]	0: Binning disabled 1: Binning enabled
COLOR_MODE	0	4	[0]	0: Mono 1: Color

The sensor supports both color and mono-chrome binning modes. In this mode, the values of 4 pixels will be summed, before the ADC. This will reduce the read out resolution with x4, but increases full well charge, dynamic range and SNR. In color mode, the Bayer pattern is preserved.

In binning mode, the summed value of 4 pixels is readout on the bottom-left position of each binning square. For every row N read at the output, two internal rows are accessed. As seen in Figure 105 in binning mode, the summed value of 4 pixels is readout on the bottom-left position of each binning square. This means only 1 out 2 columns will be read out.

Figure 105 :
Color and Monochrome Binning Modes



Setting **YWINi.SUBS** to 0 will output binned rows N, N+1, N+2 and N+3.

YWINi.SIZE refers to the number of physical rows in the array. The number of binned rows at the output will be half of this number.

Binning mode cannot be combined with horizontal subsampling. For correct operation of the sensor, XSUBS must be set to 0 when binning mode is enabled.

Binning mode may be combined with vertical subsampling.

E.g. setting YWINi.SUBS to 1 will readout binned rows N, N+1, N+4, N+5 … in color mode and binned rows N, N+2, N+4 … in mono-chrome mode.

In binning mode, the start of a pipelined exposure must occur during an internal even row access. Depending on the control mode a distinction must be made on how to achieve this.

In full external mode, the edges of REQ_EXP must be timed after the edge of REQ_FRAME in one of the discrete windows given by the equations below:

Equation 13:

$$t_{REQ\_EXP} - t_{REQ\_FRAME} > T_{PIX} \times ((2 \times n \times ROW\_LENGTH) + 2)$$

$$t_{REQ\_EXP} - t_{REQ\_FRAME} < T_{PIX} \times ((2 \times (n+1) \times ROW\_LENGTH) - 2)$$

For positive n and with $T_{PIX} = 1/f_{CLK\_PIX}$

Information

In dual exposure mode, the equations must be satisfied for both edges of REQ_EXP.

In programmed external mode, the time between two sequential REQ_EXP pulses must be timed according to the equations:

Equation 14:

$$t_{REQ\_EXP} - t_{REQ\_EXP\_prev} > T_{PIX} \times (TIME\_UNIT \times EXP\_TIME\_i + (2 \times n \times ROW\_LENGTH) + 2)$$

$$t_{REQ\_EXP} - t_{REQ\_EXP\_prev} < T_{PIX} \times (TIME\_UNIT \times EXP\_TIME\_i + (2 \times (n+1) \times ROW\_LENGTH) - 2)$$

For both EXP_TIME_L and EXP_TIME_S register settings (in dual exposure mode) and with $t_{REQ\_EXP\_prev}$ = the time of the previous REQ_EXP.

The EXP_TIME_*i* register settings are the ones at $t_{REQ\_EXP\_prev}$ in case they are updated between frames.

In Triggered internal and streaming modes, the EXP_TIME_*i* registers must be programmed to satisfy the equations:

Equation 15:

$$2 \times n \times ROW\_LENGTH < TIME\_UNIT \times (FRAME\_TIME - EXP\_TIME\_i) < 2 \times (n+1) \times ROW\_LENGTH$$

7.6 Configuring the Output Data Format

7.6.1 Main Output Format

Using the register **OUTP_FORMAT** one of the data readout formats introduced in section 7.3 can be selected.

Figure 106:
Output Format Register

Reg. Name	Bank	Addr	Bits	Description
OUTP_FORMAT	0	6	[1:0]	0: Pixel-based 1: Packet-based.

A soft reset is required after changing **OUTP_FORMAT**. Refer to the flow chart in section 7.4.2.

7.6.2 Word Alignment

Depending on the selected output format, word alignment must be done in a different way.

Pixel-Based Word Alignment

Figure 107:
Training Word Register

Reg. Name	Bank	Addr	Bits	Description
TRAINING_WORD	0	79-80	[13:0]	See below. Default value is 85

Whenever a data channel is not sending valid data (*), a training word is being transmitted continuously. The content of the training word can be set with the **TRAINING_WORD** register. As the sensor operates in 12-bit mode, only the lowest 12 bits of the register are sent as training word.

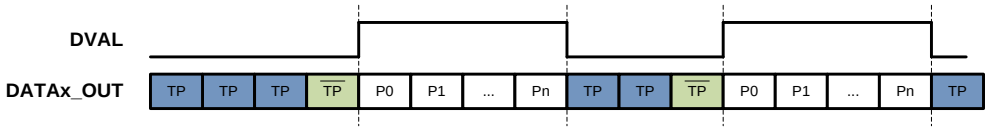
On all DATAx_OUT channels, the last word cycle before DVAL, the training word is inverted. If the overhead time between two DVAL cycles is only 1 word wide, only the inverted training word is sent.

(*) Valid data is:

- **DATAx_OUT:** Valid pixel data (DVAL = '1')
- **OBL_OUT:** Valid OB pixel data (LOBVAL = '1')
- **OBR_OUT:** Valid OB pixel data (ROBVAL = '1')

The figure below shows illustrates this timing (drawn in the parallel domain).

Figure 108 :
Training Pattern



When the sensor is not transmitting valid data, the training word can be used by the external controller to do word alignment (in other words: finding the position of bit [0]). Detecting the inverted training word will alert the presence of valid pixel data 1 pixel cycle in advance.

When the sensor is IDLE, all control word bits except the LSB (SYNC) are '0'. Detecting the SYNC bit allows for easy word alignment at the receiver side. Since all channels are bit and word aligned by default, finding the LSB of 1 channel means the LSB of all channels has been found.

Packet-Based Word Alignment

As detailed in section 7.3.3, word-alignment is done using the fixed SYNC code.

The HEADER field will alert the presence of valid pixel data in advance.

7.6.3 Packet Formatting

Figure 109:
Data Packet Formatting Registers

Reg. Name	Bank	Addr	Bits	Description
NOHDR_EMPTYPKT	0	79	[0]	See below
FEC_HEADER	0	79	[1]	See below

Depending on the requirements of the application, a trade-off can be made between data packet overhead (i.e. data throughput) and robustness.

When register **NOHDR_EMPTYPKT** is set to 1, the empty packet type described in section 7.3.3, will consist only of a SYNC code, without header. When register **NOHDR_EMPTYPKT** is set to 0, the empty packet type will consist of SYNC+HEADER.

When register **FEC_HEADER** is set to 1, the HEADER field will be sent as 96 bit using the 1/3 FEC described in section 7.6.3. This 1/3 FEC allows bit error corrections on the receiving side. When register **FEC_HEADER** is set to 0, the HEADER field will be sent in the short form (32 bit) and not be protected against bit-errors.

The register **DATA_PKT_CTRL** has no effect in pixel-based readout mode.

7.6.4 Outputs

As illustrated in Figure 52 the sensor has 22 output channels to transfer valid image data. This means that in the fastest configuration, the sensor can output 22 pixels at the same time. As the valid image width is 7920 columns, a complete row is transferred in 370 word cycles when utilizing all outputs.

Reduced Number of Data Channels

In many applications, it is not mandatory to use all data channels (for example when reading a limited horizontal ROI or when operating the sensor below its nominal frame rate). In these cases, it could be interesting to use less data channels to save power consumption.

The number of DATAx_OUT channels used is programmable with the **NR_OUTP** register.

Figure 110:
Number of Outputs Registers

Reg. Name	Bank	Addr	Bits	Description
NR_OUTP	0	26	[4:0]	See above. By default all channels are used
NR_OUTP_SCHEME	0	27	[0]	0: The first N channels are used 1: Channels are distributed evenly

When **NR_OUTP_SCHEME** is set to 1, the N channels are distributed evenly, starting at DATA0_OUT. The exact mapping details are given in the table below.

Figure 111:
Reduced Number of Output Settings (NR_OUTP_SCHEME=1)

NR_OUTP	Used DATAx_OUT Channels	Nr. of Pixels per Channel	Nr. of Padding Pixels
1	0	7920	0
2	0,11	3960	0
3	0,8,16	2880	720
4	0,6,12,18	2160	720
5	0,5,10,15,20	1800	1080
6	0,4,8,12,16,20	1440	720
8	0,3,6,9,12,15,18,21	1080	720
11	0,2,4,6,8,10,12,14,16,18,20	720	0
22	All (0 to 21)	360	0

When **NR_OUTP_SCHEME** is set to 0, the first N channels starting at DATA0_OUT are used.

For example, when setting **NR_OUTP** to 5, DATA0_OUT to DATA4_OUT channels are used. DATA5_OUT to DATA21_OUT are disabled. All other values in table above are still applicable.

It is not allowed to set **NR_OUTP** to any value not listed in Figure 111 (i.e. 0, 7, 9 to 10 or 12 to 21.)

All unused DATAx_OUT channels are automatically disabled (powered down).

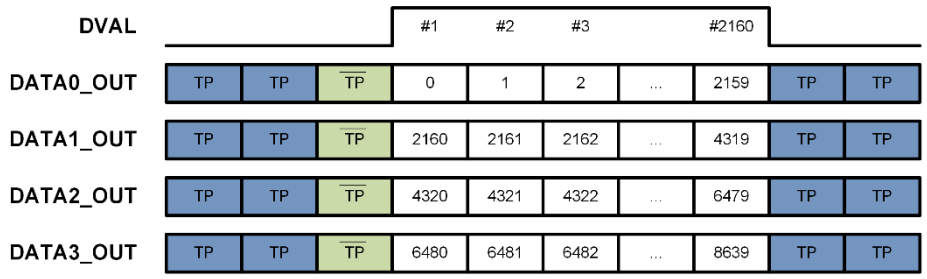
The last (or rightmost) channel of the used DATAx_OUT channels pads dummy pixels after the valid pixels when needed. Every channel sends an equal amount of pixels.

Pixel Order

The selected ROI (or full image width) is divided over 1 or more output channels. On each output, pixels are presented in-order.

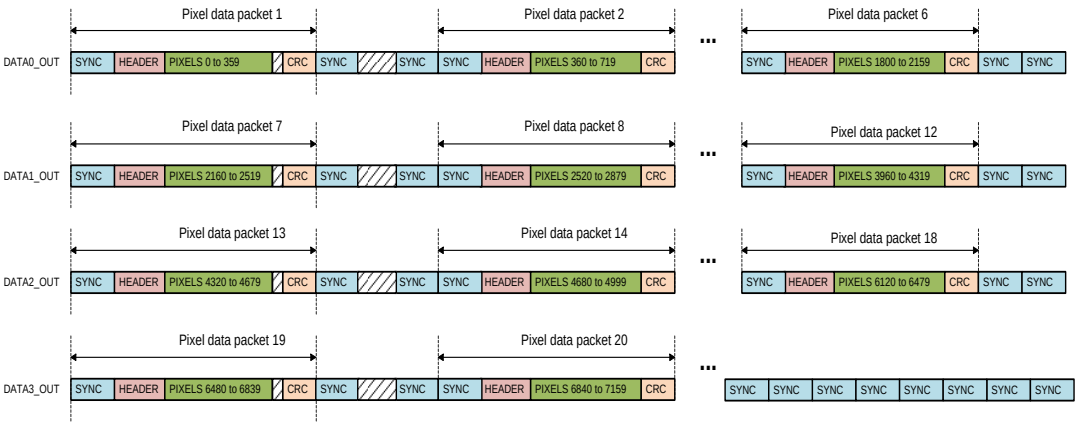
The figure below shows the timing of the readout of a single row for **NR_OUTP** set to 4 (each box represents the physical column address of the pixel). Here pixels 7920 to 8639 are dummy padding pixels and must be discarded.

Figure 112 :
Multiplexed Sub-LVDS Timing Example



A similar example for packet-based readout format is given in Figure 113.

Figure 113 :
Multiplexed Sub-LVDS Timing Example in Packet Mode



Every used data output channel outputs 6 data packets per line, separated by a number of empty packets.

DATA3_OUT transmits only 4 data packets per line, the last being #22 which contains pixels 7560 to 7919. After that, empty packets are sent on DATA3_OUT.

In packet-base mode, the word alignment between subsequent data packets might vary (depending on subsampling …). In the example above, this may be the case if the data packet is not a multiple of 4 bytes.

This translates into the need to redo word alignment between two packets on the same channel when reading out over a reduced number of data channels.

7.7 Configuring the On-Chip Data Processing

7.7.1 Optical Black Clamping

Figure 114:
Optical Black Registers

Reg. Name	Bank	Addr	Bits	Description
EOB_TARGET	0	76-77	[13:0]	Sets the target black level value in DN
EOB_BYPASS	1	42	[0]	0: OBC on (recommended) 1: OBC off
EOB_BYPASS_VALUE	1	43-44	[13:0]	Sets the ideal black level at the ADC (when OBC off).

This section explains how to set and correct the black levels.

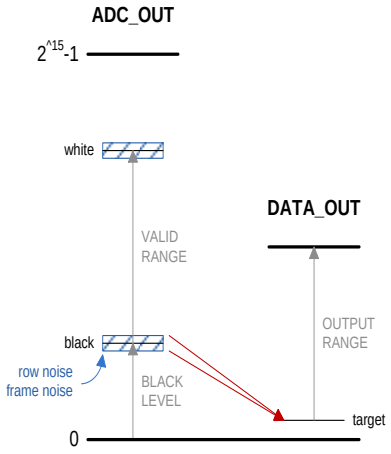
Black Level Mapping

The black level at a certain point in the pixel data path on the sensor is the analog level or digital word that corresponds to the level of an ideal dark pixel (zero illumination). In practice, it is the average of all real dark pixels (optically shielded) at that point in the data path.

The black level at the output of the ADC does not equal the desired black level in the output images for several reasons including the ADC architecture, fixed pattern and temporal noise (row noise, frame noise), dark current…

As illustrated in the figure below, the black level at the ADC output needs to be mapped on the target black level at the sensor output.

Figure 115 :
Black Level Mapping



The mapping is done using the equation:

Equation 16:

$$PIX_{DATA\_OUT} = clip[PIX_{ADC\_OUT} - BLACK\_LEVEL_{ADC\_OUT} + BLACK\_LEVEL_{DATA\_OUT}]$$

$BLACK\_LEVEL_{DATA\_OUT}$ is the target black level at the output of the sensor. It is specified with the register **EOB_TARGET**. The recommended minimal setting is 128 (lower settings may decrease the quality of the resulting image), which means the level at the output for black pixels will be around 128DN.

$BLACK\_LEVEL_{ADC\_OUT}$ is the black level at the output of the ADC. Its value is set differently depending on how the black level correction is done. This is detailed in the next two sections.

On-Chip OBC

Setting **EOB_BYPASS** to 0 enables the automatic on-chip black level correction (clamping). In this mode, $BLACK\_LEVEL_{ADC\_OUT}$ is calculated on-chip, based on OB pixels, for every row allowing to correct for row and frame noise in the image.

This is the recommended mode of operation.

Off-Chip OBC

Setting **EOB_BYPASS** to 1 disables the automatic OBC. $BLACK\_LEVEL_{ADC\_OUT}$ is now specified with register **EOB_BYPASS_VALUE**. This value is constant and cannot correct for row noise in the image.

Equation 17:

$$PIX_{DATA\_OUT} = clip[PIX_{ADC\_OUT} - EOB\_BYPASS\_VALUE + EOB\_TARGET]$$

Further external or off-chip OBC can be achieved by reading out the OB pixel data (refer to section 7.8.4).

7.7.2 Analog and Digital Gain

Register **GANA** is used to set the analog gain. When changing the analog gain, the OB black level also has to be fine-tuned to have optimal black level clamping.

Figure 116:
Analog Gain Registers

Reg. Name	Bank	Addr	Bits	Description
GANA	0	78	[7:0]	See settings in 7.4.2
EOB_OFFSET_FINE	1	38-39	[15:0]	See settings in 7.4.2

Digital gain can be specified for the 4 color channels individually (even/odd columns, even/odd rows). E.g. GDIG_RE_CO relates to **R**ows **E**ven and **C**olumns **O**dd.

The digital gain for each channel is defined by a similar equation:

Equation 18:

$$Digital\ gain\ (Rx\_Cy) = (GDIG\_Rx\_Cy + 1)/16$$

Base (default) digital gain is set by uploading a value of 15 to **GDIG_Rx_Cy**. The maximum digital gain is 16x with **GDIG_Rx_Cy** at 256. The lowest digital gain is 1/16x with **GDIG_Rx_Cy** at 0.

Figure 117:
Digital Gain Registers

Reg. Name	Bank	Addr	Bits	Description
GDIG_RE_CE	0	72	[7:0]	Even Rows & Even Columns See equation above
GDIG_RE_CO	0	73	[7:0]	Even Rows & Odd Columns See equation above
GDIG_RO_CE	0	74	[7:0]	Odd Rows & Even Columns See equation above
GDIG_RO_CO	0	75	[7:0]	Odd Rows & Odd Columns See equation above

If possible, using analog gain is preferred to using digital gain because it will improve SNR.

Analog gain is applied in the data path before the ADC and digital gain is applied after the black level correction. This means that changing the digital gain setting does not require any of the offset correction settings to be updated.

7.7.3 Color versus Monochrome Mode

Register Name	Bank	Addr	Bits	Description
COLOR_MODE	0	4	[0]	0: Mono 1: Color

As introduced in sections 7.5.6 and 7.5.7, sub sampling and binning modes behave differently for color and monochrome sensors. Set **COLOR_MODE** 1 for color sensors and 0 for monochrome sensors.

7.8 Additional Features

7.8.1 Digital Test Output

Figure 118:
Digital Test Output Register

Reg. Name	Bank	Addr	Bits	Description
DMUX1_SEL	1	99	[4:0]	Sets pin TDIGO1 function

A number of digital signals of the chip can be monitored in real-time during normal sensor operation via the sensor output pin TDIGO1. This can be very helpful for testing and debugging the system without having to rely on the sub-LVDS implementation of the control channel, so a test pad or connection to the FPGA is recommended.

Selecting which signal to be monitored is done with **DMUX1_SEL**.

7.8.2 Temperature Sensor

Figure 119:
Temperature Sensor Registers

Reg. Name	Bank	Addr	Bits	Description
TSENS1_PDN	0	103	[0]	Power down not
TSENS1_RSTN	0	103	[1]	Reset not
TSENS1_DCORRECT	0	103	[7:2]	Offset value

Reg. Name	Bank	Addr	Bits	Description
TSENS1_OUTPUT	0	104-105	[9:0]	Read-only code

The sensor has a temperature sensor placed at the top side of the sensor. In the range of -40°C to 125°C, the temperature sensor has a maximum error of ±12°C without calibration. After a one-point calibration at 25°C, the maximum error is ±5°C, after a two-point calibration, the maximum error becomes ±3°C.

To disable the temperature sensor, both **TSENS1_PDN** and **TSENS1_RSTN** must be set to '0'.

To enable the temperature sensor, both **TSENS1_PDN** and **TSENS1_RSTN** must be set to '1' and a settling time of 0.5ms must be respected before reading **TSENS1_OUTPUT**.

The bit [9] of **TSENS1_OUTPUT** is high when an overflow condition has occurred in the temperature sensor. If this condition occurs, the temperature is either out of range, or a wrong offset was programmed in the **TSENS1_DCORRECT** register.

No Calibration

In order to get the uncalibrated temperature of the die (±12°C), follow this procedure:

1. Write value 131 to TSENS1_CONTROL
2. Wait 0.5ms (settling time)
3. Read **TSENS1_OUTPUT**
4. Calculate the measured die temperature according to the equation:
   $T_m = (\mathbf{TSENS1\_OUTPUT[8:0]} / 2) - 100$

1-Point Calibration

The procedure below describes how to calculate and set the calibration value for the temperature sensor to output the correct sensor temperature (±5°C) using one measurement.

1. Let the sensor reach a known temperature (T_j) around 25°C and let it settle so that the die temperature (which equals the package temperature) is stable.
2. Write value 131 to TSENS1_CONTROL
3. Wait 0.5ms (settling time)
4. Read **TSENS1_OUTPUT**
5. Calculate the uncalibrated die temperature according to the equation $T_u = (TSENS1\_OUTPUT[8:0] / 2) - 100$
6. Calculate the calibration error: $T_e = T_j - T_u$
7. Update **TSENS1_DCORRECT** to $32 + (2 \times T_e)$

From now on, to measure the die temperature within ±5°C accuracy in the range from -40°C to 125°C:

1. Read **TSENS1_OUTPUT**
2. Calculate the measured die temperatures according to the equation $T_m = (TSENS1\_OUTPUT[8:0] / 2) - 100$

An example:

- We let the sensor settle unpowered to a known ambient temperature of 28°C. We power up the sensor and immediately read out **TSENS1_OUTPUT[8:0**]. This way the junction temperature will be very close to the ambient temperature. **TSENS1_OUTPUT[8:0**] contains 260.
- So now $T_u = (260/2) - 100 = 30$ and $T_e = 28 - 30 = -2$.
- Upload **TSENS1_DCORRECT** with the value $32 + (2 \times T_e) = 28$.
- Reading out **TSENS1_OUTPUT[8:0]** now gives a value of 256, which corresponds to the correct temperature $T_m = (256/2) - 100 = 28$.
- When during operation, you read out **TSENS1_OUTPUT[8:0]** as, for example, 338, you know that the junction temperature is equal to $Tj = Tm = (338/2) - 100 = 69°C$ (±5°C)

2-Point Calibration

A 2-point calibration will correct for the offset as well as the slope over temperature.

The procedure below describes how to calculate and set the calibration value for the temperature sensor to output the correct sensor temperature (±3°C) using two measurements.

1. Let the sensor reach a known temperature (T_{j1}) and let it settle so that the die temperature (which equals the package temperature) is stable.
2. Write value 131 to TSENS1_CONTROL, which will
3. Wait 0.5ms (settling time)
4. Read **TSENS1_OUTPUT[8:0]** and save it as B1.
5. Change the temperature to T_{j2} (preferably more than 30°C difference with T_{j1}) and let it settle.
6. Read out **TSENS1_OUTPUT[8:0]** and save it as B2.
7. Calculate the slope as: $M = (T_{j2} - T_{j1})/(B2\text{-}B1)$. For an ideal and perfect temperature sensor the slope will be 0.5.
8. Calculate the offset as: $C = T_{j1}$ - $M*B1 = T_{j2} - M \times B2$
9. Store the values M and C, which define a straight line.

From now on, to measure the die temperature within ±3ºC accuracy in the range from -40°C to 125°C:

1. Read TSENS1_OUTPUT
2. Calculate the measured die temperatures according to the equation $T_m = M \times TSENS1\_OUTPUT[8:0] + C$

Information

For 2-point calibration **TSENS1_DCORRECT** must be left at its default value (32).

7.8.3 Version ID

Figure 120:
Version ID Register

Reg. Name	Bank	Addr	Bits	Description
VERSION_ID	0	116	[7:0]	Read only

The read-only register **VERSION_ID** contains the revision number of the sensor.

7.8.4 Enable Optical Black Outputs

By default, the *OBx_OUT* channels are disabled.

To enable (or disabling again) the OB channels, use the following SPI sequence:

Figure 121:
Enable OB Outputs Sequence

Upload #	Bank	Address	Write Value
1	1	107	1
2	1	106	16
3	1	106	24
4	1	106	16
5	1	106	16
6	1	106	16
7	1	106	16
8	1	106	16
9	1	106	16
10	1	106	16
11	1	106	16
12	1	106	16
13	1	106	16
14	1	106	16
15	1	106	16
16	1	106	16
17	1	106	16
18	1	106	16
19	1	106	16
20	1	106	16
21	1	106	16
22	1	106	16
23	1	106	16
24	1	106	16
25	1	106	16
26	1	106	16
27	1	106	24
28	1	106	16
29	1	107	0

The OB data is read out 1 row before the image data row it refers to. See also section 7.3.2.

OB channel enabling/disabling can only be done when the PLL's are locked, enabled and reset is released.

7.8.5 Test Images

Right before the sub-LVDS output drivers, the data stream can be replaced with a number of test patterns. Selection of test mode is made with the **TEST_LVDS** register as indicated in the table below.

Figure 122:
Test Images Registers

Reg. Name	Bank	Addr	Bits	Description
TEST_LVDS	0	81	[2:0]	See table below
TRAINING_WORD	0	79-80	[13:0]	Choose a value

Figure 123:
Sub-LVDS Test Modes

TEST_LVDS	DATAx_OUT	OBx_OUT	CTR_OUT	CLK_OUT
0	Normal	Normal	Normal	Normal
1	Force training word continuously	Force training word continuously	Force training word continuously	Normal
2	Test image: gradient	Drive constant 0	Normal	Normal
3	Test image: LFSR	Drive constant 0	Normal	Normal

In test mode 1, the data and OB output channels are forced to output register **TRAINING_WORD** and the control channel outputs its own training word.

In test modes 2 and 3, a fixed test image is created. The CLK_OUT and CTR_OUT channels drive their normal values, so only the actual pixel data is replaced. This is useful to debug the camera system before grabbing real images.

In sub-LVDS test mode 2, the data of pixel N is replaced by the value:

Equation 19:

$$D_{TEST} = N_{COL} + N_{ROW} + N_{KERNEL} + 1$$

With:

- $\mathbf{N_{COL}}$ is the running number of pixel N in the DVAL pulse (0 for first valid pixel on each output)
- $\mathbf{N_{ROW}}$ is the running number of the DVAL pulse within FVAL (0 for first valid row in each FVAL)
- $\mathbf{N_{KERNEL}}$ is the number of the channel from which pixel N originates

The result is a 2D gradient (per channel), with a starting offset depending on the kernel number. The figure below shows an example using NR_OUTP = 4 (N_{KERNEL} is resp. 0, 6, 12, 18).

Figure 124 :
Gradient Test Image Pixel Data

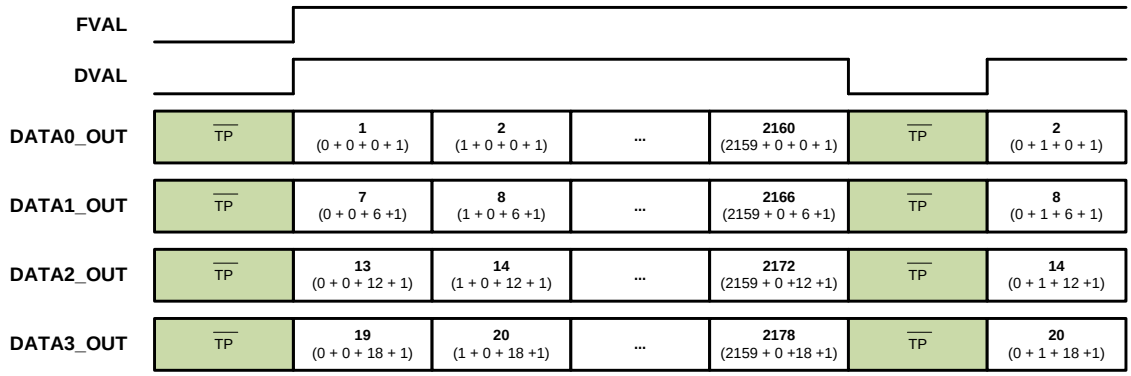
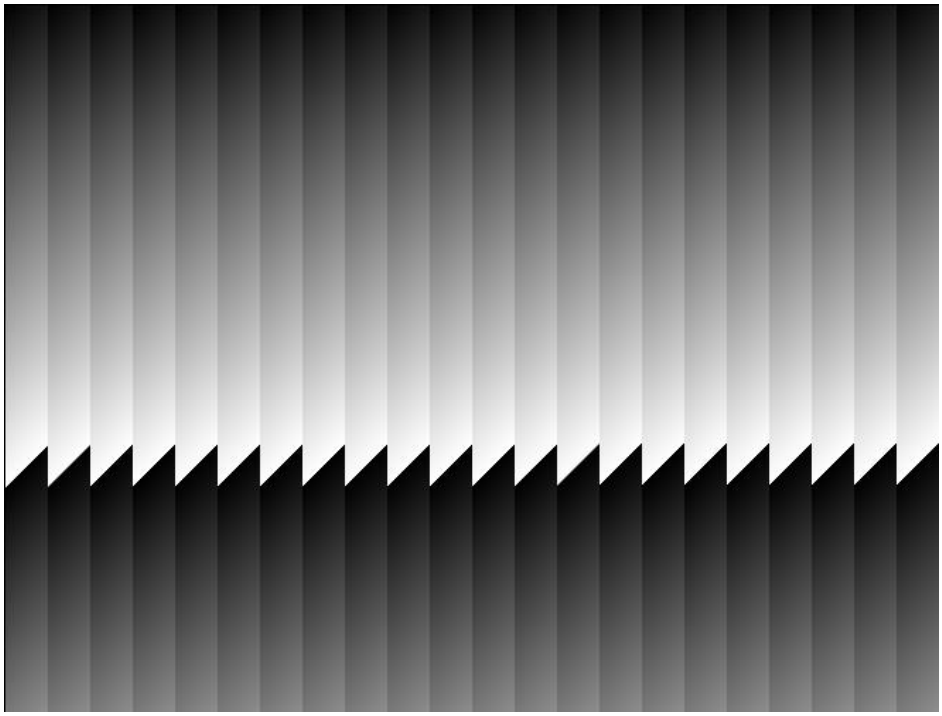
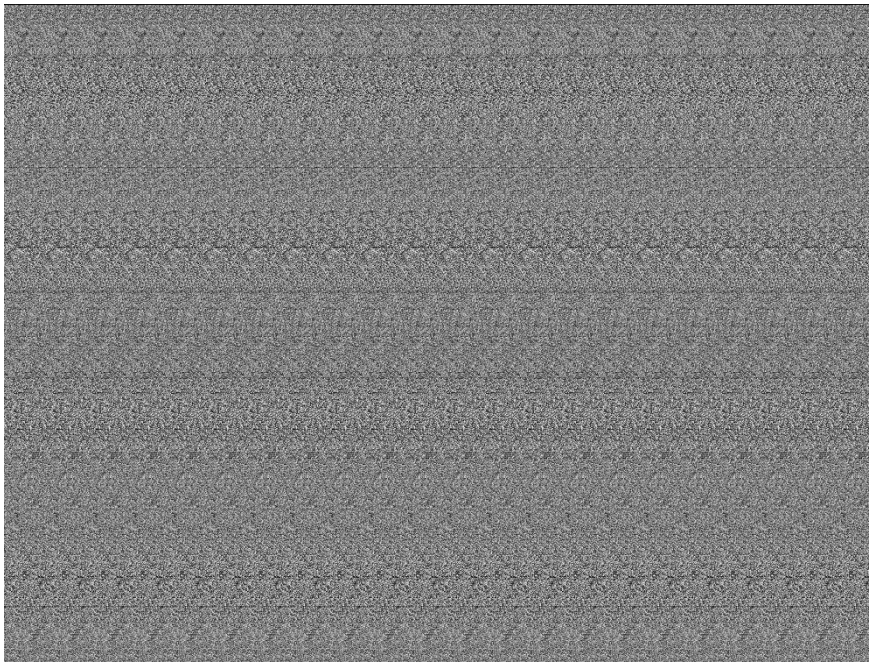


Figure 125 :
Gradient Test Image Example



In sub-LVDS test mode 3, the actual data of every pixel is replaced by the output of a pseudo-random generator. The value of the first valid pixel of a frame is 4095. All outputs drive the same output value (unlike test mode 2, where the N_{KERNEL} generates an offset between outputs).

Figure 126 :
LSFR Test Image Example



8 Register Description

8.1 Register Overview

Figure 127:
Register Overview Bank Select

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0	**BANK_SEL**	-	-	-	-	-	-	BANK_SEL [1:0]	

Figure 128:
Register Overview Bank 0

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
1	**PARAM_HOLD**	-	-	-	-	-	-	-	PARAM_ HOLD
2	**DISABLE_ FRAMESYNC**	-	-	-	-	-	-	-	DISABLE_ FRAMESYNC
3	**CMD_REGS**	-	-	-	HALT_ NBLOCK	HALT_ BLOCK	REQ_ FRAME	REQ_ EXP	RST_ SOFT_N
4	**COLOR_MODE**	-	-	-	-	-	-	-	COLOR_ MODE
5	**<RESERVED>**	-	-	-	-	-	-	-	-
6	**OUTP_FORMAT**	-	-	-	-	-	-	OUTP_FORMAT [1:0]	
7	**DATA_PKT_ CTRL**	-	-	-	-	-	-	NOHDR_ EMPTYPKT	FEC_ HEADER
8	**<RESERVED>**	-	-	-	-	-	-	-	-
9	**CTRL_MODE**	-	-	-	-	-	CTRL_MODE [2:0]		
10	**TIME_UNIT**	TIME_UNIT [7:0]							
11	**TIME_UNIT**	-	-	TIME_UNIT [13:8]					
12	**NROF_FRAMES**	NROF_FRAMES [7:0]							
13	**FRAME_TIME**	FRAME_TIME [7:0]							
14	**FRAME_TIME**	FRAME_TIME [15:8]							
15	**DUAL_ EXPOSURE**	-	-	-	-	-	-	-	DUAL_ EXPOSURE
16	**EXP_TIME_L**	EXP_TIME_L [7:0]							
17	**EXP_TIME_L**	EXP_TIME_L [15:8]							
18	**EXP_TIME_S**	EXP_TIME_S [7:0]							
19	**EXP_TIME_S**	EXP_TIME_S [15:8]							
20	**<RESERVED>**	-	-	-	-	-	-	-	-
21	**<RESERVED>**	-	-	-	-	-	-	-	-
22	**ROW_LENGTH**	ROW_LENGTH [7:0]							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
23	**ROW_LENGTH**	-	-	ROW_LENGTH [13:8]					
24	**XSUBS**	-	-	-	-	-	-	XSUBS [1:0]	
25	**BIN_MODE**	-	-	-	-	-	-	-	BIN_MODE
26	**NR_OUTP**	-	-	-	NR_OUTP [4:0]				
27	**NR_OUTP_ SCHEME**	-	-	-	-	-	-	-	NR_OUTP_ SCHEME
28	**YWIN_ENA**	YWIN_ENA [7:0]							
29	**YWIN_ENA**	-	-	-	-	-	-	YWIN_ENA [9:8]	
30	**YWIN_BLACK**	YWIN_BLACK [7:0]							
31	**YWIN_BLACK**	-	-	-	-	-	-	YWIN_BLACK [9:8]	
32	**YWIN0**	SIZE [7:0]							
33	**YWIN0**	START [2:0]			SIZE [12:8]				
34	**YWIN0**	START [10:3]							
35	**YWIN0**	-	-	-	SUBS [2:0]			START [12:11]	
36	**YWIN1**	SIZE [7:0]							
37	**YWIN1**	START [2:0]			SIZE [12:8]				
38	**YWIN1**	START [10:3]							
39	**YWIN1**	SIZE [7:0]							
40	**YWIN2**	START [2:0]			SIZE [12:8]				
41	**YWIN2**	START [10:3]							
42	**YWIN2**	-	-	-	SUBS [2:0]			START [12:11]	
43	**YWIN2**	-	-	-	SUBS [2:0]			START [12:11]	
44	**YWIN3**	SIZE [7:0]							
45	**YWIN3**	START [2:0]			SIZE [12:8]				
46	**YWIN3**	START [10:3]							
47	**YWIN3**	-	-	-	SUBS [2:0]			START [12:11]	
48	**YWIN4**	SIZE [7:0]							
49	**YWIN4**	START [2:0]			SIZE [12:8]				
50	**YWIN4**	START [10:3]							
51	**YWIN4**	-	-	-	SUBS [2:0]			START [12:11]	
52	**YWIN5**	SIZE [7:0]							
53	**YWIN5**	START [2:0]			SIZE [12:8]				
54	**YWIN5**	START [10:3]							
55	**YWIN5**	-	-	-	SUBS [2:0]			START [12:11]	
56	**YWIN6**	SIZE [7:0]							
57	**YWIN6**	START [2:0]			SIZE [12:8]				
58	**YWIN6**	START [10:3]							
59	**YWIN6**	-	-	-	SUBS [2:0]			START [12:11]	
60	**YWIN7**	SIZE [7:0]							
61	**YWIN7**	START [2:0]			SIZE [12:8]				
62	**YWIN7**	START [10:3]							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
63	YWIN7	-	-	-	SUBS [2:0]			START [12:11]	
64	YWIN8	SIZE [7:0]							
65	YWIN8	START [2:0]			SIZE [12:8]				
66	YWIN8	START [10:3]							
67	YWIN8	-	-	-	SUBS [2:0]			START [12:11]	
68	YWIN9	SIZE [7:0]							
69	YWIN9	START [2:0]			SIZE [12:8]				
70	YWIN9	START [10:3]							
71	YWIN9	-	-	-	SUBS [2:0]			START [12:11]	
72	GDIG_RE_CE	GDIG_RE_CE [7:0]							
73	GDIG_RE_CO	GDIG_RE_CO [7:0]							
74	GDIG_RO_CE	GDIG_RO_CE [7:0]							
75	GDIG_RO_CO	GDIG_RO_CO [7:0]							
76	EOB_TARGET	EOB_TARGET [7:0]							
77	EOB_TARGET	-	-	EOB_TARGET [13:8]					
78	GANA	GANA [7:0]							
79	TRAINING_WORD	TRAINING_WORD [7:0]							
80	TRAINING_WORD	-	-	TRAINING_WORD [13:8]					
81	TEST_LVDS	-	-	-	-	-	TEST_LVDS [2:0]		
82 - 100	<RESERVED>	-	-	-	-	-	-	-	-
101	OTP_DOUT	OTP_DOUT [7:0]							
102	OTP_DOUT	OTP_DOUT [15:8]							
103	TSENS1_CONTROL	DCORRECT [5:0]						RSTN	PDN
104	TSENS1_OUTPUT	TSENS1_OUTPUT [7:0]							
105	TSENS1_OUTPUT	-	-	-	-	-	-	TSENS1_OUTPUT [9:8]	
106	PLL1_ENABLE	-	-	-	-	-	-	-	PLL1_ENABLE
107	PLL1_PRE_DIV	-	-	-	-	-	-	PLL1_PRE_DIV [1:0]	
108	PLL1_NDIV	PLL1_NDIV [7:0]							
109	PLL1_CLKOUT_SEL	-	-	-	-	-	-	PLL1_CLKOUT_SEL [1:0]	
110	PLL2_ENABLE	-	-	-	-	-	-	-	PLL2_ENABLE
111	<RESERVED>	-	-	-	-	-	-	-	-
112	PLL2_NDIV	PLL2_NDIV [7:0]							
113	<RESERVED>	-	-	-	-	-	-	-	-
114	PLL_CLKDIV_RSTN	-	-	-	-	-	-	-	PLL_CLKDIV_RSTN
115	PLL_LOCK	-	-	-	-	-	-	PLL2_LOCK	PLL1_LOCK

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
116	**VERSION_ID**	VERSION_ID [7:0]							
117	**NO_ SHUTTER_LAG**	-	-	-	-	-	-	-	NO_ SHUTTER_ LAG
118	**DUAL_EXP_ GROUPING**	-	-	-	-	-	-	-	DUAL_EXP_ GROUPING

Figure 129:
Register Overview Bank 1

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
1 - 4	**<RESERVED>**	-	-	-	-	-	-	-	-
5	**GRAN_GLOB**	GRAN_GLOB [7:0]							
6	**CLKGEN_CFG**	-	<RESERVED> [2:0]			<RE SERVED>	CLKGEN_PHASE [1:0]		<RE SERVED>
7 - 98	**<RESERVED>**	-	-	-	-	-	-	-	-
99	**TDIG**	<RESERVED> [2:0]			DMUX1_SEL [4:0]				
100 - 109	**<RESERVED>**	-	-	-	-	-	-	-	-
110	**TG_LENGTH**	TG_LENGTH [7:0]							
111	**TG_LENGTH**	-	-	TG_LENGTH [13:8]					
112 - 113	**<RESERVED>**	-	-	-	-	-	-	-	-
114	**SHUTTER_LAG**	SHUTTER_LAG [7:0]							
115	**SHUTTER_LAG**			SHUTTER_LAG [13:8]					
116 - 119	**<RESERVED>**	-	-	-	-	-	-	-	-

Figure 130:
Register Overview Bank 2

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
1 - 127	**<RESERVED>**	-	-	-	-	-	-	-	-

Figure 131:
Register Overview Bank 3

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
1 - 48	**<RESERVED>**	-	-	-	-	-	-	-	-
49	**PLL1_DISABLE _CLKOUT**	-	-	-	-	-	-	-	PLL1_ DISABLE_ CLKOUT

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
50 - 57	<RESERVED>	-	-	-	-	-	-	-	-

8.2 Detailed Register Description

8.2.1 BANK_SEL Register (Address 0)

Figure 132:
BANK_SEL Register

Addr: 0		BANK_SEL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[1:0]	BANK_SEL	0	-	0: Bank 0 1: Bank 1 2: Bank 2 3: Bank 3

8.2.2 PARAM_HOLD Register (Bank 0, Address 1)

Figure 133:
PARAM_HOLD Register

Bank: 0 Addr: 1		PARAM_HOLD		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	PARAM_HOLD	0	-	0: Frame sync 1: During SPI upload

8.2.3 DISABLE_FRAMESYNC Register (Bank 0, Address 2)

Figure 134:
DISABLE_FRAMESYNC Register

Bank: 0 Addr: 2		DISABLE_FRAMESYNC		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	DISABLE_FRAMESYNC	0	-	0: Enable frame sync 1: Disable frame sync

8.2.4 CMD_REGS Register (Bank 0, Address 3)

Figure 135:
CMD_REGS Register

Bank: 0 Addr: 3		CMD_REGS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	RST_SOFT_N	0	-	0: Assert soft reset 1: Release soft reset
[1]	REQ_EXP	0	-	0: - 1: Sensor in EXPOSURE state
[2]	REQ_FRAME	0	-	0: - 1: Sensor in GLOB state
[3]	HALT_BLOCK	0	-	0: - 1: Finish active READOUT state and go to IDLE state
[4]	HALT_NBLOCK	0	-	0: - 1: Immediately stop sensor and go to IDLE state

8.2.5 COLOR_MODE Register (Bank 0, Address 4)

Figure 136:
COLOR_MODE Register

Bank: 0 Addr: 4		COLOR_MODE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	COLOR_MODE	0	DC	0: Monochrome mode 1: Color mode

8.2.6 OUTP_FORMAT Register (Bank 0, Address 6)

Figure 137:
OUTP_FORMAT Register

Bank: 0 Addr: 6		OUTP_FORMAT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[1:0]	OUTP_FORMAT	0	RST	0: Pixel based format 1: Packet based format

8.2.7 DATA_PKT_CTRL Register (Bank 0, Address 7)

Figure 138:
DATA_PKT_CTRL Register

Bank: 0 Addr: 7		DATA_PKT_CTRL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	NOHDR_EMPTYPKT	1	DC	0: SYNC + HEADER in empty packet. 1: Only SYNC in empty packet
[1]	FEC_HEADER	1	DC	0: 32b HEADER 1: 96b HEADER with 1/3 FEC

8.2.8 CTRL_MODE Register (Bank 0, Address 9)

Figure 139:
CTRL_MODE Register

Bank: 0 Addr: 9		CTRL_MODE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[2:0]	CTRL_MODE	1	DC	0: Full External (FE) 1: Programmed External (PE) 2: Triggered Internal (TI) 3: Streaming (S)

8.2.9 TIME_UNIT Register (Bank 0, Address 10-11)

Figure 140:
TIME_UNIT Register

Bank: 0 Addr: 10-11		TIME_UNIT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[13:0]	TIME_UNIT	69	FRAME	Sets unit for frame and exposure time

8.2.10 NROF_FRAMES Register (Bank 0, Address 12)

Figure 141:
NROF_FRAMES Register

Bank: 0 Addr: 12		NROF_FRAMES		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[7:0]	NROF_FRAMES	1	-	Sets sequence length for TI control mode

8.2.11 FRAME_TIME Register (Bank 0, Address 13-14)

Figure 142:
FRAME_TIME Register

Bank: 0 Addr: 13-14		FRAME_TIME		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	FRAME_TIME	33000	DC	Sets the frame time in time units

8.2.12 DUAL_EXPOSURE Register (Bank 0, Address 15)

Figure 143:
DUAL_EXPOSURE Register

Bank: 0 Addr: 15		DUAL_EXPOSURE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	DUAL_EXPOSURE	0	DC	0: Disable dual exposure HDR 1: Enable dual exposure HDR

8.2.13 EXP_TIME_L Register (Bank 0, Address 16-17)

Figure 144:
EXP_TIME_L Register

Bank: 0 Addr: 16-17		EXP_TIME_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	EXP_TIME_L	10000	FRAME	Sets the exposure time of pixels in group L in time units

8.2.14 EXP_TIME_S Register (Bank 0, Address 18-19)

Figure 145:
EXP_TIME_S Register

Bank: 0 Addr: 18-19		EXP_TIME_S		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	EXP_TIME_S	0	FRAME	Sets the exposure time of pixels in group S in time units

8.2.15 ROW_LENGTH Register (Bank 0, Address 22-23)

Figure 146:
ROW_LENGTH Register

Bank: 0 Addr: 16-17		ROW_LENGTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[13:0]	ROW_LENGTH	380	SYNC	Sets the row time

8.2.16 XSUBS Register (Bank 0, Address 24)

Figure 147:
XSUBS Register

Bank: 0 Addr: 24		XSUBS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[1:0]	XSUBS	0	SYNC	Set horizontal subsampling ratio to $1/(2^{XSUBS})$

8.2.17 BIN_MODE Register (Bank 0, Address 25)

Figure 148:
BIN_MODE Register

Bank: 0 Addr: 25		BIN_MODE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	BIN_MODE	0	SYNC	0: Disable binning 1: Enable binning

8.2.18 NR_OUTP Register (Bank 0, Address 26)

Figure 149:
NR_OUTP Register

Bank: 0 Addr: 26		NR_OUTP		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[4:0]	NR_OUTP	22	DC	Sets the number of data outputs used to 1, 2, 3, 4, 5, 6, 8, 11 or 22.

8.2.19 NR_OUTP_SCHEME Register (Bank 0, Address 27)

Figure 150:
NR_OUTP_SCHEME Register

Bank: 0 Addr: 27		NR_OUTP_SCHEME		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	NR_OUTP_SCHEME	0	DC	0: Use the first NR_OUTP data outputs 1: Used channels are distributed evenly

8.2.20 YWIN_ENA Register (Bank 0, Address 28-29)

Figure 151:
YWIN_ENA Register

Bank: 0 Addr: 28-29		YWIN_ENA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[9:0]	YWIN_ENA	1	SYNC	Enables/disables one window per bit 0: Disable window N 1: Enable window N

8.2.21 YWIN_BLACK Register (Bank 0, Address 30-31)

Figure 152:
YWIN_BLACK Register

Bank: 0 Addr: 30-31		YWIN_BLACK		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[9:0]	YWIN_BLACK	0	SYNC	Enables/disables Electrical Black for one window per bit 0: Disable EB of window N 1: Enable EB of window N

8.2.22 YWIN0 Register (Bank 0, Address 32-35)

Figure 153:
YWIN0 Register

Bank: 0 Addr: 32-35		YWIN0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[12:0]	SIZE	6004	SYNC	Number of rows in this window
[25:13]	START	22	SYNC	Physical start address of the first row of this window
[28:26]	SUBS	0	SYNC	Set row subsampling in this window with ratio $1/(2^{SUBS})$

8.2.23 YWIN1 Register (Bank 0, Address 36-39)

Figure 154:
YWIN1 Register

Bank: 0 Addr: 36-39		YWIN1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[12:0]	SIZE	0	SYNC	Number of rows in this window
[25:13]	START	0	SYNC	Physical start address of the first row of this window
[28:26]	SUBS	0	SYNC	Set row subsampling in this window with ratio $1/(2^{SUBS})$

8.2.24 YWIN2 Register (Bank 0, Address 40-43)

Figure 155:
YWIN2 Register

Bank: 0 Addr: 40-43		YWIN2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[12:0]	SIZE	0	SYNC	Number of rows in this window
[25:13]	START	0	SYNC	Physical start address of the first row of this window
[28:26]	SUBS	0	SYNC	Set row subsampling in this window with ratio $1/(2^{SUBS})$

8.2.25 YWIN3 Register (Bank 0, Address 44-47)

Figure 156:
YWIN3 Register

Bank: 0 Addr: 44-47		YWIN3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[12:0]	SIZE	0	SYNC	Number of rows in this window
[25:13]	START	0	SYNC	Physical start address of the first row of this window

Bank: 0 Addr: 44-47		YWIN3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[28:26]	SUBS	0	SYNC	Set row subsampling in this window with ratio 1/(2^{SUBS})

8.2.26 YWIN4 Register (Bank 0, Address 48-51)

Figure 157:
YWIN4 Register

Bank: 0 Addr: 48-51		YWIN4		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[12:0]	SIZE	0	SYNC	Number of rows in this window
[25:13]	START	0	SYNC	Physical start address of the first row of this window
[28:26]	SUBS	0	SYNC	Set row subsampling in this window with ratio 1/(2^{SUBS})

8.2.27 YWIN5 Register (Bank 0, Address 52-55)

Figure 158:
YWIN5 Register

Bank: 0 Addr: 52-55		YWIN5		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[12:0]	SIZE	0	SYNC	Number of rows in this window
[25:13]	START	0	SYNC	Physical start address of the first row of this window
[28:26]	SUBS	0	SYNC	Set row subsampling in this window with ratio 1/(2^{SUBS})

8.2.28 YWIN6 Register (Bank 0, Address 56-59)

Figure 159:
YWIN6 Register

Bank: 0 Addr: 56-59		YWIN6		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[12:0]	SIZE	0	SYNC	Number of rows in this window
[25:13]	START	0	SYNC	Physical start address of the first row of this window
[28:26]	SUBS	0	SYNC	Set row subsampling in this window with ratio $1/(2^{SUBS})$

8.2.29 YWIN7 Register (Bank 0, Address 60-63)

Figure 160:
YWIN7 Register

Bank: 0 Addr: 60-63		YWIN7		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[12:0]	SIZE	0	SYNC	Number of rows in this window
[25:13]	START	0	SYNC	Physical start address of the first row of this window
[28:26]	SUBS	0	SYNC	Set row subsampling in this window with ratio $1/(2^{SUBS})$

8.2.30 YWIN8 Register (Bank 0, Address 64-67)

Figure 161:
YWIN8 Register

Bank: 0 Addr: 64-67		YWIN8		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[12:0]	SIZE	0	SYNC	Number of rows in this window
[25:13]	START	0	SYNC	Physical start address of the first row of this window

Bank: 0 Addr: 64-67		YWIN8		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[28:26]	SUBS	0	SYNC	Set row subsampling in this window with ratio 1/(2^{SUBS})

8.2.31 YWIN9 Register (Bank 0, Address 68-71)

Figure 162:
YWIN9 Register

Bank: 0 Addr: 68-71		YWIN9		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[12:0]	SIZE	0	SYNC	Number of rows in this window
[25:13]	START	0	SYNC	Physical start address of the first row of this window
[28:26]	SUBS	0	SYNC	Set row subsampling in this window with ratio 1/(2^{SUBS})

8.2.32 GDIG_RE_CE Register (Bank 0, Address 72)

Figure 163:
GDIG_RE_CE Register

Bank: 0 Addr: 72		GDIG_RE_CE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[7:0]	GDIG_RE_CE	15	SYNC	Sets the digital gain for the pixels in the even rows and even columns

8.2.33 GDIG_RE_CO Register (Bank 0, Address 73)

Figure 164:
GDIG_RE_CO Register

Bank: 0 Addr: 73		GDIG_RE_CO		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[7:0]	GDIG_RE_CO	15	SYNC	Sets the digital gain for the pixels in the even rows and odd columns

8.2.34 GDIG_RO_CE Register (Bank 0, Address 74)

Figure 165:
GDIG_RO_CE Register

Bank: 0 Addr: 74		GDIG_RO_CE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[7:0]	GDIG_RO_CE	15	SYNC	Sets the digital gain for the pixels in the odd rows and even columns

8.2.35 GDIG_RO_CO Register (Bank 0, Address 75)

Figure 166:
GDIG_RO_CO Register

Bank: 0 Addr: 75		GDIG_RO_CO		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[7:0]	GDIG_RO_CO	15	SYNC	Sets the digital gain for the pixels in the odd rows and odd columns

8.2.36 EOB_TARGET Register (Bank 0, Address 76-77)

Figure 167:
EOB_TARGET Register

Bank: 0 Addr: 76-77		EOB_TARGET		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[13:0]	EOB_TARGET	32	SYNC	Sets the target black level value in DN 128: 128DN

8.2.37 GANA Register (Bank 0, Address 78)

Figure 168:
GANA Register

Bank: 0 Addr: 78		GANA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[7:0]	GANA	0	SYNC	Sets the analog gain. Non-binning / binning mode: 255 / 223: x1 243 / 211: x2 241 / 209: x4

8.2.38 TRAINING_WORD Register (Bank 0, Address 79-80)

Figure 169:
TRAINING_WORD Register

Bank: 0 Addr: 79-80		TRAINING_WORD		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[13:0]	TRAINING_WORD	85	-	The training word on the data outputs

8.2.39 TEST_LVDS Register (Bank 0, Address 81)

Figure 170:
TEST_LVDS Register

Bank: 0 Addr: 81		TEST_LVDS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[2:0]	TEST_LVDS	0	-	Sets the output test mode. 0: Normal data output 1: Continuous training word 2: Gradient test image 3: LFSR test image

8.2.40 OTP_CONTROL Register (Bank 0, Address 97)

Figure 171:
OTP_CONTROL Register

Bank: 0 Addr: 97		OTP_CONTROL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[3:0]	OTP_CONTROL	0	-	OTP control input

8.2.41 OTP_A Register (Bank 0, Address 98)

Figure 172:
OTP_A Register

Bank: 0 Addr: 98		OTP_A		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[6:0]	OTP_A	0	-	OTP address input

8.2.42 OTP_DOUT Register (Bank 0, Address 101-102)

Figure 173:
OTP_DOUT Register

Bank: 0 Addr: 101-102		OTP_DOUT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	OTP_DOUT	0	RO	OTP data output

8.2.43 TSENS1_CONTROL Register (Bank 0, Address 103)

Figure 174:
TSENS1_CONTROL Register

Bank: 0 Addr: 103		TSENS1_CONTROL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	PDN	0	-	Temperature sensor power state: 0: Down 1: Up
[1]	RSTN	0	-	Temperature sensor reset state: 0: Assert reset 1: Release reset
[7:2]	DCORRECT	32	-	Temperature sensor correction value

8.2.44 TSENS1_OUTPUT Register (Bank 0, Address 104-105)

Figure 175:
TSENS1_OUTPUT Register

Bank: 0 Addr: 104-105		TSENS1_OUTPUT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[9:0]	TSENS1_OUTPUT	0	RO	Temperature sensor output

8.2.45 PLL1_ENABLE Register (Bank 0, Address 106)

Figure 176:
PLL1_ENABLE Register

Bank: 0 Addr: 106		PLL1_ENABLE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	PLL1_ENABLE	0	RST	0: Disable PLL1 1: Enable PLL1

8.2.46 PLL1_PRE_DIV Register (Bank 0, Address 107)

Figure 177:
PLL1_PRE_DIV Register

Bank: 0 Addr: 107		PLL1_PRE_DIV		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[1:0]	PLL1_PRE_DIV	0	RST	Set by CLK_IN frequency: 0: 6MHz – 12MHz 1: 12MHz – 24MHz 2: 24MHz – 48MHz 3: 48MHz – 96MHz

8.2.47 PLL1_NDIV Register (Bank 0, Address 108)

Figure 178:
PLL1_NDIV Register

Bank: 0 Addr: 108		PLL1_NDIV		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[7:0]	PLL1_NDIV	0	RST	PLL1 divider parameter

8.2.48 PLL1_CLKOUT_SEL Register (Bank 0, Address 109)

Figure 179:
PLL1_CLKOUT_SEL Register

Bank: 0 Addr: 109		PLL1_CLKOUT_SEL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[1:0]	PLL1_CLKOUT_SEL	0	RST	Set by target output data rate: 0: 460 – 830Mbit/s 1: 230 – 460Mbit/s 2: 120 – 230Mbit/s

8.2.49 PLL2_ENABLE Register (Bank 0, Address 110)

Figure 180:
PLL2_ENABLE Register

Bank: 0 Addr: 110		PLL2_ENABLE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	PLL2_ENABLE	0	RST	0: Disable PLL1 1: Enable PLL1

8.2.50 PLL2_NDIV Register (Bank 0, Address 112)

Figure 181:
PLL2_NDIV Register

Bank: 0 Addr: 112		PLL2_NDIV		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[7:0]	PLL2_NDIV	0	RST	PLL2 divider parameter

8.2.51 PLL_CLKDIV_RSTN Register (Bank 0, Address 114)

Figure 182:
PLL_CLKDIV_RSTN Register

Bank: 0 Addr: 114		PLL_CLKDIV_RSTN		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	PLL_CLKDIV_RSTN	0	-	0: Assert CLK_IN divider reset 1: Release CLK_IN divider reset

8.2.52 PLL_LOCK Register (Bank 0, Address 115)

Figure 183:
PLL_LOCK Register

Bank: 0 Addr: 115		PLL_LOCK		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	PLL1_LOCK	0	RO	0: PLL1 out of lock 1: PLL1 in lock
[1]	PLL2_LOCK	0	RO	0: PLL2 out of lock 1: PLL2 in lock

8.2.53 VERSION_ID Register (Bank 0, Address 116)

Figure 184:
VERSION_ID Register

Bank: 0 Addr: 116		VERSION_ID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[7:0]	VERSION_ID	1	RO	Sensor revision number

8.2.54 NO_SHUTTER_LAG Register (Bank 0, Address 117)

Figure 185:
NO_SHUTTER_LAG Register

Bank: 0 Addr: 117		NO_SHUTTER_LAG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	NO_SHUTTER_LAG	0	DC	0: Enable shutter lag 1: Disable shutter lag

8.2.55 DUAL_EXP_GROUPING Register (Bank 0, Address 118)

Figure 186:
DUAL_EXP_GROUPING Register

Bank: 0 Addr: 118		DUAL_EXP_GROUPING		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	DUAL_EXP_GROUPING	0	DC	Dual exposure column grouping: 0: Default (monochrome) 1: Paired (color)

8.2.56 GRAN_GLOB Register (Bank 1, Address 5)

Figure 187:
GRAN_GLOB Register

Bank: 1 Addr: 5		GRAN_GLOB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[7:0]	GRAN_GLOB	1	-	Sets shutter timing granularity

8.2.57 CLKGEN_CFG Register (Bank 1, Address 6)

Figure 188:
CLKGEN_CFG Register

Bank: 1 Addr: 6		CLKGEN_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	<RESERVED>	0	RST	
[2:1]	PHASE	1	RST	Sets the phase of the output clock to the data. 0: 0° 1: 90° 2: 180° 3: 270°
[3]	<RESERVED>	1	RST	
[6:4]	<RESERVED>	0	RST	

8.2.58 EOB_OFFSET_FINE Register (Bank 1, Address 38-39)

Figure 189:
EOB_OFFSET_FINE Register

Bank: 1 Addr: 38-39		EOB_OFFSET_FINE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	EOB_OFFSET_FINE	0	-	Fine tunes the OB offset depending on gain: 32920: Analog gain x1 33083: Analog gain x2 33418: Analog gain x4

8.2.59 EOB_BYPASS Register (Bank 1, Address 42)

Figure 190:
EOB_BYPASS Register

Bank: 1 Addr: 42		EOB_BYPASS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	EOB_BYPASS	0	-	Enables Optical Black Correction (OBC) 0: OBC on (recommended) 1: OBC off

8.2.60 EOB_BYPASS_VALUE Register (Bank 1, Address 43-44)

Figure 191:
EOB_BYPASS_VALUE Register

Bank: 1 Addr: 43-44		EOB_BYPASS_VALUE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[13:0]	EOB_BYPASS_VALUE	0	-	Sets the black level at the ADC (with OBC off)

8.2.61 NR_DUMMIES Register (Bank 1, Address 46)

Figure 192:
NR_DUMMIES Register

Bank: 1 Addr: 46		NR_DUMMIES		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[3:0]	NR_DUMMIES	0	-	Sets the number of dummy rows in pipeline mode

8.2.62 TDIG Register (Bank 1, Address 99)

Figure 193:
TDIG Register

Bank: 1 Addr: 99		TDIG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[4:0]	DMUX1_SEL	0	-	Sets pin TDIGO1 function: 0: None 1: PLL_1_LOCK 2: PLL_2_LOCK 5: CLK_PIX 6: INT_REQ_FRAME 7: INT_REQ_EXP(L) 12: GLOB start 14: CTR_EXP(L)

8.2.63 TG_LENGTH Register (Bank 1, Address 110-111)

Figure 194:
TG_LENGTH Register

Bank: 1 Addr: 110-111		TG_LENGTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[13:0]	TG_LENGTH	0	DC	Sets shutter timing

8.2.64 SHUTTER_LAG Register (Bank 1, Address 114-115)

Figure 195:
SHUTTER_LAG Register

Bank: 1 Addr: 114-115		SHUTTER_LAG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[13:0]	SHUTTER_LAG	0	DC	Sets the shutter lag

8.2.65 PLL1_DISABLE_CLKOUT Register (Bank 3, Address 49)

Figure 196:
PLL1_DISABLE_CLKOUT Register

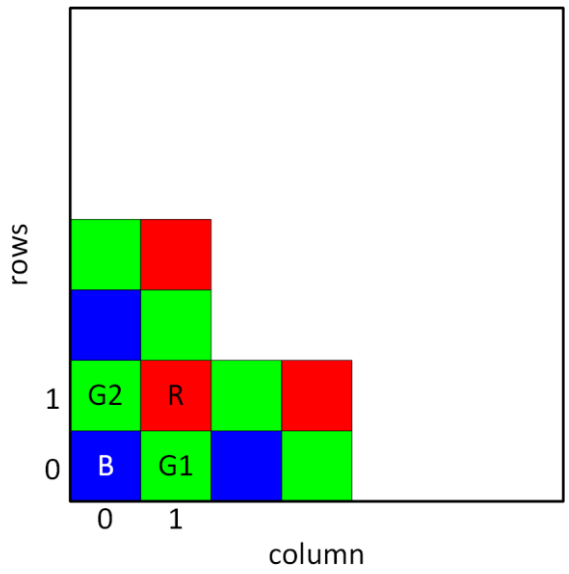
Bank: 1 Addr: 49		SHUTTER_LAG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	PLL1_DISABLE_CLKOUT	0	RST	Disables the PLL1 clock output for soft-reset. 0: Enabled 1: Disabled

9 Application Information

9.1 Color Filter

A color version of the CMV50000 has the color filters are applied in a Bayer pattern. The first pixel read-out, pixel(0, 0), is the bottom left one and has a blue filter.

Figure 197 :
Bayer Color Filter



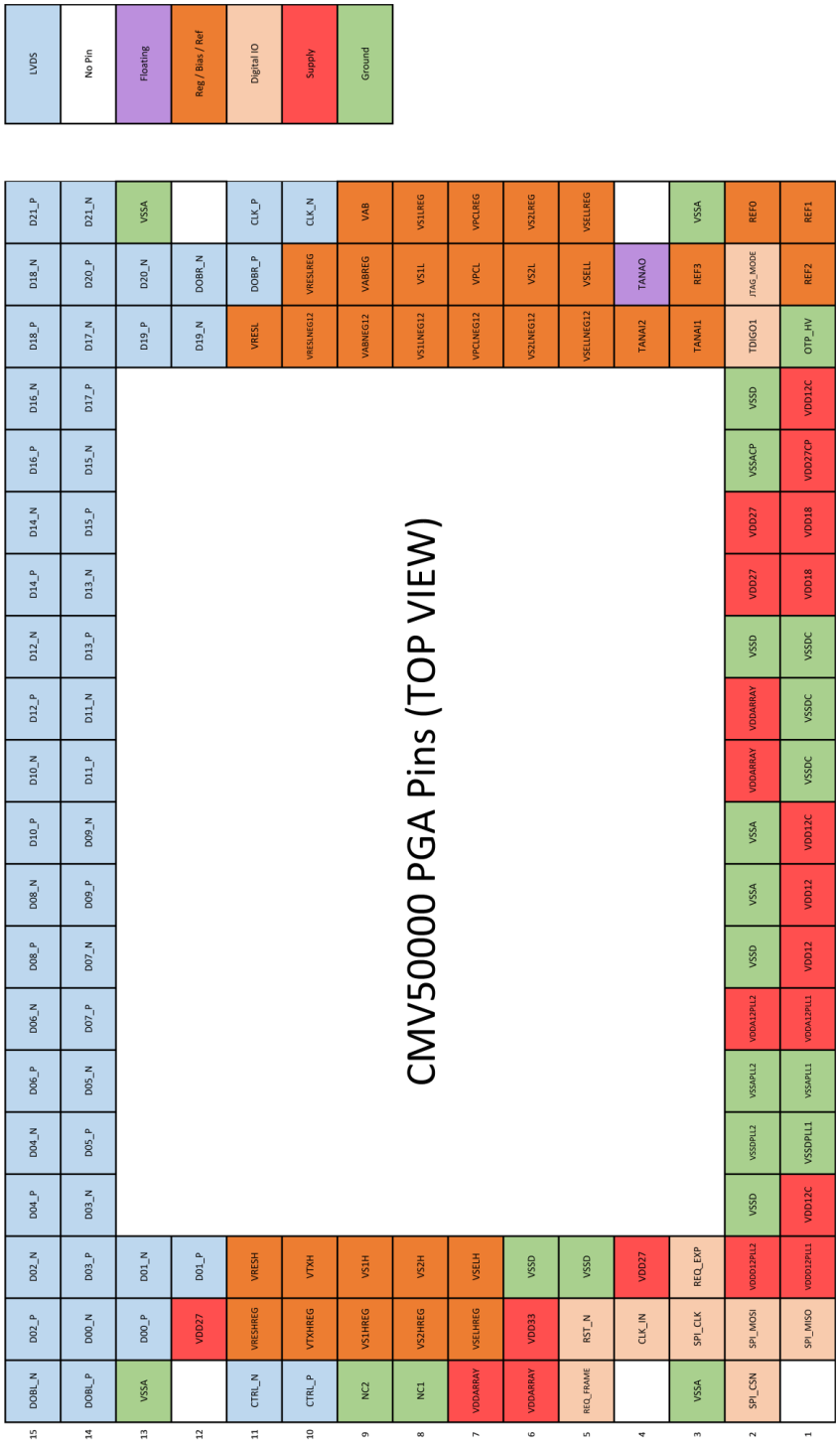
9.2 Socket

To avoid putting the sensor through the soldering heat (stressing the color filters and micro-lenses), it is advised to use a socket and place the sensor after the solder stage. Sockets for this device are available from Andon Electronics (www.andonelectronics.com) in both SMD (p/n: 575-20-19A-141-93M-R27-L14) and TH (p/n: 575-20-19A-141-01M-R27-L14) configuration.

Contact Andon Electronics directly for more information.

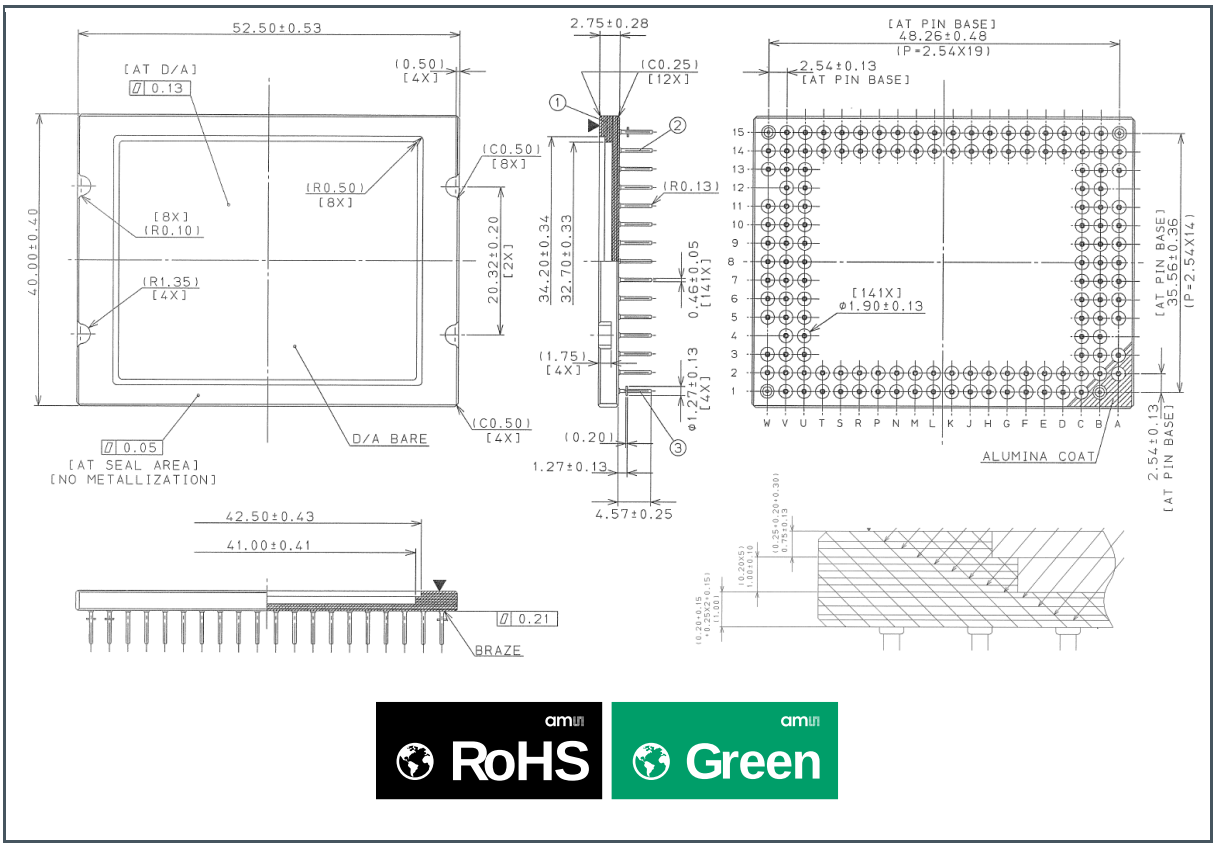
9.3 Pin Layout

Figure 198 :
Pin Layout from Top View



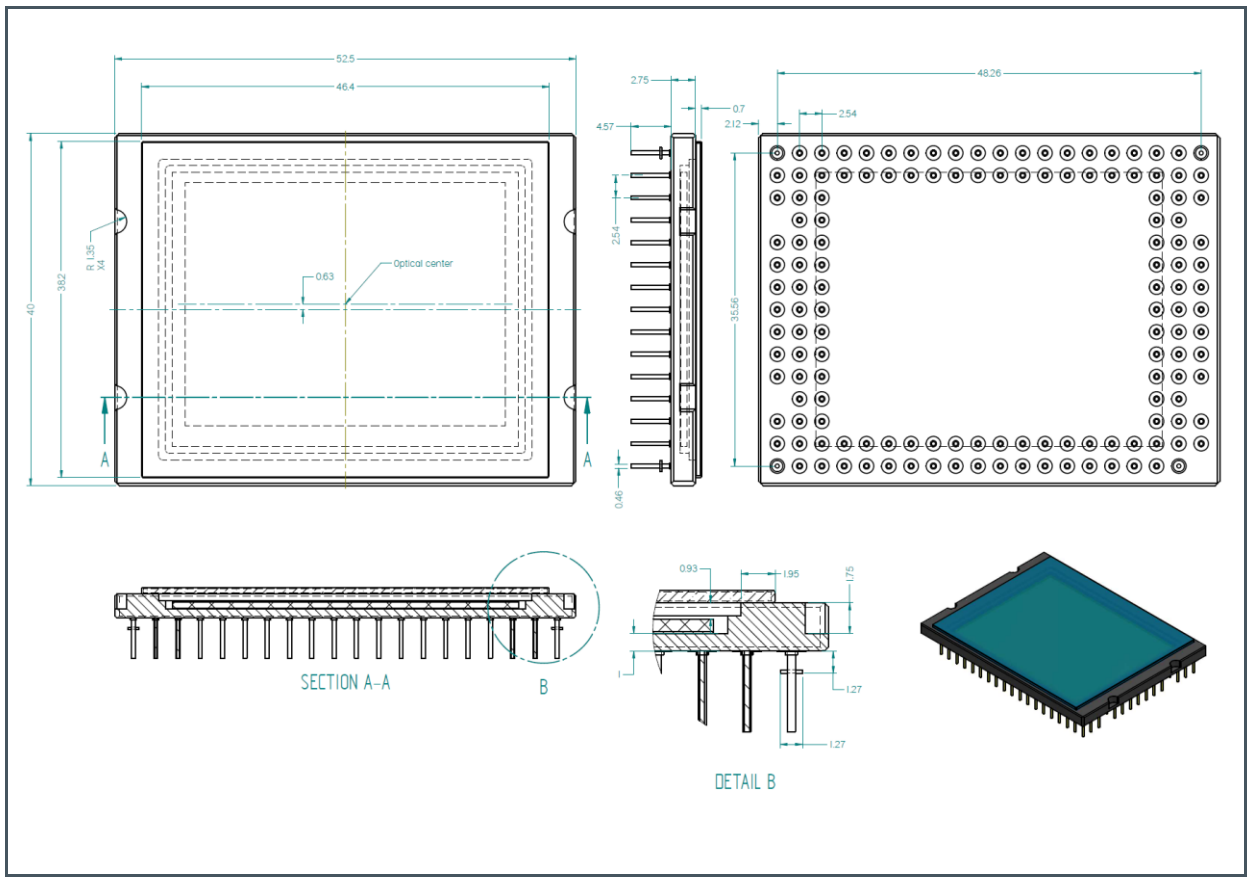
10 Package Drawings & Markings

Figure 199:
141-PGA Package Outline Drawing



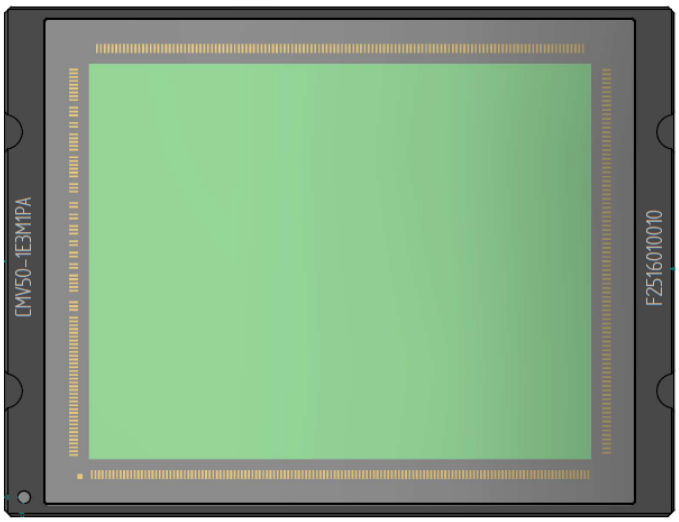
(1) All dimensions are in millimeters. Angles in degrees.
(2) Au plate 0.75µm min. over 2.0µm min Ni
(3) Unplated are on tip shall be less than Ø0.30 within 0.50 max from pin tip
(4) Materials: 1. Package: Alumina ceramic; 2. Pin: Alloy42; 3: Standoff pin: Alloy42
(5) Unless otherwise specified tolerances are ±1%; N.L.T: x.x ±0.25; x.xx ±0.13
(6) The package has a marking on top, in the left bottom corner, at pin A1 position
(7) This package contains no lead (Pb).
(8) This drawing is subject to change without notice.

Figure 200:
141-PGA Assembly Outline Drawing



(1) Die size: 39.4mm x 31.1mm, relative to the die SEAL ring edge, the dimensions after dicing will be typically larger.
(2) Optical center to die and package center offset: in X = 0, in Y = 628µm
(3) Die positioned in the middle of the package cavity
(4) Die placement accuracy: ±100µm
(5) Die rotation in package: max ±0.2°
(6) Die tilt towards cavity bottom: max ±0.1°
(7) Distance from the cavity bottom to the photosensitive pixel layer (top of the die): 0.86 ±0.06mm
(8) Distance from the top of the glass to the photosensitive pixel layer (top of the die): 1.65 ±0.20mm
(9) Glass lid positioned in the middle of the package;
(10) Glass size tolerance: ±0.1mm
(11) Glass thickness: 0.7 ±0.05mm
(12) Glass lid placement accuracy: ±200µm
(13) All dimensions are in millimeters. Angles in degrees.
(14) This package contains no lead (Pb).
(15) This drawing is subject to change without notice.
(16) The devices come covered with a heat resistant protective tape
(17) The 4 notches are not to be mechanically stressed! They can be used to measure the level and tilt of the cavity bottom (die attach surface).

Figure 201 :
141-PGA Package Marking/Code



11 Packing Information

The devices are shipped in JEDEC PGA matrix trays.

12 Soldering Information

Attention

Image sensors with color filter arrays (CFA) and micro lenses are especially sensitive to high temperatures. Prolonged heating at elevated temperatures may result in deterioration of the optical performance of the sensor.

A socket (see 9.2) is the safest way to avoid any thermal stress. When not using a socket, to avoid heating up the device we recommend to use manual hand soldering. Wave soldering can be used with precautions (see below). Reflow soldering is not recommended.

Manual soldering: Use partial heating method and use a soldering iron with temperature control. The soldering iron tip temperature is not to exceed 350°C with a 270°C maximum pin temperature. Touch for a 2 seconds maximum duration per pin. Avoid touching and global heating of the ceramic package during soldering. Failure to do so may alter device performance and reliability.

Wave soldering: Wave solder dipping can cause damage to the glass and harm the imaging capability of the device. Avoid the solder to come in contact with the glass or ceramic body.

13 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Changes from previous version to current revision v2-00	Page
Update Assembly Outline Drawing details 7, 8 (no physical change)	131

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

14 Legal Information

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- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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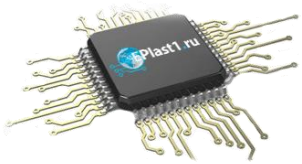
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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