REVISION HISTORY

32M Bits (2Mx16/4Mx8 Switchable)
AS6C3216A-55TIN 48pin-TSOPI PACKAGE

Revision	Details	Date
Rev 1.0	Initial Issue	Mar. 2017

FEATURES

- Fast access time : 55ns
- Low power consumption:
  Operating current : 12mA (TYP.)
  Standby current : 8µA(TYP.) SL-version
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control :
  (i) BYTE# fixed to V_{CC}
  DQ0 ~ DQ7 controlled by LB#,
  DQ8 ~ DQ15 controlled by UB#.
  (ii) BYTE# fixed to V_{SS}
  DQ15 used as address pin,
  while DQ8~DQ14 pins not used.
- Data retention voltage : 1.2V (MIN.)
- **Green package available**
- Package : 48-pin 12mm x 20mm TSOP I

GENERAL DESCRIPTION

The AS6C3216A-55TIN is a 33,554,432-bit low power CMOS static random access memory organized as 2,097,152 words by 16 bits or 4,194,304 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS6C3216A-55TIN is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The AS6C3216A-55TIN operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

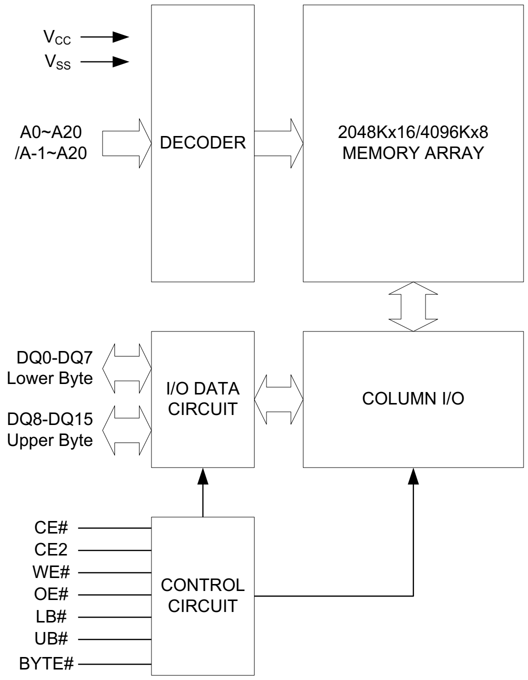
PRODUCT FAMILY

Product Family	Operating Temperature	V_{CC} Range	Speed	Power Dissipation	
				Standby(I_{SB1},TYP.)	Operating(I_{CC},TYP.)
AS6C3216A-55TIN	-40 ~ 85℃	2.7 ~ 3.6V	55ns	8µA(SL)	12mA

ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Alliance Memory Part Number
48-pin TSOP I (12mm x 20mm)	55	Special Ultra Low Power	-40°C~85°C	Tray	AS6C3216A-55TIN
				Tape Reel	AS6C3216A-55TINTR

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 – A20	Address Inputs(word mode)
A-1 – A20	Address Inputs(byte mode)
DQ0 – DQ15	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
BYTE#	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground

PIN CONFIGURATION

TSOP I

ABSOLUTE MAXIMUN RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to Vcc+0.5	V
Operating Temperature	T_A	-40 to 85(I grade)	℃
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	BYTE#	OE#	WE#	LB#	UB#	I/O OPERATION			SUPPLY CURRENT
								DQ0-DQ7	DQ8-DQ14	DQ15	
Standby	H	X	X	X	X	X	X	High – Z	High – Z	High – Z	I_{SB1}
	X	L	X	X	X	X	X	High – Z	High – Z	High – Z	
	X	X	H	X	X	H	H	High – Z	High – Z	High – Z	
Output Disable	L	H	H	H	H	L	X	High – Z	High – Z	High – Z	I_{CC},I_{CC1}
	L	H	H	H	H	X	L	High – Z	High – Z	High – Z	
	L	H	L	H	H	L	L	High – Z	High – Z	A-1	
Read	L	H	H	L	H	L	H	D_{OUT}	High – Z	High – Z	I_{CC},I_{CC1}
	L	H	H	L	H	H	L	High – Z	D_{OUT}	D_{OUT}	
	L	H	H	L	H	L	L	D_{OUT}	D_{OUT}	D_{OUT}	
Write	L	H	H	X	L	L	H	D_{IN}	High – Z	High – Z	I_{CC},I_{CC1}
	L	H	H	X	L	H	L	High – Z	D_{IN}	D_{IN}	
	L	H	H	X	L	L	L	D_{IN}	D_{IN}	D_{IN}	
Byte# Read	L	H	L	L	H	L	L	D_{OUT}	High – Z	A-1	I_{CC},I_{CC1}
Byte # Write	L	H	L	X	L	L	L	D_{IN}	High – Z	A-1	I_{CC},I_{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP.[4]	MAX.	UNIT
Supply Voltage	V_{CC}				2.7	3.0	3.6	V
Input High Voltage	V_{IH}[1]				2.2	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}[2]				- 0.2	-	0.6	V
Input Leakage Current	I_{LI}	$V_{CC} \geq V_{IN} \geq V_{SS}$			- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geq V_{OUT} \geq V_{SS}$ Output Disabled			- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -1mA			2.2	2.7	-	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA			-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = Min. CE# $\leq$ 0.2V and CE2 $\geq$ V_{CC}-0.2V $I_{I/O}$ = 0mA Other pins at 0.2V or V_{CC}-0.2V			-	12	20	mA
	I_{CC1}	Cycle time = 1µs CE# $\leq$ 0.2V and CE2 $\geq$ V_{CC}-0.2V $I_{I/O}$ = 0mA Other pins at 0.2V or V_{CC}-0.2V			-	3	5	mA
Standby Power Supply Current	I_{SB1}	CE# $\geq V_{CC}$-0.2V or CE2 $\leq$ 0.2V Other pins at 0.2V or V_{CC}-0.2V	-SL[5]	25℃	-	8	18	µA
			-SLI[5]	40℃	-	8	20	µA
			-SL[6]		-	-	50	µA
			-SLI[7]		-	-	80	µA

Notes:
1. $V_{IH(max)} = V_{CC}$ + 2.0V for pulse width less than 6ns.
2. $V_{IL(min)} = V_{SS}$ - 2.0V for pulse width less than 6ns.
3. Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
4. Typical values, measured at $V_{CC} = V_{CC}$(TYP.) and T_A = 25℃, are included for reference only and are not guaranteed or tested.
5. This parameter is measured at V_{CC}=3.0V.
6. This parameter is measured at T_A = 70℃
7. This parameter is measured at T_A = 85℃

CAPACITANCE (T_A = 25℃, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V_{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	AS6C3216A-55TIN		UNIT
		MIN.	MAX.	
Read Cycle Time	t_{RC}	55	-	ns
Address Access Time	t_{AA}	-	55	ns
Chip Enable Access Time	t_{ACE}	-	55	ns
Output Enable Access Time	t_{OE}	-	30	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	20	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	20	ns
Output Hold from Address Change	t_{OH}	10	-	ns
LB#, UB# Access Time	t_{BA}	-	55	ns
LB#, UB# to High-Z Output	t_{BHZ}*	-	20	ns
LB#, UB# to Low-Z Output	t_{BLZ}*	10	-	ns

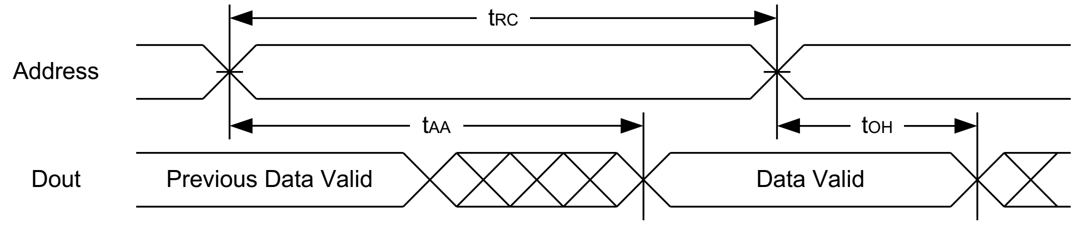
(2) WRITE CYCLE

PARAMETER	SYM.	AS6C3216A-55TIN		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	55	-	ns
Address Valid to End of Write	t_{AW}	50	-	ns
Chip Enable to End of Write	t_{CW}	50	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Write Pulse Width	t_{WP}	45	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Data to Write Time Overlap	t_{DW}	25	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	ns
Output Active from End of Write	t_{OW}*	5	-	ns
Write to Output in High-Z	t_{WHZ}*	-	20	ns
LB#, UB# Valid to End of Write	t_{BW}	50	-	ns

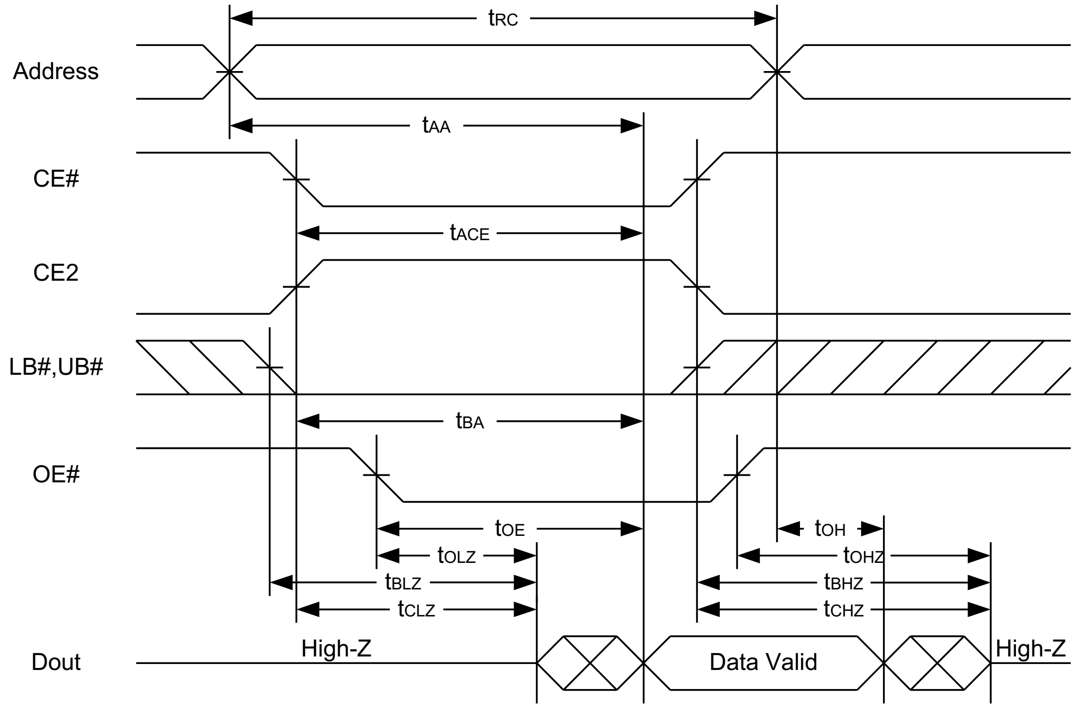
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

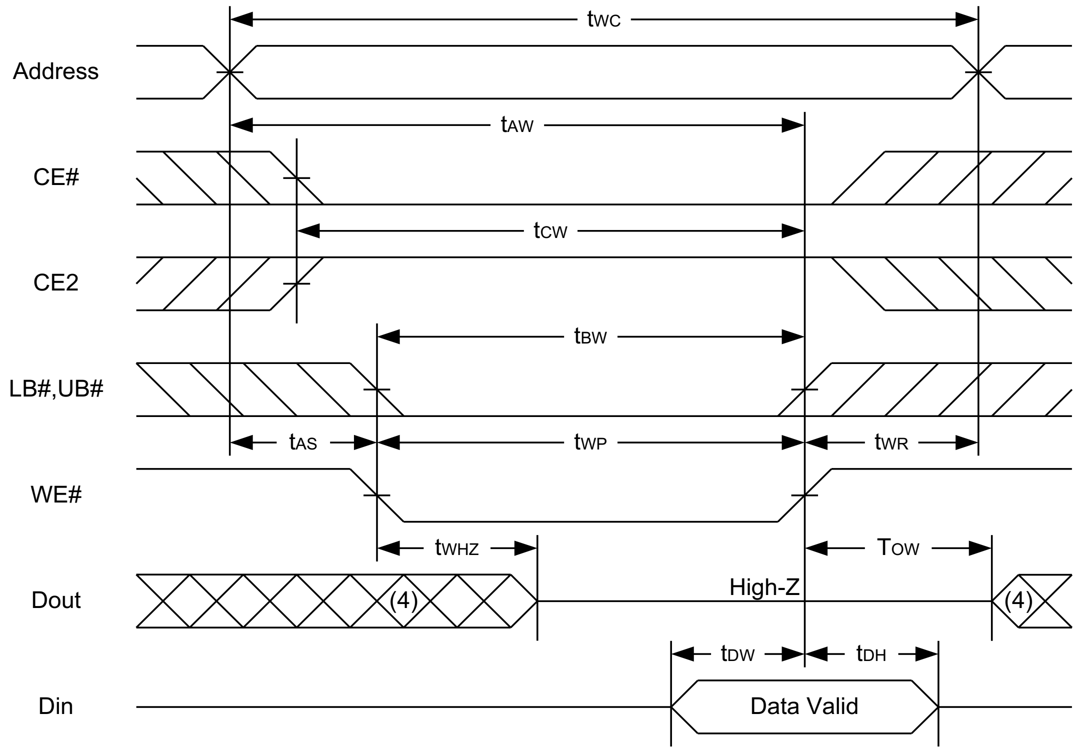


READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

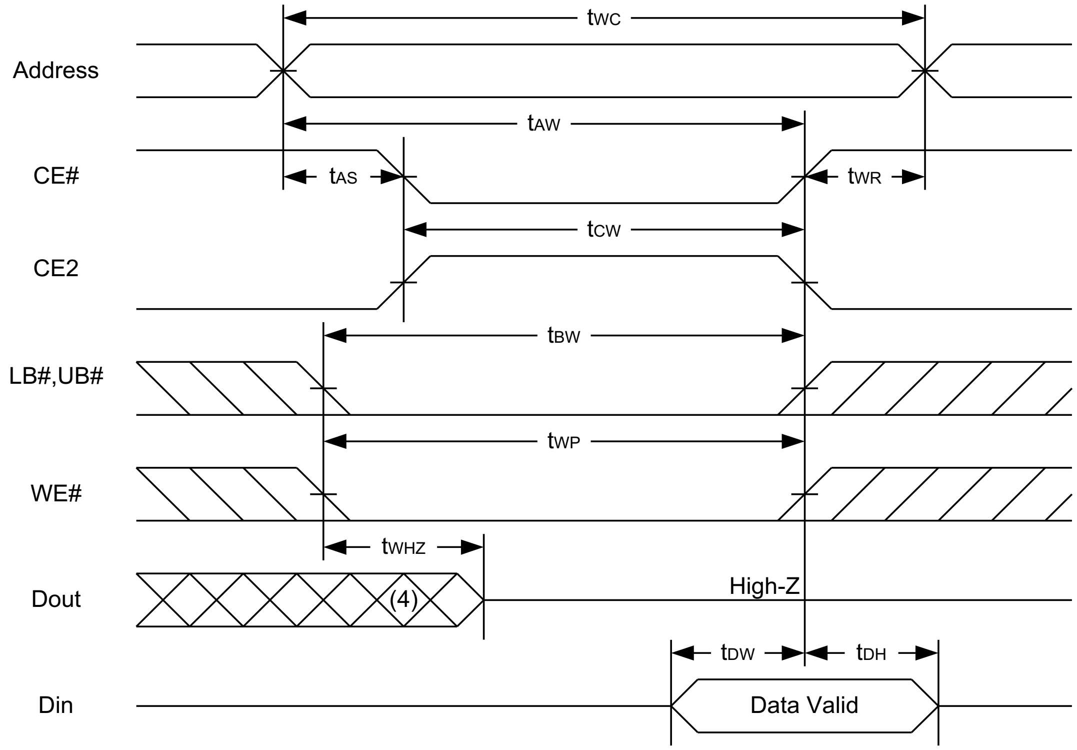


Notes :
1.WE# is high for read cycle.
2.Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low.
3.Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4.t_{CLZ}, t_{BLZ}, t_{OLZ}, t_{CHZ}, t_{BHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
5.At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ}, t_{OHZ} is less than t_{OLZ}.

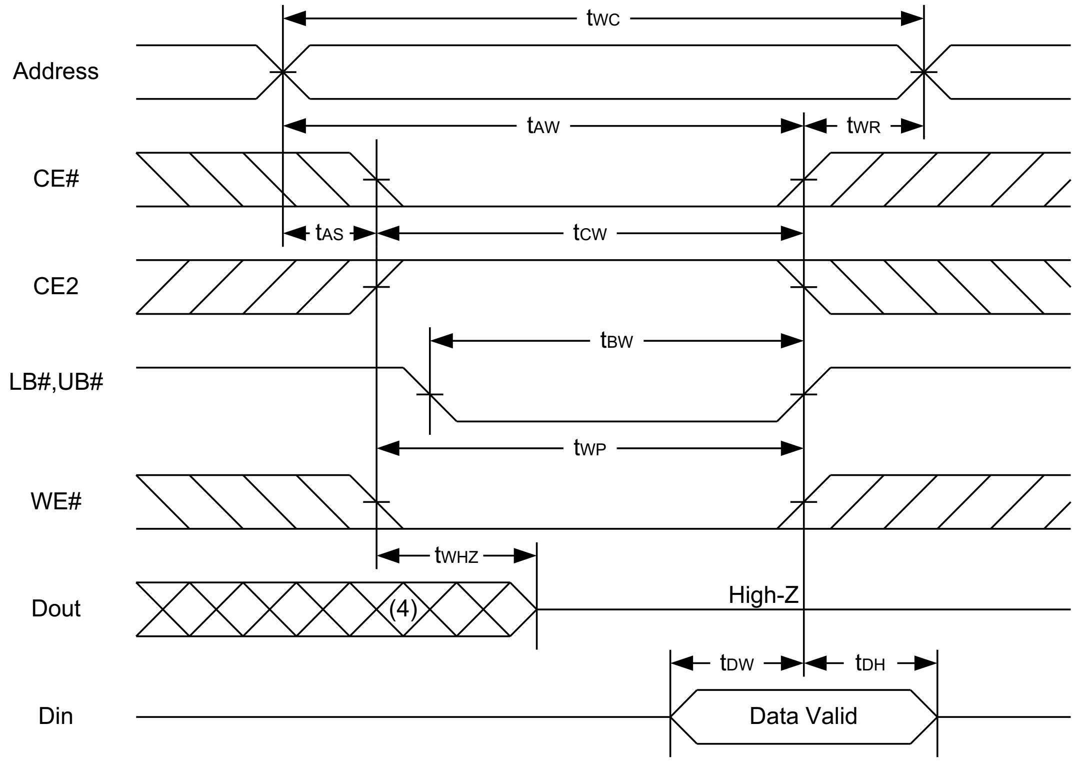
WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)



WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)



Notes :

1.A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.

2.During a WE# controlled write cycle with OE# low, t_{WP} must be greater than t_{WHZ} + t_{DW} to allow the drivers to turn off and data to be placed on the bus.

3.During this period, I/O pins are in the output state, and input signals must not be applied.

4.If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.

5.t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

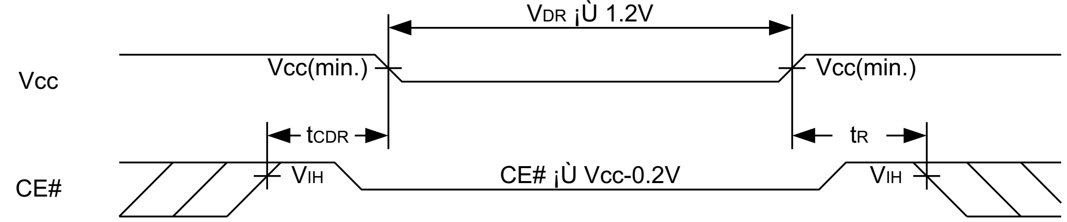
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE#≧V_{CC} - 0.2V or CE2≦0.2V			1.2	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 1.2V CE# ≧V_{CC}-0.2V or CE2≦0.2V other pins at 0.2V or V_{CC}-0.2V	-SL	25℃	-	6.5	16	μA
			-SLI	40℃	-	6.5	20	μA
			-SL		-	-	50	μA
			-SLI		-	-	80	μA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)			0	-	-	ns
Recovery Time	t_R				t_{RC*}	-	-	ns

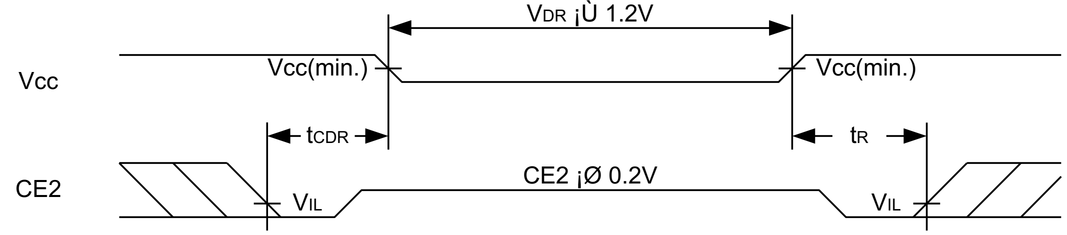
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

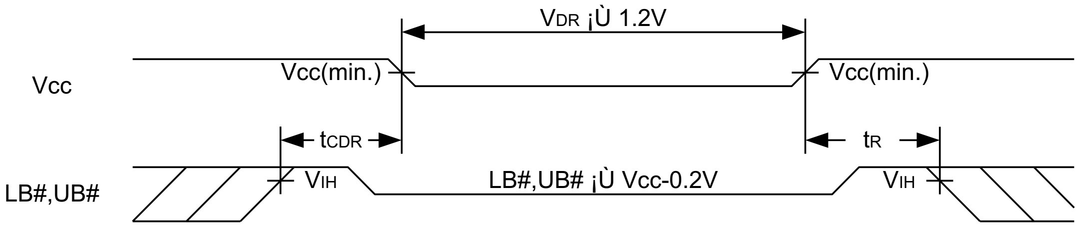
Low Vcc Data Retention Waveform (1) (CE# controlled)



Low Vcc Data Retention Waveform (2) (CE2 controlled)

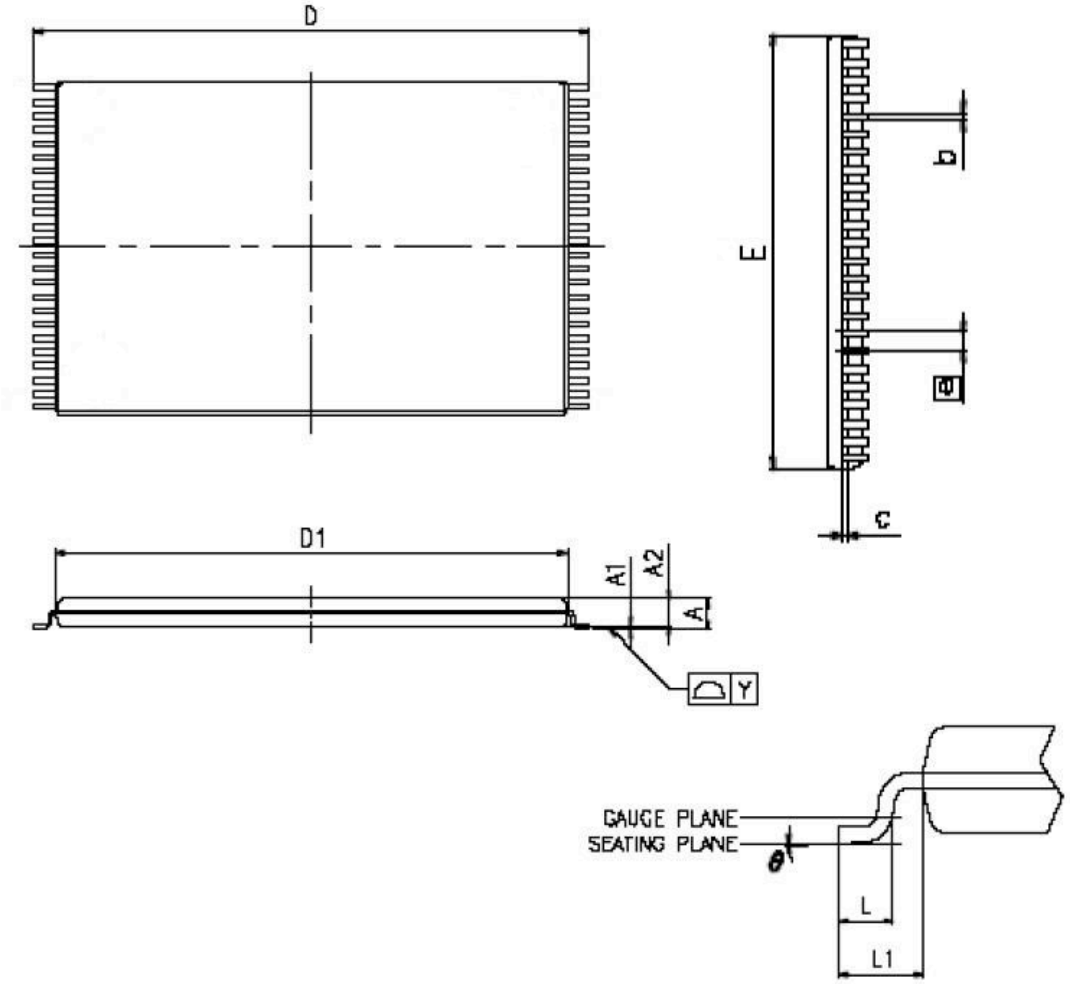


Low Vcc Data Retention Waveform (3) (LB#, UB# controlled)



PACKAGE OUTLINE DIMENSION

48-pin 12mm x 20mm TSOP I Package Outline Dimension



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

	SYMBOLS	MIN.	NOM.	MAX
	A	–	–	1.20
	A1	0.05	–	0.15
	A2	0.95	1.00	1.05
	b	0.17	0.22	0.27
	c	0.10	–	0.21
⚠	D	19.80	20.00	20.20
⚠	D1	18.30	18.40	18.50
⚠	E	11.90	12.00	12.10
	e	0.50 BASIC		
	L	0.50	0.60	0.70
⚠	L1	–	0.80	–
⚠	Y	–	–	0.10
⚠	θ	0°	–	5°

NOTES:

1 JEDEC OUTLINE : MO-142 DD

2.PROFILE TOLERANCE ZONES FOR D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.

3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUN MATERIAL CONDITION DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

PART NUMBERING SYSTEM

AS6C	3216A	55	T	I	N
SRAM	32 = 32M 16 = x16 A = A die	55=55ns	T = TSOPI	I=Industrial (-40° C~+85° C)	Indicates Pb and Halogen Free

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- Поставка более 17-ти миллионов наименований электронных компонентов;
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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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