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October 1995 Revised August 2004

#### NC7S02

## TinyLogic® HS 2-Input NOR Gate

#### **General Description**

The NC7S02 is a single 2-Input high performance CMOS NOR Gate. Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation over a broad  $V_{CC}$  range. ESD protection diodes inherently guard both inputs and output with respect to the  $V_{CC}$  and GND rails. Three stages of gain between inputs and outputs assures high noise immunity and reduced sensitivity to input edge rate.

#### **Features**

- Space saving SOT23 or SC70 5-lead packages
- Ultra small MicroPak™ leadless package
- High Speed; t<sub>PD</sub> 3.5 ns typ
- $\blacksquare$  Low Quiescent Power;  $I_{CC} < 1~\mu\text{A}$
- Balanced Output Drive; 2 mA I<sub>OL</sub>, -2 mA I<sub>OH</sub>
- Broad V<sub>CC</sub> Operating Range; 2V–6V
- Balanced Propagation Delays
- Specified for 3V operation

#### **Ordering Code:**

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7S02M5X	MA05B	7S02	5-Lead SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel
NC7S02P5X	MAA05A	S02	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel
NC7S02L6X	MAC06A	E4	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

### **Logic Symbol**



#### **Pin Descriptions**

Pin Names	Description
A, B	Inputs
Y	Output
NC	No Connect

#### **Function Table**

$$Y = \overline{A + B}$$

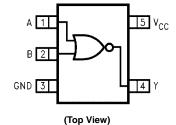
Inp	Output				
Α	A B				
L	L	Н			
L	Н	L			
Н	L	L			
Н	Н	L			

H = HIGH Logic Level L = LOW Logic Level

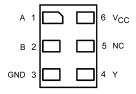
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#### **Connection Diagrams**

#### Pin Assignments for SOT23 and SC70



#### Pad Assignments for MicroPak



(Top Through View)

#### **Absolute Maximum Ratings**(Note 1)

# $$\begin{split} & \text{Supply Voltage (V}_{CC}) & -0.5 \text{V to } +7.0 \text{V} \\ & \text{DC Input Diode Current (I}_{IK}) \\ & @ V_{IN} \leq -0.5 \text{V} & -20 \text{ mA} \\ & @ V_{IN} \geq V_{CC} +0.5 \text{V} & +20 \text{ mA} \\ & \text{DC Input Voltage (V}_{IN}) & -0.5 \text{V to } V_{CC} +0.5 \text{V} \end{split}$$

DC Output Diode Current (I<sub>OK</sub>)

 $\begin{tabular}{llll} @ V_{OUT} < -0.5V & -20 \ mA \\ \hline @ V_{OUT} > V_{CC} + 0.5V & +20 \ mA \\ \hline DC Output Voltage (V_{OUT}) & -0.5V \ to \ V_{CC} + 0.5V \\ \hline \end{tabular}$ 

DC Output Source

or Sink Current ( $I_{OUT}$ )  $\pm 12.5 \text{ mA}$ 

DC  $V_{CC}$  or Ground Current

per Output Pin ( $I_{CC}$  or  $I_{GND}$ )  $\pm 25$  mA Storage Temperature ( $T_{STG}$ )  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ 

Junction Temperature (T<sub>J</sub>) 150°C

Lead Temperature (T<sub>L</sub>)

(Soldering, 10 seconds) 260°C

Power Dissipation (PD) @  $+85^{\circ}$ C

SOT23-5 200 mW SC70-5 150 mW

# Recommended Operating Conditions (Note 2)

Thermal Resistance ( $\theta_{JA}$ )

SOT23-5 300°C/W SC70-5 425°C/W

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

#### **DC Electrical Characteristics**

Symbol	Parameter	v <sub>cc</sub>	•	Γ <sub>A</sub> = +25°(	;	$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Units	Conditions	
Syllibol	raiametei	(V)	Min	Тур	Max	Min	Max	Units	Conditions	
V <sub>IH</sub>	HIGH Level Input Voltage	2.0	1.50			1.50		V		
		3.0-6.0	0.7 V <sub>CC</sub>			0.7 V <sub>CC</sub>		V		
V <sub>IL</sub>	LOW Level Input Voltage	2.0			0.50		0.50	V		
		3.0-6.0			$0.3\mathrm{V}_{\mathrm{CC}}$		$0.3\mathrm{V}_{\mathrm{CC}}$	V		
V <sub>OH</sub>	HIGH Level Output Voltage	2.0	1.90	2.0		1.90				
		3.0	2.90	3.0		2.90		V	$I_{OH} = -20 \mu A$	
		4.5	4.40	4.5		4.40		V	$V_{IN} = V_{IL}$	
		6.0	5.90	6.0		5.90				
									$V_{IN} = V_{IL}$	
		3.0	2.68	2.85		2.63		V	$I_{OH} = -1.3 \text{ mA}$	
		4.5	4.18	4.35		4.13		V	$I_{OH} = -2 \text{ mA}$	
		6.0	5.68	5.85		5.63			$I_{OH} = -2.6 \text{ mA}$	
V <sub>OL</sub>	LOW Level Output Voltage	2.0		0.0	0.10		0.10			
		3.0		0.0	0.10		0.10	V	$I_{OL} = 20 \ \mu A$	
		4.5		0.0	0.10		0.10	V	$V_{IN} = V_{IH}$	
		6.0		0.0	0.10		0.10			
									$V_{IN} = V_{IH}$	
		3.0		0.1	0.26		0.33	V	$I_{OL} = 1.3 \text{ mA}$	
		4.5		0.1	0.26		0.33	v I	$I_{OL} = 2 \text{ mA}$	
		6.0		0.1	0.26		0.33		I <sub>OL</sub> = 2.6 mA	
I <sub>IN</sub>	Input Leakage Current	6.0			±0.1		±1.0	μΑ	$V_{IN} = V_{CC}$ , GND	
I <sub>CC</sub>	Quiescent Supply Current	6.0			1.0		10.0	μΑ	$V_{IN} = V_{CC}$ , GND	

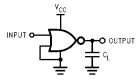
#### **AC Electrical Characteristics**

Symbol	Parameter	v <sub>cc</sub>		T <sub>A</sub> = +25°C		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions	Figure
Symbol	raiailletei	(V)	Min	Тур	Max	Min	Max	Units	Conditions	Number
t <sub>PLH</sub> ,	Propagation Delay	5.0		3.5	15			ns	$C_L = 15 pF$	
t <sub>PHL</sub>		2.0		19	100		125			1
		3.0		10.5	27		35		C 50 = E	Figures 1, 3
		4.5		7.5	20		25	ns	$C_L = 50 \text{ pF}$	1, 3
		6.0		6.5	17 21					
t <sub>TLH</sub> ,	Output Transition Time	5.0		3	10			ns	C <sub>L</sub> = 15 pF	
$t_{THL}$		2.0		25	125		155			1
		3.0		16	35		45		$C_1 = 50 \text{ pF}$	Figures 1, 3
		4.5		11	25		31	ns	CL = 50 pr	., 0
		6.0		9	21		26			
C <sub>IN</sub>	Input Capacitance	Open		2	10		10	pF		
C <sub>PD</sub>	Power Dissipation Capacitance	5.0		6				pF	(Note 3)	Figure 2

Note 3: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I<sub>CCD</sub>) at no output loading and operating at 50% duty cycle. (See Figure 2.) C<sub>PD</sub> is related to I<sub>CCD</sub> dynamic operating current by the expression:

I<sub>CCD</sub> = (C<sub>PD</sub>)(V<sub>CC</sub>)(f<sub>IN</sub>) + (I<sub>CC</sub>static).

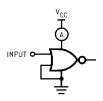
## **AC Loading and Waveforms**



C<sub>L</sub> includes load and stray capacitance

Input PRR = 1.0 MHz;  $t_w = 500 \text{ ns}$ 

FIGURE 1. AC Test Circuit



Input = AC Waveform;

PRR = variable; Duty Cycle = 50%

FIGURE 2.  $I_{\rm CCD}$  Test Circuit

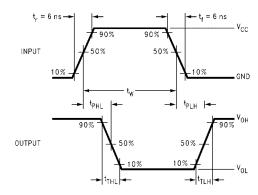
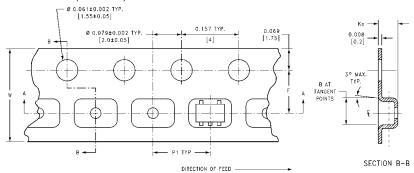


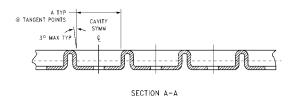
FIGURE 3. AC Waveforms

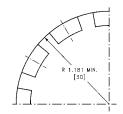
# Tape and Reel Specification TAPE FORMAT for SOT23 and SC70

Package	Tape	Number	Cavity	Cover Tape
Designator	Section	Cavities	Status	Status
	Leader (Start End)	125 (typ)	Empty	Sealed
M5X, P5X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

#### TAPE DIMENSIONS inches (millimeters)



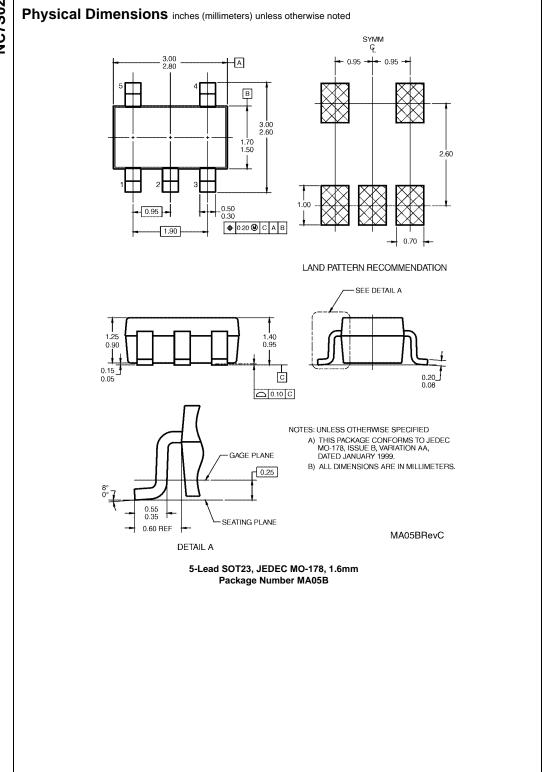


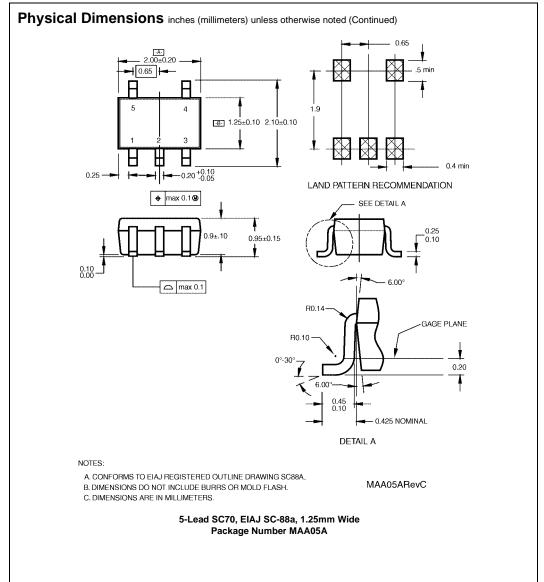


BEND RADIUS NOT TO SCALE

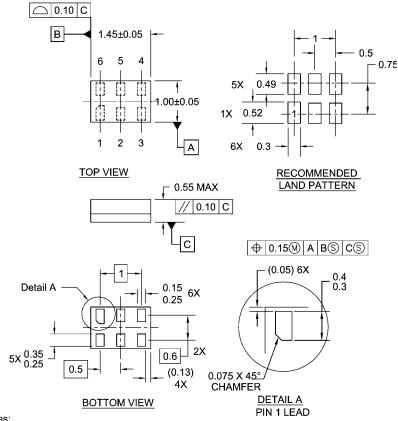
Package	Tape Size	DIM A	DIM B	DIM F	DIM K <sub>o</sub>	DIM P1	DIM W
SC70-5	8 mm	0.093	0.096	$0.138 \pm 0.004$	$0.053 \pm 0.004$	0.157	$0.315 \pm 0.004$
		(2.35)	(2.45)	$(3.5 \pm 0.10)$	$(1.35 \pm 0.10)$	(4)	(8 ± 0.1)
SOT23-5	8 mm	0.130	0.130	$0.138 \pm 0.002$	$0.055 \pm 0.004$	0.157	$0.315 \pm 0.012$
		(3.3)	(3.3)	$(3.5 \pm 0.05)$	$(1.4 \pm 0.11)$	(4)	$(8 \pm 0.3)$

#### Tape and Reel Specification (Continued) TAPE FORMAT for MicroPak Tape Package Number Cavity Cover Tape Designator Cavities Status Section Status Leader (Start End) 125 (typ) Empty Sealed L6X 5000 Filled Sealed Trailer (Hub End) 75 (typ) Empty Sealed 1.75±0.10 8.00 <sup>+0.30</sup> -0.10 3.50±0.05 1.15±0.05 0 В -ø 0.50 ±0.05 SECTION B-B DIRECTION OF FEED SCALE:10X 0.254±0.020 ┌ 0.70±0.05 1.60±0.05 SECTION A-A SCALE:10X **REEL DIMENSIONS** inches (millimeters) TAPE SLOT DETAIL X DETAIL X SCALE: 3X Tape В С D N W1 W2 W3 7.0 0.059 0.512 0.795 2.165 0.331 + 0.059/-0.000 0.567 W1 + 0.078/-0.039 8 mm (177.8)(1.50)(13.00)(20.20)(55.00)(8.40 + 1.50 / -0.00)(14.40)(W1 + 2.00/-1.00)





#### Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



#### Notes:

- 1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED
- 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

6-Lead MicroPak, 1.0mm Wide Package Number MAC06A

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**Телефон:** 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: <u>org@eplast1.ru</u>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина,

дом 2, корпус 4, литера А.