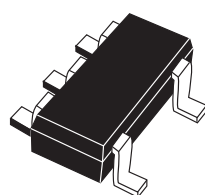


5-pin supervisor with watchdog timer and push-button reset

Datasheet - production data



SOT23-5 (WY)

Features

- Precision V_{CC} monitoring of 5, 3.3, 3, or 2.5 V power supplies
- \overline{RST} outputs (active low, push-pull or open drain)
- RST outputs (active high, push-pull)
- Reset pulse width of 1.4 ms, 200 ms and 240 ms (typ.)
- Watchdog timeout period of 1.6 s (typ.)
- Manual reset input (\overline{MR})
- Low supply current - 3 μ A (typ.)
- Guaranteed \overline{RST} (RST) assertion down to $V_{CC} = 1.0$ V
- Operating temperature: -40 to $+85$ °C (industrial grade)
- RoHS compliance
Lead-free components are compliant with the RoHS directive

Table 1. Device summary

| Part number | | Watchdog input | Manual reset input | Reset output | | |
|-------------|---------|----------------|--------------------|------------------------|-------------------------|-------------------------|
| | | | | Active low (push-pull) | Active high (push-pull) | Active low (open drain) |
| STM632x | STM6321 | ✓ | | | ✓ | ✓ |
| | STM6322 | | ✓ | | ✓ | ✓ |
| STM682x | STM6821 | ✓ | ✓ | | ✓ | |
| | STM6822 | ✓ | ✓ | | | ✓ |
| | STM6823 | ✓ | ✓ | ✓ | | |
| | STM6824 | ✓ | | ✓ | ✓ | |
| | STM6825 | | ✓ | ✓ | ✓ | |

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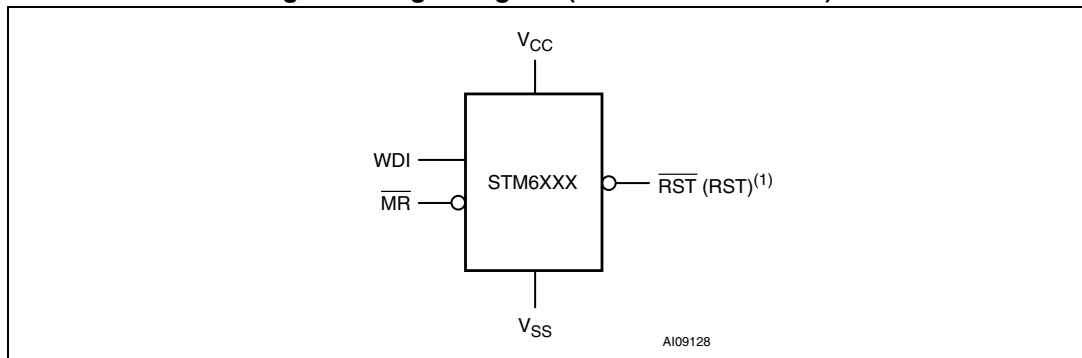
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1 Description

The STM6xxx supervisors are self-contained devices which provide microprocessor supervisory functions. A precision voltage reference and comparator monitors the V_{CC} input for an out-of-tolerance condition. When an invalid V_{CC} condition occurs, the reset output (\overline{RST}) is forced low (or high in the case of RST). These devices also offer a watchdog timer (except for STM6322/6825) and/or a push-button (\overline{MR}) reset input.

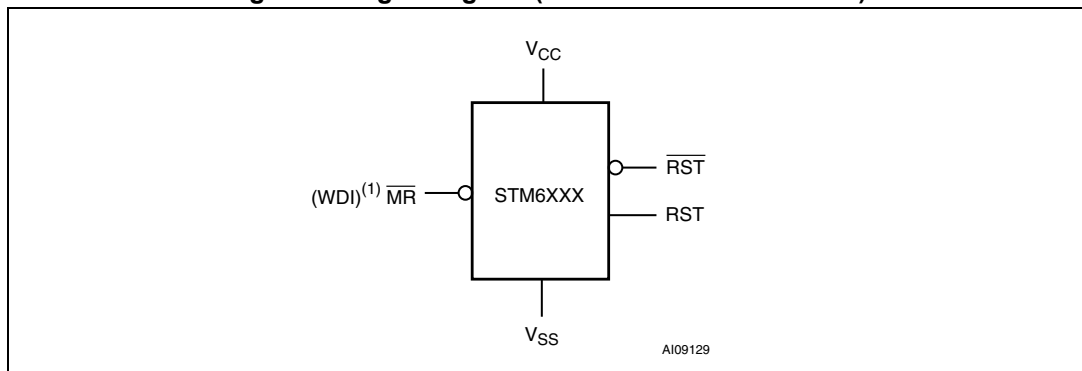
These devices are available in a standard 5-pin SOT23 package.

Figure 1. Logic diagram (STM6821/6822/6823)



1. For STM6821 only.

Figure 2. Logic diagram (STM6321/6322/6824/6825)



1. For STM6321/6824.

Table 2. Signal names

| Name | Function |
|------------------|--------------------------|
| \overline{MR} | Push-button reset input |
| WDI | Watchdog input |
| \overline{RST} | Active low reset output |
| RST | Active high reset output |
| V_{CC} | Supply voltage |
| V_{SS} | Ground |

Figure 3. STM6822/6823 SOT23-5 connections



- 1. Open drain for STM6822.

Figure 4. STM6821 SOT23-5 connections



- 1. Push-pull only.

Figure 5. STM6322/6825 SOT23-5 connections



- 1. Open drain for STM6322.
- 2. Push-pull only.

Figure 6. STM6321/6824 SOT23-5 connections



- 1. Open drain for STM6321.
- 2. Push-pull only.

1.1 Pin description

1.1.1 Active low, push-pull reset output ($\overline{\text{RST}}$) - 6823/6824/6825

Pulses low when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{\text{MR}}$ is a logic low. It remains low for t_{rec} after either V_{CC} rises above the reset threshold, the watchdog triggers a reset, or $\overline{\text{MR}}$ goes from low to high.

1.1.2 Active low, open drain reset output ($\overline{\text{RST}}$) - STM6321/6322/6822

Pulses low when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{\text{MR}}$ is a logic low. It remains low for t_{rec} after either V_{CC} rises above the reset threshold, the watchdog triggers a reset, or $\overline{\text{MR}}$ goes from low to high. Connect a pull-up resistor to supply voltage.

1.1.3 Push-button reset input ($\overline{\text{MR}}$)

A logic low on $\overline{\text{MR}}$ asserts the reset output. Reset remains asserted as long as $\overline{\text{MR}}$ is low and for t_{rec} after $\overline{\text{MR}}$ returns high. This active low input has an internal 52 k Ω pull-up. It can be driven from a TTL or CMOS logic line, or shorted to ground with a switch. Leave open if unused.

1.1.4 Watchdog input (WDI)

If WDI remains high or low for at least 1.6 s, the internal watchdog timer expires and reset is asserted. The internal watchdog timer clears while reset is asserted or when WDI sees a rising or falling edge. The watchdog function **CAN** be disabled if WDI is left unconnected or is connected to a tristate buffer output.

1.1.5 Active high reset output (RST)

Active high, push-pull reset output; inverse of $\overline{\text{RST}}$.

Table 3. Pin function

| Pin | | | | Name | Function |
|--------------------|---------|--------------------|--------------------|-------------------------|--------------------------|
| STM6822 STM6823 | STM6821 | STM6321 STM6824 | STM6322 STM6825 | | |
| 1 | — | 1 | 1 | $\overline{\text{RST}}$ | Active low reset output |
| 3 | 3 | — | 4 | $\overline{\text{MR}}$ | Push-button reset input |
| 4 | 4 | 4 | — | WDI | Watchdog Input |
| — | 1 | 3 | 3 | RST | Active high reset output |
| 5 | 5 | 5 | 5 | V_{CC} | Supply voltage |
| 2 | 2 | 2 | 2 | V_{SS} | Ground |

Figure 7. Block diagram (STM6821/6822/6823)



1. Push-pull for STM6823, open drain for STM6822.
2. Active high (push-pull) for STM6821.

Figure 8. Block diagram (STM6321/6824)



1. Active low (open drain) for STM6321, active low (push-pull) for STM6824.
2. Push-pull only.

Figure 9. Block diagram (STM6322/6825)



1. Active low (open drain) for STM6322, active low (push-pull) for STM6825.
2. Push-pull only.

Figure 10. Hardware hookup



1. For STM6321/6821/6822/6823/6824.
2. For STM6322/6821/6822/6823/6825.
3. For STM6821/ (RST output only).
4. For STM6321/6322/6824/6825 (both RST and $\overline{\text{RST}}$ outputs).

2 Operation

2.1 Reset output

The STM6xxx supervisor asserts a reset signal to the MCU whenever V_{CC} goes below the reset threshold (V_{RST}), a watchdog timeout occurs, or when the push-button reset input (\overline{MR}) is taken low. Reset is guaranteed valid for $V_{CC} < V_{RST}$ down to $V_{CC} = 1\text{ V}$ for $T_A = 0$ to $85\text{ }^\circ\text{C}$.

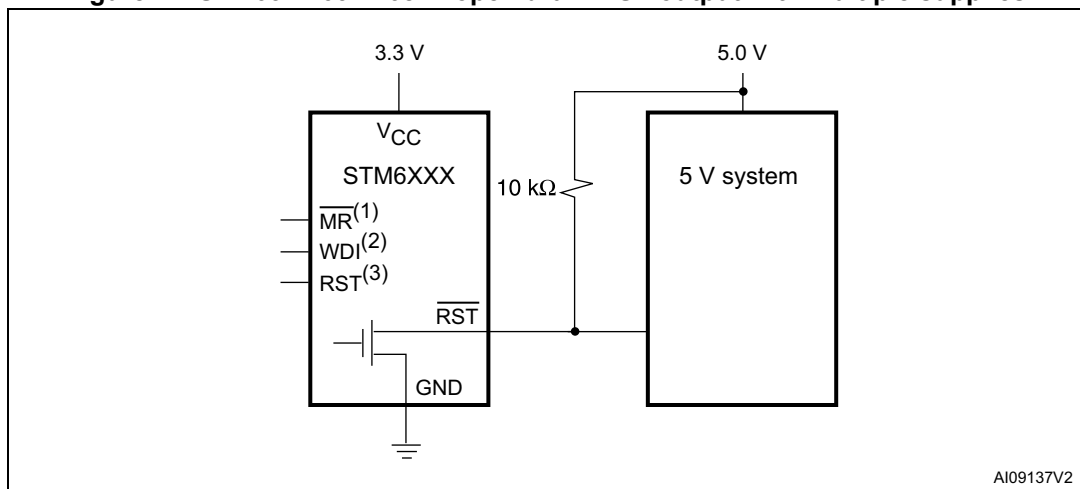
During power-up, once V_{CC} exceeds the reset threshold an internal timer keeps reset low for the reset timeout period, t_{rec} . After this interval reset is de-asserted.

Each time \overline{RST} is asserted, it stays low for at least the reset timeout period (t_{rec}). Any time V_{CC} goes below the reset threshold the internal timer clears. The reset timer starts when V_{CC} returns above the reset threshold.

2.2 Open drain \overline{RST} output

The STM6321/6322/6822 have an active low, open drain reset output. This output structure will sink current when \overline{RST} is asserted. Connect a pull-up resistor from \overline{RST} to any supply voltage up to 6 V (see [Figure 11](#)). Select a resistor value large enough to register a logic low, and small enough to register a logic high while supplying all input current and leakage paths connected to the reset output line. A 10 k Ω pull-up resistor is sufficient in most applications.

Figure 11. STM6321/6322/6822 open drain \overline{RST} output with multiple supplies



AI09137V2

1. STM6322/6822.
2. STM6321/6822.
3. STM6321/6322.

2.3 Push-button reset input (STM6322/6821/6822/6823/6825)

A logic low on \overline{MR} asserts reset. Reset remains asserted while \overline{MR} is low, and for t_{rec} (see [Figure 25 on page 19](#)) after it returns high. The MR input has an internal 52 k Ω pull-up resistor, allowing it to be left open if not used. This input can be driven with TTL/CMOS-logic levels or with open drain/collector outputs. Connect a normally open momentary switch from \overline{MR} to GND to create a manual reset function; external debounce circuitry is not required. If \overline{MR} is driven from long cables or the device is used in a noisy environment, connect a 0.1 μ F capacitor from MR to GND to provide additional noise immunity. MR may float, or be tied to V_{CC} when not used.

2.4 Watchdog input (STM6321/6821/6822/6823/6824)

The watchdog timer can be used to detect an out-of-control MCU. If the MCU does not toggle the Watchdog Input (WDI) within t_{WD} (1.6 sec), the reset is asserted. The internal watchdog timer is cleared by either:

1. a reset pulse, or
2. by toggling WDI (high to low or low to high), which can detect pulses as short as 50 ns.

The timer remains cleared and does not count for as long as reset is asserted. As soon as reset is released, the timer starts counting.

Note: The watchdog function may be disabled by floating WDI or tristating the driver connected to WDI. When tristated or disconnected, the maximum allowable leakage current is 10 μ A and the maximum allowable load capacitance is 200 pF.

2.5 Applications information

2.5.1 Watchdog input current

The WDI input is internally driven through a buffer and series resistor from the watchdog counter. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog timeout period. When high, WDI can draw as much as 160 μ A. Pulsing WDI high at a low duty cycle will reduce the effect of the large input current. When WDI is left unconnected, the watchdog timer is serviced within the watchdog timeout period by a low-high-low pulse from the counter chain.

2.5.2 Ensuring a valid reset output down to $V_{CC} = 0$ V

The STM6xxx supervisors are guaranteed to operate properly down to $V_{CC} = 1$ V. In applications that require valid reset levels down to $V_{CC} = 0$, a pull-down resistor to active low outputs (push/pull only, see [Figure 12 on page 12](#)) and a pull-up resistor to active high outputs (push/pull only, see [Figure 13 on page 12](#)) will ensure that the reset line is valid while the reset output can no longer sink or source current. This scheme does not work with the open drain outputs of the STM6321/6322/6822.

The resistor value used is not critical, but it must be large enough not to load the reset output when V_{CC} is above the reset threshold. For most applications, 100 k Ω is adequate.

Figure 12. Ensuring $\overline{\text{RST}}$ valid to $V_{\text{CC}} = 0$, (active low push-pull outputs)

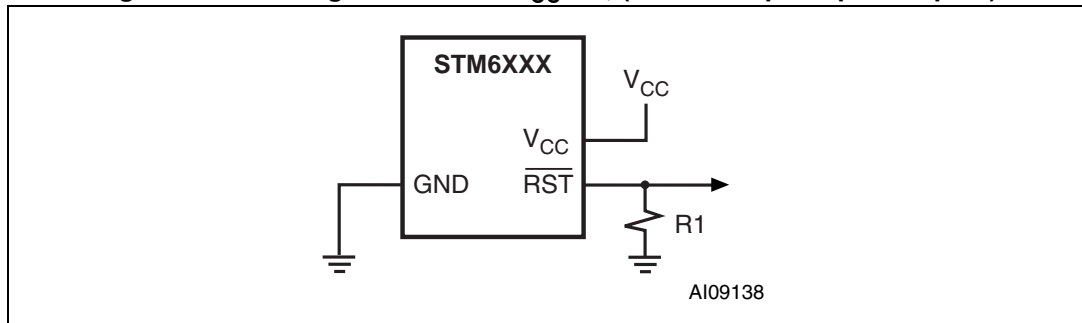


Figure 13. Ensuring RST valid to $V_{\text{CC}} = 0$, (active high, push-pull outputs)



1. This configuration does not work on open drain outputs of the STM6321/6322/6822.

2.6 Interfacing to microprocessors with bidirectional reset pins

Microprocessors with bidirectional reset pins can contend with the STM6321/6322/6821/6822/6823/6824/6825 reset output. For example, if the reset output is driven high and the microprocessor wants to pull it low, signal contention will result. To prevent this from occurring, connect a 4.7 k Ω resistor between the reset output and the microprocessor's reset I/O as in [Figure 14](#).

Figure 14. Interfacing to microprocessors with bidirectional reset I/O



3 Typical operating characteristics

Figure 15. V_{CC} -to-reset output delay vs. temperature



Figure 16. Supply current vs. temperature



Figure 17. $\overline{\text{MR}}$ -to-reset output delay vs. temperature

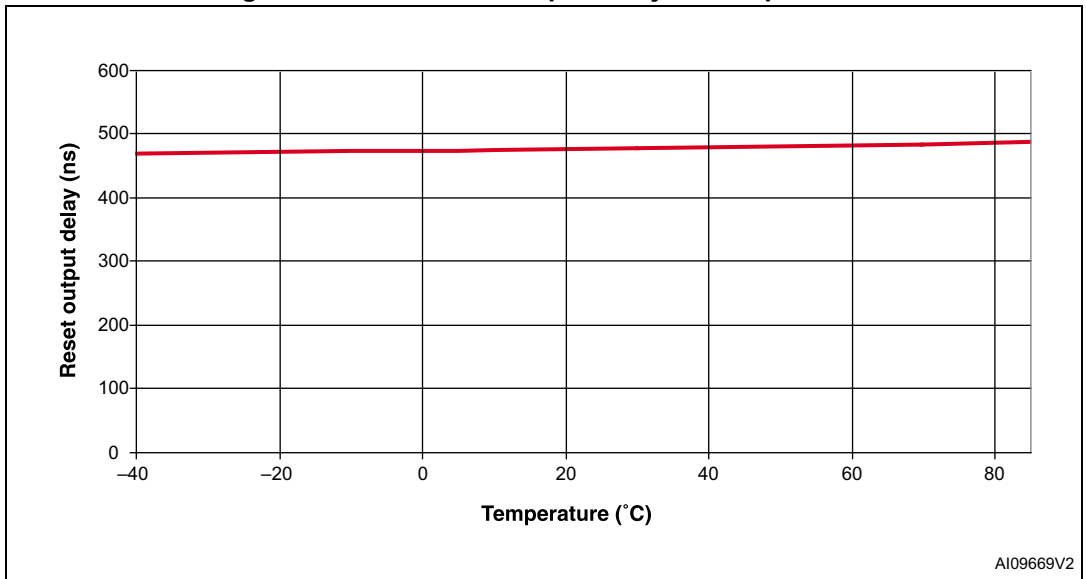


Figure 18. Normalized power-up t_{rec} vs. temperature

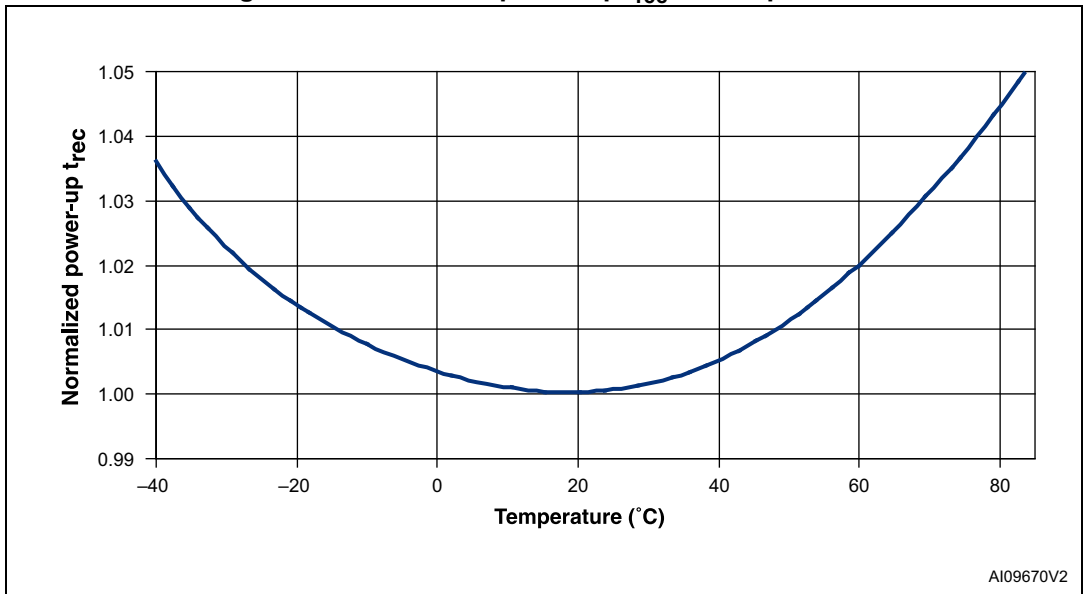


Figure 19. Normalized reset threshold voltage vs. temperature



Figure 20. Normalized power-up watchdog timeout period vs. temperature



Figure 21. Voltage output low vs. I_{SINK}

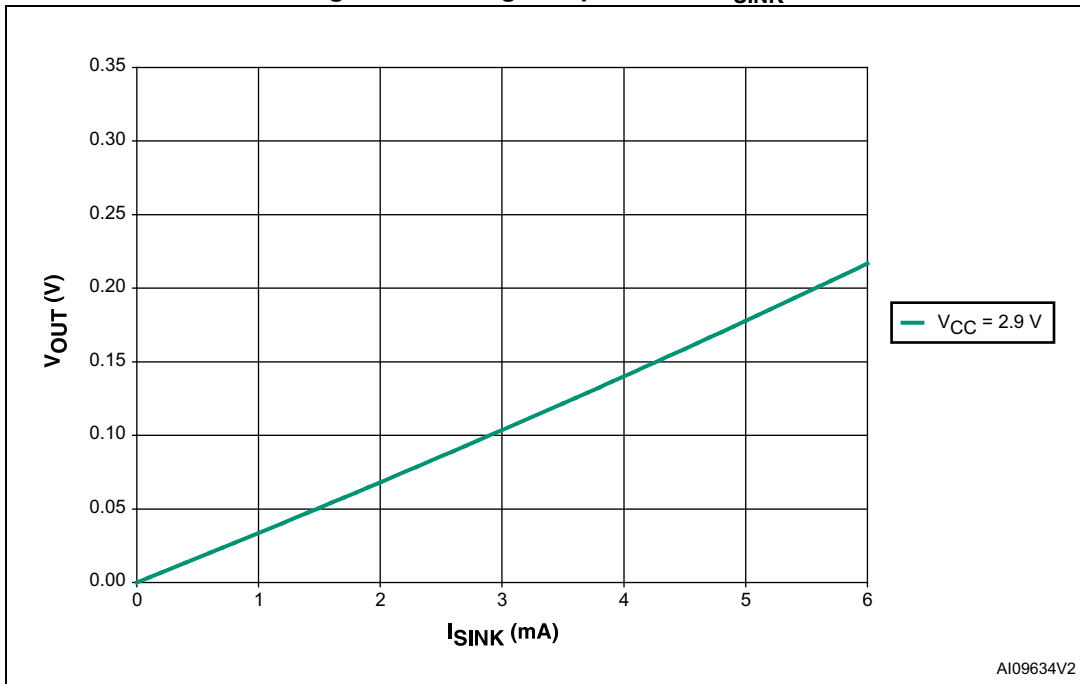


Figure 22. Voltage output high vs. I_{SOURCE}

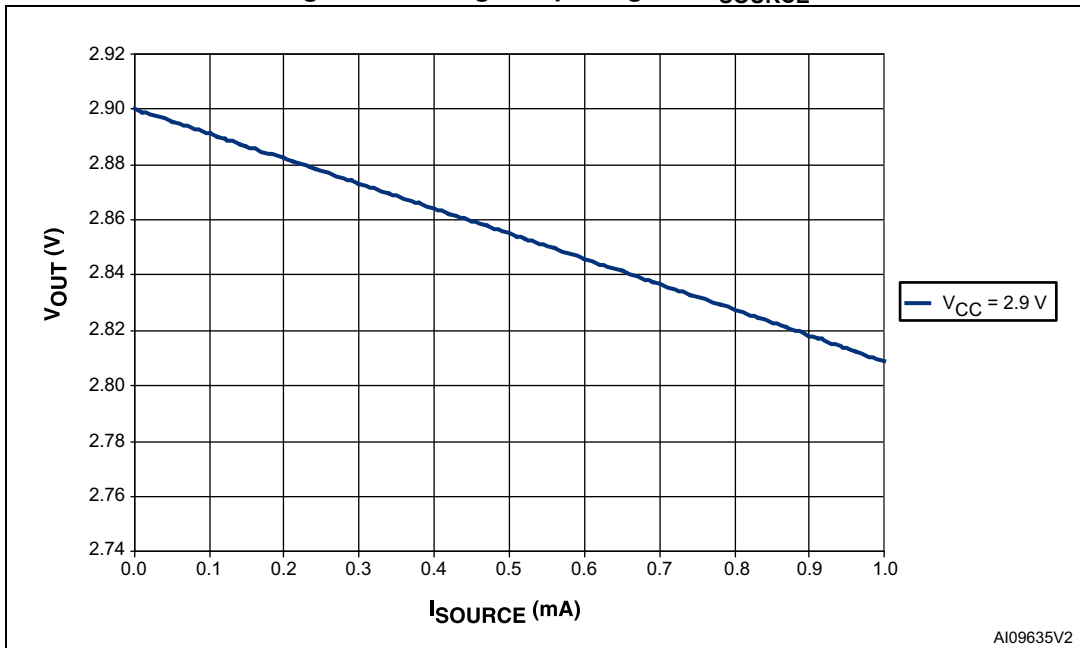
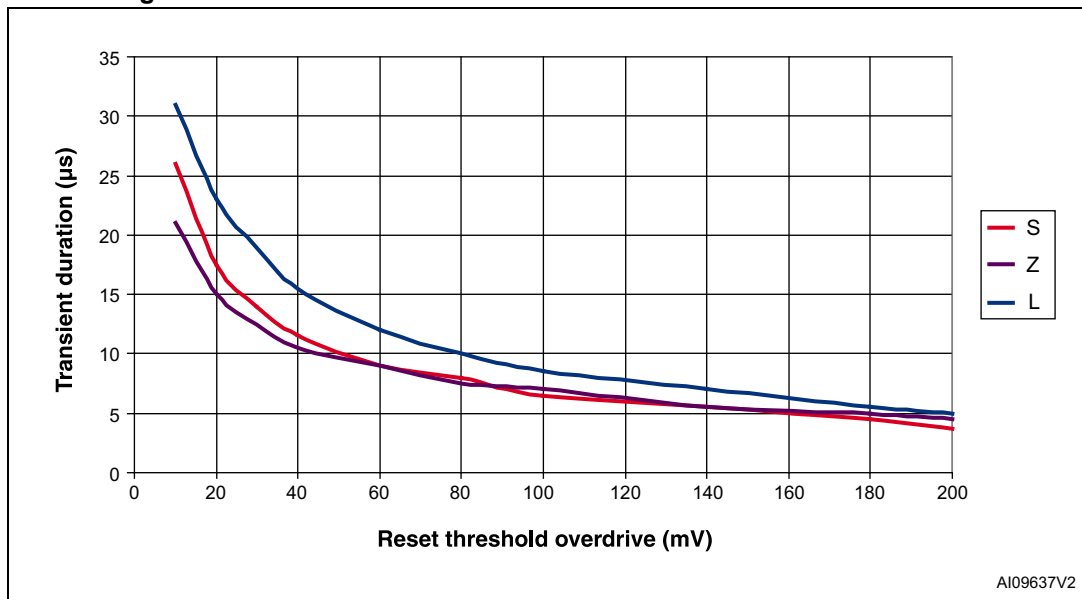


Figure 23. Maximum transient duration vs. reset threshold overdrive



4 Maximum ratings

Stressing the device above the rating listed in [Table 4: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in [Table 5: Operating and AC measurement conditions](#) of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics™ SURE program and other relevant quality documents.

Table 4. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-----------------|--|------------------------|------|
| T_{STG} | Storage temperature (V_{CC} off) | -55 to 150 | °C |
| $T_{SLD}^{(1)}$ | Lead solder temperature for 10 seconds | 260 | °C |
| V_{IO} | Input or output voltage | -0.3 to $V_{CC} + 0.3$ | V |
| V_{CC} | Supply voltage | -0.3 to 7.0 | V |
| I_O | Output current | 20 | mA |
| P_D | Power dissipation | 320 | mW |

1. Reflow at peak temperature of 260 °C (total thermal budget not to exceed 245 °C for greater than 30 seconds).

5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in [Table 6: DC and AC characteristics](#), are derived from tests performed under the measurement conditions summarized in [Table 5: Operating and AC measurement conditions](#). Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 5. Operating and AC measurement conditions

| Parameter | STM6xxx | Unit |
|---|----------------------------|------|
| V _{CC} supply voltage | 1.0 to 5.5 | V |
| Ambient operating temperature (T _A) | -40 to 85 | °C |
| Input rise and fall times | ≤ 5 | ns |
| Input pulse voltages | 0.2 to 0.8 V _{CC} | V |
| Input and output timing ref. voltages | 0.3 to 0.7 V _{CC} | V |

Figure 24. AC testing input/output waveforms

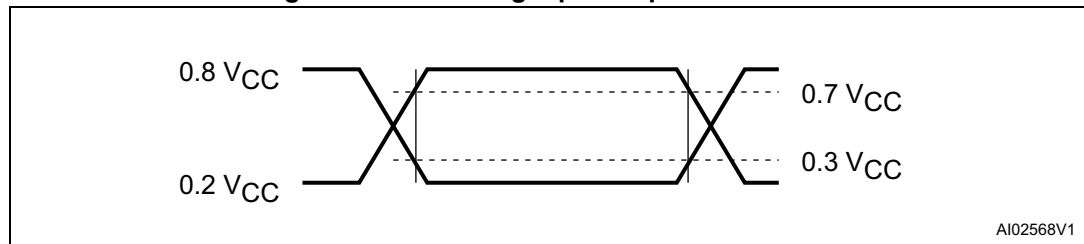
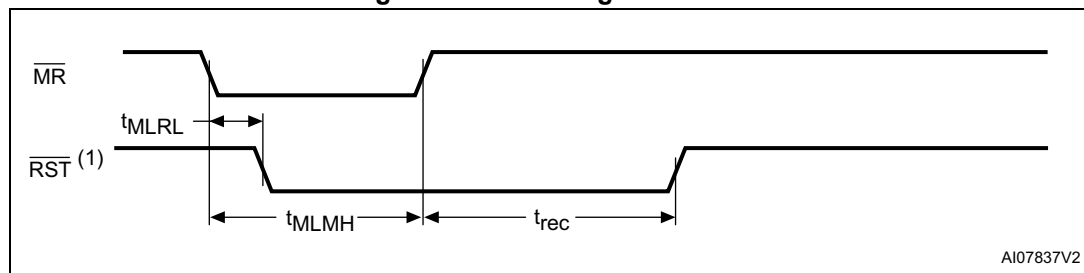


Figure 25. MR timing waveform



1. RST for STM6322/6821/6825.

Figure 26. Watchdog timing



Table 6. DC and AC characteristics

| Symbol | Alternative | Description | Test condition ⁽¹⁾ | Min. | Typ. | Max. | Unit | |
|-----------------|-------------|---|---|--------------------------------------|------|---------------------|------|----|
| V _{CC} | | Operating voltage | | 1.2 ⁽²⁾ | | 5.5 | V | |
| I _{CC} | | V _{CC} supply current (MR and WDI unconnected) | T/S/R/Z/Y (V _{CC} < 3.6 V) | | 4 | 12 | μA | |
| | | | L/M (V _{CC} < 5.5 V) | | 6 | 17 | μA | |
| | | V _{CC} supply current (MR unconnected; STM6322/6825) | T/S/R/Z/Y (V _{CC} < 3.6 V) | | 3 | 8 | μA | |
| | | | L/M (V _{CC} < 5.5 V) | | 3 | 12 | μA | |
| I _{LI} | | Input leakage current | 0 V = V _{IN} = V _{CC} | -1 | | +1 | μA | |
| | | | Input leakage current (WDI) ⁽³⁾ | WDI = V _{CC} , time average | | 120 | 160 | μA |
| | | | | WDI = GND, time average | -20 | -15 | | μA |
| I _{LO} | | Open drain reset output leakage current | V _{CC} > V _{RST} , Reset not asserted | -1 | | +1 | μA | |
| V _{IH} | | Input high voltage (MR) | V _{RST} > 4.0 V | 2.0 | | | V | |
| | | | V _{RST} < 4.0 V | 0.7 V _{CC} | | | V | |
| V _{IH} | | Input high voltage (WDI) ⁽⁴⁾ | V _{RST} (max.) < V _{CC} < 5.5 V | 0.7 V _{CC} | | | V | |
| V _{IL} | | Input low voltage (MR) | V _{RST} > 4.0 V | | | 0.8 | V | |
| | | | V _{RST} < 4.0 V | | | 0.3 V _{CC} | V | |
| V _{IL} | | Input low voltage (WDI) ⁽⁴⁾ | V _{RST} (max.) < V _{CC} < 5.5 V | | | 0.3 V _{CC} | V | |
| V _{OL} | | Output low voltage (RST; push-pull or open drain) | V _{CC} ≥ 1.0 V, I _{SINK} = 50 μA, Reset asserted | | | 0.3 | V | |
| | | | V _{CC} ≥ 1.2 V, I _{SINK} = 100 μA, Reset asserted | | | 0.3 | V | |
| | | | V _{CC} ≥ 2.7 V, I _{SINK} = 1.2 mA, Reset asserted | | | 0.3 | V | |
| | | | V _{CC} ≥ 4.5 V, I _{SINK} = 3.2 mA, Reset asserted | | | 0.4 | V | |
| | | Output low voltage (RST; push-pull only) | V _{CC} ≥ 2.7 V, I _{SINK} = 1.2 mA, Reset not asserted | | | 0.3 | V | |
| | | | V _{CC} ≥ 4.5 V, I _{SINK} = 3.2 mA, Reset not asserted | | | 0.4 | V | |

Table 6. DC and AC characteristics (continued)

| Symbol | Alternative | Description | Test condition ⁽¹⁾ | Min. | Typ. | Max. | Unit | | | |
|---------------------------------|---------------------------------|--|---|---------------------|----------------------------|--------------------|-------|-------|----|----|
| V _{OH} | | Output high voltage ($\overline{\text{RST}}$) | V _{CC} ≥ 2.7 V, I _{SOURCE} = 500 μA, Reset not asserted | 0.8 V _{CC} | | | V | | | |
| | | | V _{CC} ≥ 4.5 V, I _{SOURCE} = 800 μA, Reset not asserted | 0.8 V _{CC} | | | V | | | |
| | | Output high voltage (RST) | V _{CC} ≥ 1.0 V, I _{SOURCE} = 1 μA, Reset asserted (0 °C to 85 °C) | 0.8 V _{CC} | | | V | | | |
| | | | V _{CC} ≥ 1.5 V, I _{SOURCE} = 100 μA, Reset asserted | 0.8 V _{CC} | | | V | | | |
| | | | V _{CC} ≥ 2.55 V, I _{SOURCE} = 500 μA, Reset asserted | 0.8 V _{CC} | | | V | | | |
| | | | V _{CC} ≥ 4.25 V, I _{SOURCE} = 800 μA, Reset asserted | 0.8 V _{CC} | | | V | | | |
| | Reset thresholds | | | | | | | | | |
| | V _{RST} ⁽⁵⁾ | | Reset threshold | STM6xxxL | 25 °C | 4.561 | 4.630 | 4.699 | V | |
| -40 to 85 °C | | | | | 4.514 | | 4.746 | V | | |
| STM6xxxM | | | | 25 °C | 4.314 | 4.390 | 4.446 | V | | |
| | | | | -40 to 85 °C | 4.270 | | 4.490 | V | | |
| STM6xxxT | | | | 25 °C | 3.040 | 3.080 | 3.110 | V | | |
| | | | | -40 to 85 °C | 3.000 | | 3.150 | V | | |
| STM6xxxS | | | | 25 °C | 2.890 | 2.930 | 2.960 | V | | |
| | | | | -40 to 85 °C | 2.857 | | 3.000 | V | | |
| STM6xxxR | | | | 25 °C | 2.590 | 2.630 | 2.660 | V | | |
| | | | | -40 to 85 °C | 2.564 | | 2.696 | V | | |
| STM6xxxZ | | | | 25 °C | 2.266 | 2.300 | 2.335 | V | | |
| | | | | -40 to 85 °C | 2.243 | | 2.358 | V | | |
| STM6xxxY | | | | 25 °C | 1.970 | 2.000 | 2.030 | V | | |
| | | | | -40 to 85 °C | 1.950 | | 2.050 | V | | |
| | | | | | Reset threshold hysteresis | L/M versions | | | 10 | mV |
| | | | | | | T/S/R/Z/Y versions | | | 5 | mV |
| | | V _{CC} to $\overline{\text{RST}}$ delay (V _{RST} - V _{CC} = 100 mV, V _{CC} falling at 1 mV/μs) | | | 20 | | μs | | | |
| t _{rec} ⁽⁶⁾ | | Reset pulse width | A | 1 | 1.4 | 2 | ms | | | |
| | | | Blank | 140 | 200 | 280 | ms | | | |
| | | | J | 240 | 360 | 480 | ms | | | |

Table 6. DC and AC characteristics (continued)

| Sym- bol | Alter- native | Description | Test condition ⁽¹⁾ | Min. | Typ. | Max. | Unit |
|--------------------------------|------------------|--|-------------------------------|------|------|------|-----------|
| | | Reset threshold temperature coefficient | | | 40 | | ppm/ C |
| Push-button reset input | | | | | | | |
| t _{MLMH} | t _{MR} | $\overline{\text{MR}}$ pulse width | | 1 | | | μs |
| t _{MLRL} | t _{MRD} | $\overline{\text{MR}}$ to RST output delay | | | 500 | | ns |
| | | $\overline{\text{MR}}$ glitch immunity | | | 100 | | ns |
| | | $\overline{\text{MR}}$ pull-up resistor | | 35 | 52 | 75 | kΩ |
| Watchdog timer | | | | | | | |
| t _{WD} ⁽⁶⁾ | | Watchdog timeout period | | 1.12 | 1.60 | 2.24 | s |
| | | WDI pulse width ⁽⁷⁾ | V _{CC} ≥ 3.0 V | 50 | | | ns |

- Valid for ambient operating temperature: T_A = -40 to 85 °C; V_{CC} = 4.5 to 5.5 V for "L/M" versions; V_{CC} = 2.7 to 3.6 V for "T/S/R" versions; and V_{CC} = 1.2 to 2.75 V for "Z/Y" version (except where noted).
- V_{CC} (min.) = 1.0 V for T_A = 0 to +85 °C.
- WDI input is designed to be driven by a three-state output device. To float WDI, the "high-impedance mode" of the output device must have a maximum leakage current of 10 μA and a maximum output capacitance of 200 pF. The output device must also be able to source and sink at least 200 μA when active.
- WDI is internally serviced within the watchdog period if WDI is left unconnected.
- The leakage current measured on the RST pin is tested with the reset asserted (output high impedance).
- Other t_{rec} offered for t_{WD} (102 ms, 6.3 ms, and 25.6 s options). Minimum order quantities may apply. Contact local sales office for availability.
- For V_{CC} < 3.0 V, t_{WD}(min.) = 100 ns.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SOT23-5 package information

Figure 27. SOT23-5 package outline



1. Drawing is not to scale.

Table 7. SOT23-5 mechanical data

| Symbol | Dimensions | | | | | |
|--------|------------|------|------|--------|-------|-------|
| | mm | | | inches | | |
| | Typ. | Min. | Max. | Typ. | Min. | Max. |
| A | 1.20 | 0.90 | 1.45 | 0.047 | 0.035 | 0.057 |
| A1 | | | 0.15 | | | 0.006 |
| A2 | 1.05 | 0.90 | 1.30 | 0.041 | 0.035 | 0.051 |
| B | 0.40 | 0.35 | 0.50 | 0.016 | 0.014 | 0.020 |
| C | 0.15 | 0.09 | 0.20 | 0.006 | 0.004 | 0.008 |
| D | 2.90 | 2.80 | 3.00 | 0.114 | 0.110 | 0.118 |
| D1 | 1.90 | | | 0.075 | | |
| E | 2.80 | 2.60 | 3.00 | 0.110 | 0.102 | 0.118 |
| e | 0.95 | | | 0.037 | | |
| F | 1.60 | 1.50 | 1.75 | 0.063 | 0.059 | 0.069 |
| K | | 0° | 10° | | 0° | 10° |
| L | 0.35 | 0.10 | 0.60 | 0.014 | 0.004 | 0.024 |

Figure 28. SOT23-5 carrier tape

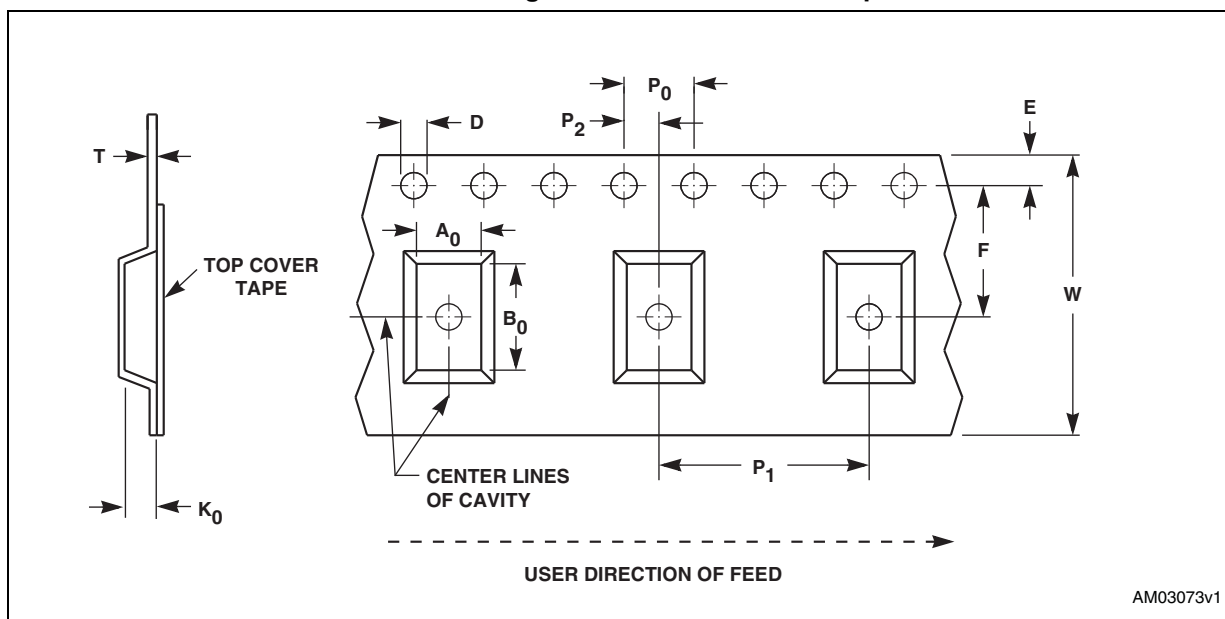


Table 8. SOT23-5 carrier tape dimensions

| Package | W | D | E | P ₀ | P ₂ | F | A ₀ | B ₀ | K ₀ | P ₁ | T | Unit | Bulk qty. |
|---------|------------------------|-------------------------|---------------|----------------|----------------|---------------|----------------|----------------|----------------|----------------|-----------------|------|-----------|
| SOT23-5 | 8.00 +0.30 -0.10 | 1.50 +0.10/ -0.00 | 1.75 ±0.10 | 4.00 ±0.10 | 2.00 ±0.10 | 3.50 ±0.05 | 3.23 ±0.10 | 3.17 ±0.10 | 1.37 ±0.10 | 4.00 ±0.10 | 0.254 ±0.013 | mm | 3000 |

7 Part numbering

Table 9. Ordering information scheme

| Example: | STM6xxx | L | WY | 6 | E |
|--|---|---|----|---|---|
| Device type | STM6xxx | | | | |
| Reset threshold voltage | L: $V_{RST} = 4.514$ to 4.746 V M: $V_{RST} = 4.270$ to 4.490 V T: $V_{RST} = 3.000$ to 3.150 V S: $V_{RST} = 2.850$ to 3.000 V R: $V_{RST} = 2.564$ to 2.696 V Z: $V_{RST} = 2.243$ to 2.358 V Y: $V_{RST} = 1.950$ to 2.050 V | | | | |
| Reset pulse width⁽¹⁾ | A: $t_{rec} = 1$ to 2 ms Blank: $t_{rec} = 140$ to 280 ms J: $t_{rec} = 240$ to 480 ms | | | | |
| Package | WY = SOT23-5 | | | | |
| Temperature range | 6 = -40 to 85 °C | | | | |
| Shipping method | E = ECOPACK® package, tubes F = ECOPACK® package, tape and reel | | | | |

1. Contact local sales office for availability. Other t_{rec} offered for t_{WD} (102 ms, 6.3 ms, and 25.6 s options). Minimum order quantities may apply.

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.



Table 10. Marking description

| Part number | Reset threshold (V) | Reset pulse width (ms) | Topside marking ⁽¹⁾ |
|---------------|---------------------|------------------------|--------------------------------|
| STM6321LWY6F | 4.630 | 200 | 5AU or 5AUx |
| STM6321MAWY6F | 4.390 | 1.4 | 5CR or 5CRx |
| STM6321MWY6F | 4.390 | 200 | 5AV or 5AVx |
| STM6321TWY6F | 3.080 | 200 | 5AW or 5AWx |
| STM6321SWY6F | 2.930 | 200 | 5AX or 5AXx |
| STM6321RWY6F | 2.630 | 200 | 5AY or 5AYx |
| STM6322LWY6F | 4.630 | 200 | 5BA or 5BAx |
| STM6322MWY6F | 4.390 | 200 | 5BB or 5BBx |
| STM6322TWY6F | 3.080 | 200 | 5BC or 5BCx |
| STM6322SWY6F | 2.930 | 200 | 5BD or 5BDx |
| STM6322RWY6F | 2.630 | 200 | 5BE or 5BEx |
| STM6821LWY6F | 4.630 | 200 | 5BG or 5BGx |
| STM6821MWY6F | 4.390 | 200 | 5BH or 5BHx |
| STM6821TWY6F | 3.080 | 200 | 5BJ or 5BJx |
| STM6821SWY6F | 2.930 | 200 | 5BK or 5BKx |
| STM6821RWY6F | 2.630 | 200 | 5BL or 5BLx |
| STM6822LWY6F | 4.630 | 200 | 5BN or 5BNx |
| STM6822MWY6F | 4.390 | 200 | 5BP or 5BPx |
| STM6822TWY6F | 3.080 | 200 | 5BQ or 5BQx |
| STM6822SWY6F | 2.930 | 200 | 5BR or 5BRx |
| STM6822RWY6F | 2.630 | 200 | 5BS or 5BSx |
| STM6822ZWY6F | 2.300 | 200 | 5BT or 5BTx |
| STM6822YWY6F | 2.000 | 200 | 5CT or 5CTx |
| STM6823LWY6F | 4.630 | 200 | 5BU or 5BUx |
| STM6823MWY6F | 4.390 | 200 | 5BV or 5BVx |
| STM6823JWY6F | 3.080 | 280 | 5CM or 5CMx |
| STM6823TWY6F | 3.080 | 200 | 5BW or 5BWx |
| STM6823SJWY6F | 2.930 | 280 | 5CN or 5CNx |
| STM6823SWY6F | 2.930 | 200 | 5BX or 5BXx |
| STM6823RJWY6F | 2.630 | 280 | 5CP or 5CPx |
| STM6823RWY6F | 2.630 | 200 | 5BY or 5BYx |
| STM6823ZWY6F | 2.300 | 200 | 5BZ or 5BZx |
| STM6824LWY6F | 4.630 | 200 | 5CA or 5CAx |
| STM6824MWY6F | 4.390 | 200 | 5CB or 5CBx |
| STM6824TWY6F | 3.080 | 200 | 5CC or 5CCx |

Table 10. Marking description (continued)

| Part number | Reset threshold (V) | Reset pulse width (ms) | Topside marking ⁽¹⁾ |
|--------------|---------------------|------------------------|--------------------------------|
| STM6824SWY6F | 2.930 | 200 | 5CD or 5CDx |
| STM6824RWY6F | 2.630 | 200 | 5CE or 5CEx |
| STM6825LWY6F | 4.630 | 200 | 5CG or 5CGx |
| STM6825MWY6F | 4.390 | 200 | 5CH or 5CHx |
| STM6825TWY6F | 3.080 | 200 | 5CJ or 5CJx |
| STM6825SWY6F | 2.930 | 200 | 5CK or 5CKx |
| STM6825RWY6F | 2.630 | 200 | 5CL or 5CLx |

1. Where "x" = assembly work week (A to Z), such that "A" = WW01-02, "B" = WW03-04, and so forth.

8 Revision history

Table 11. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 25-Aug-2004 | 1 | First draft |
| 15-Dec-2004 | 2 | Update characteristics (Figure 15, 16, 17; Table 6, and 9) |
| 10-Mar-2005 | 3 | Document promoted to Datasheet status |
| 17-Jun-2005 | 4 | Package marking update (Table 10) |
| 11-Apr-2006 | 5 | Update characteristics, Lead-free text, availability (Figure 3, 4, 5, 6, 7, 8, and 9; Table 1, 6, 9, and 10) |
| 11-Aug-2006 | 6 | Update Description, Table 9, and 10. |
| 25-May-2007 | 7 | Formatting changes, updated Table 10. |
| 03-Jun-2008 | 8 | Updated cover page; updated reset threshold values in Table 6, 9, and 10; addition of text to Section 6; updated Figure 27 and Table 6 and 7; minor text changes. |
| 09-Apr-2009 | 9 | Updated Section 1.1.1, Section 6; added tape and reel specifications Figure 28, Table 8. |
| 06-Jan-2011 | 10 | Document reformatted, Doc ID added, updated Table 10, corrected typo in Features, Section 1.1.4, Section 2.1, Section 2.3, Section 4, Table 4, Table 6, Table 9, Figure 7 to Figure 11, Figure 14 to Figure 26. |
| 14-Jul-2011 | 11 | Updated Table 10, corrected typo in Table 6, Table 7 and Table 8, reformatted Figure 27, updated Disclaimer. |
| 27-Jun-2012 | 12 | Removed note from Features, added cross-references to Section 4 and Section 5, minor text corrections throughout document. |
| 13-Jun-2016 | 13 | Updated document layout Table 6 : updated footnote 6 Table 9 : updated footnote 1 |

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