19-3282; Rev 1; 7/04

MAXIM

Positive High-Voltage, Hot-Swap Controllers with Selectable Fault Management and Status Polarity

General Description

The MAX5934/MAX5934A are fully integrated hot-swap controllers for +9V to +80V (MAX5934A) positive supply rails. The MAX5934 is optimized for +33V to +80V power-supply rails. These devices allow for the safe insertion and removal of circuit cards into a live backplane without causing glitches on the backplane power-supply rail. The MAX5934/MAX5934A feature a programmable analog foldback current limit, programmable undervoltage lockout, and programmable output-voltage slew rate through an external n-channel MOSFET. In addition, if these devices remain in current limit for more than a programmable time, the external n-channel MOSFET latches off.

The MAX5934/MAX5934A feature pin-selectable PWRGD_ assertion polarity (active low or active high) and pin-selectable fault management (latched or autoretry). Other features include automatic restart after a circuit-breaker fault, selectable duty-cycle (DC) options, and thermal-shutdown mode for overtemperature protection.

The MAX5934/MAX5934A operate in the extended (-40°C to +85°C) temperature range and are available in a 16-pin QSOP package.

Applications

Hot Board Insertion

Electronic Circuit Breakers

Industrial High-Side Switch/Circuit Breakers

Network Routers and Switches

24V/48V Industrial/Alarm Systems

Typical Application Circuit appears at end of data sheet.

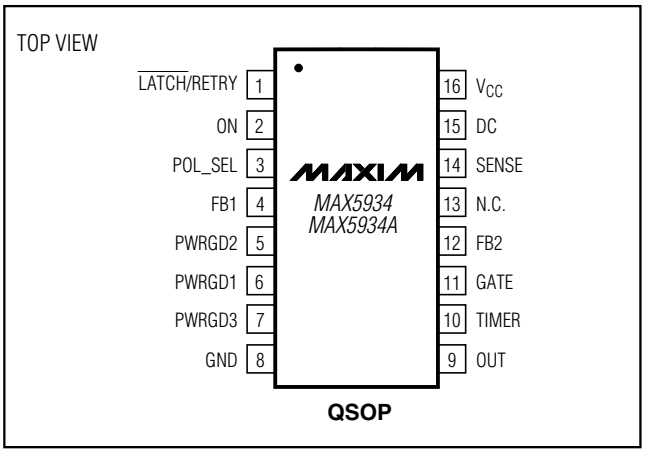
Features

- **Provides Safe Hot Swap for +9V to +80V Power Supplies (MAX5934A)**
- **Safe Board Insertion and Removal from a Live Backplane**
- **Pin-Selectable Active-Low or Active-High Power-Good Output**
- **Pin-Selectable Latched or Autoretry Fault Management**
- **Programmable Foldback Current Limiting**
- **High-Side Drive for an External N-Channel MOSFET**
- **Built-In Thermal Shutdown**
- **Undervoltage Lockout (UVLO)**
- **Pin-Selectable Duty-Cycle Options (0.94%, 1.88%, 3.75%)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5934EEE	-40°C to +85°C	16 QSOP
MAX5934AEEE	-40°C to +85°C	16 QSOP

Pin Configuration



Selector Guide

PART	DEFAULT UVLO (V)	SUPPLY VOLTAGE RANGE (V)	LATCHED/ AUTORETRY FAULT PROTECTION	DUTY CYCLE	PWRGD_ OUTPUT LOGIC
MAX5934	31	+33 to +80	Pin-selectable	Pin-selectable	Pin-selectable
MAX5934A	8.3	+9 to +80	Pin-selectable	Pin-selectable	Pin-selectable

Positive High-Voltage, Hot-Swap Controllers with Selectable Fault Management and Status Polarity

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
V_{CC} .....-0.3V to +85V
SENSE, FB_, ON.....-0.3V to (V_{CC} + 0.3V)
TIMER, PWRGD_, DC, $\overline{LATCH}$/RETRY, POL_SEL ....-0.3V to +85V
GATE .....-0.3V to +95V
OUT .....(V_{GATE} - 14V) to the lower of (V_{GATE} + 0.3V) and (V_{CC} + 0.3V)
Maximum GATE Current .....-50mA, +150mA
Maximum Current into Any Other Pin.....±50mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C).....667mW
Operating Temperature Range .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
ESD Rating (Human Body Model).....2000V
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +24V (MAX5934A), V_{CC} = +48V (MAX5934), GND = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	MAX5934A		9		80	V
		MAX5934		33		80	
Supply Current	I_{CC}	V_{ON} = 3V, V_{CC} = 80V			1.4	3.5	mA
V_{CC} Undervoltage Lockout	V_{LKO}	V_{CC} low-to-high transition	MAX5934A	7.5	8.3	8.8	V
			MAX5934	29.5	31	32.5	
V_{CC} Undervoltage-Lockout Hysteresis	$V_{LKOHYST}$	MAX5934A			0.4		V
		MAX5934			2		
FB1 High-Voltage Threshold	V_{FB1H}	FB1 low-to-high transition		1.280	1.313	1.345	V
FB2 High-Voltage Threshold	V_{FB2H}	FB2 low-to-high transition		1.280	1.313	1.345	V
FB1 Low-Voltage Threshold	V_{FB1L}	FB1 high-to-low transition		1.221	1.233	1.245	V
FB2 Low-Voltage Threshold	V_{FB2L}	FB2 high-to-low transition		1.202		1.264	V
FB_ Hysteresis	V_{FBHYST}				80		mV
FB_ Input Bias Current	I_{INFB}	$V_{FB\_}$ = 0V		-1		+1	µA
FB1 Threshold Line Regulation	ΔV_{FB1}	$V_{CC(MIN)} \le V_{CC} \le 80V$, MAX5934A, ON = 0V				0.05	mV/V
FB2 Threshold Line Regulation	ΔV_{FB2}	$V_{CC(MIN)} \le V_{CC} \le 80V$, MAX5934A, ON = 0V				0.05	mV/V
SENSE Trip Voltage (V_{CC} - V_{SENSE})	$V_{SENSETRIP}$	$V_{FB\_}$ = 0V, T_A = 0°C to +70°C		8	12	17	mV
		$V_{FB\_}$ = 1V, T_A = 0°C to +70°C		39	47	55	
GATE Pullup Current	I_{GATEUP}	Charge pump on, V_{GATE} = 7V		-5	-10	-20	µA
GATE Pulldown Current	I_{GATEDN}	Any fault condition, V_{GATE} = 2V		35	70	100	mA
(V_{GATE} - V_{CC}) at PWRGD3 Assertion	$\Delta V_{GATEPWRGD3}$	V_{GATE} - V_{CC}, low-to-high transition		3.8	4.3	5	V
External N-Channel Gate Drive	ΔV_{GATE}	V_{GATE} - V_{CC}, MAX5934		10	13.6	18	V
		V_{GATE} - V_{CC}, MAX5934A	V_{CC} = 10.8V to 20V	4.5	13.6	18.0	
			V_{CC} = 20V to 80V	10	13.6	18	
TIMER Pullup Current	$I_{TIMERUP}$	V_{TIMER} = 0V		-24	-75	-120	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +24V (MAX5934A), V_{CC} = +48V (MAX5934), GND = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TIMER Pulldown Current	$I_{TIMERON}$	V_{TIMER} = 1V	DC = 3.75%, DC = floating	1.5	3	4.5	µA
			DC = 1.88%, DC = high	0.75	1.5	2.25	
			DC = 0.94%, DC = low	0.37	0.75	1.12	
ON High Threshold	V_{ONH}	ON low-to-high transition		1.280	1.313	1.355	V
ON Low Threshold	V_{ONL}	ON high-to-low transition		1.221	1.233	1.245	V
ON Hysteresis	V_{ONHYST}				80		mV
ON Input Bias Current	I_{INON}	V_{ON} = 0V		-1		+1	µA
$\overline{LATCH}$/RETRY and POL_SEL Low-Voltage Threshold	V_{LRIL}, $V_{POS\_SEL\_IL}$			0.4			V
$\overline{LATCH}$/RETRY and POL_SEL High-Voltage Threshold	V_{LRIH}, $V_{POS\_SEL\_IH}$					3.2	V
$\overline{LATCH}$/RETRY and POL_SEL Input Current	I_{LR_IN}, $I_{POS\_SEL\_IN}$	V_{POL_SEL} = 80V			4.5		µA
		V_{POL_SEL} = 0V			-37		
Source GATE Clamp Voltage	V_{SGZ}	V_{GATE} - V_{OUT}		15	16.4	19	V
PWRGD_ Output Low Voltage	V_{OL}	I_O = 2mA				0.4	V
		I_O = 4mA				2.5	
PWRGD_ Leakage Current	I_{OH}	$V_{PWRGD\_}$ = 80V				10	µA
Thermal Shutdown		Temperature rising			+150		°C
Thermal-Shutdown Hysteresis					20		°C
SENSE Input Bias Current	I_{SENSE}	V_{SENSE} = 0 to V_{CC}		-1		+3	µA
DC High-Voltage Threshold 1	V_{DCHTH}	Rising edge, DC transition from 3.75% to 1.88%		2.150	2.600	2.850	V
DC High-Voltage Threshold 2	V_{DCLTH}	Rising edge, DC transition from 0.94% to 3.75%		1.075	1.250	1.425	V
DC High-Voltage Threshold 1 Hysteresis	V_{DCLHYS}				45		mV
DC High-Voltage Threshold 2 Hysteresis	V_{DCLHYS}				45		mV
DC Input Open-Circuit Voltage	V_{DCOC}				1.9		V
DC Input Impedance	R_{DC_IN}				57		kΩ
DC Input Current	I_{DC_IN}	$V_{\_DC}$ = 80V			50		µA
		$V_{\_DC}$ = 0V			-34		
ON Low-to-GATE Low Propagation Delay	t_{PHLON}	C_{GATE} = 0, Figures 1 and 2			6		µs
ON High-to-GATE High Propagation Delay	t_{PLHON}	C_{GATE} = 0, Figures 1 and 2			1.7		µs

Positive High-Voltage, Hot-Swap Controllers with Selectable Fault Management and Status Polarity

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +24V (MAX5934A), V_{CC} = +48V (MAX5934), GND = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FB_ Low-to-PWRGD_ Low Propagation Delay	$t_{PHLFB\_}$	Figures 1, 3		3.2		µs
FB_ High-to-PWRGD_ High Propagation Delay	$t_{PLHFB\_}$	Figures 1, 3		1.5		µs
(V_{CC} - V_{SENSE}) High-to-GATE Low Propagation Delay	$t_{PHLSENSE}$	T_A = +25°C, C_{GATE} = 0, Figures 1 and 4	0.5	1.8	2.5	µs

Note 1: All currents into the device are positive and all currents out of the device are negative. All voltages are referenced to ground, unless noted otherwise.

Test Circuit and Timing Diagrams

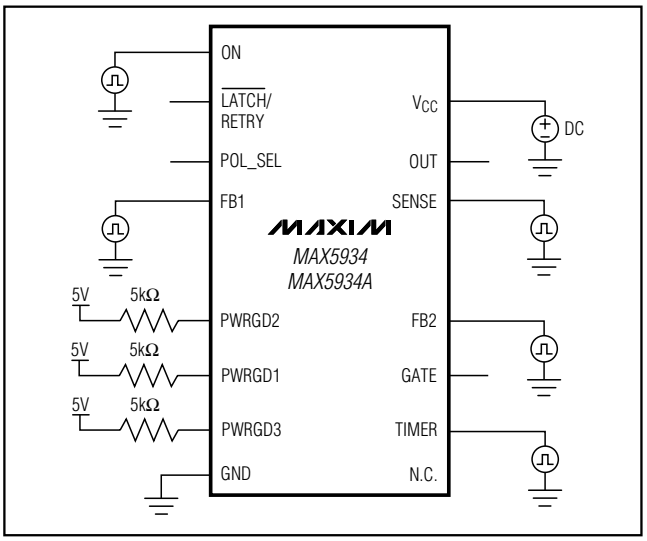


Figure 1. Test Circuit

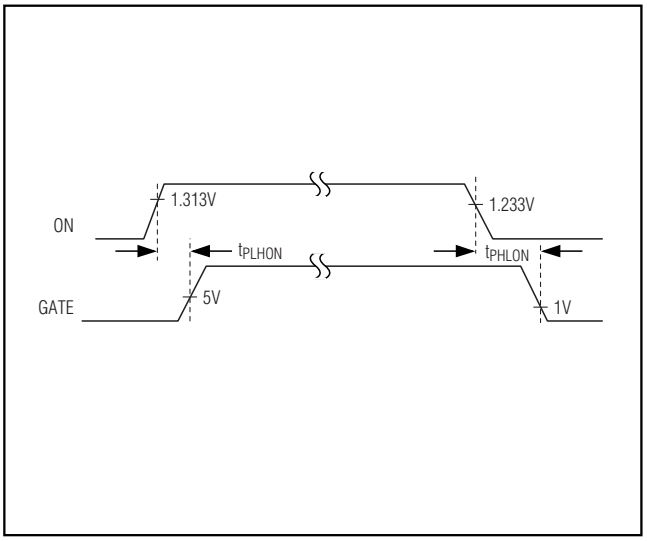


Figure 2. ON-to-GATE Timing

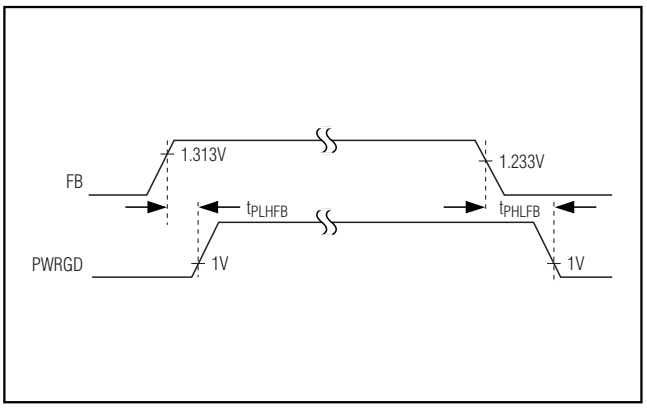


Figure 3. FB_-to-PWRGD_ Timing

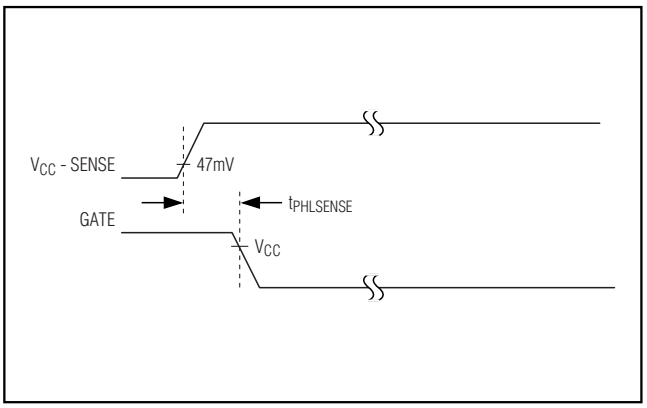
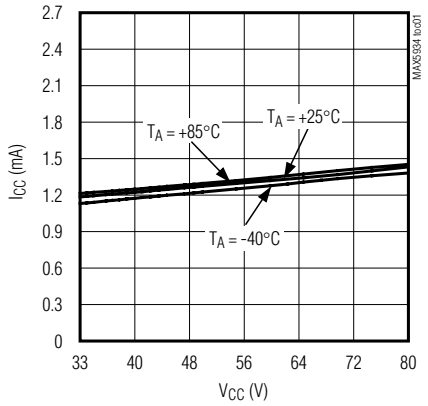


Figure 4. SENSE-to-GATE Timing

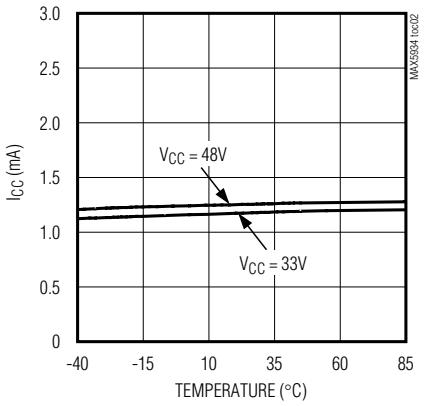
Typical Operating Characteristics

(V_{CC} = +48V, T_A = +25°C, unless otherwise noted.)

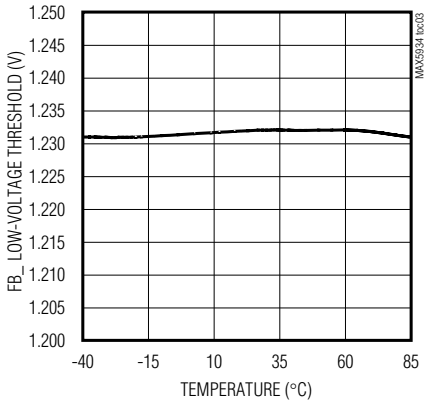
SUPPLY CURRENT vs. SUPPLY VOLTAGE



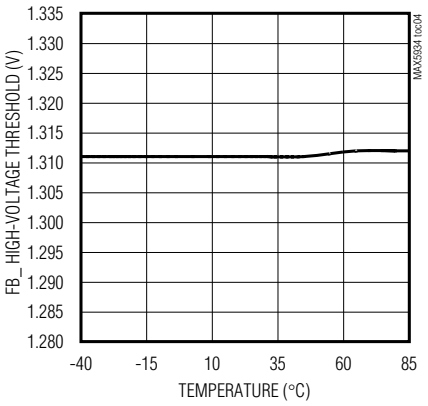
SUPPLY CURRENT vs. TEMPERATURE



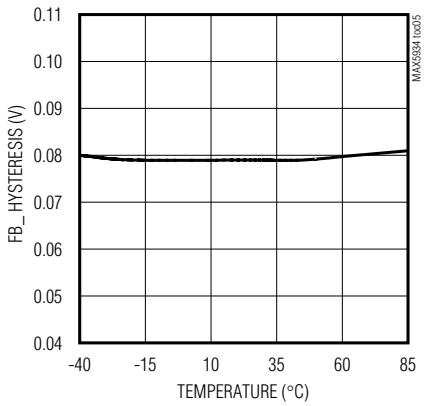
FB_ LOW-VOLTAGE THRESHOLD vs. TEMPERATURE



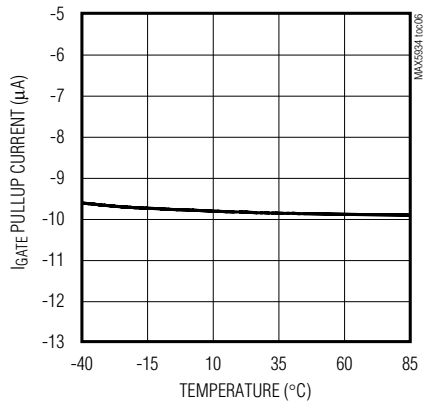
FB_ HIGH-VOLTAGE THRESHOLD vs. TEMPERATURE



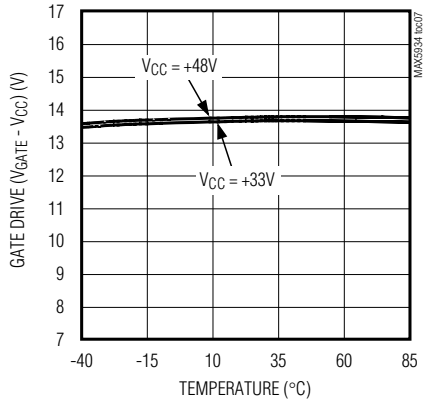
FB_ HYSTERESIS vs. TEMPERATURE



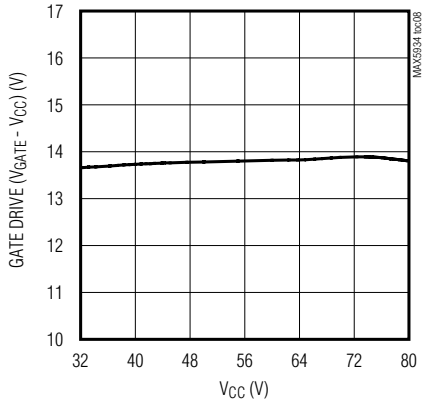
IGATE PULLUP CURRENT vs. TEMPERATURE



GATE DRIVE vs. TEMPERATURE



GATE DRIVE vs. SUPPLY VOLTAGE

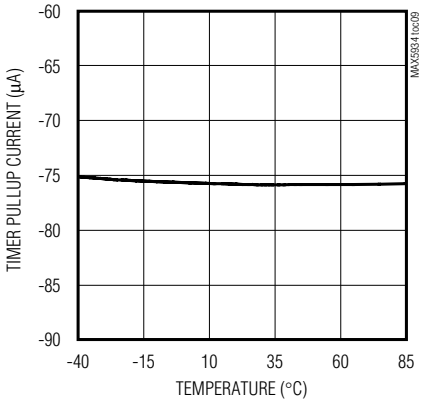


Positive High-Voltage, Hot-Swap Controllers with Selectable Fault Management and Status Polarity

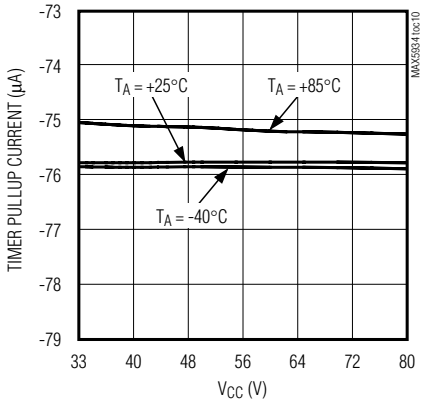
Typical Operating Characteristics (continued)

(V_{CC} = +48V, T_A = +25°C, unless otherwise noted.)

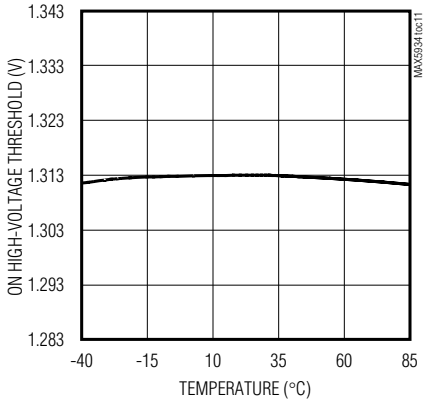
TIMER PULLUP CURRENT vs. TEMPERATURE



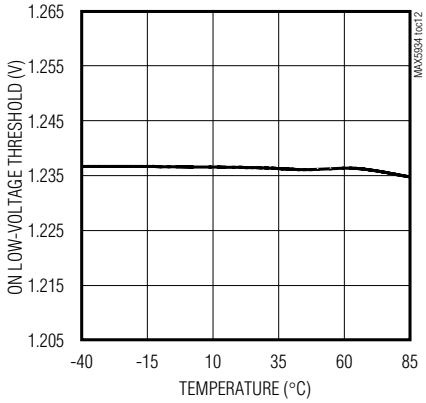
TIMER PULLUP CURRENT vs. SUPPLY VOLTAGE



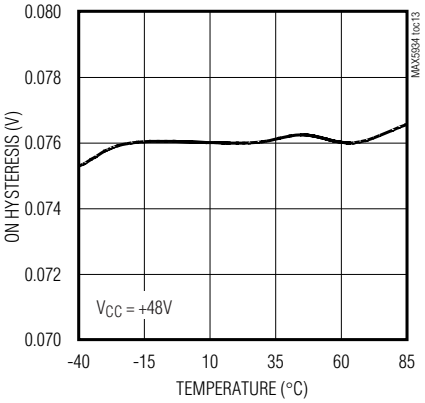
ON HIGH-VOLTAGE THRESHOLD vs. TEMPERATURE



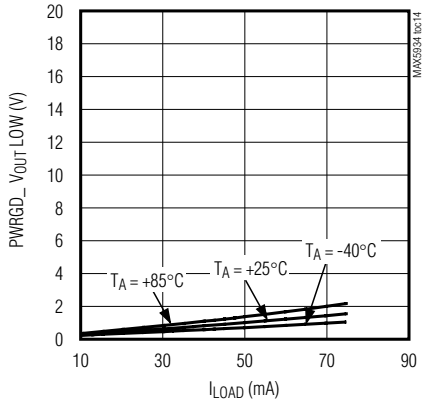
ON LOW-VOLTAGE THRESHOLD vs. TEMPERATURE



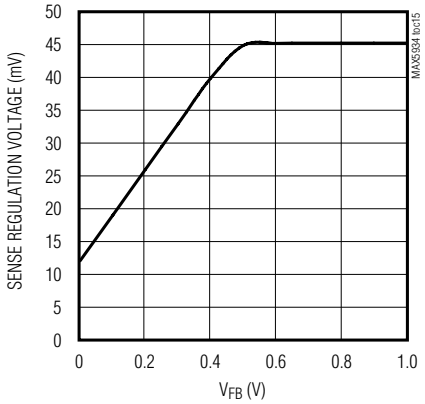
ON HYSTERESIS vs. TEMPERATURE



PWRGD_ OUTPUT VOLTAGE LOW vs. LOAD CURRENT



SENSE REGULATION VOLTAGE vs. FB_ VOLTAGE

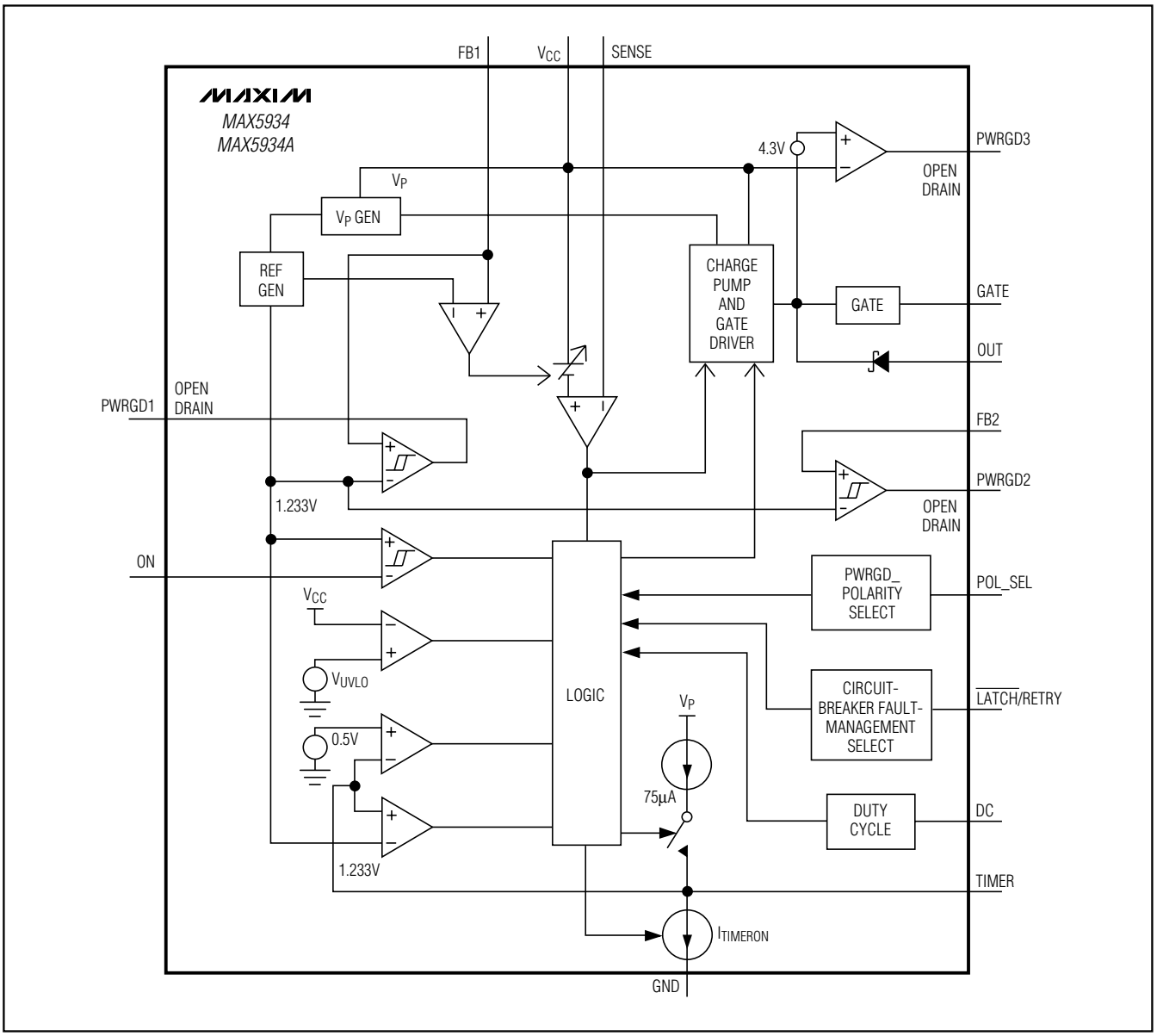


Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{LATCH}}$/ RETRY	Circuit-Breaker Fault-Management Select Input. Connect $\overline{\text{LATCH}}$/RETRY to GND to latch off after a circuit-breaker fault. Leave $\overline{\text{LATCH}}$/RETRY open or drive to logic-high voltage for automatic restart after a circuit-breaker fault.
2	ON	On/Off Control Input. ON implements the undervoltage-lockout threshold and resets the part after a fault latch (see the *Fault Management ($\overline{\text{LATCH}}$/RETRY)* section).
3	POL_SEL	PWRGD_ Polarity Select Input. Leave POL_SEL open or drive to logic-high voltage for PWRGD_ asserted high. Connect POL_SEL to GND for PWRGD_ asserted low.
4	FB1	Power-Good Comparator Input. Connect a resistive divider between output, FB1, and GND to monitor the output voltage (see the *Power-Good (PWRGD_) Detection* section). FB1 is also used as feedback for the current-limit foldback function.
5	PWRGD2	Open-Drain Power-Good Output. POL_SEL determines the output polarity of PWRGD2. PWRGD2 is asserted when FB2 is higher than V_{FB2H}. PWRGD2 deasserts when FB2 is lower than V_{FB2L} (see the *Power-Good (PWRGD_) Detection* section).
6	PWRGD1	Open-Drain Power-Good Output. POL_SEL determines the output polarity of PWRGD1. PWRGD1 is asserted when FB1 is higher than V_{FB1H}. PWRGD1 deasserts when FB1 is lower than V_{FB1L} (see the *Power-Good (PWRGD_) Detection* section).
7	PWRGD3	Open-Drain Power-Good Output. POL_SEL determines the output polarity of PWRGD3. PWRGD3 asserts when GATE is at maximum voltage. PWRGD3 deasserts after the timeout following an overcurrent event (see the *Power-Good (PWRGD_) Detection* section).
8	GND	Ground
9	OUT	Output Voltage. OUT is used as the return path for the internal GATE protection clamping circuitry.
10	TIMER	Timing Input. Connect a capacitor from TIMER to GND to program the maximum time the part is allowed to remain in current limit (see the *TIMER* section).
11	GATE	Gate-Drive Output. The high-side gate drive for the external n-channel MOSFET (see the *GATE* section).
12	FB2	Noninverting Comparator Input. FB2 is used to monitor any other voltage in the system. When FB2 rises higher than V_{FB2H}, PWRGD2 asserts. When FB2 drops below V_{FB2L}, PWRGD2 deasserts.
13	N.C.	No Connection. Not internally connected.
14	SENSE	Current-Sense Input. Connect a sense resistor from V_{CC} to SENSE and the drain of the external n-channel MOSFET.
15	DC	Duty-Cycle Select. When DC is floating, the default duty cycle is 3.75%. Connect DC to V_{CC} to set the duty cycle to 1.88%. Connect DC to GND to set the duty cycle to 0.94%.
16	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with a 0.1µF capacitor. The input voltage range is from +9V to +80V for the MAX5934A and +33V to +80V for the MAX5934.

Positive High-Voltage, Hot-Swap Controllers with Selectable Fault Management and Status Polarity

Functional Diagram



Detailed Description

The MAX5934/MAX5934A are fully integrated hot-swap controllers for positive supply rails. These devices allow for the safe insertion and removal of circuit cards into live backplanes without causing glitches on the backplane power-supply rail. During startup, the MAX5934/MAX5934A act as current regulators using an external sense resistor and MOSFET to limit the amount of current drawn by the load.

The MAX5934A operates from a +9V to +80V supply voltage range and has a default UVLO set to +8.3V. The MAX5934 operates from a +33V to +80V supply voltage range and has a default UVLO set to +31V. The UVLO threshold is adjustable using a resistive divider connected from V_{CC} to ON to GND (see R2 and R3 in Figure 5).

The MAX5934/MAX5934A monitor input voltage, output voltage, output current, and die temperature. These devices feature three power-good outputs (PWRGD_) to indicate status by monitoring the voltage at FB1, FB2, and GATE (see the *Power-Good (PWRGD_) Detection* section). PWRGD1 indicates an output-voltage status, PWRGD2 can be used to indicate an overvoltage condition on the main power-supply rail, and PWRGD3 asserts when GATE voltage has charged to 4.3V above the supply rail. PWRGD3 deasserts when the TIMER voltage exceeds a 1.233V threshold in response to an extended fault condition.

The MAX5934/MAX5934A control gate voltage on the external MOSFET to limit load current at startup and at overload to a value determined as:

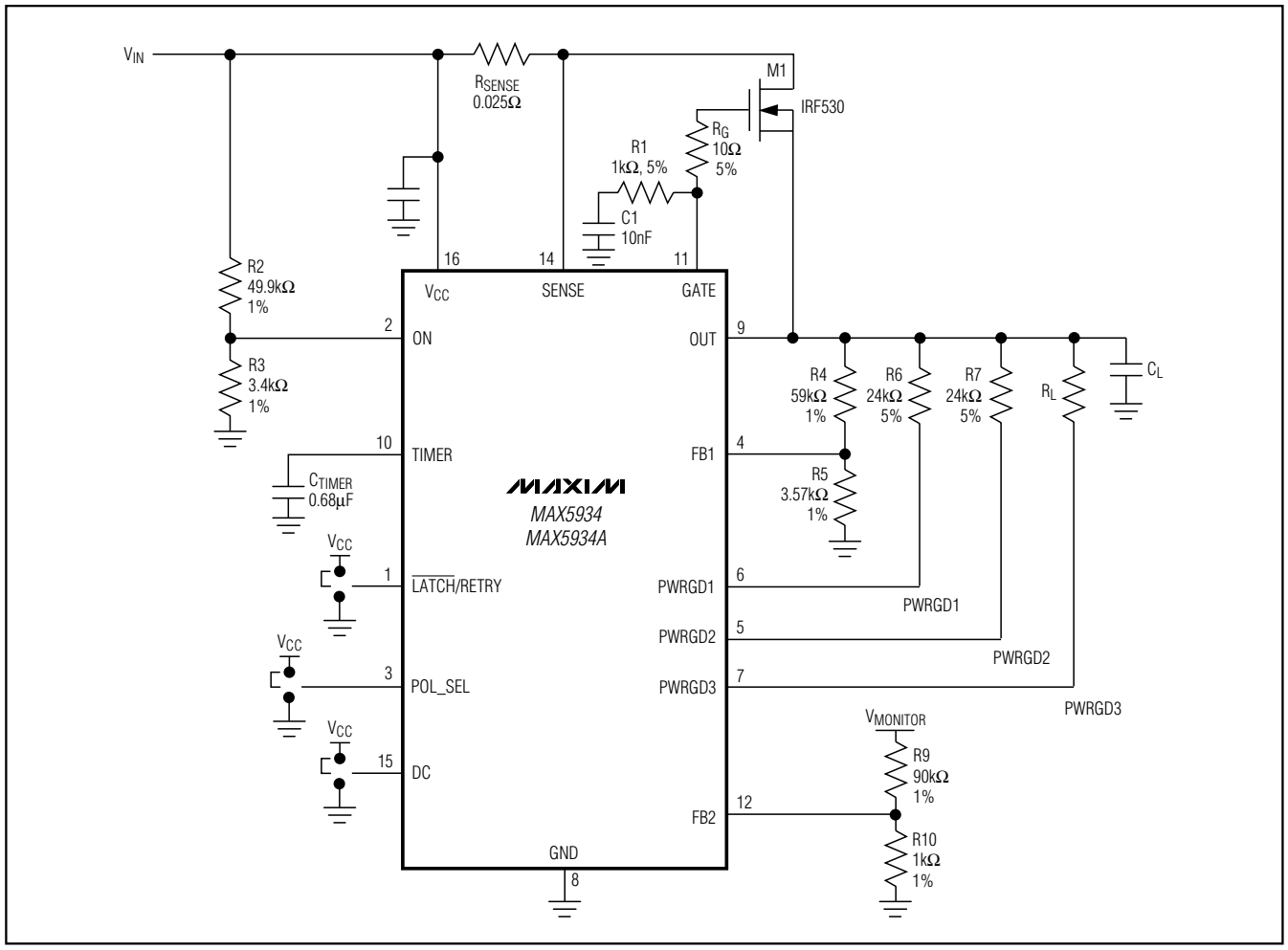


Figure 5. Application Circuit

Positive High-Voltage, Hot-Swap Controllers with Selectable Fault Management and Status Polarity

$$I_{LOAD} = \frac{V_{SENSETRIP}}{R_{SENSE}}$$

where:

$$V_{SENSETRIP} = V_{IN} - V_{SENSE}$$

$V_{SENSETRIP}$ varies from a low of 12mV when the voltage at FB1 = 0V and increases to 47mV as the voltage at FB1 increases to 0.5V and beyond (see Figure 6). Thus, the current limit is low at a low output voltage, and increases as the output voltage reaches its final value. This gradually increases the limiting load current at startup and creates a foldback current limit under overload or short-circuit conditions. See Figure 5 for FB1 and R_{SENSE} connections.

Power-Up Mode

During power-up, the MAX5934/MAX5934A gradually turn on the external n-channel MOSFETs. The MAX5934/MAX5934A monitor and provide current-limit protection to the load at all times. The current limit is programmable using an external current-sense resistor connected from V_{CC} to SENSE. The MAX5934/MAX5934A feature current-limit foldback and duty-cycle limit to ensure robust operation during load-fault and short-circuit conditions *(*see the *Detailed Description* and *Overcurrent Protection* sections*)*.

TIMER

Connect an external capacitor from TIMER to ground to set the maximum overcurrent timeout limit. When the voltage at TIMER reaches 1.233V, GATE goes low and the 75µA pullup current turns off (see the *Functional Diagram*). As a result, a preset pulldown current ($I_{TIMERON}$) discharges the capacitor. To reset the internal fault latch, these two conditions must be met:

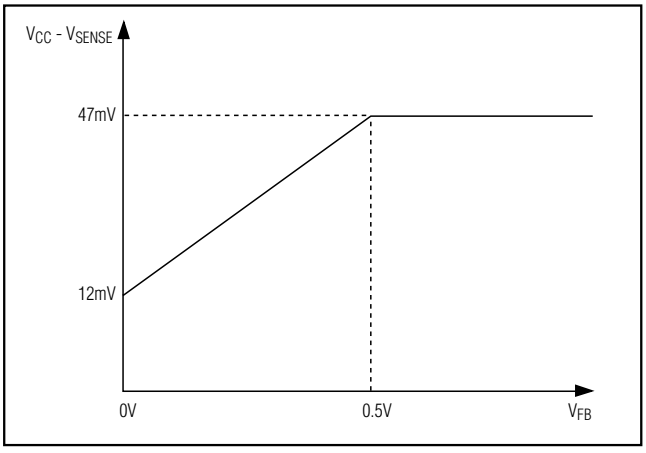


Figure 6. Current-Limit Sense Voltage vs. Feedback Voltage

1) TIMER's voltage goes below 0.5V
2) ON goes low

When the current limit is not active, TIMER goes low by the $I_{TIMERON}$ current source. After the current limit becomes active, the $I_{TIMEROFF}$ pullup current source is connected to TIMER and the voltage rises with a slope of 75µA/C_{TIMER} as long as the current limit remains active. A capacitor from TIMER to GND (C_{TIMER}) sets the desired current-limit timeout:

$$T_{LIMIT} = (C_{TIMER} / 75\mu A) \times 1.233V$$

GATE

GATE provides a high-side gate drive for the external n-channel MOSFET. An internal charge-pump circuit guarantees at least 10V of gate drive for supply voltages higher than 20V (MAX5934A) and a 4.5V gate drive for supply voltages between 10.8V and 20V (MAX5934A) (for the MAX5934, see the *Electrical Characteristics* table). Connect an external capacitor from GATE to ground to set the rising slope of the voltage at GATE.

The voltage at GATE is adjusted to maintain a constant voltage across R_{SENSE} when the current limit is reached while the TIMER capacitor starts to charge. When the voltage at TIMER exceeds 1.233V, the voltage at GATE goes low.

The MAX5934/MAX5934A monitor voltages at ON, V_{CC}, and TIMER. GATE is pulled to GND whenever ON goes low, or the V_{CC} supply voltage decreases below the UVLO threshold, or TIMER increases above the 1.233V threshold.

Gate Voltage

The Gate Drive vs. Supply Voltage graph in the *Typical Operating Characteristics* illustrates that GATE clamps to a maximum of 18V above the input voltage. The MAX5934 minimum gate-drive voltage is 10V at a minimum input-supply voltage of 33V. The MAX5934A minimum gate-drive voltage is 4.5V at a minimum supply of 10.8V. Therefore, a logic-level MOSFET must be used if the input supply is below 20V.

Fault Management ($\overline{LATCH}$/RETRY)

The MAX5934/MAX5934A feature either latched-off or autoretry fault management configurable by the $\overline{LATCH}$/RETRY input. To select automatic restart after a circuit-breaker fault, drive $\overline{LATCH}$/RETRY high (above V_{LRIH}) or leave it floating (see Figure 5).

In latch mode, the MAX5934/MAX5934A turn the MOSFET off and keep it off after an overcurrent fault. After the fault condition goes away and TIMER falls below 0.5V, recycle the power supplies or toggle ON low and high again to unlatch the device.

In autoretry mode, the MAX5934/MAX5934A turn the MOSFET off after an overcurrent fault occurs. After the fault condition is removed, the device waits for TIMER to fall below 0.5V and then automatically restarts. If the fault is due to an overtemperature condition, the MAX5934/MAX5934A wait for the die temperature to cool down below the +130°C threshold before restarting.

Power-Good (PWRGD_) Detection

The MAX5934/MAX5934A feature three power-good outputs (PWRGD_) to indicate the status of three separate voltages. PWRGD_ asserts if the device detects an error condition.

PWRGD_ is true when FB_ voltages exceed the low-to-high threshold voltage (V_{FB_H}). PWRGD_ is false when FB_ voltages go lower than the high-to-low threshold voltage (V_{FB_L}).

Connect external pullup resistors between PWRGD_ and OUT to pull up the PWRGD_ voltages to V_{OUT}.

PWRGD2 can be used to indicate an overvoltage condition on the main power-supply rail.

PWRGD3 asserts when GATE voltage has charged to 4.3V above the supply rail. PWRGD3 deasserts when the TIMER voltage exceeds 1.233V threshold in response to an extended fault condition.

The output polarity of PWRGD_ is determined by POL_SEL. Drive POL_SEL high or leave it floating to select PWRGD_ active high. Connect POL_SEL to GND for PWRGD_ active low.

Undervoltage Lockout (UVLO)

The MAX5934A operates from a +9V to +80V supply voltage range and has a default UVLO set at +8.3V. The MAX5934 operates from a +33V to +80V supply voltage range and has a default UVLO set at +31V. The UVLO thresholds are adjustable using a resistive divider connected to V_{CC} (see R2 and R3 in Figure 5). When the input voltage (or V_{CC}) is below the UVLO threshold, the MOSFET is held off. When the input voltage (or V_{CC}) is above the UVLO threshold, the MAX5934/MAX5934A go into normal operation (or begin to turn on the external MOSFET).

To adjust the UVLO threshold, connect an external resistive divider from V_{IN} (or V_{CC}) to ON and then from ON to GND. The following equation is used to calculate the new UVLO threshold:

$$V_{UVLO\_TH} = V_{REF} (1 + (R2 / R3))$$

where V_{REF} is typically 1.233V.

Applications Information

Hot-Circuit Insertion

The supply bypass capacitors on a circuit board can draw high peak currents from the backplane power bus as they charge when the circuit boards are inserted into a live backplane. This can cause permanent damage to the connector pins and glitch the system supply causing other boards in the system to reset.

The MAX5934/MAX5934A are capable of controlling a board's power-supply voltage allowing for the safe insertion or removal of a board from a live backplane. These devices provide undervoltage and overcurrent protection and power-good output signals (PWRGD_).

Overcurrent Protection

The MAX5934/MAX5934A provide sophisticated overcurrent protection to ensure robust operation under output-current-transient and overcurrent fault conditions. The current-protection circuit employs a foldback current limit and a short-circuit or excessive output-current protection.

The MAX5934/MAX5934A offer a current foldback feature where the current folds back as a function of the output voltage that is sensed at FB1. As Figure 6 illustrates, the voltage across R_{SENSE} decreases linearly when FB1 drops below 0.5V and stops at 12mV when V_{FB1} = 0V. The maximum current-limit equation is:

$$I_{LIMIT} = 47mV / R_{SENSE}$$

For R_{SENSE} = 0.025Ω, the current limit is set to 1.88A and goes down to 480mA at short circuit (output shorted to GND).

In addition, the MAX5934/MAX5934A feature an adjustable overcurrent response time. The required time to regulate the MOSFET current depends on the input capacitance of the MOSFET, GATE capacitor (C1), compensation resistor (R1), and the internal delay from SENSE to GATE. Figure 7 shows the propagation delay from a voltage step at SENSE until GATE starts to fall, as a function of overdrive.

Positive High-Voltage, Hot-Swap Controllers with Selectable Fault Management and Status Polarity

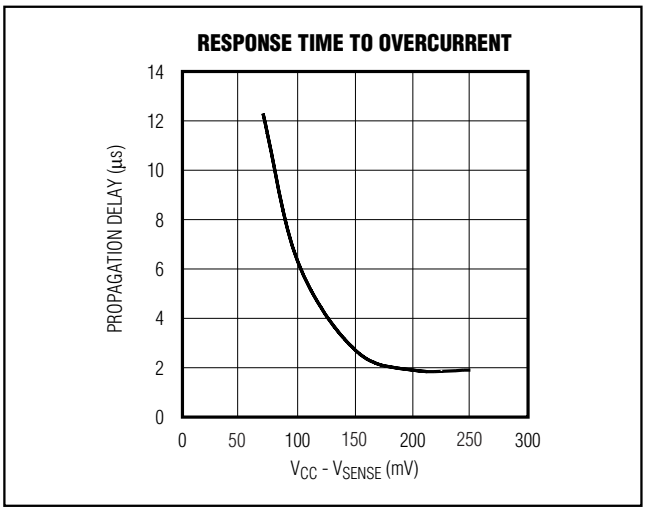


Figure 7. Response Time to Overcurrent

Undervoltage and Overvoltage Detection

An undervoltage fault is detected when V_{ON} goes below the trip point (V_{ONL} = 1.233V). When this occurs, GATE pulls low and stays low until V_{ON} rises above (V_{ONH} = 1.313V).

An example of overvoltage protection is shown in Figure 8. Zener diode D1 turns on when V_{IN} exceeds the diode's breakdown voltage and begins to pull TIMER high. When V_{TIMER} goes higher than 1.233V, a fault is detected and GATE pulls low. As a result, Q1 turns off. Figure 9 shows overvoltage waveforms for V_{IN} (see the *Fault Management (LATCH/RETRY)* section for restart conditions).

Supply Transient Protection

The MAX5934/MAX5934A are guaranteed to be safe from damage with supply voltages of up to 85V. Spikes at voltages above 85V may damage the part. Instantaneous short-circuit conditions, can cause large

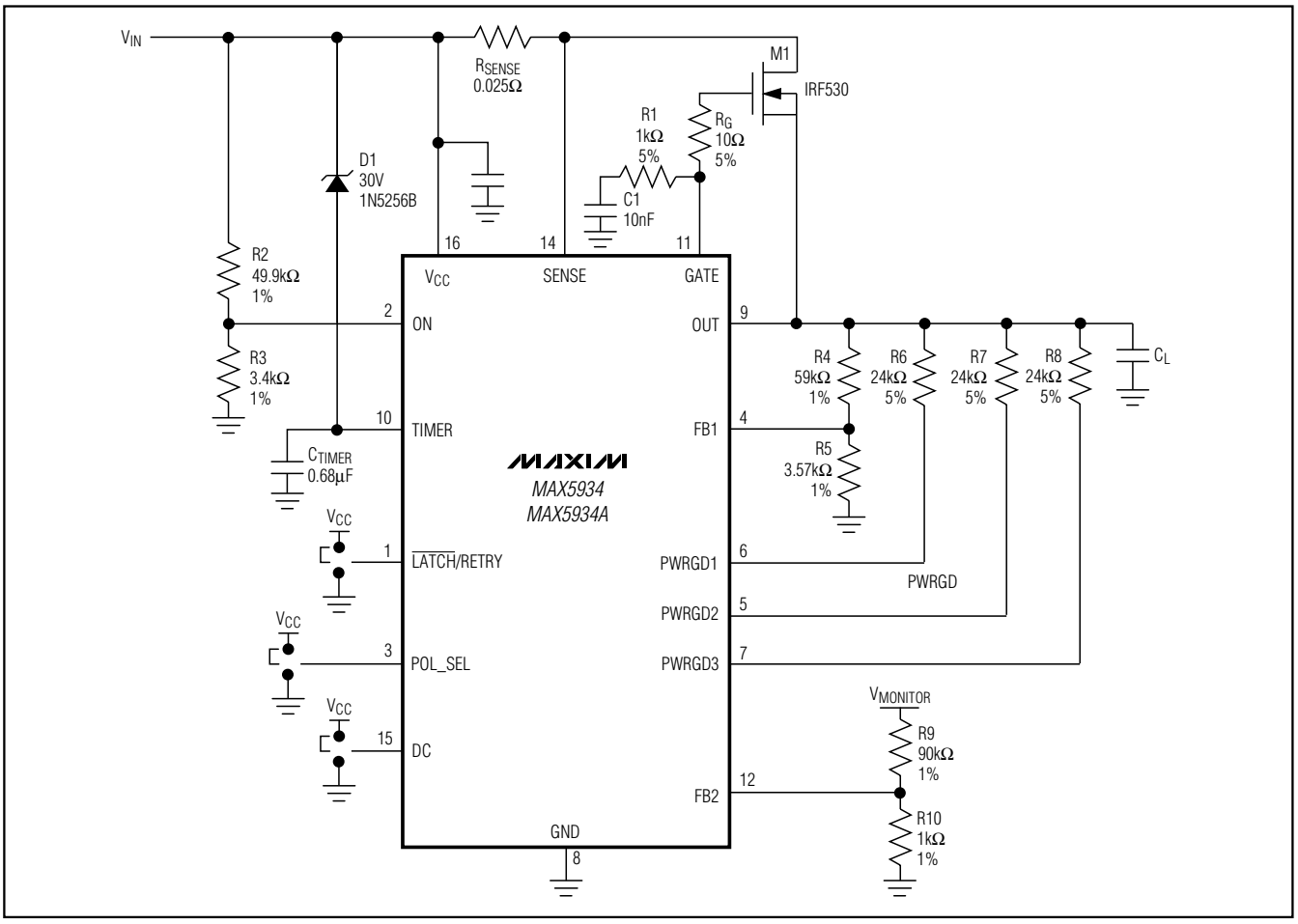


Figure 8. Overvoltage Detection

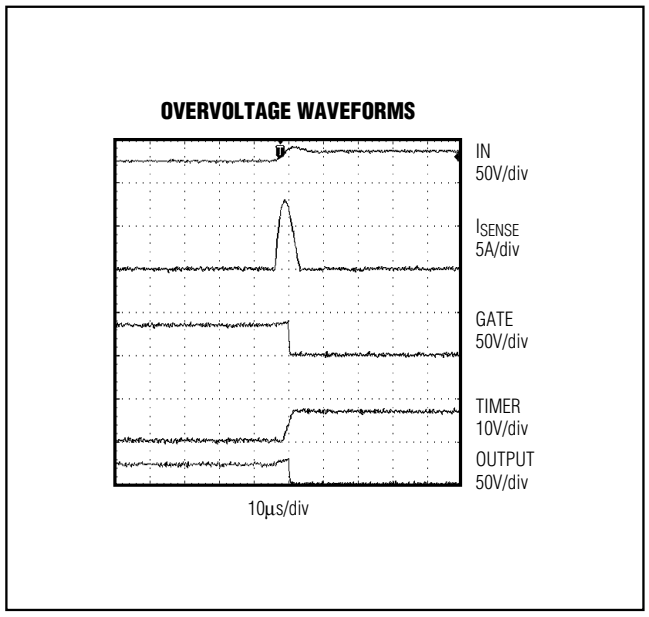


Figure 9. Overvoltage Waveforms

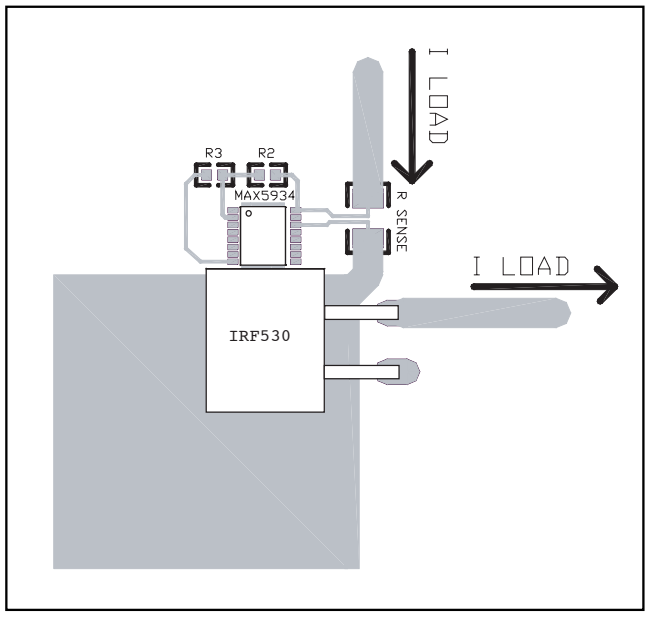


Figure 10. Recommended Layout for R2, R3, and R_{SENSE}

changes in currents flowing through the power-supply traces. This can cause inductive voltage spikes that could exceed 85V. Use wider traces or heavier trace plating and connect a 0.1µF capacitor between V_{CC} and GND to minimize these inductive spikes. Use a transient voltage suppressor (TVS) at the input to prevent damage from voltage surges. An SMBJ54A is recommended.

Power-Up Sequence

At power-up, transistor Q1 (see the *Typical Application Circuit*) is off until these three conditions are met:

- V_{ON} exceeds the turn-on threshold voltage
- V_{CC} exceeds the UVLO threshold
- V_{TIMER} stays below 1.233V

The voltage at GATE increases with a slope of 10µA/C1 (where C1 is shown in the *Typical Application Circuit*) and $I_{INRUSH} = C_L \times 10\mu A / C1$. When the voltage across R_{SENSE} goes too high, the inrush current is limited by the internal current-limit circuitry that adjusts the GATE voltage to keep a constant voltage across R_{SENSE}.

Thermal Shutdown

If the MAX5934/MAX5934A die temperature reaches +150°C, an overtemperature fault is generated. As a result, GATE goes low and turns the external MOSFET off. The MAX5934/MAX5934A die temperature must cool down below +120°C before the overtemperature fault condition is removed.

Board Layout and Bypassing

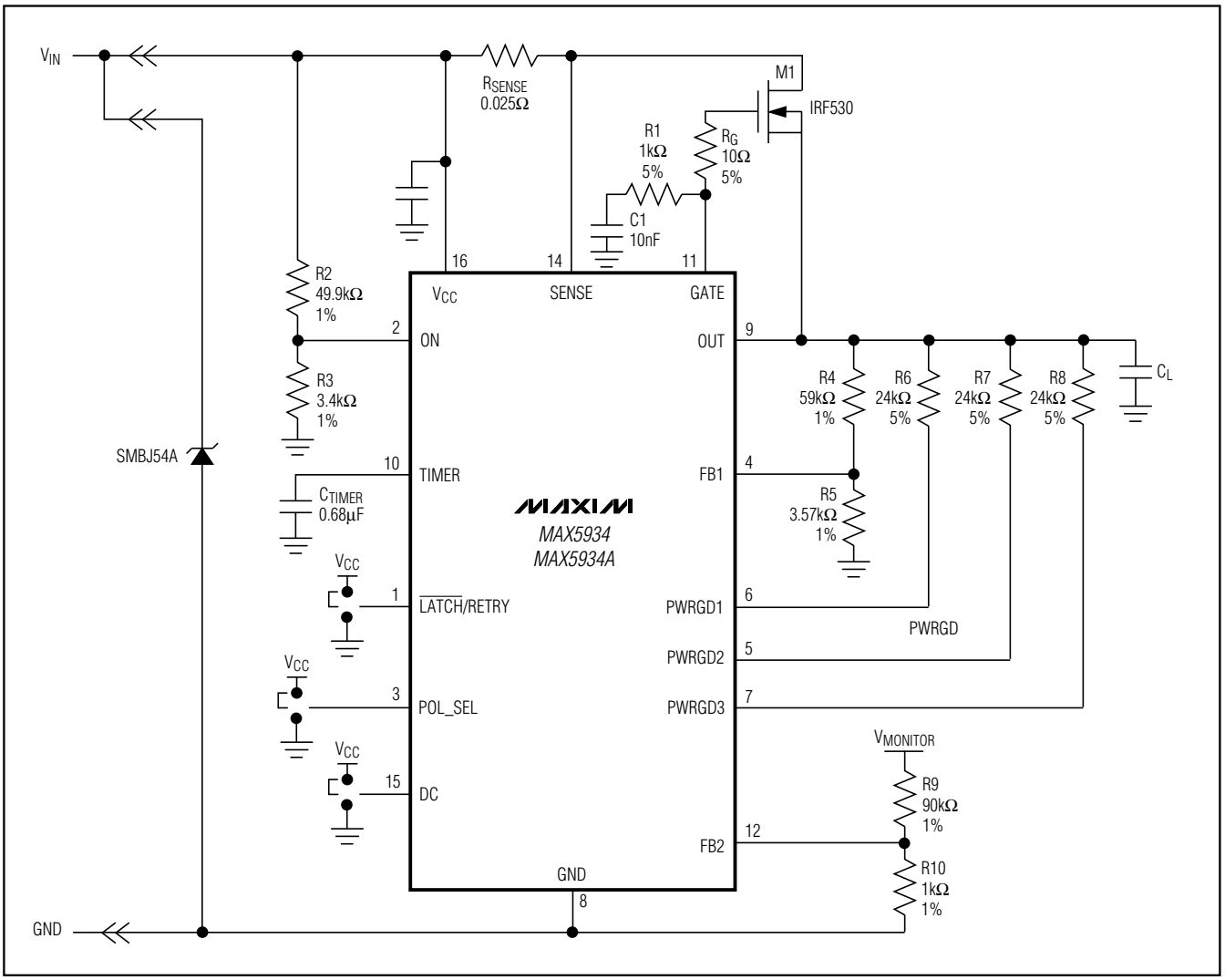
Kelvin connections are recommended for accurate current sensing. Make sure the minimum trace width for 2oz copper is 1.5mm per amp. A width of 4mm per amp is recommended.

Connect a resistive divider from V_{CC} to ON as close as possible to ON and have short traces from V_{CC} and GND. To decrease induced noise connect a 0.1µF capacitor between ON and GND (see Figure 10).

The external MOSFET must be thermally coupled to the MAX5934/MAX5934A to ensure proper thermal shutdown operation.

Positive High-Voltage, Hot-Swap Controllers with Selectable Fault Management and Status Polarity

Typical Application Circuit



Chip Information

TRANSISTOR COUNT: 1573

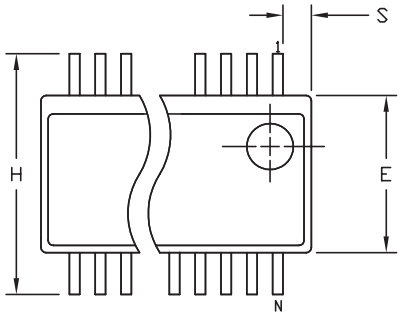
PROCESS: BiCMOS

Positive High-Voltage, Hot-Swap Controllers with Selectable Fault Management and Status Polarity

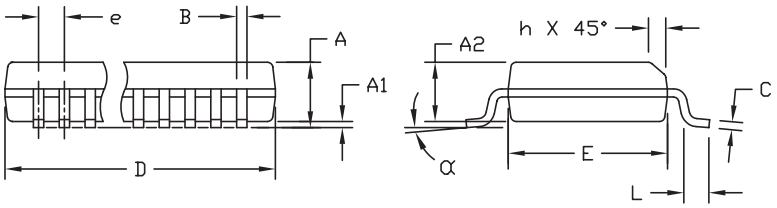
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	E	1/1

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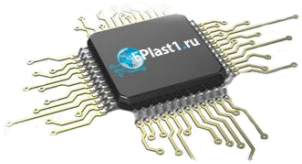
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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