

## ISL59910, ISL59913

Triple Differential Receiver/Equalizer

FN6406  
Rev 1.00  
Sep 28, 2018

The [ISL59910](#) and [ISL59913](#) are triple channel differential receivers and equalizers. They each contain three high speed differential receivers with five programmable poles. The outputs of these pole blocks are then summed into an output buffer. The equalization length is set with the voltage on a single pin. The ISL59910 and ISL59913 output can also be put into a high impedance state, enabling multiple devices to be connected in parallel and used in multiplexing applications.

The gain can be adjusted up or down on each channel by 6dB using the  $V_{GAIN}$  control signal. In addition, a further 6dB of gain can be switched in to provide a matched drive into a cable.

The ISL59910 and ISL59913 have a bandwidth of 150MHz and consume just 108mA on  $\pm 5V$  supply. A single input voltage sets the compensation levels for the required length of cable.

The ISL59910 is a special version of the ISL59913 that decodes syncs encoded onto the common modes of three pairs of CAT-5 cable by the EL4543 refer to the EL4543 datasheet for details.

The ISL59910 and ISL59913 are available in a 28 Ld QFN package and are specified for operation across the full  $-40^{\circ}C$  to  $+85^{\circ}C$  temperature range.

### Features

- 150MHz -3dB bandwidth
- CAT-5 compensation
  - 100MHz at 600ft
  - 135MHz at 300ft
- 108mA supply current
- Differential input range: 3.2V
- Common-mode input range: -4V to +3.5V
- $\pm 5V$  supply
- Output to within 1.5V of supplies
- Available in 28 Ld QFN package
- Pb-free plus anneal available (RoHS compliant)

### Applications

- Twisted-pair receiving/equalizer
- KVM (Keyboard/Video/Mouse)
- VGA over twisted-pair
- Security video

### Related Literature

For a full list of related documents, visit our website:

- [ISL59910](#) and [ISL59913](#) product pages

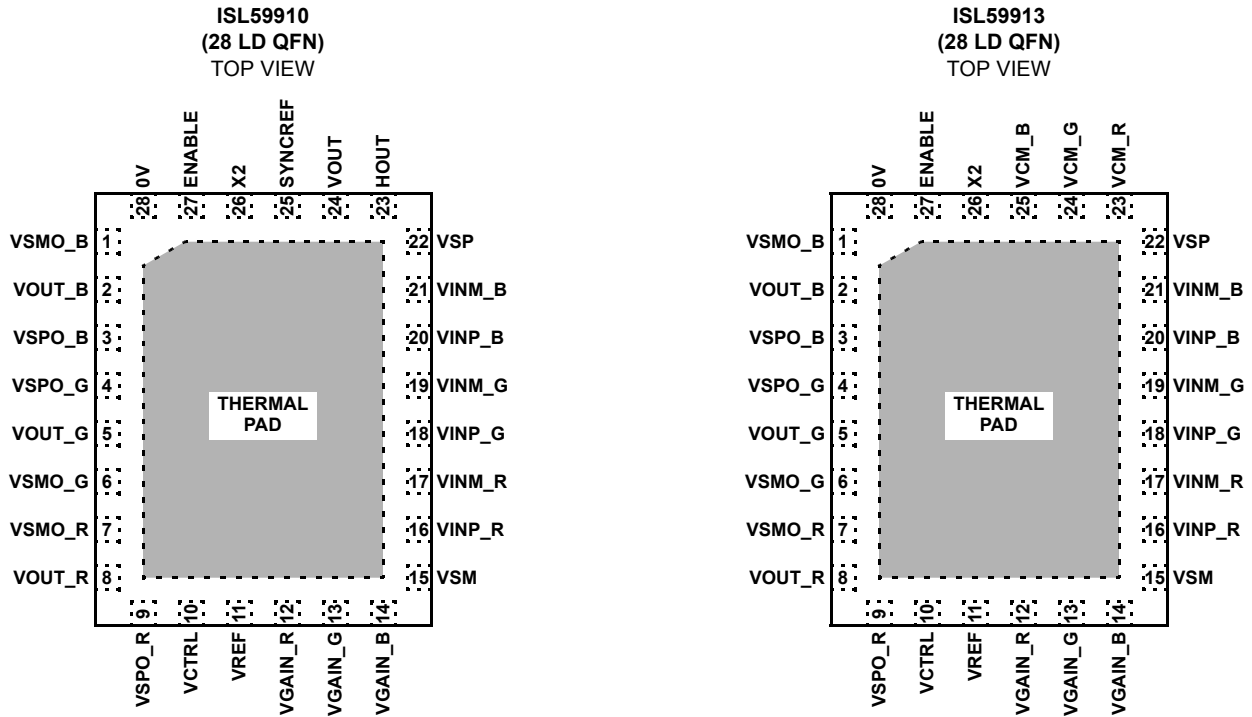
## Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL59910IRZ	59910 CRZ	-	28 Ld QFN	L28.4x5
ISL59910IRZ-T7	59910 CRZ	1k	28 Ld QFN	L28.4x5
ISL59913IRZ	59913 IRZ	-	28 Ld QFN	L28.4x5
ISL59913IRZ-T7	59913 IRZ	1k	28 Ld QFN	L28.4x5
ISL59913IRZ-EVALZ	Evaluation Board			
ISL59910IRZ-EVALZ	Evaluation Board			

NOTES:

1. Refer to [TB347](#) for details about reel specifications.
2. Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the [ISL59910](#) and [ISL59913](#) product information pages. For more information about MSL, see [TB363](#).

## Pinouts



EXPOSED DIEPLATE SHOULD BE CONNECTED TO -5V

## Pin Descriptions

PIN NUMBER	ISL59910		ISL59913	
	PIN NAME	PIN FUNCTION	PIN NAME	PIN FUNCTION
1	VSMO_B	-5V to blue output buffer	VSMO_B	-5V to blue output buffer
2	VOUT_B	Blue output voltage referenced to 0V pin	VOUT_B	Blue output voltage referenced to 0V pin
3	VSPO_B	+5V to blue output buffer	VSPO_B	+5V to blue output buffer
4	VSPO_G	+5V to green output buffer	VSPO_G	+5V to green output buffer

**Pin Descriptions** (Continued)

PIN NUMBER	ISL59910		ISL59913	
	PIN NAME	PIN FUNCTION	PIN NAME	PIN FUNCTION
5	VOUT_G	Green output voltage referenced to 0V pin	VOUT_G	Green output voltage referenced to 0V pin
6	VSMO_G	-5V to green output buffer	VSMO_G	-5V to green output buffer
7	VSMO_R	-5V to red output buffer	VSMO_R	-5V to red output buffer
8	VOUT_R	Red output voltage referenced to 0V pin	VOUT_R	Red output voltage referenced to 0V pin
9	VSPO_R	+5V to red output buffer	VSPO_R	+5V to red output buffer
10	VCTRL	Equalization control voltage (0V to 0.95V)	VCTRL	Equalization control voltage (0V to 0.95V)
11	VREF	Reference voltage for logic signals, V <sub>CTRL</sub> , and V <sub>GAIN</sub> pins	VREF	Reference voltage for logic signals, V <sub>CTRL</sub> , and V <sub>GAIN</sub> pins
12	VGAIN_R	Red channel gain voltage (0V to 1V)	VGAIN_R	Red channel gain voltage (0V to 1V)
13	VGAIN_G	Green channel gain voltage (0V to 1V)	VGAIN_G	Green channel gain voltage (0V to 1V)
14	VGAIN_B	Blue channel gain voltage (0V to 1V)	VGAIN_B	Blue channel gain voltage (0V to 1V)
15	VSM	-5V to core of chip	VSM	-5V to core of chip
16	VINP_R	Red positive differential input	VINP_R	Red positive differential input
17	VINM_R	Red negative differential input	VINM_R	Red negative differential input
18	VINP_G	Green positive differential input	VINP_G	Green positive differential input
19	VINM_G	Green negative differential input	VINM_G	Green negative differential input
20	VINP_B	Blue positive differential input	VINP_B	Blue positive differential input
21	VINM_B	Blue negative differential input	VINM_B	Blue negative differential input
22	VSP	+5V to core of chip	VSP	+5V to core of chip
23	HOUT	Decoded horizontal sync referenced to SYNCREF	VCM_R	Red common-mode voltage at inputs
24	VOUT	Decoded vertical sync referenced to SYNCREF	VCM_G	Green common-mode voltage at inputs
25	SYNCREF	Reference level for H <sub>OUT</sub> and V <sub>OUT</sub> logic outputs	VCM_B	Blue common-mode voltage at inputs
26	X2	Logic signal for x1/x2 output gain setting	X2	Logic signal for x1/x2 output gain setting
27	ENABLE	Chip enable logic signal	ENABLE	Chip enable logic signal
28	0V	0V reference for output voltage	0V	0V reference for output voltage
Thermal Pad		Must be connected to -5V		

**Absolute Maximum Ratings** ( $T_A = +25^\circ\text{C}$ )

Supply Voltage between $V_{S+}$ and $V_{S-}$ .....	12V
Maximum Continuous Output Current per Channel.....	30mA
Power Dissipation.....	See <a href="#">"Typical Performance Curves"</a>
Pin Voltages.....	$V_{S-} -0.5\text{V}$ to $V_{S+} +0.5\text{V}$
Storage Temperature.....	$-65^\circ\text{C}$ to $+150^\circ\text{C}$

**Operating Conditions**

Ambient Operating Temperature.....	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
Die Junction Temperature.....	$+150^\circ\text{C}$

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" can permanently damage the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**IMPORTANT NOTE:** All parameters having Min/Max specifications are ensured. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$

**Electrical Specifications**  $V_{SA+} = V_{A+} = +5\text{V}$ ,  $V_{SA-} = V_{A-} = -5\text{V}$ ,  $T_A = +25^\circ\text{C}$ , exposed die plate =  $-5\text{V}$ , unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
<b>AC PERFORMANCE</b>						
Bandwidth	BW	(See <a href="#">Figure 1</a> )		150		MHz
Slew Rate	SR	$V_{IN} = -1\text{V}$ to $+1\text{V}$ , $V_G = 0.39$ , $V_C = 0$ , $R_L = 75 + 75\Omega$		1.5		kV/ $\mu\text{s}$
Total Harmonic Distortion	THD	10MHz 2V <sub>P-P</sub> out, $V_G = 1\text{V}$ , X2 gain, $V_C = 0$		-50		dBc
<b>DC PERFORMANCE</b>						
Offset Voltage	$V(V_{OUT})_{OS}$	X2 = high, no equalization	-110	-15	+110	mV
Channel-to-Channel Offset Matching	$\Delta V_{OS}$	X2 = high, no equalization	-140	0	+140	mV
<b>INPUT CHARACTERISTICS</b>						
Common-Mode Input Range	CMIR			-4/+3.5		V
Output Noise	$O_{NOISE}$	$V_G = 0\text{V}$ , $V_C = 0\text{V}$ , X2 = HIGH, $R_{LOAD} = 150\Omega$ , Input 50 $\Omega$ to GND, 10MHz		-110		dBm
Common-Mode Rejection Ratio	CMRR	Measured at 10kHz		-80		dB
Common-Mode Rejection Ratio	CMRR	Measured at 10MHz		-55		dB
CM Amplifier Bandwidth	CMBW	10k    10pF load		50		MHz
CM Slew Rate	$CM_{SLEW}$	Measured at $+1\text{V}$ to $-1\text{V}$		100		V/ $\mu\text{s}$
Differential Input Capacitance	$C_{INDIFF}$	Capacitance $V_{INP}$ to $V_{INM}$		600		fF
Differential Input Resistance	$R_{INDIFF}$	Resistance $V_{INP}$ to $V_{INM}$	1			M $\Omega$
CM Input Capacitance	$C_{INCM}$	Capacitance $V_{INP} = V_{INM}$ to GND		1.2		pF
CM Input Resistance	$R_{INCM}$	Resistance $V_{INP} = V_{INM}$ to GND	1			M $\Omega$
Positive Input Current	$+I_{IN}$	DC bias at $V_{INP} = V_{INM} = 0\text{V}$		1		$\mu\text{A}$
Negative Input Current	$-I_{IN}$	DC bias at $V_{INP} = V_{INM} = 0\text{V}$		1		$\mu\text{A}$
Differential Input Range	$V_{INDIFF}$	$V_{INP} - V_{INM}$ when slope gain falls to 0.9	2.5			V
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage Swing	$V(V_{OUT})$	$R_L = 150\Omega$		$\pm 3.5$		V
Output Drive Current	$I(V_{OUT})$	$R_L = 10\Omega$ , $V_{INP} = 1\text{V}$ , $V_{INM} = 0\text{V}$ , X2 = high, $V_G = 0.39$	50	60		mA
CM Output Resistance of VCM_R/G/B (ISL59913 only)	$R(V_{CM})$	At 100kHz		30		$\Omega$
Gain	Gain	$V_C = 0$ , $V_G = 0.39$ , X2 = 5, $R_L = 150\Omega$	0.85	1.0	1.1	
Channel-to-Channel Gain Matching	$\Delta\text{Gain at DC}$	$V_C = 0$ , $V_G = 0.39$ , X2 = 5, $R_L = 150\Omega$		3	8	%
Channel-to-Channel Gain Matching	$\Delta\text{Gain at 15MHz}$	$V_C = 0.6$ , $V_G = 0.39$ , X2 = 5, $R_L = 150\Omega$ , Frequency = 15MHz		3	11	%

**Electrical Specifications**  $V_{SA+} = V_{A+} = +5V$ ,  $V_{SA-} = V_{A-} = -5V$ ,  $T_A = +25^{\circ}C$ , exposed die plate =  $-5V$ , unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
High Level output on V/H <sub>OUT</sub> (ISL59910 only)	V(SYNC) <sub>HI</sub>		V(V <sub>SP</sub> ) - 0.1V		V(V <sub>SP</sub> )	
Low Level output on V/H <sub>OUT</sub> (ISL59910 only)	V(SYNC) <sub>LO</sub>		V(SYNCREF)		V(SYNCREF) + 0.1V	
<b>SUPPLY</b>						
Supply Current per Channel	I <sub>SON</sub>	V <sub>ENBL</sub> = 5, V <sub>INM</sub> = 0	32	36	39	mA
Supply Current per Channel	I <sub>SOFF</sub>	V <sub>ENBL</sub> = 0, V <sub>INM</sub> = 0	0.2		0.4	mA
Power Supply Rejection Ratio	PSRR	DC to 100kHz, ±5V supply		65		dB
<b>LOGIC CONTROL PINS (ENABLE, X2)</b>						
Logic High Level	V <sub>HI</sub>	V <sub>IN</sub> - V <sub>LOGIC</sub> reference for ensured high level	1.4			V
Logic Low Level	V <sub>LOW</sub>	V <sub>IN</sub> - V <sub>LOGIC</sub> reference for ensured low level			0.8	V
Logic High Input Current	I <sub>LOGICH</sub>	V <sub>IN</sub> = 5V, V <sub>LOGIC</sub> = 0V			50	μA
Logic Low Input Current	I <sub>LOGICL</sub>	V <sub>IN</sub> = 0V, V <sub>LOGIC</sub> = 0V			15	μA

**Typical Performance Curves**

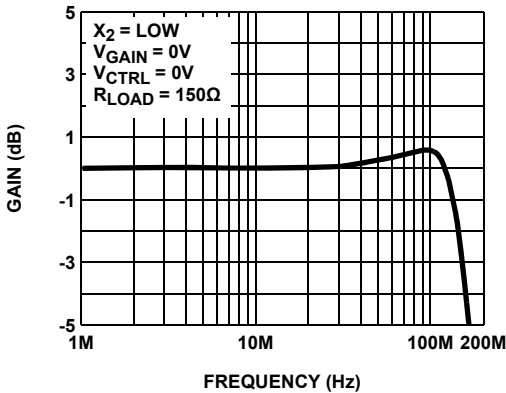


FIGURE 1. FREQUENCY RESPONSE OF ALL CHANNELS

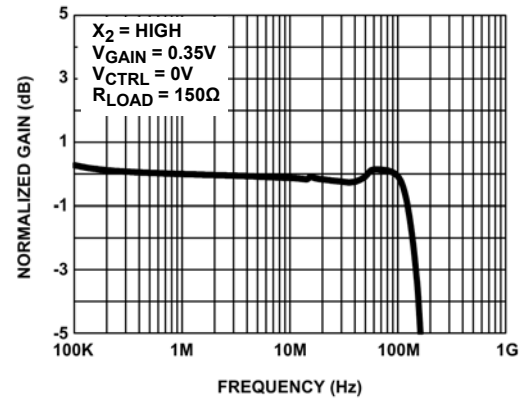


FIGURE 2. GAIN vs FREQUENCY ALL CHANNELS

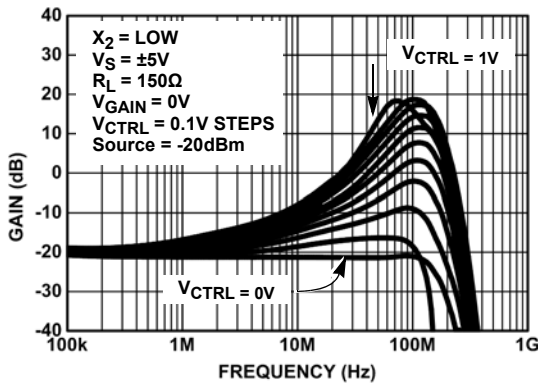


FIGURE 3. GAIN vs FREQUENCY FOR VARIOUS V<sub>CTRL</sub>

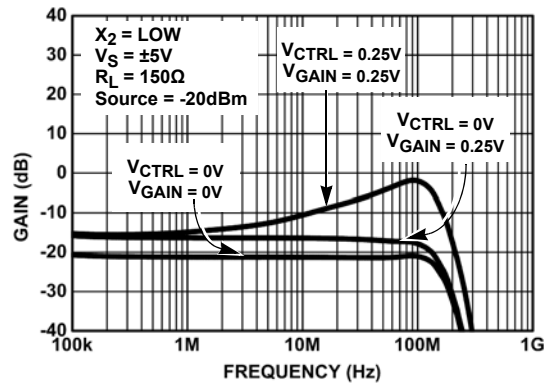


FIGURE 4. GAIN vs FREQUENCY FOR VARIOUS V<sub>CTRL</sub> AND V<sub>GAIN</sub>

**Typical Performance Curves** (Continued)

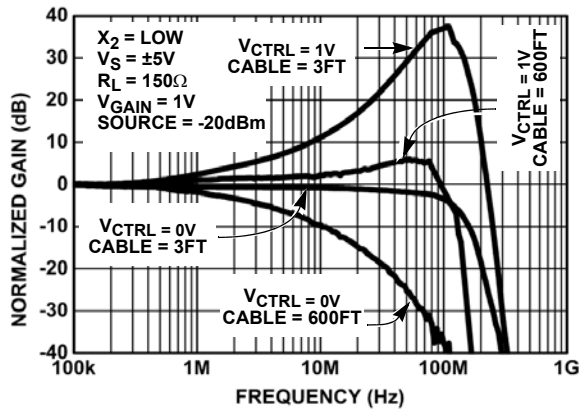


FIGURE 5. GAIN vs FREQUENCY FOR VARIOUS  $V_{CTRL}$  AND CABLE LENGTHS

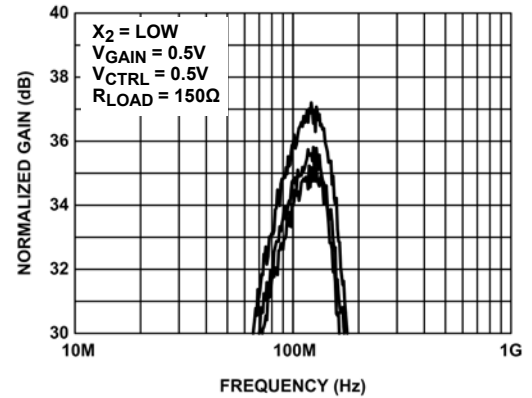


FIGURE 6. CHANNEL MISMATCH

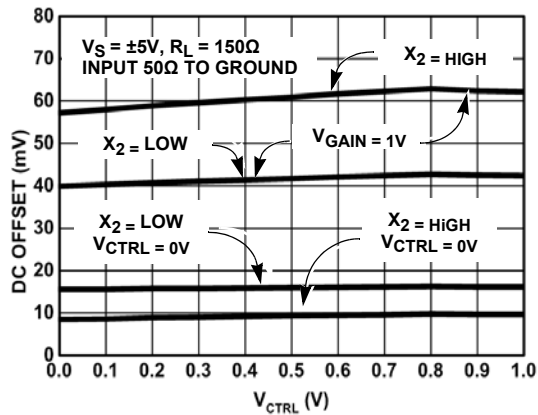


FIGURE 7. OFFSET vs  $V_{CTRL}$

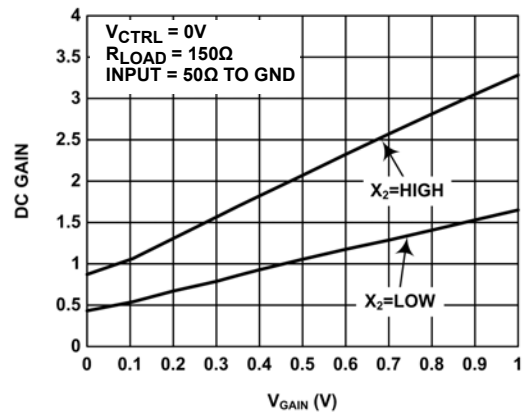


FIGURE 8. DC GAIN vs  $V_{GAIN}$

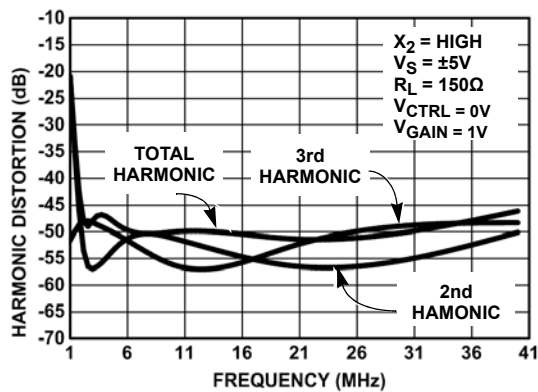


FIGURE 9. HARMONIC DISTORTION vs FREQUENCY

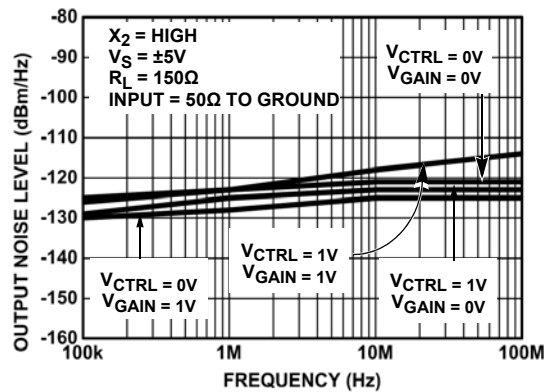


FIGURE 10. OUTPUT NOISE

**Typical Performance Curves** (Continued)

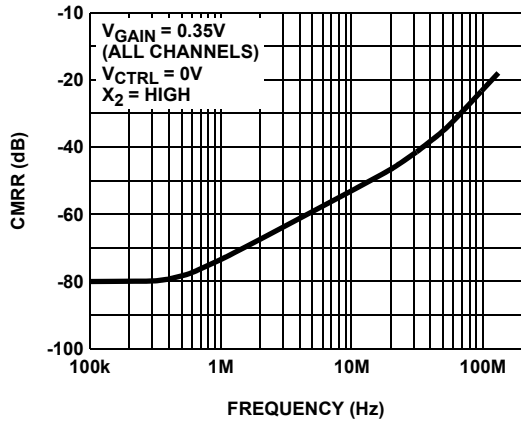


FIGURE 11. COMMON-MODE REJECTION

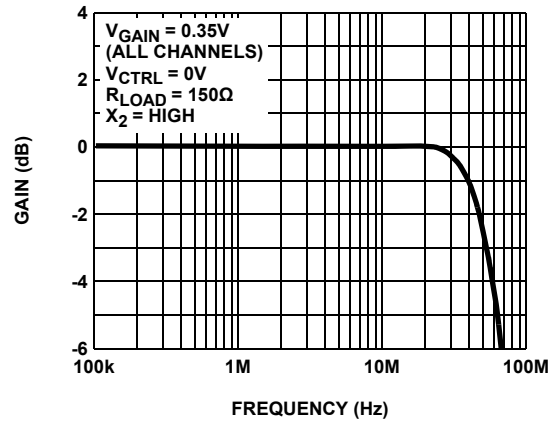


FIGURE 12. CM AMPLIFIER BANDWIDTH

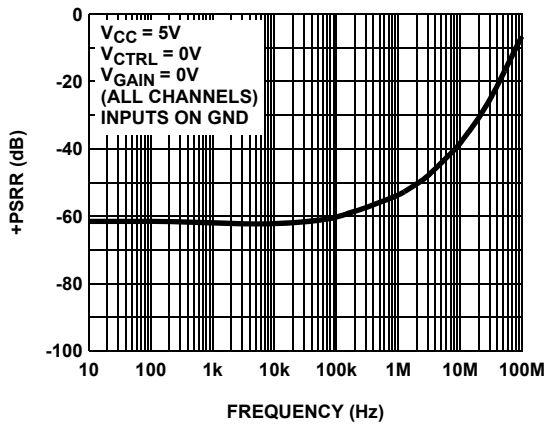


FIGURE 13. (+)PSRR vs FREQUENCY

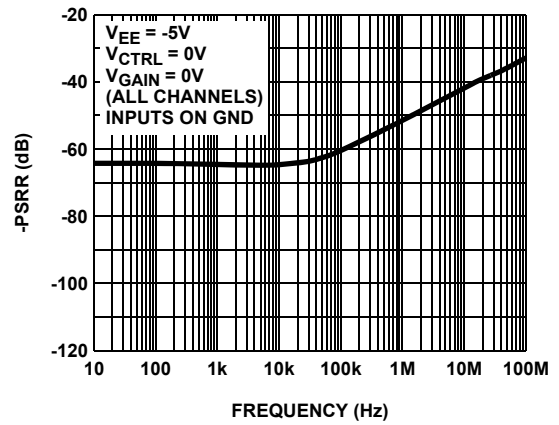


FIGURE 14. (-)PSRR vs FREQUENCY

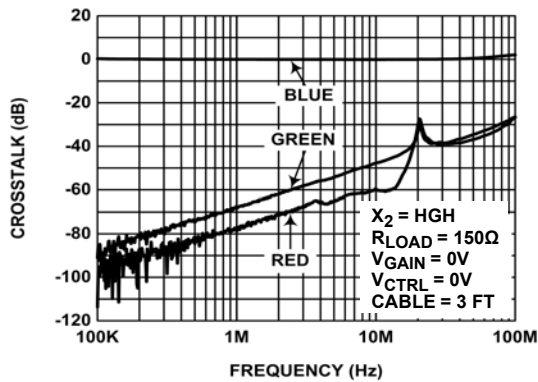


FIGURE 15. BLUE CROSSTALK (CABLE LENGTH = 3ft.)

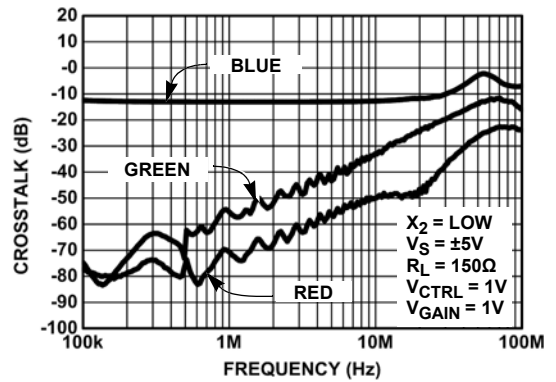


FIGURE 16. BLUE CROSSTALK (CABLE LENGTH = 600ft.)

**Typical Performance Curves** (Continued)

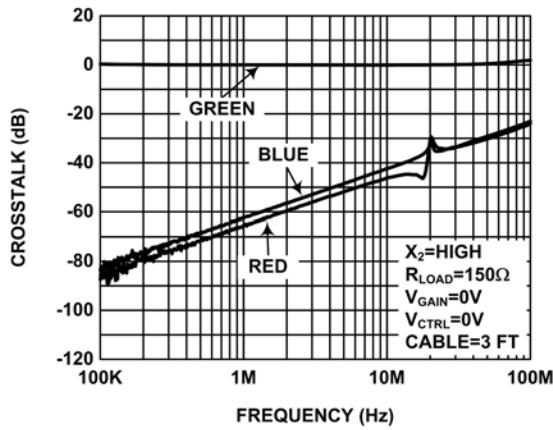


FIGURE 17. GREEN CROSSTALK (CABLE LENGTH = 3ft.)

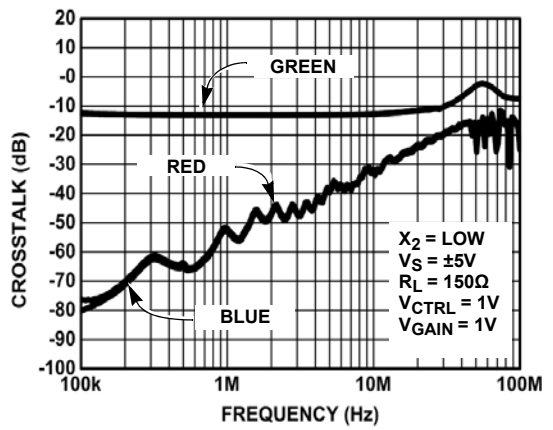


FIGURE 18. GREEN CROSSTALK (CABLE LENGTH = 600ft.)

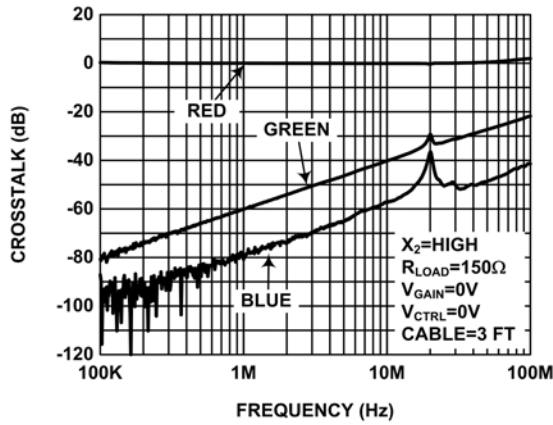


FIGURE 19. RED CROSSTALK (CABLE LENGTH = 3ft.)

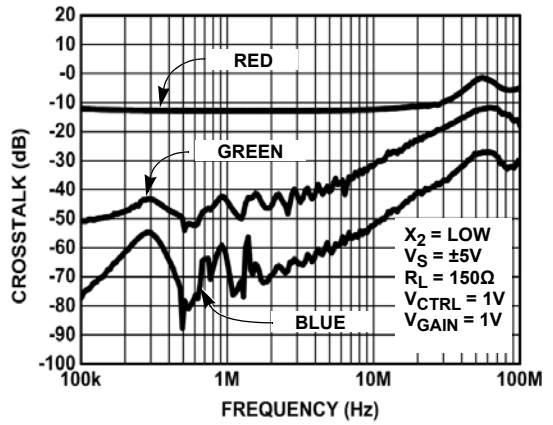


FIGURE 20. RED CROSSTALK (CABLE LENGTH = 600ft.)

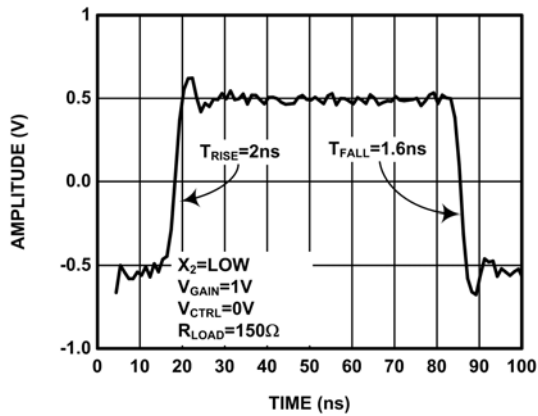


FIGURE 21. RISE TIME AND FALL TIME

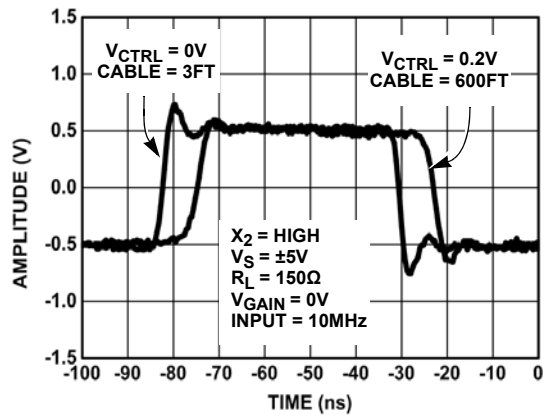


FIGURE 22. PULSE RESPONSE FOR VARIOUS CABLE LENGTHS



## Typical Performance Curves (Continued)

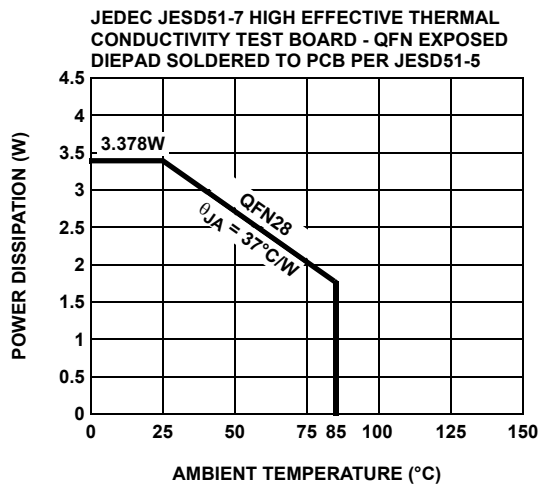


FIGURE 23. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

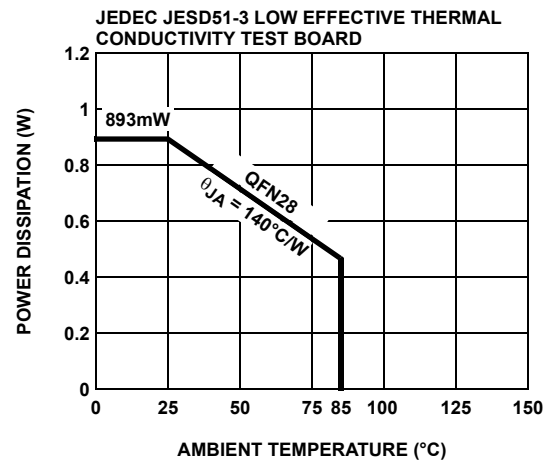


FIGURE 24. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

## Applications Information

### Logic Control

The ISL59913 has two logical input pins, Chip Enable (ENABLE) and Switch Gain (X2). The logic circuits all have a nominal threshold of 1.1V above the potential of the logic reference pin (VREF). In most applications it is expected that this chip runs from a +5V, 0V, -5V supply system with logic being run between 0V and +5V. In this case, tie the logic reference voltage to the 0V supply. If the logic is referenced to the -5V rail, connect the logic reference to -5V. The logic reference pin sources about 60 $\mu$ A and this rises to about 200 $\mu$ A if all inputs are true (positive).

The logic inputs all source up to 10 $\mu$ A when they are held at the logic reference level. When taken positive, the inputs sink a current dependent on the high level, up to 50 $\mu$ A for a high level 5V above the reference level.

If the logic inputs are not used, tie them to the appropriate voltage to define their state.

### Control Reference and Signal Reference

Analog control voltages are required to set the equalizer and contrast levels. These signals are voltages in the range 0V to 1V, which are referenced to the control reference pin. It is expected that the control reference pin is tied to 0V and the control voltage varies from 0V to 1V. It is, however, acceptable to connect the control reference to any potential between -5V and 0V to which the control voltages are referenced.

The control voltage pins themselves are high impedance. The control reference pin sources between 0 $\mu$ A and 200 $\mu$ A depending on the control voltages being applied.

The control reference and logic reference effectively remove the necessity for the 0V rail and operation from  $\pm$ 5V (or 0V and 10V) only is possible. However, we still need a further reference to

define the 0V level of the single-ended output signal. The reference for the output signal is provided by the 0V pin. The output stage cannot pull fully up or down to either supply so it is important that the reference is positioned to allow full output swing. Tie the 0V reference to a quiet reference as any noise on this pin is transferred directly to the output. The 0V pin is a high impedance pin and draws DC bias currents of a few  $\mu$ A and similar levels of AC current.

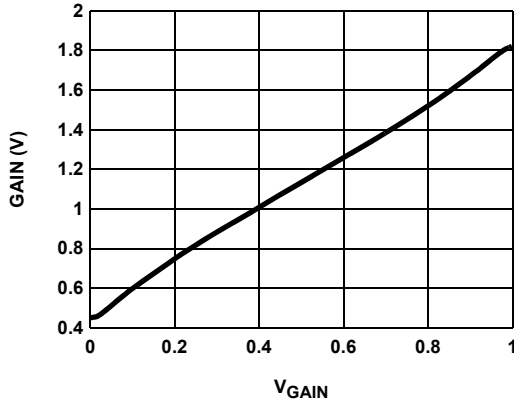
### Equalizing

When transmitting a signal across a twisted pair cable, the high frequency (above 1MHz) information is attenuated more significantly than the information at low frequencies. The attenuation is predominantly due to resistive skin effect losses and has a loss curve which depends on the resistivity of the conductor, surface condition of the wire, and the wire diameter. For the range of high performance twisted pair cables based on 24awg copper wire (CAT-5 etc), these parameters vary only a little between cable types and in general cables exhibit the same frequency dependence of loss. (The lower loss cables can be compared with somewhat longer lengths of similar cables.) This enables a single equalizing law equation to be built into the ISL59913.

With a control voltage applied between pins VCTRL and VREF, the frequency dependence of the equalization is shown in [Figure 8 on page 6](#). The equalization matches the cable loss up to about 100MHz. Above this, system gain is rolled off rapidly to reduce noise bandwidth. The roll-off occurs more rapidly for higher control voltages, thus the system (cable + equalizer) bandwidth reduces as the cable length increases. This is desirable, as noise increases as the equalization increases.

**Contrast**

By varying the voltage between pins VGAIN and VREF, the gain of the signal path can be changed in the ratio 4:1. The gain change varies almost linearly with control voltage. For normal operation it is anticipated the X2 mode is selected and the output load is back matched. A unity gain to the output load is achieved with a gain control voltage of about 0.35V. This allows the gain to be trimmed up or down by 6dB to compensate for any gain/loss errors that affect the contrast of the video signal. [Figure 25](#) shows an example plot of the gain to the load with gain control voltage.



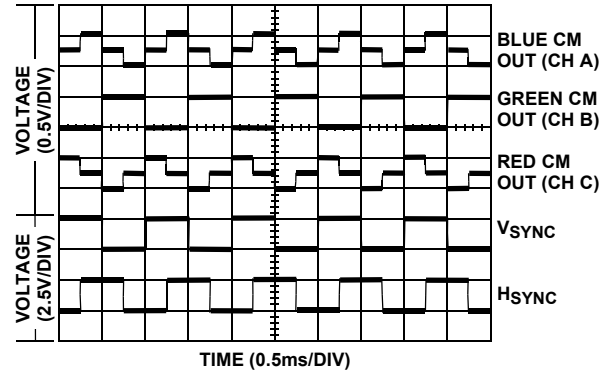
**FIGURE 25. VARIATION OF GAIN WITH GAIN CONTROL VOLTAGE**

**Common-Mode Sync Decoding**

The ISL59910 features common-mode decoding to allow horizontal and vertical synchronization information, which has been encoded on the three differential inputs by the EL4543, to be decoded. The entire RGB video signal can therefore be transmitted, along with the associated synchronization information, by using just three twisted pairs.

Decoding is based on the EL4543 encoding scheme, as described in [Figure 26](#) and [Table 1](#). The scheme is a three-level system, which has been designed such that the sum of the common-mode voltages results in a fixed average DC level with no AC content. This eliminates the effect of EMI radiation into the common-mode signals along the twisted pairs of the cable

The common-mode voltages are initially extracted by the ISL59910 from the three input pairs. These are then passed to an internal logic decoding block to provide Horizontal and Vertical sync output signals (H<sub>OUT</sub> and V<sub>OUT</sub>).



**FIGURE 26. H AND V SYNCs ENCODED**

**TABLE 1. H AND V SYNC DECODING**

RED CM	GREEN CM	BLUE CM	H <sub>SYNC</sub>	V <sub>SYNC</sub>
Mid	High	Low	Low	Low
High	Low	Mid	Low	High
Low	High	Mid	High	Low
Mid	Low	High	High	High

NOTE: Level 'Mid' is halfway between 'High' and 'Low'

**Power Dissipation**

The ISL59910 and ISL59913 are designed to operate with ±5V supply voltages. The supply currents are tested in production and specified to be less than 39mA per channel. Operating at ±5V power supply, the total power dissipation is:

$$PD_{MAX} = 3 \times \left[ 2 \times V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \right] \tag{EQ. 1}$$

where:

- PD<sub>MAX</sub> = Maximum power dissipation
- V<sub>S</sub> = Supply voltage = 5V
- I<sub>SMAX</sub> = Maximum quiescent supply current per channel = 39mA
- V<sub>OUTMAX</sub> = Maximum output voltage swing of the application = 2V
- R<sub>L</sub> = Load resistance = 150Ω

$$PD_{MAX} = 1.29W \tag{EQ. 2}$$

$\theta_{JA}$  required for long term reliable operation can be calculated using [Equation 3](#):

$$\theta_{JA} = \frac{(T_J - T_A)}{PD} = 50.4 \text{CW} \quad (\text{EQ. 3})$$

where

- $T_J$  is the maximum junction temperature (+150°C)
- $T_A$  is the maximum ambient temperature (+85°C)

For a QFN 28 package in a properly laid out PCB heatsinking copper area, +37°C/W  $\theta_{JA}$  thermal resistance can be achieved. To disperse the heat, the bottom heatspreader must be soldered to the PCB. Heat flows through the heatspreader to the circuit board copper, then spreads and converts to air. Thus the PCB copper plane becomes the heatsink. This has proven to be a very effective technique.

**Revision History** The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Sep 28, 2018	FN6406.1	Added Related Literature section. Moved Pinouts after Ordering Information table. Updated Ordering Information table by updating brand for ISL59913 parts, adding Notes 1 and 3, adding Evaluation boards, updating POD number, and updating tape and reel column. Added Revision History. Updated disclaimer and moved to end of document. Updated POD from MDP0046 to L28.4x5.

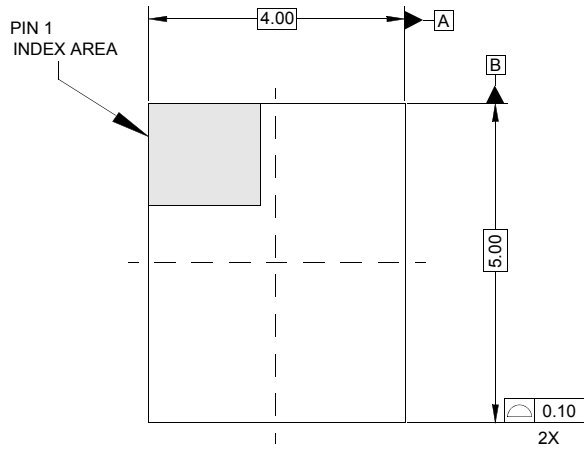
**Package Outline Drawing**

For the most recent package outline drawing, see [L28.4x5](#).

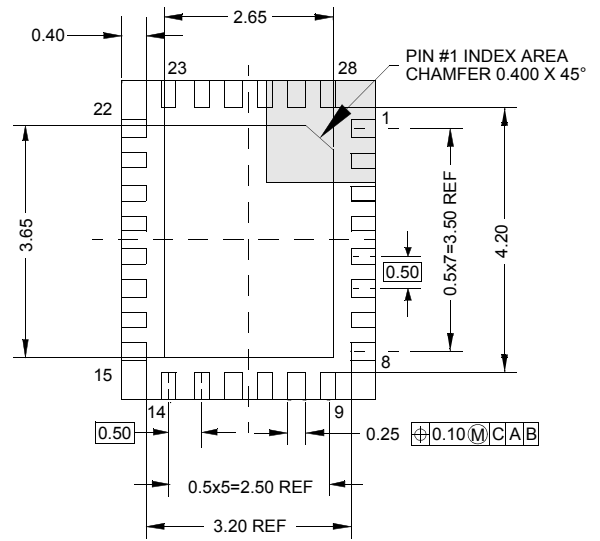
**L28.4x5**

**28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE**

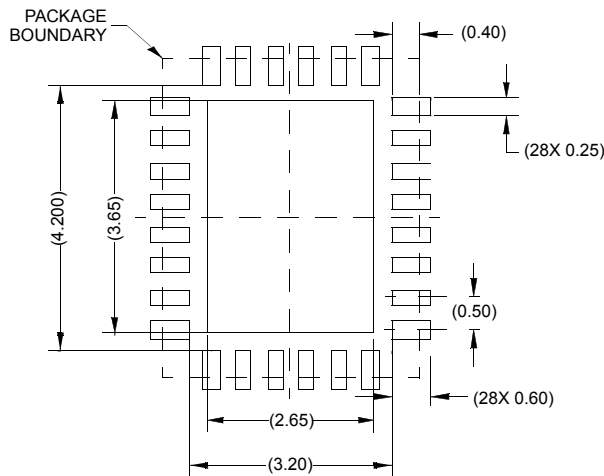
Rev 0, 9/06



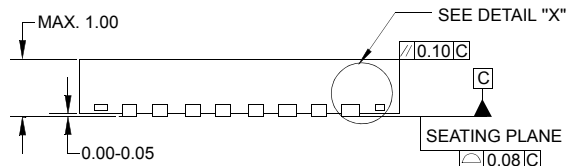
TOP VIEW



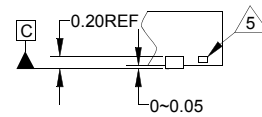
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

**NOTES:**

1. Controlling dimensions are in mm.  
Dimensions in ( ) for reference only.
2. Unless otherwise specified, tolerance : Decimal  $\pm 0.05$   
Angular  $\pm 2^\circ$
3. Dimensioning and tolerancing conform to AMSE Y14.5M-1994.
4. Bottom side Pin#1 ID is diepad chamfer as shown.
5. Tiebar shown (if present) is a non-functional feature.

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#### Renesas Electronics Corporation

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

#### Renesas Electronics America Inc.

1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.  
Tel: +1-408-432-8888, Fax: +1-408-434-5351

#### Renesas Electronics Canada Limited

9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3  
Tel: +1-905-237-2004

#### Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K  
Tel: +44-1628-651-700

#### Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

#### Renesas Electronics (China) Co., Ltd.

Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

#### Renesas Electronics (Shanghai) Co., Ltd.

Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China  
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

#### Renesas Electronics Hong Kong Limited

Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2265-6688, Fax: +852 2886-9022

#### Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan  
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

#### Renesas Electronics Singapore Pte. Ltd.

80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949  
Tel: +65-6213-0200, Fax: +65-6213-0300

#### Renesas Electronics Malaysia Sdn.Bhd.

Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jin Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

#### Renesas Electronics India Pvt. Ltd.

No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India  
Tel: +91-80-67208700, Fax: +91-80-67208777

#### Renesas Electronics Korea Co., Ltd.

17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea  
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#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.