Polar Encoder/Decoder v1.0

PB051 August 30, 2018 **LogiCORE IP Product Brief**

Introduction

The Polar Encoder/Decoder soft IP core supports Polar encoding and decoding. The Polar codes are configurable and can be used on a block-by-block basis.

Note: In this document, a block is the general term for an atomic unit of data processed by an encoder or decoder. A codeword is the specific form of an encoded block and is used when discussing the code parameters used to generate it.

Additional Documentation

A product guide is available for this core. Access to this material can be requested by clicking on this registration link: www.xilinx.com/member/polar-cores.html

Features

- Supports *3GPP TS 38.212 V15.1.1 3rd Generation Partnership Project; Technical Specification Group Radio Access Network; NR; Multiplexing and channel coding (Release 15)*
- Throughput(1) up to:
  - >80 Mb/s for decoder (N=1024, K=200)
  - >700 Mb/s for encoder (N=1024, K=200)
- High bandwidth AXI4-Stream interfaces

1. See performance in the Polar Encoder/Decoder Product Guide (PG280). Figures are for a clock frequency of 400 MHz and should be scaled for achieved clock frequency. Throughput is a function of many factors including code size, code mix, clock frequency and augmentation parameters

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	UltraScale™, UltraScale+™ 7 Series
Supported User Interfaces	AXI4-Lite, AXI4-Stream
Provided with Core	
Design Files	N/A
Example Design	IP Integrator Block Diagram
Test Bench	N/A
Constraints File	Xilinx Design Constraints (XDC)
Simulation Model	System Verilog Secure model Bit-accurate C model MEX file for use with MATLAB
Supported S/W Driver	Standalone
Tested Design Flows(2)	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide(3).
Synthesis	Vivado
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.
3. The Early Access version of this core only supports Mentor Graphics Questa Advanced Simulator v10.5c

Overview

Forward Error Correction (FEC) codes such as Polar codes provide a means to control errors in data transmissions over unreliable or noisy communication channels. The Polar Encoder/Decoder core provides an optimized block for encoding and soft-decision decoding of these codes. Codes can be specified through an AXI4-Lite bus. A block diagram of the Polar Encoder/Decoder core is shown in Figure 1.

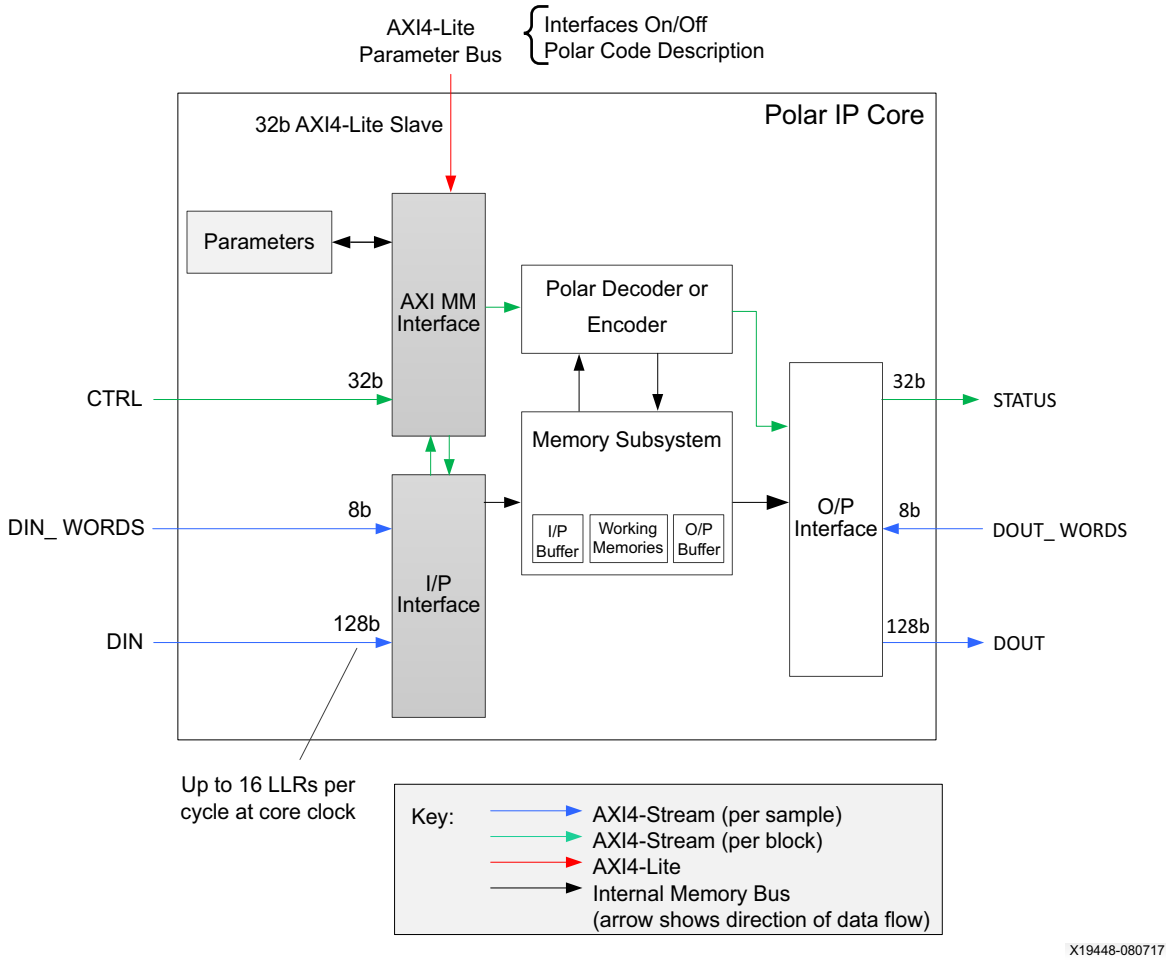

Figure 1: **Polar Encoder/Decoder Core Block Diagram**

Feature Summary

The Polar Encoder/Decoder soft IP core is a highly flexible soft-decision implementation for Polar codes offering the following features.

- Decoder performs Successive Cancellation List decoding with a list size of eight augmented by parity and/or CRC bits according to *3GPP TS 38.212 V15.1.1*.
- Ability to specify number of inputs and outputs on either a block-by-block basis or transfer basis.
- Up to 128 codes configured over an AXI4-Lite interface.
- Codes selected on a block-by-block basis.
- Codeword sizes from N=32 to N=1024, K from 2 to N, K_{max} is 140 when interleaved.
- As an encoder, the core accepts K bits of information and outputs N encoded bits; as a decoder, the core accepts N soft value log-likelihood ratios (LLR) and outputs K hard decision bits.
- 8 bit soft value LLR inputs are accepted by the decoder, with external saturation to symmetric range assumed.
- Supports only in-order execution of blocks.
- Wide data interfaces on input and output.
- Separate input and output streams allow control parameters and status to be provided on a block-by-block basis.

Applications

The Polar Encoder/Decoder core is intended for, but not limited to, use in applications requiring Polar encode/decode, such as 5G wireless (*3GPP TS 38.212 V15.1.1 Multiplexing and channel coding (Release 15)*). UCI, DCI, and BCH use cases are supported.

Technical Support

Xilinx provides technical support at the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

Licensing and Ordering Information

This Xilinx LogiCORE™ IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado® Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. To generate a full license, visit the product licensing web page. Evaluation licenses and hardware timeout licenses might be available for this core or subsystem. Contact your local Xilinx sales representative for information about pricing and availability.

For more information, visit the Polar Encoder/Decoder product web page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

Revision History

The following table shows the revision history for this document:

Date	Version	Revision
08/30/2018	1.0	Updated Feature Summary and Applications to align with PG280 (2018.2).
11/15/2017	1.0	Initial Xilinx Release.

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- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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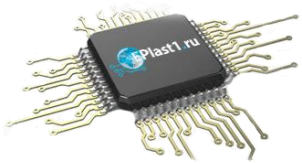
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.