CMOS Linear Integrated Circuits Silicon Monolithic

# TC75S70L6X

#### 1. Functional Description

Single Comparator

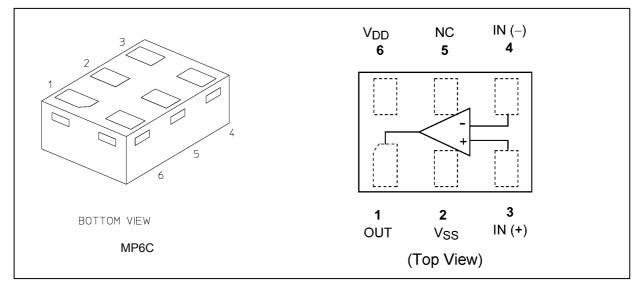
#### 2. General

This is a CMOS Input/Output full swing comparator with low operating voltage and low supply current. The comparator have low operating voltage  $V_{DD}$  = 1.3 V to 5.5 V and low supply current  $I_{DD}$  = 18 µA (typ.) @V<sub>DD</sub> = 1.5 V. Output circuit type is push-pull circuit. The package MP6C (1.0 mm × 1.45 mm, t: 0.55 mmMAX) is ultra small, so that it is ideal for high-density assembly such as cellular phone.

#### 3. Features

- (1) Single circuit, Input/Output full swing comparator
- (2) Low operating voltage:  $V_{DD}$  = 1.3 V to 5.5 V
- (3) Low supply current:  $I_{DD} = 18 \ \mu A$  (typ.) (@V<sub>DD</sub> = 1.5 V)
- (4) Ultra Small package: MP6C (1.0 mm  $\times$  1.45 mm, t = 0.55 mmMAX)
- (5) Low input bias current: 1 pA (typ.)
- (6) Push-pull output circuit
- (7) Single power supply operation

#### 4. Packaging and Pin Assignment



#### 5. Absolute Maximum Ratings (Note) (Unless otherwise specified, T<sub>a</sub> = 25 °C)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V <sub>DD</sub>		±3.0 or 6.0	V
Differential input voltage	$\Delta V_{IN}$		±6.0	V
Input voltage	V <sub>IN</sub>		$V_{SS}$ to $V_{DD}$	V
Output current	I <sub>OUT</sub>		±35	mA
Power dissipation	PD	(Note 1)	250	mW
Operating temperature	T <sub>opr</sub>		-40 to 85	°C
Storage temperature	T <sub>stg</sub>		-55 to 125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note: Since this device is susceptible to latch-up, a phenomenon inherent to CMOS devices, follow these considerations:

- Don't raise the voltage level of the output pins above  $V_{\text{DD}}$  or lower it below  $V_{\text{SS}}.$ 

Consider the power-on timing as well.

- Ensure that any abnormal noise is not introduced into the device.

Note 1: Mounted on an FR4 board.

#### 6. Operating Ratings (Unless otherwise specified, $T_a = 25 \text{ °C}$ )

Characteristics	Symbol	Rating	Unit	
Supply voltage	V <sub>DD</sub>	1.3 to 5.5	V	
Supply voltage	V <sub>DD</sub> ,V <sub>SS</sub>	±0.65 to 2.75	V	

#### 7. Electrical Characteristics

#### 7.1. $V_{DD}$ = 3.0 V (Unless otherwise specified, T<sub>a</sub> = 25 °C, V<sub>SS</sub> = GND)

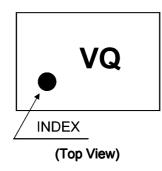
Characteristics	Symbol	Note	Test Condition	Test Circuit	Min	Тур.	Max	Unit
Input offset voltage	V <sub>IO</sub>		—	_	_	±1	±6	mV
Input offset current	I <sub>IO</sub>		—	_	—	1	_	pА
Input bias current	Ц		—	_	_	1	_	pА
Common-mode input voltage range	V <sub>ICM</sub>		—	—	0	_	3.0	V
Supply current	I <sub>DD</sub>	(Note 1)	—	Fig.10.3	_	20	35	μA
Sink current	I <sub>SINK</sub>		V <sub>OL</sub> = 0.5 V	Fig.10.2	9	18	_	mA
Source current	ISOURCE		V <sub>OH</sub> = 2.5 V	Fig.10.1	7	15	_	mA
Low-level output voltage	V <sub>OL</sub>		I <sub>SINK</sub> = 5.0 mA	Fig.10.2	_	0.15	0.30	V
High-level output voltage	V <sub>OH</sub>		I <sub>SOURCE</sub> = 5.0 mA	Fig.10.1	2.70	2.85	_	V
Propagation delay time (L/H)	t <sub>PLH</sub>		Over drive = 100 mV	Fig.10.4	_	400	_	ns
Propagation delay time (H/L)	t <sub>PHL</sub>		Over drive = 100 mV	Fig.10.4	_	800	_	ns
Response time (low-to-high)	t <sub>TLH</sub>		Over drive = 100 mV	Fig.10.4	_	14	_	ns
Response time (high-to-low)	t <sub>THL</sub>		Over drive = 100 mV	Fig.10.4	_	14		ns

### 7.2. $V_{DD}$ = 1.5 V (Unless otherwise specified, T<sub>a</sub> = 25 °C, V<sub>SS</sub> = GND)

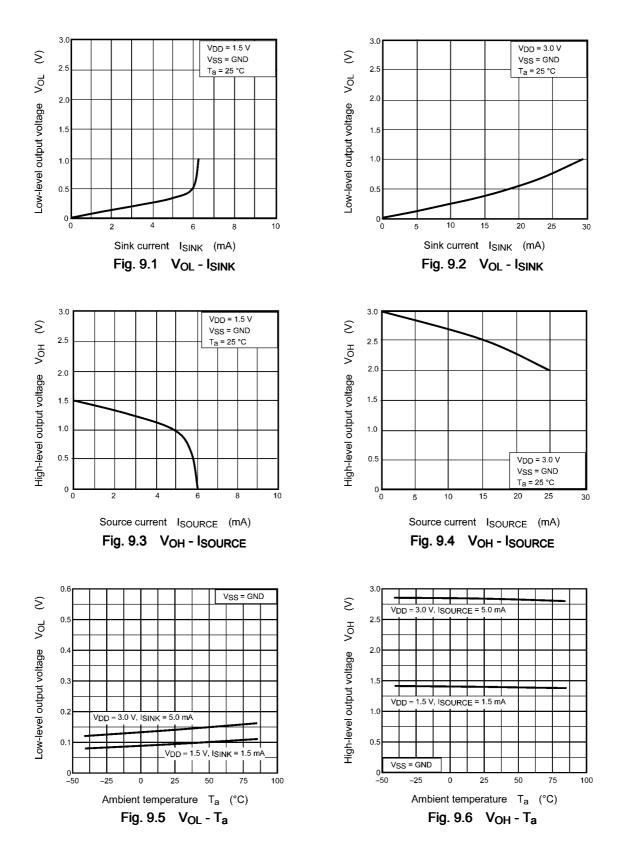
Characteristics	Symbol	Note	Test Condition	Test Circuit	Min	Тур.	Max	Unit
Input offset voltage	V <sub>IO</sub>		—	_	_	±1	±6	mV
Input offset current	I <sub>IO</sub>		—	_	—	1	_	pА
Input bias current	I <sub>I</sub>		_	_	_	1	_	pА
Common-mode input voltage range	V <sub>ICM</sub>		_	_	0	_	1.5	V
Supply current	I <sub>DD</sub>	(Note 1)	_	Fig.10.3	_	18	34	μA
Sink current	I <sub>SINK</sub>		V <sub>OL</sub> = 0.5 V	Fig.10.2	2.5	6.0	_	mA
Source current	ISOURCE		V <sub>OH</sub> = 1.0 V	Fig.10.1	1.5	5.0	_	mA
Low-level output voltage	V <sub>OL</sub>		I <sub>SINK</sub> = 1.5 mA	Fig.10.2	_	0.10	0.25	V
High-level output voltage	V <sub>OH</sub>		I <sub>SOURCE</sub> = 1.5 mA	Fig.10.1	1.25	1.40	_	V
Propagation delay time (L/H)	t <sub>PLH</sub>		Over drive = 100 mV	Fig.10.4	_	400	_	ns
Propagation delay time (H/L)	t <sub>PHL</sub>		Over drive = 100 mV	Fig.10.4	_	720	_	ns
Response time (low-to-high)	t <sub>TLH</sub>		Over drive = 100 mV	Fig.10.4	_	20	_	ns
Response time (high-to-low)	t <sub>THL</sub>		Over drive = 100 mV	Fig.10.4	_	33	_	ns

Note 1: The current consumption of the device increases with its operating frequency. Ensure that its power dissipation does not exceed the rated allowable power dissipation.

#### 8. Marking



#### 9. Characteristics Curves (Note)



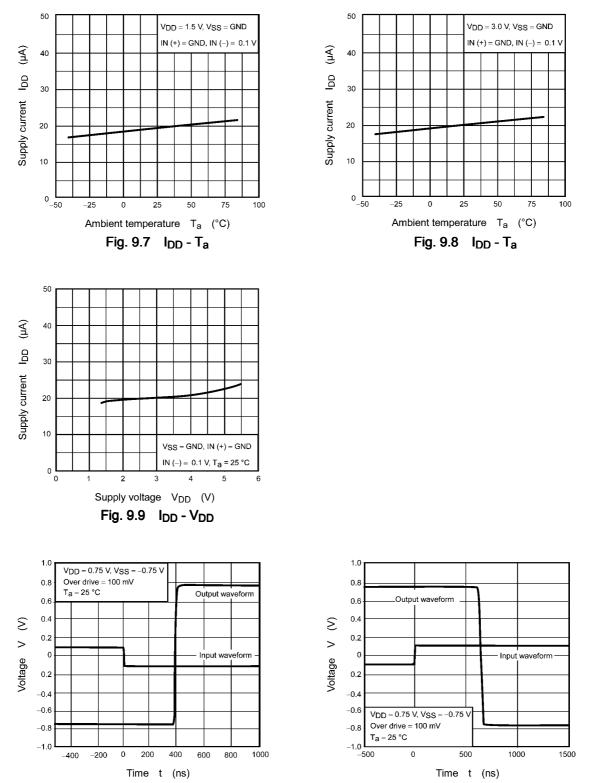
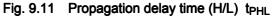
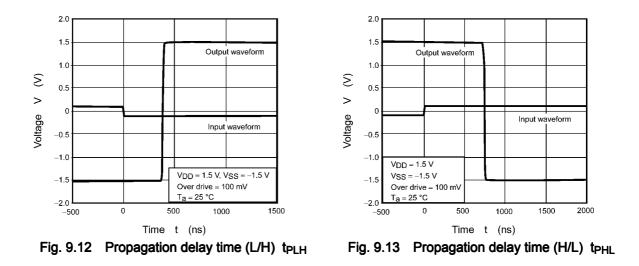


Fig. 9.10 Propagation delay time (L/H) t<sub>PLH</sub>





Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

10. Test Circuits

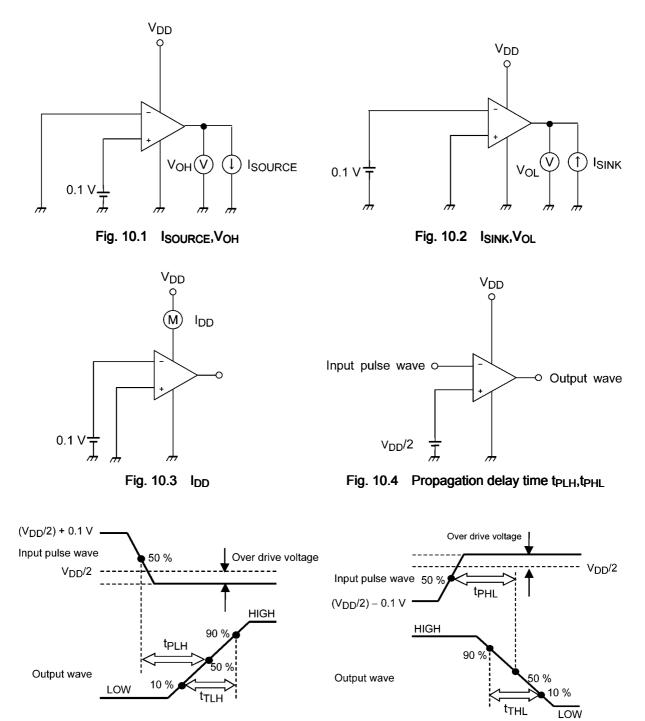
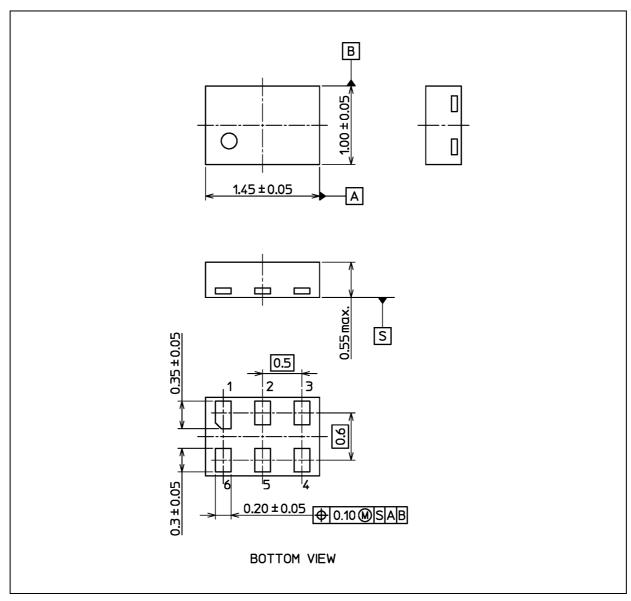


Fig. 10.5 Propagation delay time (L/H) tPLH wave Fig. 10.6 Propagation delay time (H/L) tPHL wave

#### **Package Dimensions**

TC75S70L6X

Unit: mm



Weight: 0.0024 g (typ.)

Package Name(s)						
TOSHIBA: P-UFLGA6-0102-0.50-003						
Nickname: MP6C						

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