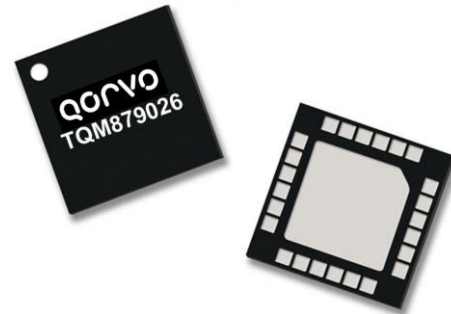


Product Overview

The TQM879026 is a digital variable gain amplifier (DVGA) featuring high linearity and digital variable gain control in 0.5 dB step sizes. This DVGA integrates a gain block, a digital-step attenuator (DSA), and a high linearity ¼-watt amplifier into a compact 4x4 mm package. The internal 6-bit DSA provides a 31.5 dB gain control range and is controlled with a serial peripheral interface (SPI™). The individual stages are accessible to external ports to allow for optimization of the last stage amplifier for use in any 3GPP telecom band and also allowing other functional blocks to be added in-between the stages.

The TQM879026 features variable gain from 1 dB to 32 dB at 2.14 GHz, +42.5 dBm output IP3, and +24 dBm P1dB while only consuming 174 mA current from a 5V supply. The module is available in a compact 24-pin 4x4 mm leadless SMT package.

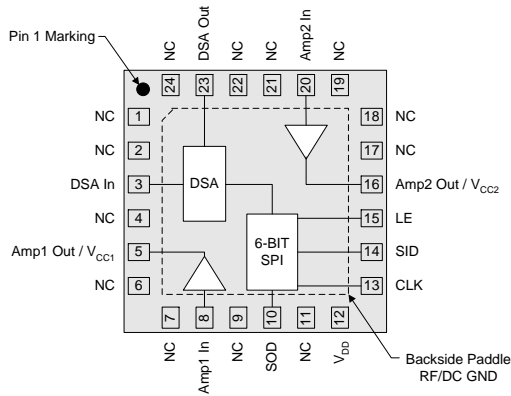


24 Pin 4x4 mm leadless SMT Package

Key Features

- 450-4000 MHz
- 32 dB Maximum Gain at 2140 MHz
- 31.5 dB Gain Range in 0.5 dB Steps
- +42.5 dBm Output IP3
- +24 dBm Output P1dB
- 1.6 dB Noise Figure
- 3-wire SPI™ Control DSA
- Tunable for any 3GPP telecom band

Functional Block Diagram



Top View

Applications

- Wireless Infrastructure
- Small cell BTS
- Pre-5G / 5G Massive MIMO systems
- TDD-based architectures

Ordering Information

Part No.	Description
TQM879026TR13	2500 pieces on a 13" reel
TQM879026-PCB900	900 MHz Evaluation Board
TQM879026-PCB2140	2140 MHz Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to 150°C
RF Input Power, CW, 50Ω, T=25°C	+12 dBm
Supply Voltage (V _{DD})	+5.5 V
Digital Input Voltage	V _{DD} + 0.5 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V _{DD})	4.75	5.0	5.25	V
T _{CASE}	-40		+85	°C
T _j for >10 ⁶ hours MTTF			+170	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD} = +5V, Temp = +25°C, matched 2140 MHz reference circuit, max. gain setting

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		450		4000	MHz
Test Frequency			2140		MHz
Gain		29	32	35	dB
Gain Control Range	0.5 dB Step Size		31.5		dB
Accuracy Error		±(0.3+5% of Attenuation setting)			dB
Input Return Loss			17		dB
Output Return Loss			13		dB
Output P1dB		+23	+24		dBm
Output IP3	P _{out} = +11 dBm/tone, Δf = 1 MHz	+38	+42.5		dBm
Noise Figure			1.5		dB
Total Supply Current		140	174	211	mA
Amp 1 Current			85		mA
Amp 2 Current			87		mA
DSA Current			2		mA
Thermal Resistance, θ _{jc}	Junction to case			36.7	°C/W

Serial Control Interface

The TQM879026 has a CMOS SPI™ input compatible serial interface. This serial control interface converts the serial data input stream to parallel output word. The input is 3-wire (CLK, LE and SID) SPI™ input compatible. At power up, the serial control interface resets the DSA to the minimum gain state. The 6-bit SID (Serial Input Data) word is loaded into the register on rising edge of the CLK, MSB first. When LE is high, CLK is internally disabled.

Serial Control Timing Characteristics (Test conditions: $V_{DD} = +5\text{ V}$, $\text{Temp.} = 25^\circ\text{C}$)

Parameter	Condition	Min	Max	Units
Clock Frequency	50% Duty Cycle		10	MHz
LE Setup Time, t_{LESUP}	after last CLK rising edge	10		ns
LE Pulse Width, t_{LEPW}		30		ns
SID set-up time, t_{SDSUP}	before CLK rising edge	10		ns
SID hold-time, t_{SDHLD}	after CLK rising edge	10		ns
LE Pulse Spacing t_{LE}	LE to LE pulse spacing	630		ns
Propagation Delay t_{PLO}	LE to Parallel output valid		30	ns

Serial Control DC Logic Characteristics (Test conditions: $V_{DD} = +5\text{ V}$, $\text{Temp.} = 25^\circ\text{C}$)

Parameter	Condition	Min	Max	Units
Input Low State Voltage, V_{IL}		0	0.8	V
Input High State Voltage, V_{IH}		2.4	V_{DD}	V
Output High State Voltage, V_{OH}	On SOD pin	2.0	V_{DD}	V
Output Low State Voltage, V_{OL}	On SOD pin	0	0.8	V
Input Current, I_{IH} / I_{IL}	On SID, LE and CLK pins	-10	+10	μA

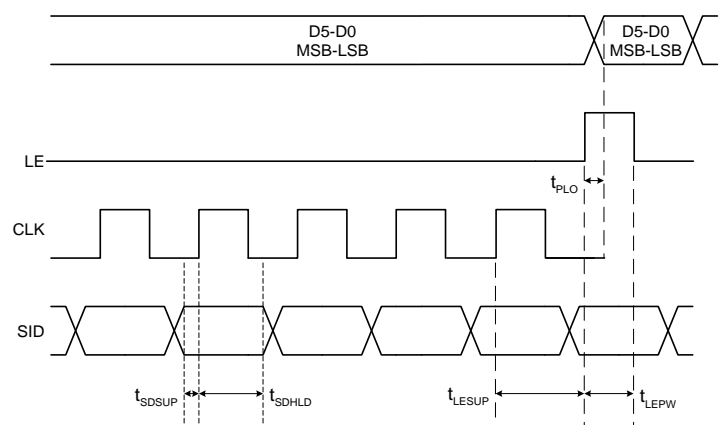
SID Control Logic Truth Table

6-Bit Control Word						Gain Relative to Maximum Gain
MSB			LSB			
D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	Maximum Gain
1	1	1	1	1	0	-0.5 dB
1	1	1	1	0	1	-1 dB
1	1	1	0	1	1	-2 dB
1	1	0	1	1	1	-4 dB
1	0	1	1	1	1	-8 dB
0	1	1	1	1	1	-16 dB
0	0	0	0	0	0	-31.5 dB

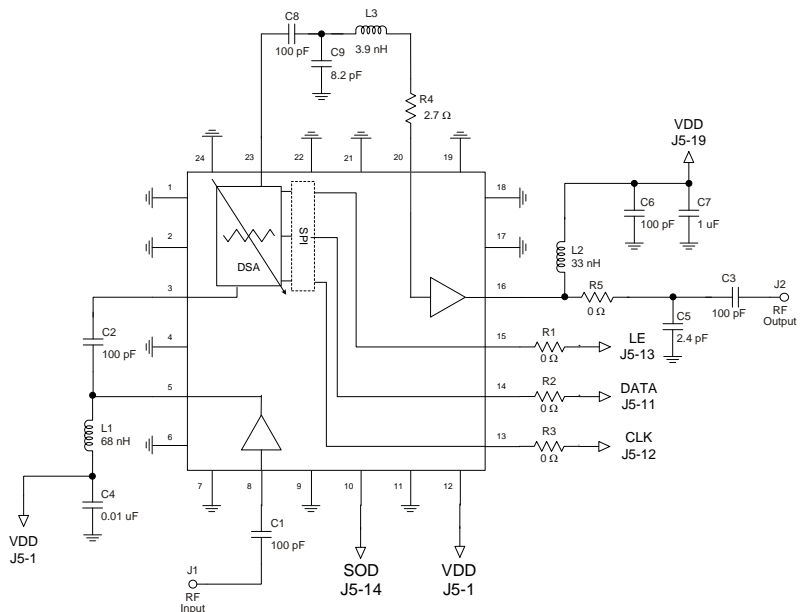
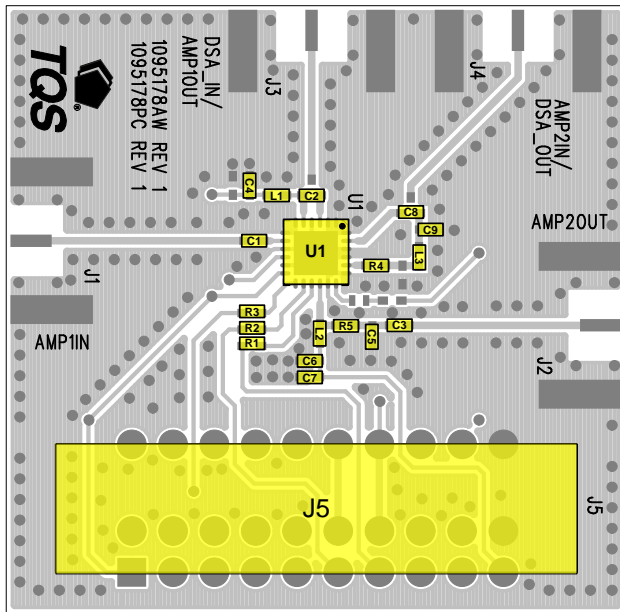
Any combination of the possible 64 states will provide a reduction in gain of approximately the sum of the bits selected.

Timing Diagram

CLK is internally disabled when LE is high



TQM879026 617 – 652 MHz Reference Design



Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. All components are of 0402 size.
3. The left edge of C8 is placed 88 mil from the device package.

Bill of Material 617 – 652 MHz Reference Design

Reference Des.	Value	Description	Manuf.	Part Number
U1	n/a	¼ W DVGA	Qorvo	TQM879026
C1, C2, C3, C6, C8	100 pF	CAP, 0402, 5%. 50V. NPO/COG	various	
C4	0.01 µF	CAP, 0402, 10%, 16V, X7R	various	
C5	2.4 pF	CAP, 0402, +/- 0.1PF. 25V. NPO/COG	various	
C7	1 µF	CAP, 0402, 10%, 10V, X5R	various	
C9	8.2 pF	CAP, 0402, +/- 0.1PF. 25V. NPO/COG	various	
L1	68 nH	IND, 0402, 5%, ceramic core	Coilcraft	0402CS-68NXJL
L2	33 nH	IND, 0402, 5%, ceramic core	Coilcraft	0402CS-33NXJL
L3	3.9 nH	IND, 0402, CHIP	Toko	LL1005-FHL3N9S
R4	2.7 Ω	RES, 0402, +/- 1%, 1/10W	various	
R1, R2, R3, R5	0 Ω	RES, 0402, CHIP	various	

Typical Performance 617–652 MHz Reference Design

Test conditions unless otherwise noted: $V_{DD} = +5V$, Temp = $+25^{\circ}C$, DSA at max. gain setting

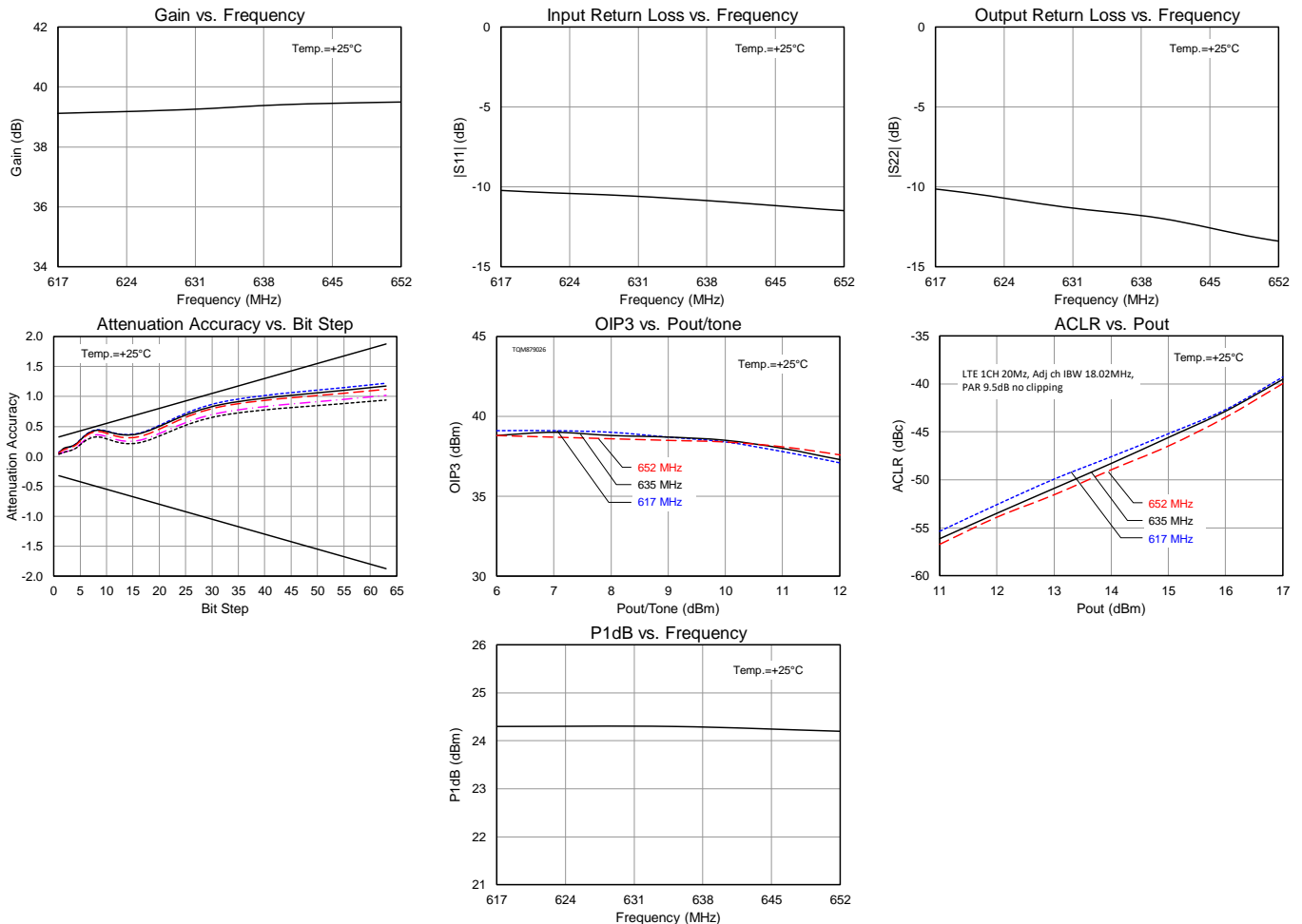
Parameter	Conditions	Typical Values			Units
Frequency		617	635	652	MHz
Gain		39.1	39.4	39.5	dB
Input Return Loss		10	11	12	dB
Output Return Loss		10	12	13	dB
Output P1dB		+24.3	+24.3	+23.2	dBm
Output IP3	Pout = +8 dBm/tone, $\Delta f = 1$ MHz	+39.0	+38.8	+38.6	dBm
LTE Chan. Power ⁽¹⁾	-50 dBc ACLR	+13.0	+13.3	+13.6	dBm

Notes:

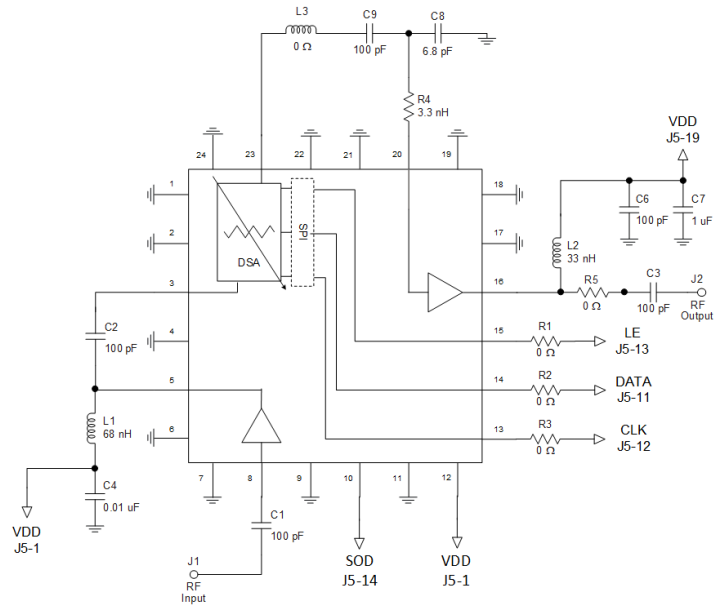
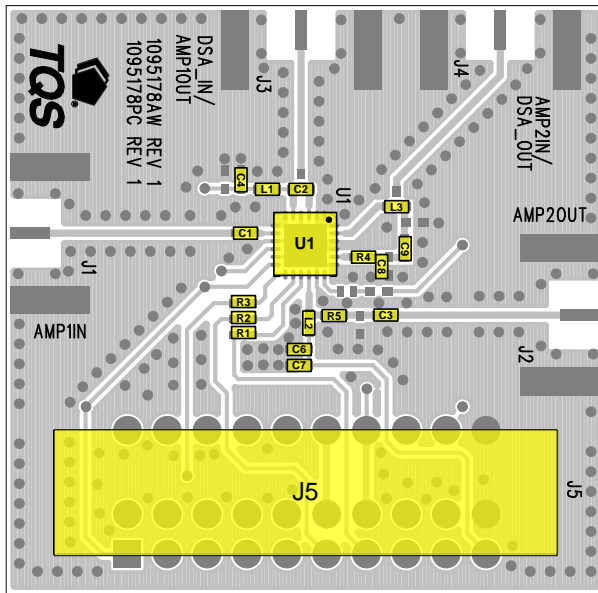
1. ACLR test set-up: 1 CH, 20 MHz BW, LTE E-TM1.1, 9.5 dB PAR at 0.01% Probability

Performance Plots 617–652 MHz Reference Design

Test conditions unless otherwise noted: $V_{DD} = +5V$, Temp = $+25^{\circ}C$, DSA at max. gain setting



TQM879026-PCB900 Evaluation Board (869–960 MHz)



Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. All components are of 0402 size.
3. The left edge of C8 is placed 88 mil from the device package.

Bill of Material TQM879026-PCB900

Reference Des.	Value	Description	Manuf.	Part Number
U1	n/a	¼ W DVGA	Qorvo	TQM879026
C1, C2, C3, C6, C9	100 pF	CAP, 0402, 5%, 50V. NPO/COG	various	
C4	0.01 µF	CAP, 0402, 10%, 16V, X7R	various	
C7	1 µF	CAP, 0402, 10%, 10V, X5R	various	
C8	6.8 pF	CAP, 0402, +/- 0.1PF. 25V. NPO/COG	various	
L1	68 nH	IND, 0402, 5%, ceramic core	Coilcraft	0402CS-68NXJL
L2	33 nH	IND, 0402, 5%, ceramic core	Coilcraft	0402CS-33NXJL
R4	3.3 nH	IND, 0402, CHIP	Toko	LL1005-FHL3N3S
R1, R2, R3, R5, L3	0 Ω	RES, 0402, CHIP	various	

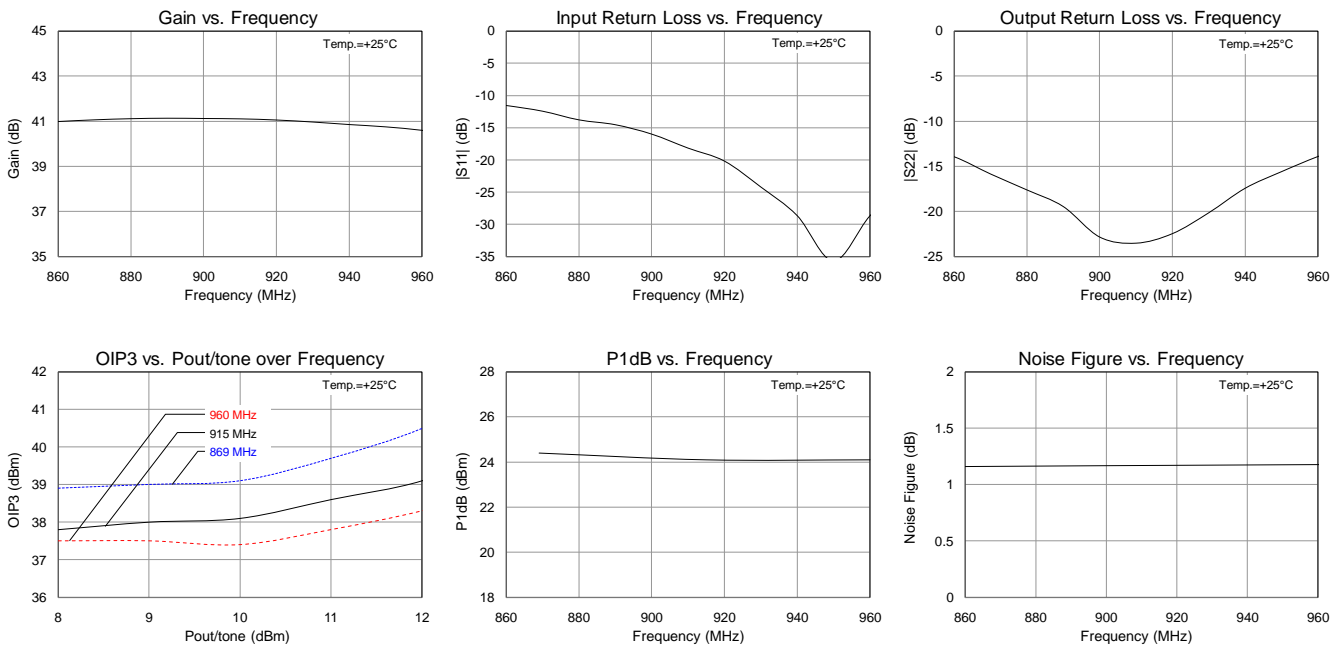
Typical Performance TQM879026-PCB900

Test conditions unless otherwise noted: $V_{DD} = +5V$, Temp = $+25^{\circ}C$, DSA at max. gain setting

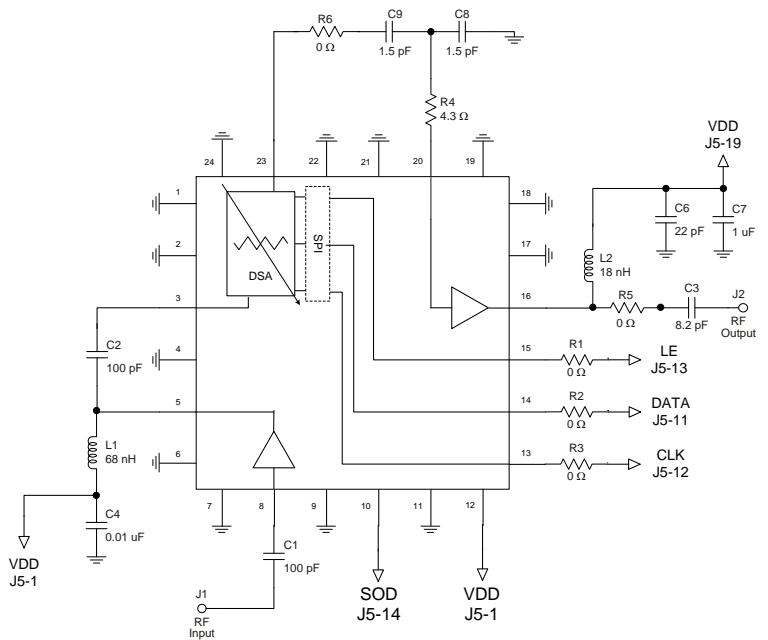
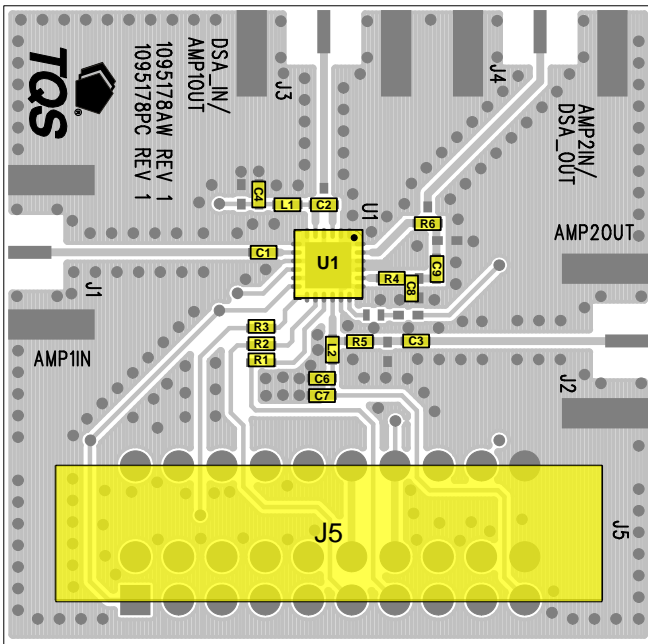
Parameter	Conditions	Typical Values			Units
Frequency		869	915	960	MHz
Gain		41.0	41.0	40.5	dB
Input Return Loss		11.5	17	28	dB
Output Return Loss		14	22	14	dB
Output P1dB		24.4	24.1	24.1	dBm
Output IP3	Pout = +11 dBm/tone, $\Delta f = 1$ MHz	39.5	38.5	37.7	dBm
Noise figure		1.2	1.2	1.2	dB

Performance Plots TQM879026-PCB900

Test conditions unless otherwise noted: $V_{DD} = +5V$, Temp = $+25^{\circ}C$, DSA at max. gain setting



Evaluation Board 1805 – 1880 MHz Reference Design



Notes:

1. See Evaluation Board PCB Information section for PCB material and stack-up.
2. Components are 0402 unless specified otherwise
3. 0 Ohm resistors may be replaced with 50 Ohm traces in the target application layout.

Bill of Material 1805 – 1880 MHz Reference Design

Reference Des.	Value	Description	Manuf.	Part Number
U1	n/a	TQM879026 Sample	Qorvo	TQM879026
C1, C2	100 pF	CAP, 0402, 5%. 50V. NPO/COG	various	
C3	8.2 pF	CAP, 0402, +/-0.25PF. 50V. NPO/COG	various	
C6	22 pF	CAP, 0402, 5%. 50V. NPO/COG	various	
C4	0.01 μF	CAP, 0402, 10%, 16V, X7R	various	
C7	1 μF	CAP, 0402, 10%, 10V, X5R	various	
C8, C9	1.5 pF	CAP, 0402, +/- 0.1PF. 25V. NPO/COG	various	
L1	68 nH	IND, 5PCT. 1.6 GHz	Coilcraft	0402CS-68NXJL
L2	18 nH	IND, 0402, 5%, ceramic core.	Coilcraft	0402CS-18NXJL
R4	4.3 Ω	RES, 0402, 5%, 1/10W, CHIP	various	
R1, R2, R3, R5, R6	0 Ω	RES, 0402, CHIP	various	

Typical Performance 1805 – 1880 MHz Reference Design

Test conditions unless otherwise noted: $V_{DD} = +5V$, $Temp = +25^{\circ}C$, DSA at max. gain setting

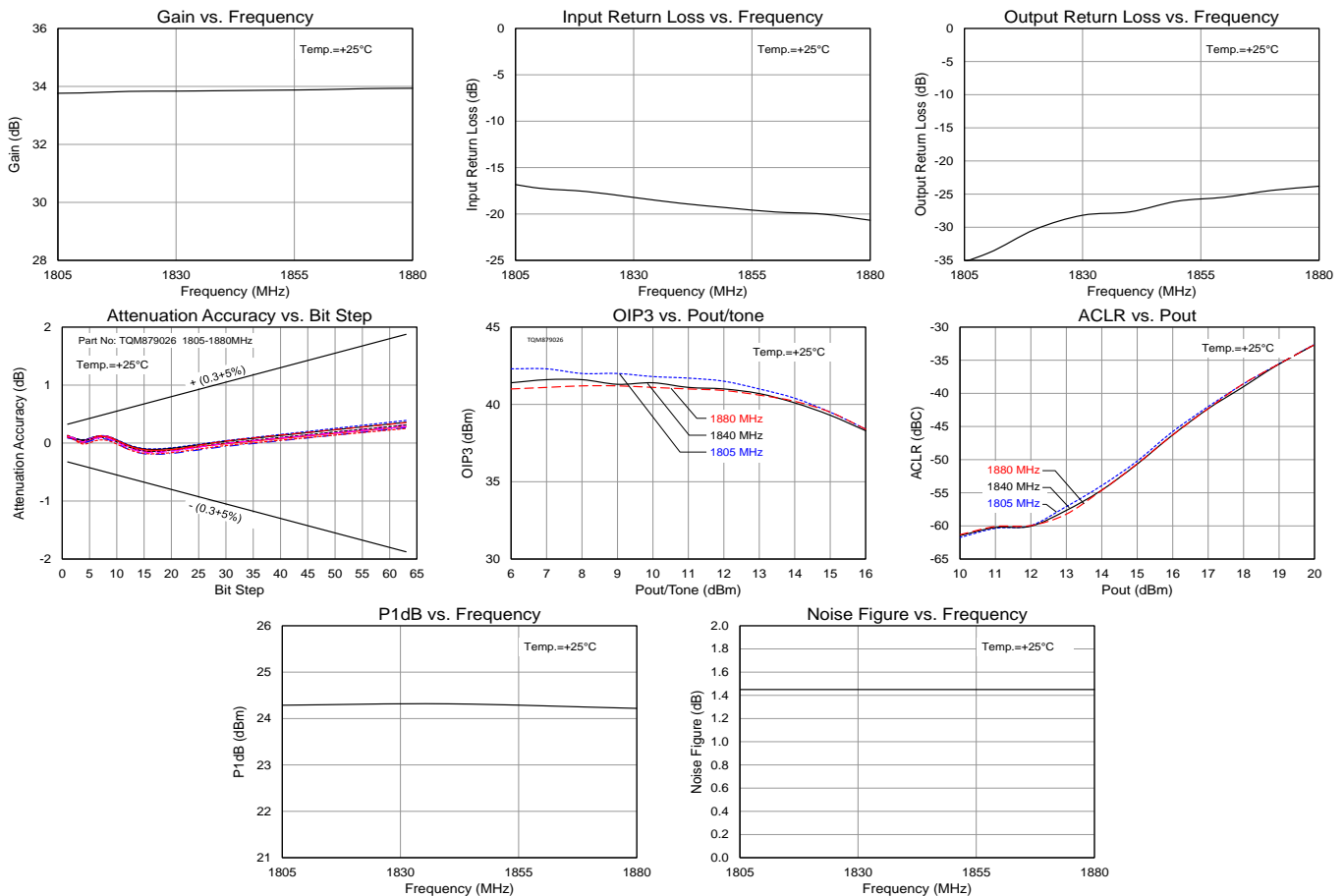
Parameter	Conditions	Typical Values			Units
Frequency		1805	1840	1880	MHz
Gain		33.8	33.9	33.9	dB
Input Return Loss		-16	-18	-20	dB
Output Return Loss		-20	-20	-20	dB
Output P1dB		+24.3	+24.3	+23.2	dBm
Output IP3	Pout= +8 dBm/tone, $\Delta f=1$ MHz	+42.0	+41.6	+41.2	dBm
WCDMA Channel Power ⁽¹⁾	At -50 dBC ACLR	+15.1	+15.2	+15.2	dBm
Noise Figure		1.5	1.5	1.5	dB

Notes:

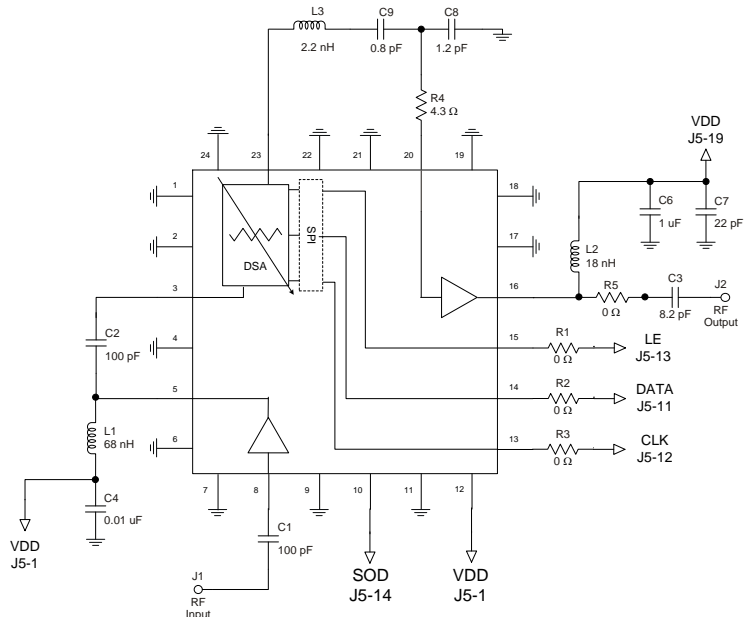
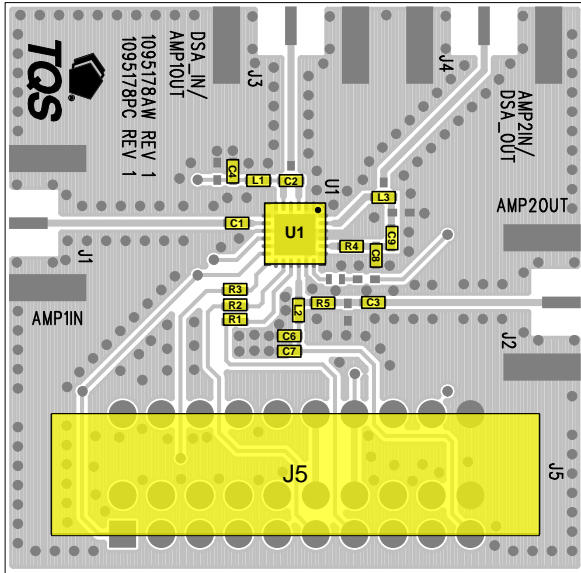
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob

Performance Plots 1805 – 1880 MHz Reference Design

Test conditions unless otherwise noted: $V_{DD} = +5V$, $Temp = +25^{\circ}C$, DSA at max. gain setting



TQM879026-PCB2140 Evaluation Board (2110–2170 MHz)



Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. All components are of 0402 size.

Bill of Material TQM879026-PCB2140

Reference Des.	Value	Description	Manuf.	Part Number
U1	n/a	¼ W DVGA	Qorvo	TQM879026
C1, C2	100 pF	Cap 0402 5% 50V NPO/COG	various	
C3	8.2 pF	Cap 0402 ±0.1 pF 50V NPO/COG	AVX	04025U8R2BAT2A
C4	0.01 µF	Cap 0402 ±10% 16V X7R	various	
C6	1 µF	Cap 0402 ±10% 10V X5R	various	
C7	22 pF	Cap 0402 5% 50V NPO/COG	various	
C8	1.2 pF	Cap 0402 ±0.1 pF 25V NPO/COG	AVX	04023U1R2CAT2A
C9	0.8 pF	Cap 0402 ±0.075 pF 25V NPO/COG	AVX	04025U0R8BAT2A
L1	68 nH	Ind 0402	various	
L2	18 nH	Ind 0402	various	
L3	2.2 nH	Ind 0402	various	
R1, R2, R3, R5	0 Ω	Res 0402	various	
R4	4.3 Ω	Res 0402	various	

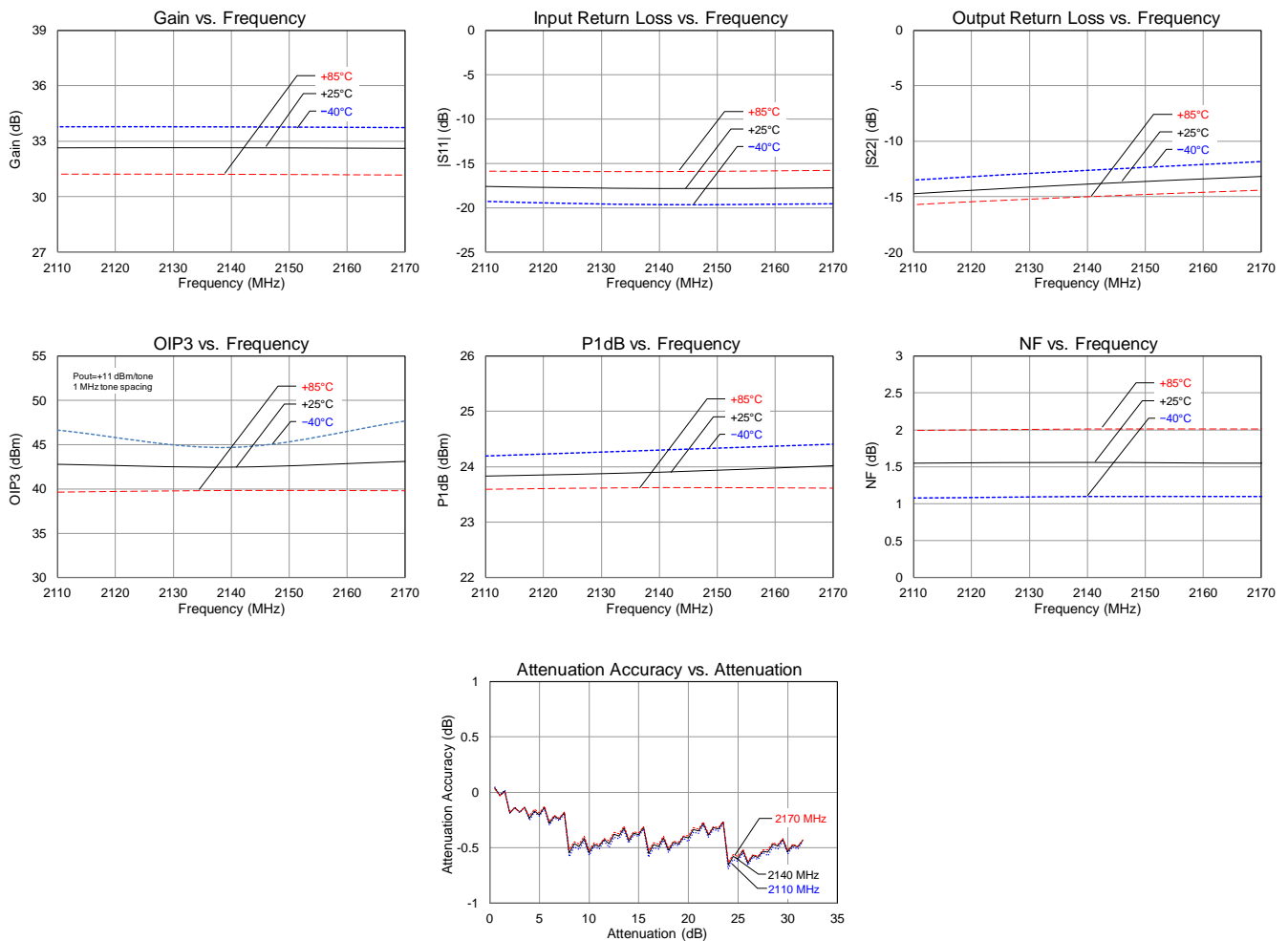
Typical Performance TQM879026-PCB2140

Test conditions unless otherwise noted: $V_{DD} = +5V$, Temp = $+25^{\circ}C$, DSA at max. gain setting

Parameter	Conditions	Typical Values			Units
Frequency		2110	2140	2170	MHz
Gain		32.6	32.6	32.6	dB
Input Return Loss		18	18	18	dB
Output Return Loss		15	14	13	dB
Output P1dB		23.8	23.9	24.0	dBm
OIP3	Pout = +11 dBm/tone, $\Delta f = 1$ MHz	42.8	42.5	43	dBm
Noise figure		1.6	1.6	1.6	dB

Performance Plots TQM879026-PCB2140

Test conditions unless otherwise noted: $V_{DD} = +5V$, Temp = $+25^{\circ}C$, DSA at max. gain setting



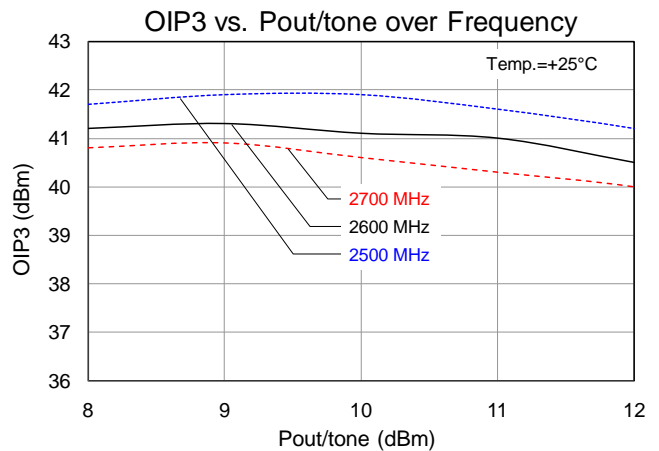
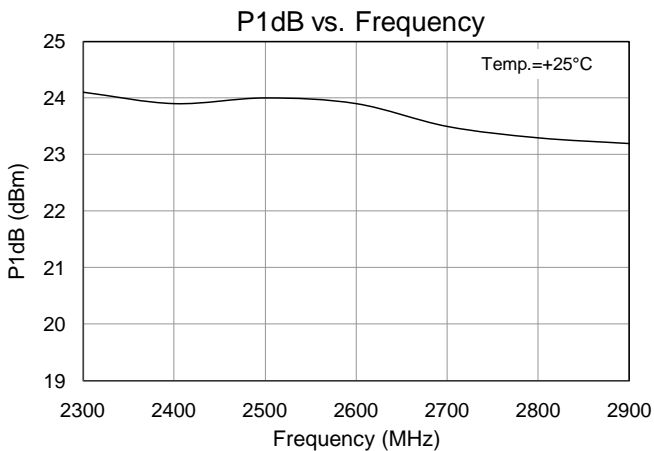
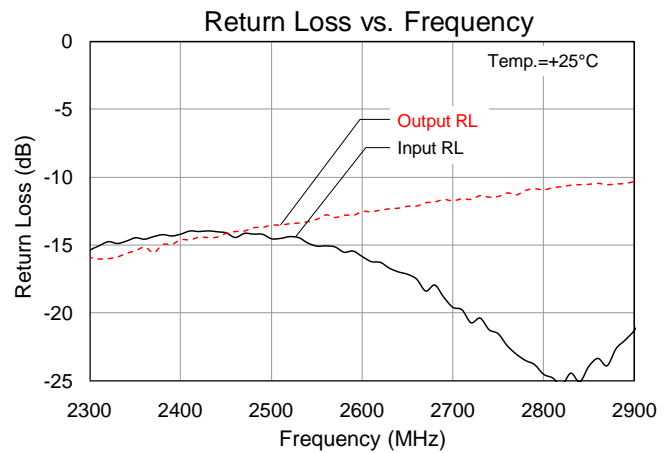
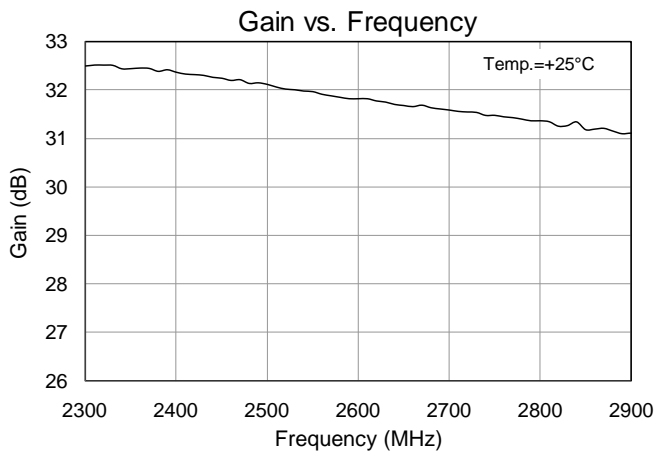
Typical Performance 2300 – 2700 MHz Reference Design

Test conditions unless otherwise noted: $V_{DD} = +5V$, Temp = +25°C, DSA at max. gain setting

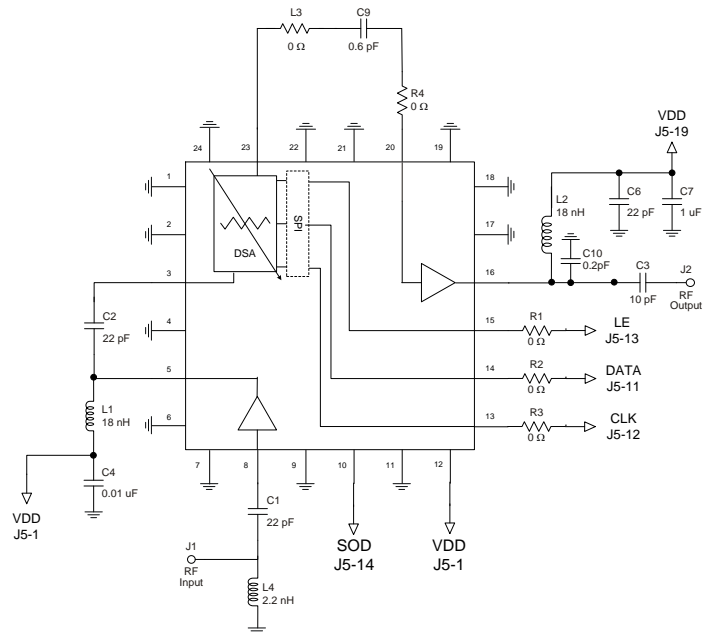
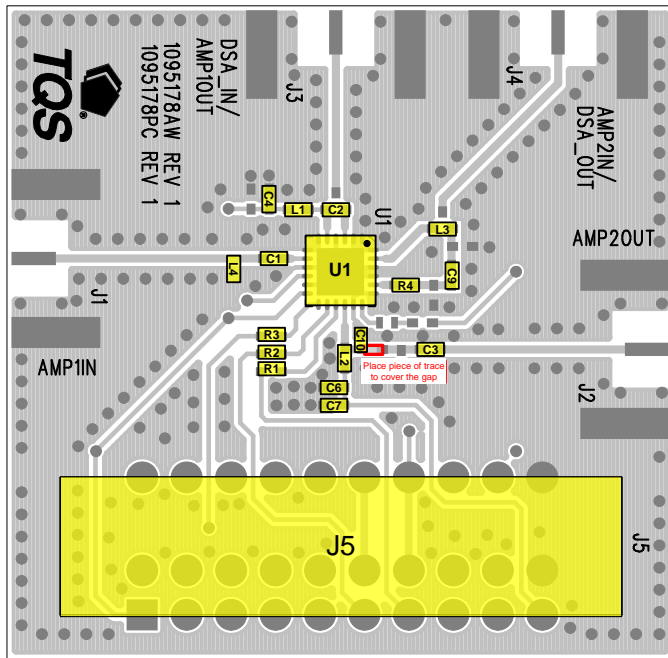
Parameter	Conditions	Typical Values					Units
Frequency		2300	2500	2600	2700	2900	MHz
Gain		32.5	32.0	31.8	31.6	31.1	dB
Input Return Loss		15	14	16	19	20	dB
Output Return Loss		16	13	12	11	10	dB
Output P1dB		+24.0	+24.0	+23.9	+23.5	+23.2	dBm
Output IP3	Pout = +11 dBm/tone, $\Delta f = 1$ MHz	+41.5	+41.5	+41.0	+40.5	+40.2	dBm

Performance Plots 2300 – 2700 MHz Reference Design

Test conditions unless otherwise noted: $V_{DD} = +5 V$, Temp = +25 °C, DSA at max. gain setting



TQM879026 3400 – 3600 MHz Reference Design



Notes:

1. See Evaluation Board PCB Information section for PCB material and stack-up.
2. Components are 0402 unless specified otherwise
3. 0 Ohm resistors may be replaced with 50 Ohm traces in the target application layout.
4. Critical component placement:
 - a. Distance between U1 to L4 (left edge): 183 mils
 - b. Distance between L2 to C10 (edge to edge): 10 mils

Bill of Material 3400 – 3600 MHz Reference Design

Reference Des.	Value	Description	Manuf.	Part Number
N/A	N/A	Printed Circuit Board	Qorvo	1095178
U1	N/A	Variable Gain Amplifier	Qorvo	TQM879026
C1, C2, C6	22 pF	CAP, 0402, 5%, 50V. NPO/COG	various	
C3	10 pF	CAP, 0402, +/- 0.5PF. 50V. NPO/COG	various	
C4	0.01 uF	CAP, 0402, 10%, 16V, X7R	various	
C7	1 uF	CAP, 0402, 10%, 10V, X5R	various	
R5		Use Copper/Metal strip to connect gap	various	
C9	0.6 pF	CAP, 0402, +/- 0.05PF. 25V. ACCU-P	AVX	04023J0R2BBSTR
C10	0.2pF	CAP, 0402, +/- 0.05PF. 25V. ACCU-P	AVX	04023J0R2ABSTR
L1, L2	18 nH	IND, 0402, 5%, ceramic core.	Coilcraft	0402CS-18NXJL
L4	2.2nH	IND, 0402 Multilayer Chip	Toko	LL1005-FHL2N2S
R1, R2, R3, R4, L3	0 Ohm	RES, 0402, CHIP	various	

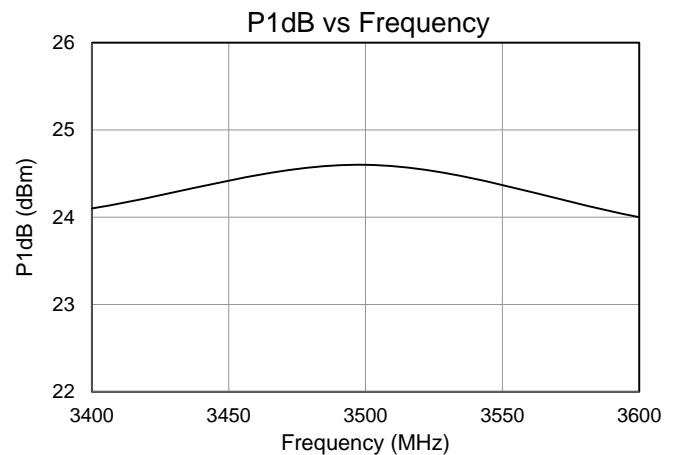
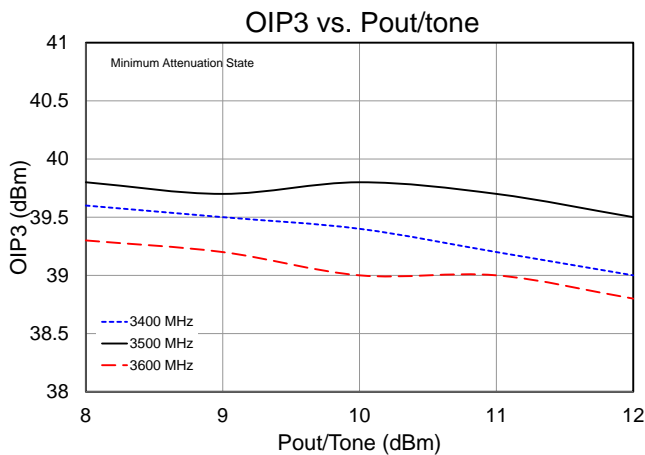
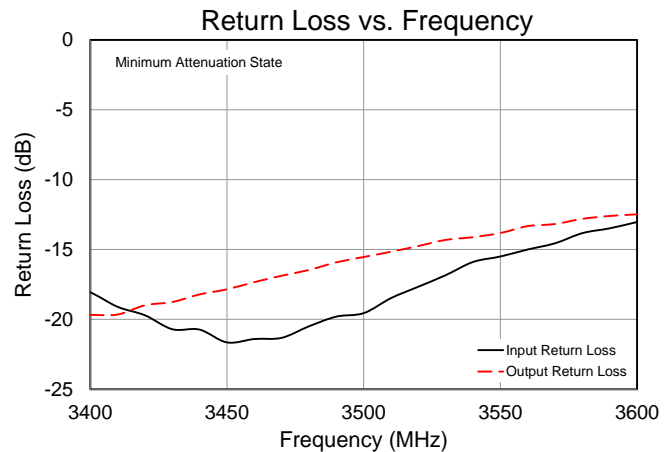
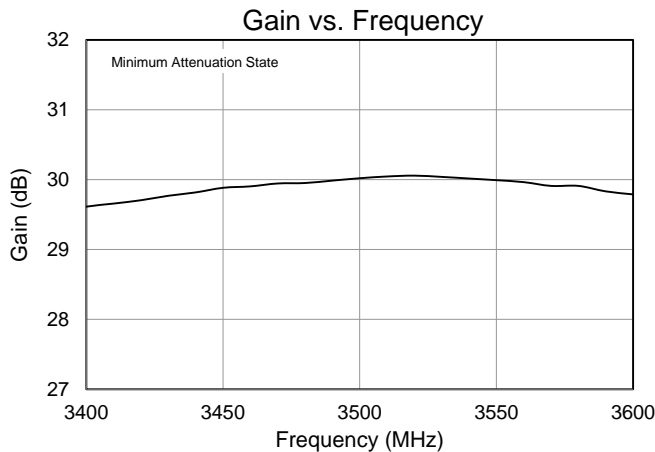
Typical Performance 3400 – 3600 MHz Reference Design

Test conditions unless otherwise noted: $V_{DD} = +5V$, $Temp = +25^{\circ}C$, DSA at max. gain setting

Parameter	Conditions	Typical Values			Units
Frequency		3400	3500	3600	MHz
Gain		29.6	30	29.8	dB
Input Return Loss		18	19	13	dB
Output Return Loss		19	15.5	12.5	dB
Output P1dB		+24.1	+24.6	+24	dBm
Output IP3	Pout= +11 dBm/tone, $\Delta f = 1$ MHz	+39.2	+39.7	+39	dBm

Performance Plots 3400 – 3600 MHz Reference Design

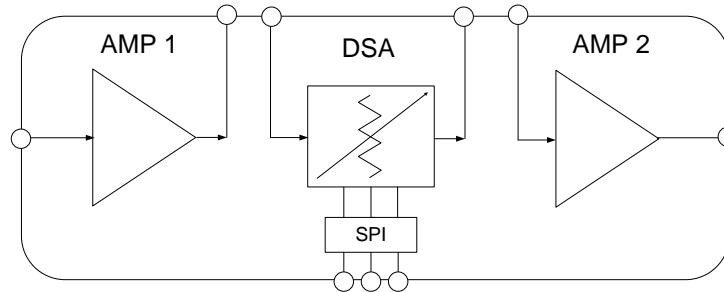
Test conditions unless otherwise noted: $V_{DD} = +5V$, $Temp = +25^{\circ}C$, DSA at max. gain setting



Detailed Device Description

The TQM879026 is a digital variable gain amplifier (DVGA) featuring high linearity over the entire gain control range. The amplifier module features the integration of a 50 Ω internally matched high linearity low noise amplifier gain block, a digital step attenuator (DSA), along with a high linearity ¼W amplifier as shown in the functional diagram below. The DVGA has an operational frequency range from 0.45 – 4.0 GHz. The three stages are individually accessible via package I/O contacts. This permits full flexibility to insert other components or filters between the stages.

Functional Schematic Diagram



AMP1

AMP1 is a high linearity low noise amplifier. The amplifier has high gain across a broad range of frequencies while also providing very low noise. It is internally matched and only requires an external RF choke and blocking/bypass capacitors for operation from a single +5V supply. The internal active bias circuit also enables stable operation over bias and temperature variations. At 1.9 GHz, the amplifier typically provides 19.8 dB gain, +36 dBm OIP3, and 1.3 dB Noise Figure while only drawing 85 mA of current.

DSA (Digital Step Attenuator)

The DSA is a high linearity, low insertion loss, 6-bit, 31.5 dB Digital Step Attenuator (DSA) operating over the 450 - 4000 MHz frequency range. The digital step attenuator uses a single positive 5V supply and has a serial periphery interface (SPI™) for changing attenuation states. This product maintains high attenuation accuracy over frequency and temperature. No external matching components are needed for the DSA.

AMP2

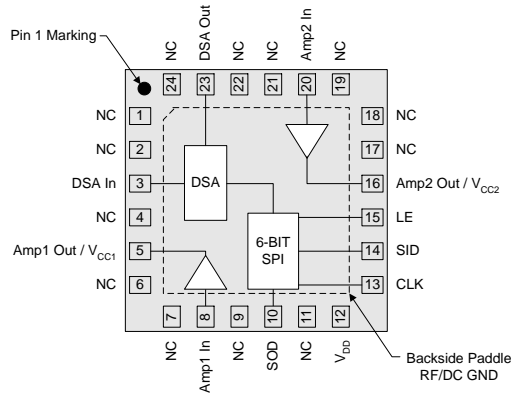
AMP2 is a high-linearity driver amplifier that delivers high performance past 4GHz. With external tuning it can achieve over +40 dBm OIP3 with +25 dBm P1dB while only consuming 87 mA of quiescent current.

Chain Analysis Table

This table provides the typical performance of individual stages in the module as well as overall module performance. Frequency = 2140 MHz.

Parameter	AMP1	DSA	AMP2	Overall Module	Units
Gain	19.8	-1.6	14.4	32.6	dB
NF	1.5	1.6	3.9	1.6	dB
OIP3	36	55	42.5	42.5	dBm
P1dB	20	30	23.9	23.9	dBm
Icc	85	2	87	174	mA

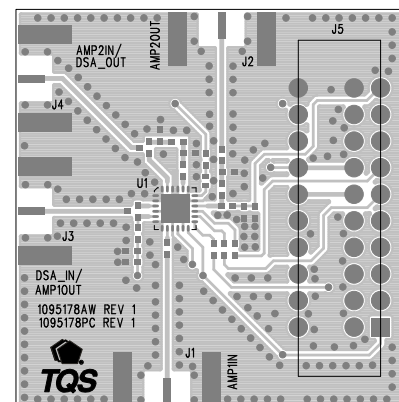
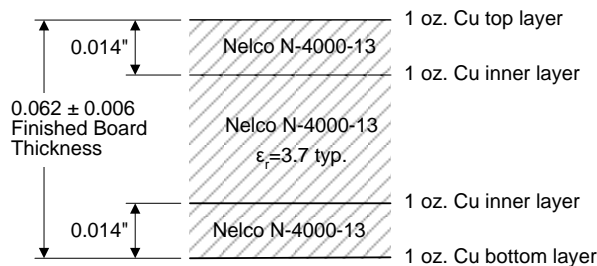
Pin Configuration and Description



Pin No.	Label	Description
1, 2, 4, 6, 7, 9, 11, 17, 18, 19, 21, 22, 24	NC	No electrical connection. Land pads should be provided for PCB mounting integrity.
3	DSA In	DSA Input
5	Amp1 Out / V _{CC1}	RF output / DC supply (Amp1).
8	Amp1 In	RF input (Amp1). Band-specific matching circuit required.
10	SOD	Reserved Serial Output Data. No application recommended.
12	V _{DD}	DC Supply
13	CLK	Serial Clock
14	SID	Serial Input Data
15	LE	Latch Enable
16	Amp2 Out / V _{CC2}	RF output / DC supply (Amp2). Band-specific matching circuit required.
20	Amp2 In	RF input (Amp2). Band-specific matching circuit required.
23	DSA Out	DSA Output
Backside Paddle	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern.

Evaluation Board PCB Information

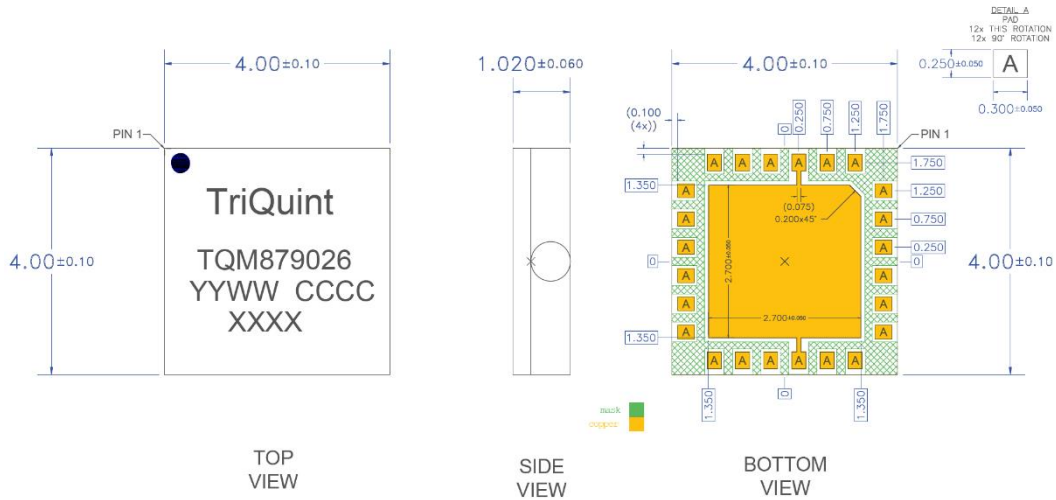
Qorvo PCB 1095178 Material and Stack-up



Mechanical Information

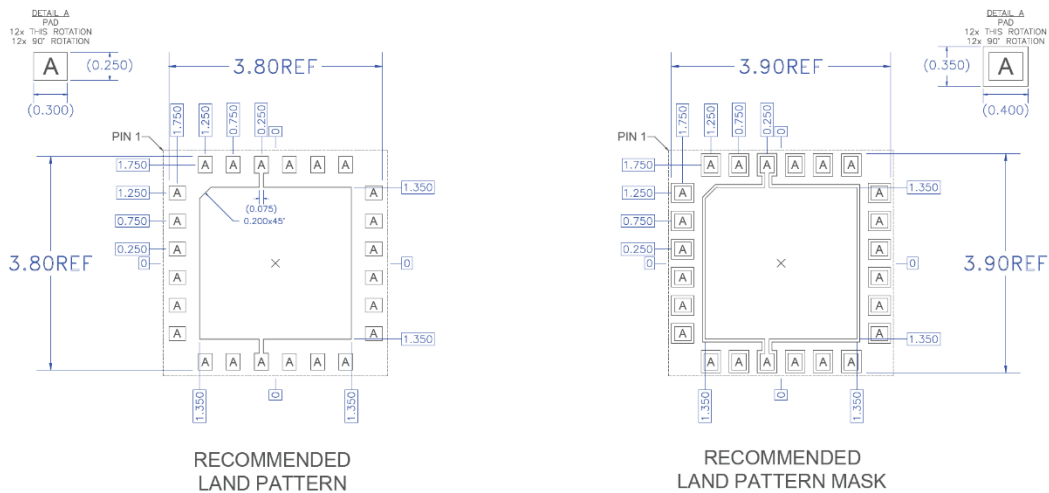
Package Marking and Dimensions

Marking: Part number – TQM879026
 Year/Work Week/Country Code - YYWW CCCC
 XXXX – Trace Code



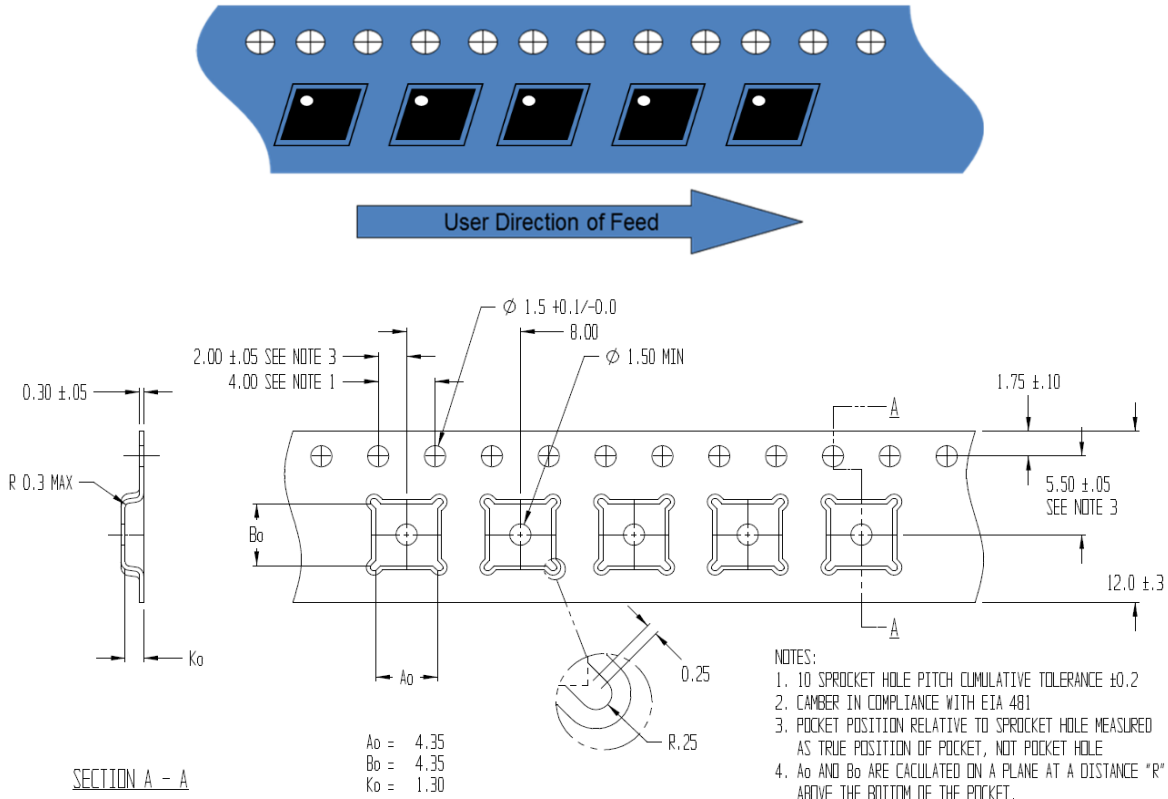
- Notes:
1. All dimensions are in millimeters. Angles are in degrees.
 2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
 3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



- Notes:
1. All dimensions are in millimeters. Angles are in degrees.
 2. Use 1 oz. copper minimum for top and bottom layer metal.
 3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation.
 4. Do not remove or minimize via hole structure in the PCB. Thermal and RF grounding is critical.
 5. We recommend a 0.35 mm ($\#80/0.0135$) dia. bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.01 ”).
 6. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.
 7. There is no effect to the RF performance if Pads 9 and 22 are removed from the land pattern.

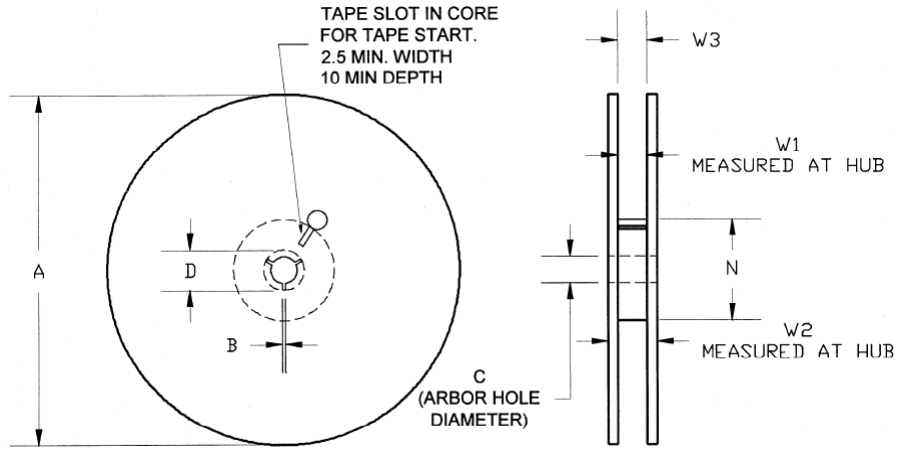
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.171	4.35
	Width	B0	0.171	4.35
	Depth	K0	0.051	1.30
	Pitch	P1	0.315	8.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.0

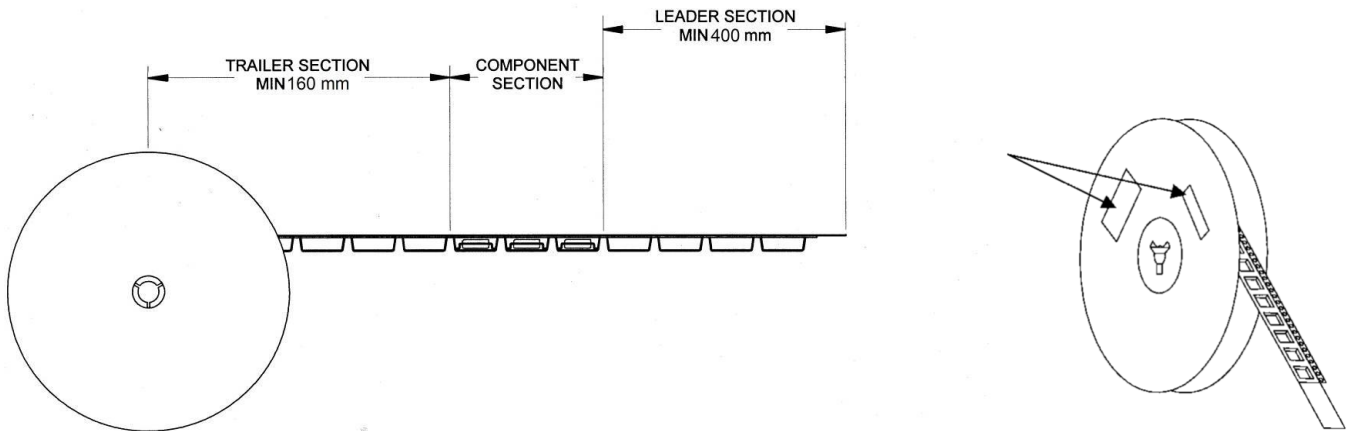
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 13" reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



- Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
 2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Level 1A	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Level C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!
 ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes. Solder profiles available upon request.

Contact plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free



Contact Information

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- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
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- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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