

**MH8S64DBKG -6,-6L-7,-7L,-8,-8L**

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

**DESCRIPTION**

The MH8S64DBKG is 8388608 - word by 64-bit Synchronous DRAM module. This consists of eight industry standard 4Mx16 Synchronous DRAMs in TSOP and one industry standard EEPROM in TSSOP.

The mounting of TSOP on a card edge Dual Inline package provides any application where high densities and large quantities of memory are required.

This is a socket type - memory modules, suitable for easy interchange or addition of modules.

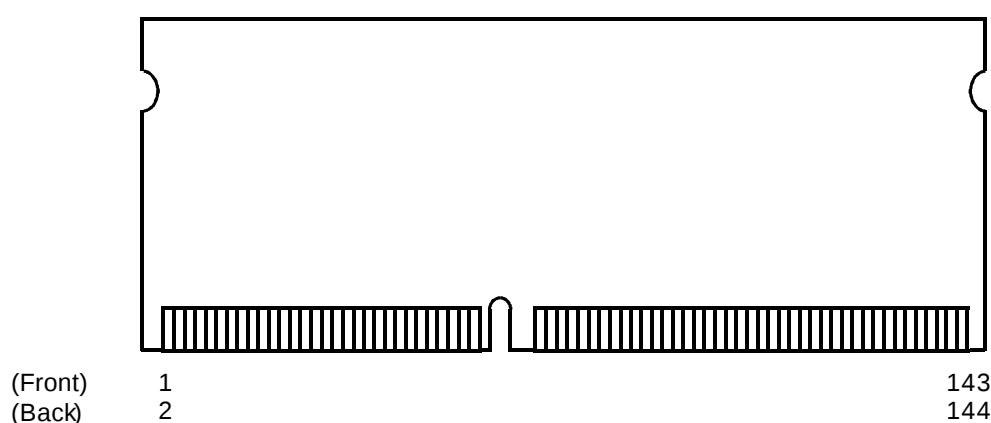
- Utilizes industry standard 4M x 16 Synchronous DRAMs TSOP and industry standard EEPROM in TSSOP
- 144-pin (72-pin dual in-line package)
- single 3.3V±0.3V power supply
- Max. Clock frequency -6:133MHz,-7,8:100MHz
- Fully synchronous operation referenced to clock rising edge
- 4 bank operation controlled by BA0,1(Bank Address)
- /CAS latency- 2/3(programmable)
- Burst length- 1/2/4/8/Full Page(programmable)
- Burst type- sequential / interleave(programmable)
- Column access - random
- Auto precharge / All bank precharge controlled by A10
- Auto refresh and Self refresh
- 4096 refresh cycle /64ms
- LVTTTL Interface

**FEATURES**

|        | Frequency | CLK Access Time<br>(Component SDRAM) |
|--------|-----------|--------------------------------------|
| -6,-6L | 133MHz    | 5.4ns(CL=3)                          |
| -7,-7L | 100MHz    | 6.0ns(CL=2)                          |
| -8,-8L | 100MHz    | 6.0ns(CL=3)                          |

**APPLICATION**

main memory or graphic memory in computer systems

**PCB Outline**

## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

## PIN CONFIGURATION

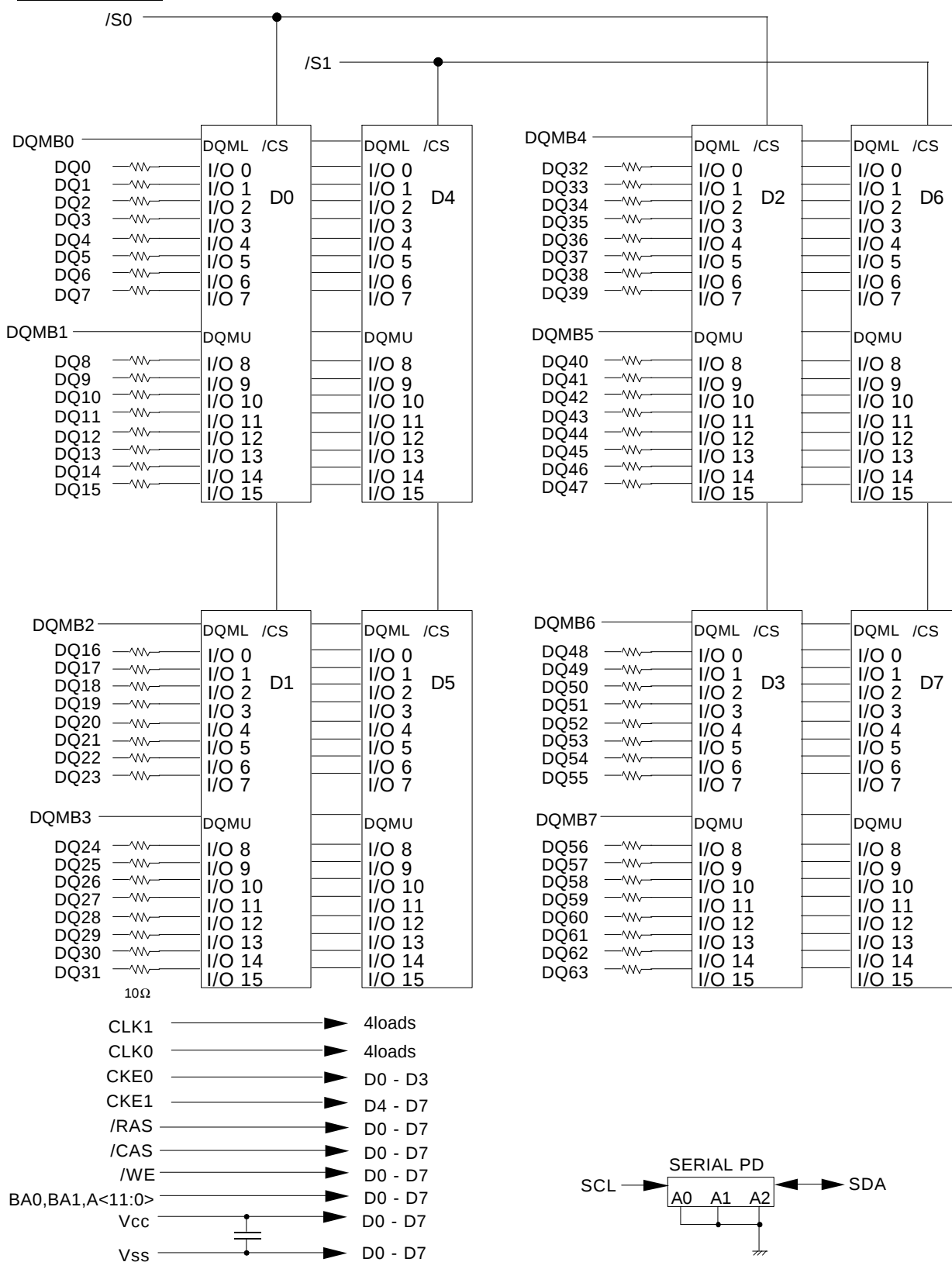
| PIN Number | Front side Pin Name | PIN Number | Back side Pin Name | PIN Number | Front side Pin Name | PIN Number | Back side Pin Name |
|------------|---------------------|------------|--------------------|------------|---------------------|------------|--------------------|
| 1          | Vss                 | 2          | Vss                | 73         | NC                  | 74         | CLK1               |
| 3          | DQ0                 | 4          | DQ32               | 75         | Vss                 | 76         | Vss                |
| 5          | DQ1                 | 6          | DQ33               | 77         | NC                  | 78         | NC                 |
| 7          | DQ2                 | 8          | DQ34               | 79         | NC                  | 80         | NC                 |
| 9          | DQ3                 | 10         | DQ35               | 81         | Vcc                 | 82         | Vcc                |
| 11         | Vcc                 | 12         | Vcc                | 83         | DQ16                | 84         | DQ48               |
| 13         | DQ4                 | 14         | DQ36               | 85         | DQ17                | 86         | DQ49               |
| 15         | DQ5                 | 16         | DQ37               | 87         | DQ18                | 88         | DQ50               |
| 17         | DQ6                 | 18         | DQ38               | 89         | DQ19                | 90         | DQ51               |
| 19         | DQ7                 | 20         | DQ39               | 91         | Vss                 | 92         | Vss                |
| 21         | Vss                 | 22         | Vss                | 93         | DQ20                | 94         | DQ52               |
| 23         | DQMB0               | 24         | DQMB4              | 95         | DQ21                | 96         | DQ53               |
| 25         | DQMB1               | 26         | DQMB5              | 97         | DQ22                | 98         | DQ54               |
| 27         | Vcc                 | 28         | Vcc                | 99         | DQ23                | 100        | DQ55               |
| 29         | A0                  | 30         | A3                 | 101        | Vcc                 | 102        | Vcc                |
| 31         | A1                  | 32         | A4                 | 103        | A6                  | 104        | A7                 |
| 33         | A2                  | 34         | A5                 | 105        | A8                  | 106        | BA0                |
| 35         | Vss                 | 36         | Vss                | 107        | Vss                 | 108        | Vss                |
| 37         | DQ8                 | 38         | DQ40               | 109        | A9                  | 110        | BA1                |
| 39         | DQ9                 | 40         | DQ41               | 111        | A10                 | 112        | A11                |
| 41         | DQ10                | 42         | DQ42               | 113        | Vcc                 | 114        | Vcc                |
| 43         | DQ11                | 44         | DQ43               | 115        | DQMB2               | 116        | DQMB6              |
| 45         | Vcc                 | 46         | Vcc                | 117        | DQMB3               | 118        | DQMB7              |
| 47         | DQ12                | 48         | DQ44               | 119        | Vss                 | 120        | Vss                |
| 49         | DQ13                | 50         | DQ45               | 121        | DQ24                | 122        | DQ56               |
| 51         | DQ14                | 52         | DQ46               | 123        | DQ25                | 124        | DQ57               |
| 53         | DQ15                | 54         | DQ47               | 125        | DQ26                | 126        | DQ58               |
| 55         | Vss                 | 56         | Vss                | 127        | DQ27                | 128        | DQ59               |
| 57         | NC                  | 58         | NC                 | 129        | Vcc                 | 130        | Vcc                |
| 59         | NC                  | 60         | NC                 | 131        | DQ28                | 132        | DQ60               |
| 61         | CLK0                | 62         | CKE0               | 133        | DQ29                | 134        | DQ61               |
| 63         | Vcc                 | 64         | Vcc                | 135        | DQ30                | 136        | DQ62               |
| 65         | /RAS                | 66         | /CAS               | 137        | DQ31                | 138        | DQ63               |
| 67         | /WE                 | 68         | CKE1               | 139        | Vss                 | 140        | Vss                |
| 69         | /S0                 | 70         | NC                 | 141        | SDA                 | 142        | SCL                |
| 71         | /S1                 | 72         | NC                 | 143        | Vcc                 | 144        | Vcc                |

NC = No Connection

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536870912-BIT (8388608 - WORD BY 64-BIT)SynchronousDRAM

## Block Diagram



## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

## Serial Presence Detect Table I

| Byte | Function described                                                         |               | SPD entry data               | SPD DATA(hex) |
|------|----------------------------------------------------------------------------|---------------|------------------------------|---------------|
| 0    | Defines # bytes written into serial memory at module mfor                  |               | 128                          | 80            |
| 1    | Total # bytes of SPD memory device                                         |               | 256 Bytes                    | 08            |
| 2    | Fundamental memory type                                                    |               | SDRAM                        | 04            |
| 3    | # Row Addresses on this assembly                                           |               | A0-A11                       | 0C            |
| 4    | # Column Addresses on this assembly                                        |               | A0-A7                        | 08            |
| 5    | # Module Banks on this assembly                                            |               | 2BANK                        | 02            |
| 6    | Data Width of this assembly...                                             |               | x64                          | 40            |
| 7    | ... Data Width continuation                                                |               | 0                            | 00            |
| 8    | Voltage interface standard of this assembly                                |               | LVTTTL                       | 01            |
| 9    | SDRAM Cycletime at Max. Supported CAS Latency (CL).<br>Cycle time for CL=3 | -6,-6L        | 7.5ns                        | 75            |
|      |                                                                            | -7,-7L,-8,-8L | 10ns                         | A0            |
| 10   | SDRAM Access from Clock<br>tAC for CL=3                                    | -6,-6L        | 5.4ns                        | 54            |
|      |                                                                            | -7,-7L,-8,-8L | 6ns                          | 60            |
| 11   | DIMM Configuration type (Non-parity,Parity,ECC)                            |               | Non-PARITY                   | 00            |
| 12   | Refresh Rate/Type                                                          |               | self refresh(15.625uS)       | 80            |
| 13   | SDRAM width,Primary DRAM                                                   |               | x16                          | 10            |
| 14   | Error Checking SDRAM data width                                            |               | N/A                          | 00            |
| 15   | Minimum Clock Delay,Back to Back Random Column Addresses                   |               | 1                            | 01            |
| 16   | Burst Lengths Supported                                                    |               | 1/2/4/8/Full page            | 8F            |
| 17   | # Banks on Each SDRAM device                                               |               | 4bank                        | 04            |
| 18   | CAS# Latency                                                               |               | 2/3                          | 06            |
| 19   | CS# Latency                                                                |               | 0                            | 01            |
| 20   | Write Latency                                                              |               | 0                            | 01            |
| 21   | SDRAM Module Attributes                                                    |               | non-buffered,non-registered  | 00            |
| 22   | SDRAM Device Attributes:General                                            |               | Precharge All,Auto precharge | 0E            |
| 23   | SDRAM Cycle time(2nd highest CAS latency)<br>Cycle time for CL=2           | -6,-6L        | 10ns                         | A0            |
|      |                                                                            | -7,-7L        | 10ns                         | A0            |
|      |                                                                            | -8,-8L        | 13ns                         | D0            |
| 24   | SDRAM Access from Clock(2nd highest CAS latency)<br>tAC for CL=2           | -6,-6L        | 6ns                          | 60            |
|      |                                                                            | -7,-7L        | 6ns                          | 60            |
|      |                                                                            | -8,-8L        | 7ns                          | 70            |
| 25   | SDRAM Cycle time(3rd highest CAS latency)                                  |               | N/A                          | 00            |
| 26   | SDRAM Access from Clock(3rd highest CAS latency)                           |               | N/A                          | 00            |
| 27   | Precharge to Active Minimum                                                |               | 20ns                         | 14            |
| 28   | Row Active to Row Active Min.                                              | -6,-6L        | 15ns                         | 0F            |
|      |                                                                            | -7,-7L,-8,-8L | 20ns                         | 14            |
| 29   | RAS to CAS Delay Min                                                       |               | 20ns                         | 14            |
| 30   | Active to Precharge Min                                                    | -6,-6L        | 45ns                         | 2D            |
|      |                                                                            | -7,-7L,-8,-8L | 50ns                         | 32            |

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## Serial Presence Detect Table II

|        |                                              |               |                      |                                      |
|--------|----------------------------------------------|---------------|----------------------|--------------------------------------|
| 31     | Density of each bank on module               |               | 32MByte              | 08                                   |
| 32     | Command and Address signal input setup time  | -6,-6L        | 1.5ns                | 15                                   |
|        |                                              | -7,-7L,-8,-8L | 2ns                  | 20                                   |
| 33     | Command and Address signal input hold time   | -6,-6L        | 0.8ns                | 08                                   |
|        |                                              | -7,-7L,-8,-8L | 1ns                  | 10                                   |
| 34     | Data signal input setup time                 | -6,-6L        | 1.5ns                | 15                                   |
|        |                                              | -7,-7L,-8,-8L | 2ns                  | 20                                   |
| 35     | Data signal input hold time                  | -6,-6L        | 0.8ns                | 08                                   |
|        |                                              | -7,-7L,-8,-8L | 1ns                  | 10                                   |
| 36-61  | Superset Information (may be used in future) |               | option               | 00                                   |
| 62     | SPD Revision                                 |               | rev 1.2B             | 12                                   |
| 63     | Checksum for bytes 0-62                      |               | Check sum for -6,-6L | 9E                                   |
|        |                                              |               | Check sum for -7,-7L | 05                                   |
|        |                                              |               | Check sum for -8,-8L | 45                                   |
| 64-71  | Manufactures Jedec ID code per JEP-108E      |               | MITSUBISHI           | 1CFFFFFFFFFFFFFF                     |
| 72     | Manufacturing location                       |               | Miyoshi, Japan       | 01                                   |
|        |                                              |               | Tajima, Japan        | 02                                   |
|        |                                              |               | NC, USA              | 03                                   |
|        |                                              |               | Germany              | 04                                   |
| 73-90  | Manufactures Part Number                     |               | MH8S64DBKG-6         | 4D483853363444424B472D362020202020   |
|        |                                              |               | MH8S64DBKG-6L        | 4D483853363444424B472D364C2020202020 |
|        |                                              |               | MH8S64DBKG-7         | 4D483853363444424B472D37202020202020 |
|        |                                              |               | MH8S64DBKG-7L        | 4D483853363444424B472D374C2020202020 |
|        |                                              |               | MH8S64DBKG-8         | 4D483853363444424B472D38202020202020 |
|        |                                              |               | MH8S64DBKG-8L        | 4D483853363444424B472D384C2020202020 |
| 91-92  | Revision Code                                |               | PCB revision         | rrrr                                 |
| 93-94  | Manufacturing date                           |               | year/week code       | yyww                                 |
| 95-98  | Assembly Serial Number                       |               | serial number        | ssssssss                             |
| 99-125 | Manufacture Specific Data                    |               | option               | 00                                   |
| 126    | Intel specification frequency                |               | 100MHz               | 64                                   |
| 127    | Intel specification CAS# Latency support     | -6,-6L,-7,-7L | CL=2/3,AP,CK0,1      | CF                                   |
|        |                                              | -8,-8L        | CL=3,AP,CK0,1        | CD                                   |
| 128+   | Unused storage locations                     |               | open                 | 00                                   |

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**PIN FUNCTION**

|                      |              |                                                                                                                                                                                                                                                                                                                                                |
|----------------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLK<br>(CLK0 ~ CLK1) | Input        | Master Clock: All other inputs are referenced to the rising edge of CK                                                                                                                                                                                                                                                                         |
| CKE0, CKE1           | Input        | Clock Enable: CKE controls internal clock. When CKE is low, internal clock for the following cycle is ceased. CKE is also used to select auto / self refresh. After self refresh mode is started, CKE E becomes asynchronous input. Self refresh is maintained as long as CKE is low.                                                          |
| /S0, /S1             | Input        | Chip Select: When /S is high, any command means No Operation.                                                                                                                                                                                                                                                                                  |
| /RAS, /CAS, /WE      | Input        | Combination of /RAS, /CAS, /WE defines basic commands.                                                                                                                                                                                                                                                                                         |
| A0-11                | Input        | A0-11 specify the Row/Column Address in conjunction with BA0,1. The Row Address is specified by A0-11. The Column Address is specified by A0-7. A10 is also used to indicate precharge option. When A10 is high at a read / write command, an auto precharge is performed. When A10 is high at a precharge command, both banks are precharged. |
| BA0,1                | Input        | Bank Address: BA0,1 is not simply BA. BA specifies the bank to which a command is applied. BA0,1 must be set with ACT, PRE, READ, WRITE commands                                                                                                                                                                                               |
| DQ0-63               | Input/Output | Data In and Data out are referenced to the rising edge of CK                                                                                                                                                                                                                                                                                   |
| DQMB0-7              | Input        | Din Mask/Output Disable: When DQMB is high in burst write, Din for the current cycle is masked. When DQMB is high in burst read, Dout is disabled at the next but one cycle.                                                                                                                                                                   |
| Vdd, Vss             | Power Supply | Power Supply for the memory mounted module.                                                                                                                                                                                                                                                                                                    |
| SCL                  | Input        | Serial clock for serial PD                                                                                                                                                                                                                                                                                                                     |
| SDA                  | Output       | Serial data for serial PD                                                                                                                                                                                                                                                                                                                      |

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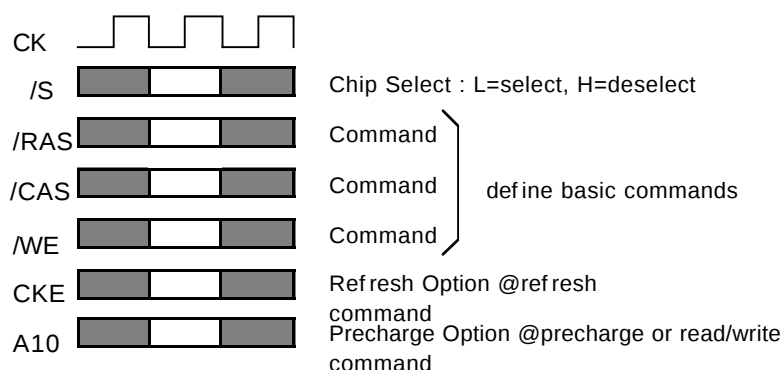
536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

**BASIC FUNCTIONS**

The MH8S64DBKG provides basic functions, bank(row) activate, burst read / write, bank(row) precharge, and auto / self refresh.

Each command is defined by control signals of /RAS, /CAS and /WE at CK rising edge. In addition to 3 signals, /S, CKE and A10 are used as chip select, refresh option, and precharge option, respectively.

To know the detailed definition of commands please see the command truth table.

**Activate(ACT) [/RAS =L, /CAS = /WE =H]**

ACT command activates a row in an idle bank indicated by BA.

**Read(READ) [/RAS =H, /CAS =L, /WE =H]**

READ command starts burst read from the active bank indicated by BA. First output data appears after /CAS latency. When A10 =H at this command, the bank is deactivated after the burst read(auto-precharge, **READA**).

**Write(WRITE) [/RAS =H, /CAS = /WE =L]**

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A10 =H at this command, the bank is deactivated after the burst write(auto-precharge, **WRITEA**).

**Precharge(PRE) [/RAS =L, /CAS =H, /WE =L]**

PRE command deactivates the active bank indicated by BA. This command also terminates burst read / write operation. When A10 =H at this command, both banks are deactivated(precharge all, **PREA**).

**Auto-Refresh(REFA) [/RAS =/CAS =L, /WE =CKE =H]**

REFA command starts auto-refresh cycle. Refresh address including bank address are generated internally. After this command, the banks are precharged automatically.

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**COMMAND TRUTH TABLE**

| COMMAND                                          | MNEMONIC | CKE <sub>n-1</sub> | CKE <sub>n</sub> | /S | /RAS | /CAS | /WE | BA0,1 | A11 | A10 | A0-9 |
|--------------------------------------------------|----------|--------------------|------------------|----|------|------|-----|-------|-----|-----|------|
| Deselect                                         | DESEL    | H                  | X                | H  | X    | X    | X   | X     | X   | X   | X    |
| No Operation                                     | NOP      | H                  | X                | L  | H    | H    | H   | X     | X   | X   | X    |
| Row Address Entry & Bank Activate                | ACT      | H                  | X                | L  | L    | H    | H   | V     | V   | V   | V    |
| Single Bank Precharge                            | PRE      | H                  | X                | L  | L    | H    | L   | V     | X   | L   | X    |
| Precharge All Bank                               | PREA     | H                  | X                | L  | L    | H    | L   | X     | X   | H   | X    |
| Column Address Entry & Write                     | WRITE    | H                  | X                | L  | H    | L    | L   | V     | V   | L   | V    |
| Column Address Entry & Write with Auto-Precharge | WRITEA   | H                  | X                | L  | H    | L    | L   | V     | V   | H   | V    |
| Column Address Entry & Read                      | READ     | H                  | X                | L  | H    | L    | H   | V     | V   | L   | V    |
| Column Address Entry & Read with Auto-Precharge  | READA    | H                  | X                | L  | H    | L    | H   | V     | V   | H   | V    |
| Auto-Refresh                                     | REFA     | H                  | H                | L  | L    | L    | H   | X     | X   | X   | X    |
| Self-Refresh Entry                               | REFS     | H                  | L                | L  | L    | L    | H   | X     | X   | X   | X    |
| Self-Refresh Exit                                | REFSX    | L                  | H                | H  | X    | X    | X   | X     | X   | X   | X    |
|                                                  |          | L                  | H                | L  | H    | H    | H   | X     | X   | X   | X    |
| Burst Terminate                                  | TERM     | H                  | X                | L  | H    | H    | L   | X     | X   | X   | X    |
| Mode Register Set                                | MRS      | H                  | X                | L  | L    | L    | L   | L     | L   | L   | V*1  |

H =High Level, L = Low Level, V = Valid, X = Don't Care, n = CK cycle number

## NOTE:

1.A7-9 = 0, A0-6 = Mode Address

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536870912-BIT (8388608 - WORD BY 64-BIT)SynchronousDRAM

**FUNCTION TRUTH TABLE**

| Current State | /S | /RAS | /CAS | /WE | Address              | Command          | Action                                                                    |
|---------------|----|------|------|-----|----------------------|------------------|---------------------------------------------------------------------------|
| IDLE          | H  | X    | X    | X   | X                    | DESEL            | NOP                                                                       |
|               | L  | H    | H    | H   | X                    | NOP              | NOP                                                                       |
|               | L  | H    | H    | L   | X                    | TBST             | ILLEGAL*2                                                                 |
|               | L  | H    | L    | X   | BA,CA,A10            | READ/WRITE       | ILLEGAL*2                                                                 |
|               | L  | L    | H    | H   | BA,RA                | ACT              | Bank Active,Latch RA                                                      |
|               | L  | L    | H    | L   | BA,A10               | PRE/PREA         | NOP*4                                                                     |
|               | L  | L    | L    | H   | X                    | REFA             | Auto-Refresh*5                                                            |
|               | L  | L    | L    | L   | Op-Code,<br>Mode-Add | MRS              | Mode Register Set*5                                                       |
| ROW ACTIVE    | H  | X    | X    | X   | X                    | DESEL            | NOP                                                                       |
|               | L  | H    | H    | H   | X                    | NOP              | NOP                                                                       |
|               | L  | H    | H    | L   | X                    | TBST             | NOP                                                                       |
|               | L  | H    | L    | H   | BA,CA,A10            | READ/READA       | Begin Read,Latch CA,<br>Determine Auto-Precharge                          |
|               | L  | H    | L    | L   | BA,CA,A10            | WRITE/<br>WRITEA | Begin Write,Latch CA,<br>Determine Auto-Precharge                         |
|               | L  | L    | H    | H   | BA,RA                | ACT              | Bank Active/ILLEGAL*2                                                     |
|               | L  | L    | H    | L   | BA,A10               | PRE/PREA         | Precharge/Precharge All                                                   |
|               | L  | L    | L    | H   | X                    | REFA             | ILLEGAL                                                                   |
|               | L  | L    | L    | L   | Op-Code,<br>Mode-Add | MRS              | ILLEGAL                                                                   |
| READ          | H  | X    | X    | X   | X                    | DESEL            | NOP(Continue Burst to END)                                                |
|               | L  | H    | H    | H   | X                    | NOP              | NOP(Continue Burst to END)                                                |
|               | L  | H    | H    | L   | X                    | TBST             | Terminate Burst                                                           |
|               | L  | H    | L    | H   | BA,CA,A10            | READ/READA       | Terminate Burst,Latch CA,<br>Begin New Read,Determine<br>Auto-Precharge*3 |
|               | L  | H    | L    | L   | BA,CA,A10            | WRITE/WRITEA     | Terminate Burst,Latch CA,<br>Begin Write,Determine Auto-<br>Precharge*3   |
|               | L  | L    | H    | H   | BA,RA                | ACT              | Bank Active/ILLEGAL*2                                                     |
|               | L  | L    | H    | L   | BA,A10               | PRE/PREA         | Terminate Burst,Precharge                                                 |
|               | L  | L    | L    | H   | X                    | REFA             | ILLEGAL                                                                   |
|               | L  | L    | L    | L   | Op-Code,<br>Mode-Add | MRS              | ILLEGAL                                                                   |

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536870912-BIT (8388608 - WORD BY 64-BIT)SynchronousDRAM

**FUNCTION TRUTH TABLE(continued)**

| Current State                   | /S | /RAS | /CAS | /WE | Address              | Command          | Action                                                              |
|---------------------------------|----|------|------|-----|----------------------|------------------|---------------------------------------------------------------------|
| WRITE                           | H  | X    | X    | X   | X                    | DESEL            | NOP(Continue Burst to END)                                          |
|                                 | L  | H    | H    | H   | X                    | NOP              | NOP(Continue Burst to END)                                          |
|                                 | L  | H    | H    | L   | X                    | TBST             | Terminate Burst                                                     |
|                                 | L  | H    | L    | H   | BA,CA,A10            | READ/READA       | Terminate Burst,Latch CA,<br>Begin Read,Determine Auto-Precharge*3  |
|                                 | L  | H    | L    | L   | BA,CA,A10            | WRITE/<br>WRITEA | Terminate Burst,Latch CA,<br>Begin Write,Determine Auto-Precharge*3 |
|                                 | L  | L    | H    | H   | BA,RA                | ACT              | Bank Active/ILLEGAL*2                                               |
|                                 | L  | L    | H    | L   | BA,A10               | PRE/PREA         | Terminate Burst,Precharge                                           |
|                                 | L  | L    | L    | H   | X                    | REFA             | ILLEGAL                                                             |
|                                 | L  | L    | L    | L   | Op-Code,<br>Mode-Add | MRS              | ILLEGAL                                                             |
| READ with<br>AUTO<br>PRECHARGE  | H  | X    | X    | X   | X                    | DESEL            | NOP(Continue Burst to END)                                          |
|                                 | L  | H    | H    | H   | X                    | NOP              | NOP(Continue Burst to END)                                          |
|                                 | L  | H    | H    | L   | X                    | TBST             | ILLEGAL                                                             |
|                                 | L  | H    | L    | H   | BA,CA,A10            | READ/READA       | ILLEGAL                                                             |
|                                 | L  | H    | L    | L   | BA,CA,A10            | WRITE/<br>WRITEA | ILLEGAL                                                             |
|                                 | L  | L    | H    | H   | BA,RA                | ACT              | Bank Active/ILLEGAL*2                                               |
|                                 | L  | L    | H    | L   | BA,A10               | PRE/PREA         | ILLEGAL*2                                                           |
|                                 | L  | L    | L    | H   | X                    | REFA             | ILLEGAL                                                             |
|                                 | L  | L    | L    | L   | Op-Code,<br>Mode-Add | MRS              | ILLEGAL                                                             |
| WRITE with<br>AUTO<br>PRECHARGE | H  | X    | X    | X   | X                    | DESEL            | NOP(Continue Burst to END)                                          |
|                                 | L  | H    | H    | H   | X                    | NOP              | NOP(Continue Burst to END)                                          |
|                                 | L  | H    | H    | L   | X                    | TBST             | ILLEGAL                                                             |
|                                 | L  | H    | L    | H   | BA,CA,A10            | READ/READA       | ILLEGAL                                                             |
|                                 | L  | H    | L    | L   | BA,CA,A10            | WRITE/<br>WRITEA | ILLEGAL                                                             |
|                                 | L  | L    | H    | H   | BA,RA                | ACT              | Bank Active/ILLEGAL*2                                               |
|                                 | L  | L    | H    | L   | BA,A10               | PRE/PREA         | ILLEGAL*2                                                           |
|                                 | L  | L    | L    | H   | X                    | REFA             | ILLEGAL                                                             |
|                                 | L  | L    | L    | L   | Op-Code,<br>Mode-Add | MRS              | ILLEGAL                                                             |

## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

**FUNCTION TRUTH TABLE(continued)**

| Current State         | /S | /RAS | /CAS | /WE | Address              | Command    | Action                    |
|-----------------------|----|------|------|-----|----------------------|------------|---------------------------|
| PRE -<br>CHARGING     | H  | X    | X    | X   | X                    | DESEL      | NOP(Idle after tRP)       |
|                       | L  | H    | H    | H   | X                    | NOP        | NOP(Idle after tRP)       |
|                       | L  | H    | H    | L   | X                    | TBST       | ILLEGAL*2                 |
|                       | L  | H    | L    | X   | BA,CA,A10            | READ/WRITE | ILLEGAL*2                 |
|                       | L  | L    | H    | H   | BA,RA                | ACT        | ILLEGAL*2                 |
|                       | L  | L    | H    | L   | BA,A10               | PRE/PREA   | NOP*4(Idle after tRP)     |
|                       | L  | L    | L    | H   | X                    | REFA       | ILLEGAL                   |
|                       | L  | L    | L    | L   | Op-Code,<br>Mode-Add | MRS        | ILLEGAL                   |
| ROW<br>ACTIVATING     | H  | X    | X    | X   | X                    | DESEL      | NOP(Row Active after tRCD |
|                       | L  | H    | H    | H   | X                    | NOP        | NOP(Row Active after tRCD |
|                       | L  | H    | H    | L   | X                    | TBST       | ILLEGAL*2                 |
|                       | L  | H    | L    | X   | BA,CA,A10            | READ/WRITE | ILLEGAL*2                 |
|                       | L  | L    | H    | H   | BA,RA                | ACT        | ILLEGAL*2                 |
|                       | L  | L    | H    | L   | BA,A10               | PRE/PREA   | ILLEGAL*2                 |
|                       | L  | L    | L    | H   | X                    | REFA       | ILLEGAL                   |
|                       | L  | L    | L    | L   | Op-Code,<br>Mode-Add | MRS        | ILLEGAL                   |
| WRITE RE-<br>COVERING | H  | X    | X    | X   | X                    | DESEL      | NOP                       |
|                       | L  | H    | H    | H   | X                    | NOP        | NOP                       |
|                       | L  | H    | H    | L   | X                    | TBST       | ILLEGAL*2                 |
|                       | L  | H    | L    | X   | BA,CA,A10            | READ/WRITE | ILLEGAL*2                 |
|                       | L  | L    | H    | H   | BA,RA                | ACT        | ILLEGAL*2                 |
|                       | L  | L    | H    | L   | BA,A10               | PRE/PREA   | ILLEGAL*2                 |
|                       | L  | L    | L    | H   | X                    | REFA       | ILLEGAL                   |
|                       | L  | L    | L    | L   | Op-Code,<br>Mode-Add | MRS        | ILLEGAL                   |

**MH8S64DBKG -6,-6L-7,-7L,-8,-8L**

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

**FUNCTION TRUTH TABLE(continued)**

| Current State               | /S | /RAS | /CAS | /WE | Address              | Command    | Action               |
|-----------------------------|----|------|------|-----|----------------------|------------|----------------------|
| RE-FRESHING                 | H  | X    | X    | X   | X                    | DESEL      | NOP(Idle after tRC)  |
|                             | L  | H    | H    | H   | X                    | NOP        | NOP(Idle after tRC)  |
|                             | L  | H    | H    | L   | X                    | TBST       | ILLEGAL              |
|                             | L  | H    | L    | X   | BA,CA,A10            | READ/WRITE | ILLEGAL              |
|                             | L  | L    | H    | H   | BA,RA                | ACT        | ILLEGAL              |
|                             | L  | L    | H    | L   | BA,A10               | PRE/PREA   | ILLEGAL              |
|                             | L  | L    | L    | H   | X                    | REFA       | ILLEGAL              |
|                             | L  | L    | L    | L   | Op-Code,<br>Mode-Add | MRS        | ILLEGAL              |
| MODE<br>REGISTER<br>SETTING | H  | X    | X    | X   | X                    | DESEL      | NOP(Idle after tRSC) |
|                             | L  | H    | H    | H   | X                    | NOP        | NOP(Idle after tRSC) |
|                             | L  | H    | H    | L   | X                    | TBST       | ILLEGAL              |
|                             | L  | H    | L    | X   | BA,CA,A10            | READ/WRITE | ILLEGAL              |
|                             | L  | L    | H    | H   | BA,RA                | ACT        | ILLEGAL              |
|                             | L  | L    | H    | L   | BA,A10               | PRE/PREA   | ILLEGAL              |
|                             | L  | L    | L    | H   | X                    | REFA       | ILLEGAL              |
|                             | L  | L    | L    | L   | Op-Code,<br>Mode-Add | MRS        | ILLEGAL              |

## ABBREVIATIONS:

H = High Level, L = Low Level, X = Don't Care

BA = Bank Address, RA = Row Address, CA = Column Address, NOP = No Operation

## NOTES:

1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.

ILLEGAL = Device operation and / or data-integrity are not guaranteed.

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536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

**FUNCTION TRUTH TABLE FOR CKE**

| Current State                     | CK <sub>n-1</sub> | CK <sub>n</sub> | /S | /RAS | /CAS | /WE | Add | Action                              |
|-----------------------------------|-------------------|-----------------|----|------|------|-----|-----|-------------------------------------|
| SELF - REFRESH*1                  | H                 | X               | X  | X    | X    | X   | X   | INVALID                             |
|                                   | L                 | H               | H  | X    | X    | X   | X   | Exit Self-Refresh (Idle after tRC)  |
|                                   | L                 | H               | L  | H    | H    | H   | X   | Exit Self-Refresh (Idle after tRC)  |
|                                   | L                 | H               | L  | H    | H    | L   | X   | ILLEGAL                             |
|                                   | L                 | H               | L  | H    | L    | X   | X   | ILLEGAL                             |
|                                   | L                 | H               | L  | L    | X    | X   | X   | ILLEGAL                             |
|                                   | L                 | L               | X  | X    | X    | X   | X   | NOP (Maintain Self-Refresh)         |
| POWER DOWN                        | H                 | X               | X  | X    | X    | X   | X   | INVALID                             |
|                                   | L                 | H               | X  | X    | X    | X   | X   | Exit Power Down to Idle             |
|                                   | L                 | L               | X  | X    | X    | X   | X   | NOP (Maintain Self-Refresh)         |
| ALL BANKS IDLE*2                  | H                 | H               | X  | X    | X    | X   | X   | Refer to Function Truth Table       |
|                                   | H                 | L               | L  | L    | L    | H   | X   | Enter Self-Refresh                  |
|                                   | H                 | L               | H  | X    | X    | X   | X   | Enter Power Down                    |
|                                   | H                 | L               | L  | H    | H    | H   | X   | Enter Power Down                    |
|                                   | H                 | L               | L  | H    | H    | L   | X   | ILLEGAL                             |
|                                   | H                 | L               | L  | H    | L    | X   | X   | ILLEGAL                             |
|                                   | H                 | L               | L  | L    | X    | X   | X   | ILLEGAL                             |
|                                   | L                 | X               | X  | X    | X    | X   | X   | Refer to Current State = Power Down |
| ANY STATE other than listed above | H                 | H               | X  | X    | X    | X   | X   | Refer to Function Truth Table       |
|                                   | H                 | L               | X  | X    | X    | X   | X   | Begin CK0 Suspend at Next Cycle*3   |
|                                   | L                 | H               | X  | X    | X    | X   | X   | Exit CK0 Suspend at Next Cycle*3    |
|                                   | L                 | L               | X  | X    | X    | X   | X   | Maintain CK0 Suspend                |

## ABBREVIATIONS:

H = High Level, L = Low Level, X = Don't Care

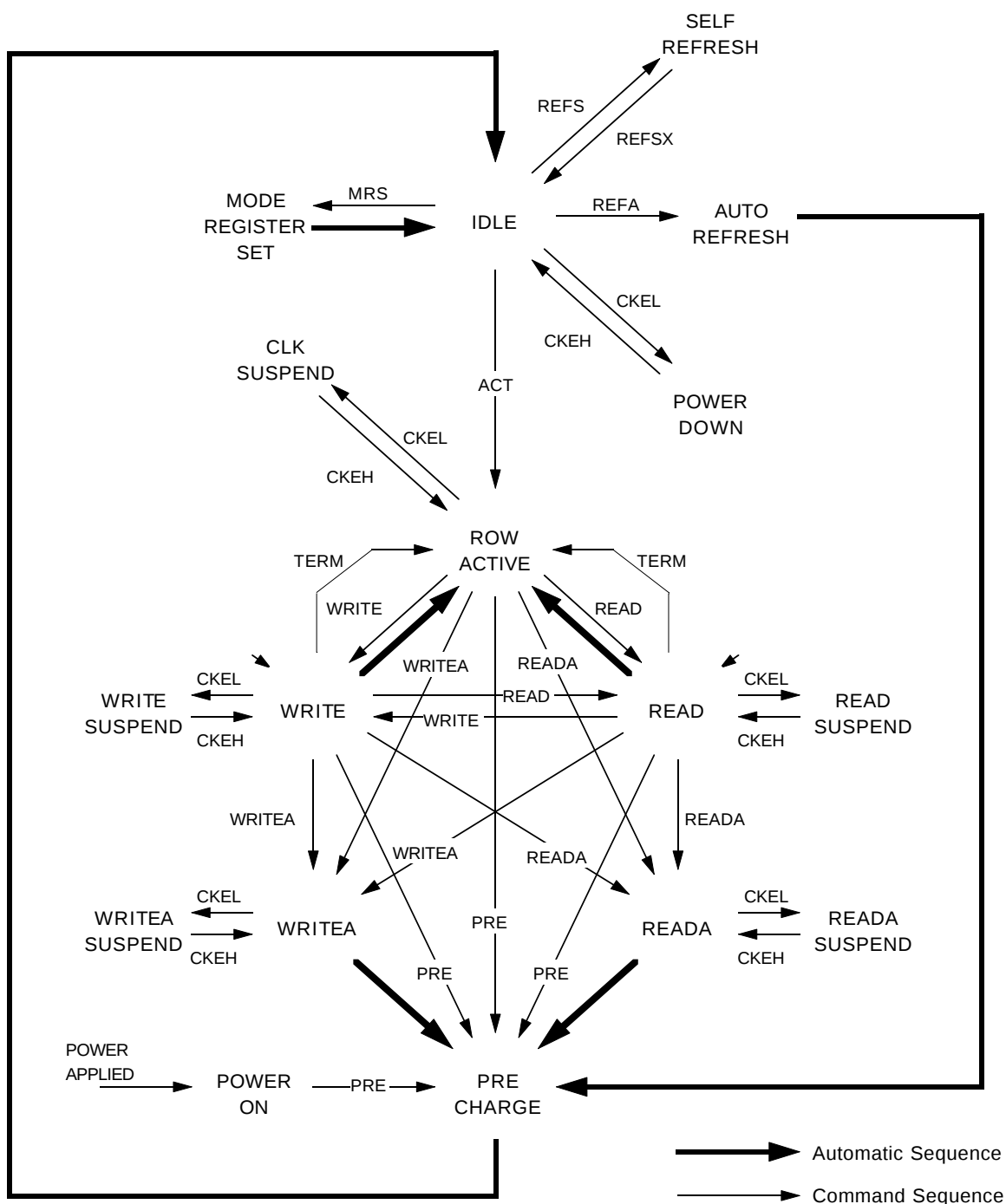
## NOTES:

1. CKE Low to High transition will re-enable CK and other inputs **asynchronously**.  
A minimum setup time must be satisfied before any command other than EXIT.
2. Power-Down and Self-Refresh can be entered only from the All banks idle State.
3. Must be legal command.

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536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

## SIMPLIFIED STATE DIAGRAM



MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT)SynchronousDRAM

POWER ON SEQUENCE

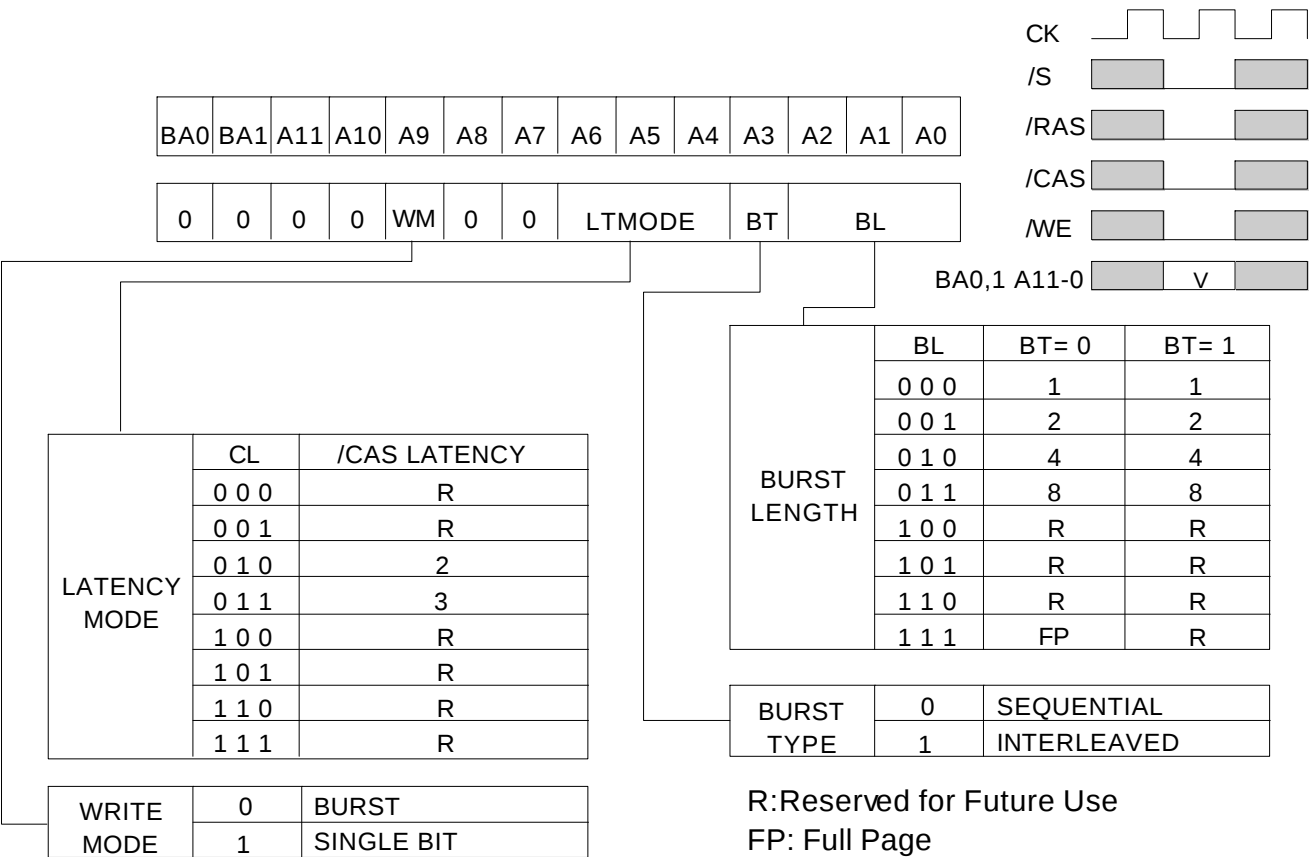
Before starting normal operation, the following power on sequence is necessary to prevent a SDRAM from damaged or malfunctioning.

1. Apply power and start clock. Attempt to maintain CKE high, DQM0-7 high and NOP condition at the inputs.
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200us.
3. Issue precharge commands for all banks. (PRE or PREA)
4. After all banks become idle state (after tRP), issue 8 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

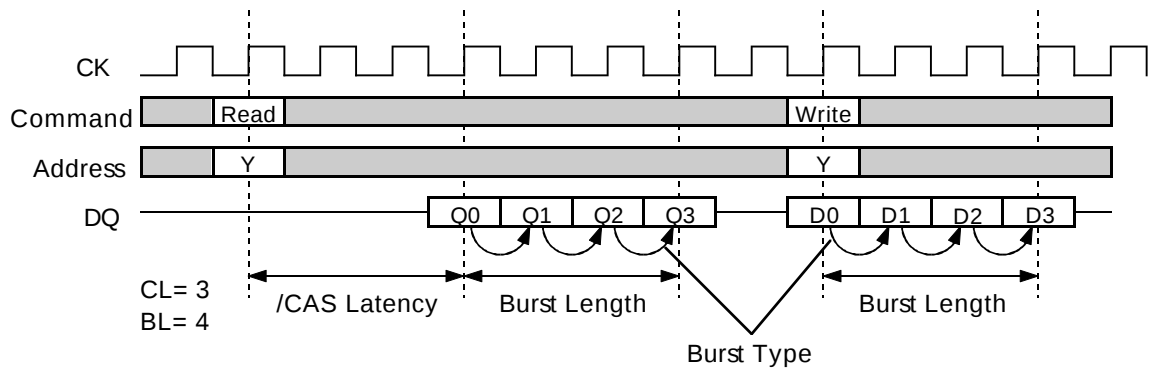
After these sequence, the SDRAM is idle state and ready for normal operation.

MODE REGISTER

Burst Length, Burst Type and /CAS Latency can be programmed by setting the mode register(MRS). The mode register stores these data until the next MRS command, which may be issued when both banks are in idle state. After tRSC from a MRS command, the SDRAM is ready for new command.



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536870912-BIT (8388608 - WORD BY 64-BIT)SynchronousDRAM



| Initial Address |    |    | BL | Column Addressing |   |   |   |   |   |   |   |             |   |   |   |   |   |   |   |
|-----------------|----|----|----|-------------------|---|---|---|---|---|---|---|-------------|---|---|---|---|---|---|---|
| A2              | A1 | A0 |    | Sequential        |   |   |   |   |   |   |   | Interleaved |   |   |   |   |   |   |   |
| 0               | 0  | 0  | 8  | 0                 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0           | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0               | 0  | 1  |    | 1                 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1           | 0 | 3 | 2 | 5 | 4 | 7 | 6 |
| 0               | 1  | 0  |    | 2                 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2           | 3 | 0 | 1 | 6 | 7 | 4 | 5 |
| 0               | 1  | 1  |    | 3                 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3           | 2 | 1 | 0 | 7 | 6 | 5 | 4 |
| 1               | 0  | 0  |    | 4                 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4           | 5 | 6 | 7 | 0 | 1 | 2 | 3 |
| 1               | 0  | 1  |    | 5                 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5           | 4 | 7 | 6 | 1 | 0 | 3 | 2 |
| 1               | 1  | 0  |    | 6                 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6           | 7 | 4 | 5 | 2 | 3 | 0 | 1 |
| 1               | 1  | 1  |    | 7                 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -               | 0  | 0  | 4  | 0                 | 1 | 2 | 3 |   |   |   |   | 0           | 1 | 2 | 3 |   |   |   |   |
| -               | 0  | 1  |    | 1                 | 2 | 3 | 0 |   |   |   |   | 1           | 0 | 3 | 2 |   |   |   |   |
| -               | 1  | 0  |    | 2                 | 3 | 0 | 1 |   |   |   |   | 2           | 3 | 0 | 1 |   |   |   |   |
| -               | 1  | 1  |    | 3                 | 0 | 1 | 2 |   |   |   |   | 3           | 2 | 1 | 0 |   |   |   |   |
| -               | -  | 0  | 2  | 0                 | 1 |   |   |   |   |   |   | 0           | 1 |   |   |   |   |   |   |
| -               | -  | 1  |    | 1                 | 0 |   |   |   |   |   |   | 1           | 0 |   |   |   |   |   |   |

**MH8S64DBKG -6,-6L-7,-7L,-8,-8L**

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

**OPERATION DESCRIPTION****BANK ACTIVATE**

One of four banks is activated by an ACT command.

A bank is selected by BA0-1. A row is selected by A0-11.

Multiple banks can be active state concurrently by issuing multiple ACT commands.

Minimum activation interval between one bank and another bank is  $t_{RRD}$ .

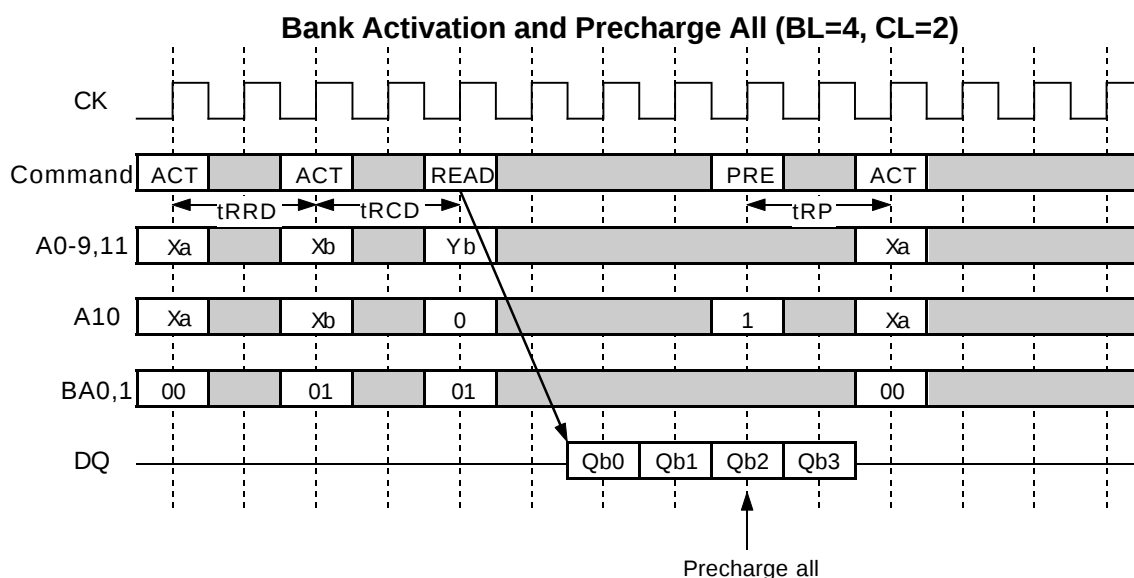
**PRECHARGE**

An open bank is deactivated by a PRE command.

A bank to be deactivated is designated by BA0-1.

When multiple banks are active, a precharge all command (PREA, PRE + A10=H) deactivates all of open banks at the same time. BA0-1 are "Don't Care" in this case.

Minimum delay time of an ACT command after a PRE command to the same bank is  $t_{RP}$ .

**READ**

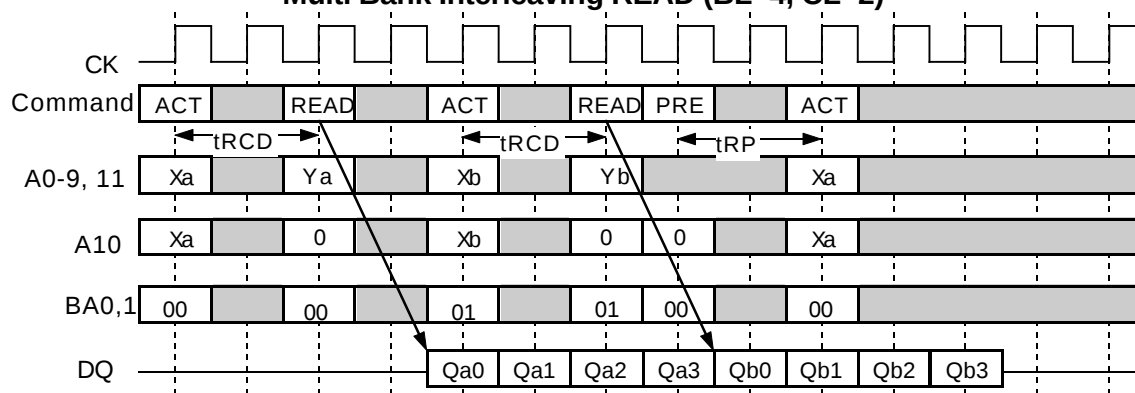
A READ command can be issued to any active bank. The start address is specified by A0-7(x16). 1st output data is available after the /CAS Latency from the READ. The consecutive data length is defined by the Burst Length. The address sequence of the burst data is defined by the Burst Type. Minimum delay time of a READ command after an ACT command to the same bank is  $t_{RCD}$ .

When A10 is high at a READ command, auto-precharge (READA) is performed. Any command (READ, WRITE, PRE, ACT, TBST) to the same bank is inhibited till the internal precharge is complete. The internal precharge starts at the BL after READA. The next ACT command can be issued after  $(BL + t_{RP})$  from the previous READA. In any case,  $t_{RCD} + BL \geq t_{RASmin}$  must be met.

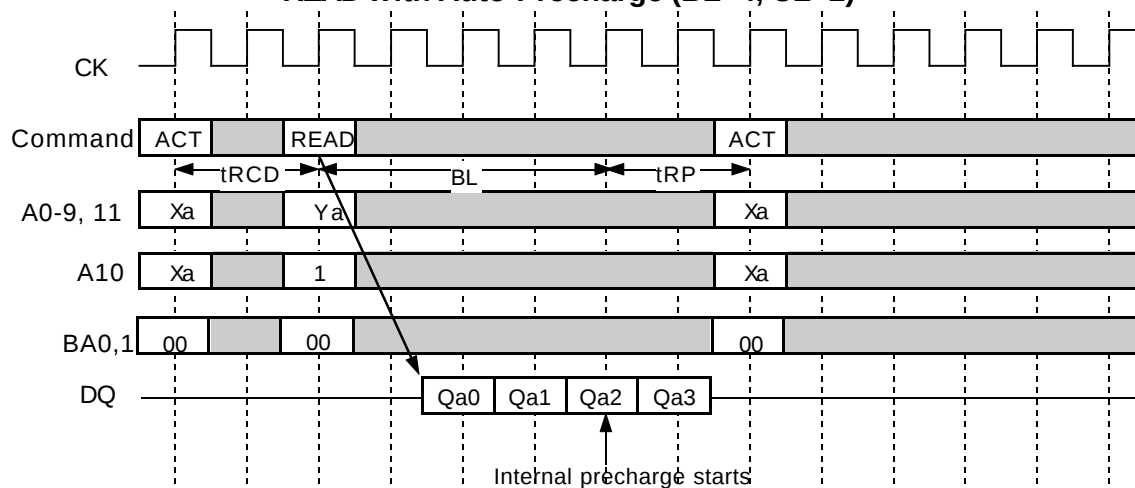
## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

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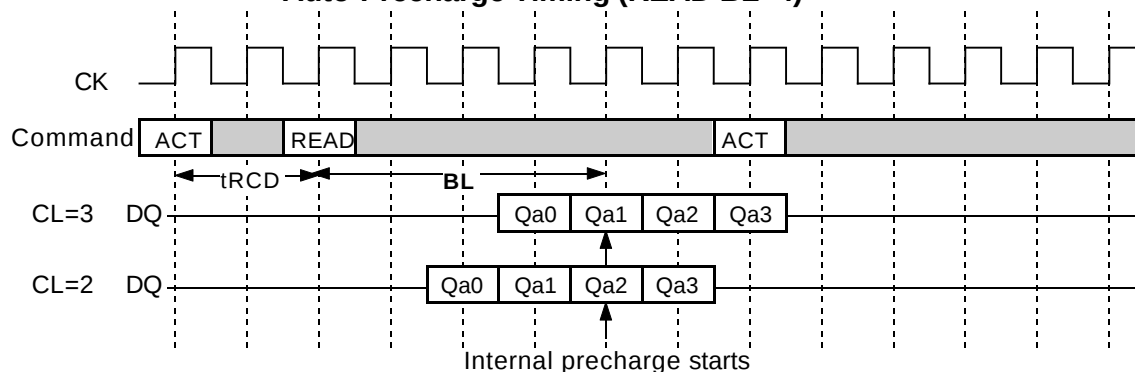
## Multi Bank Interleaving READ (BL=4, CL=2)



## READ with Auto-Precharge (BL=4, CL=2)



## Auto-Precharge Timing (READ BL=4)

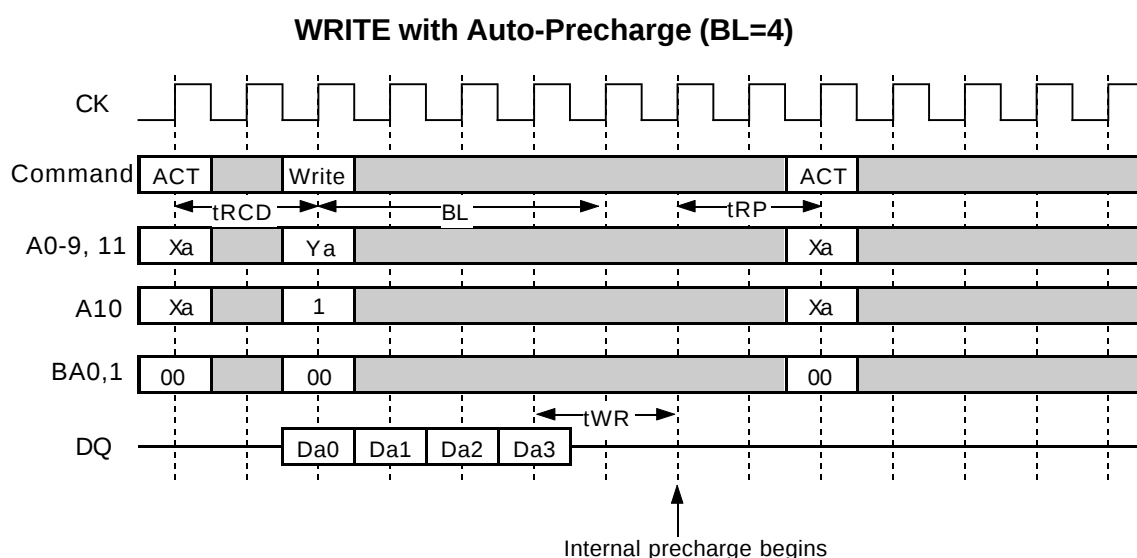
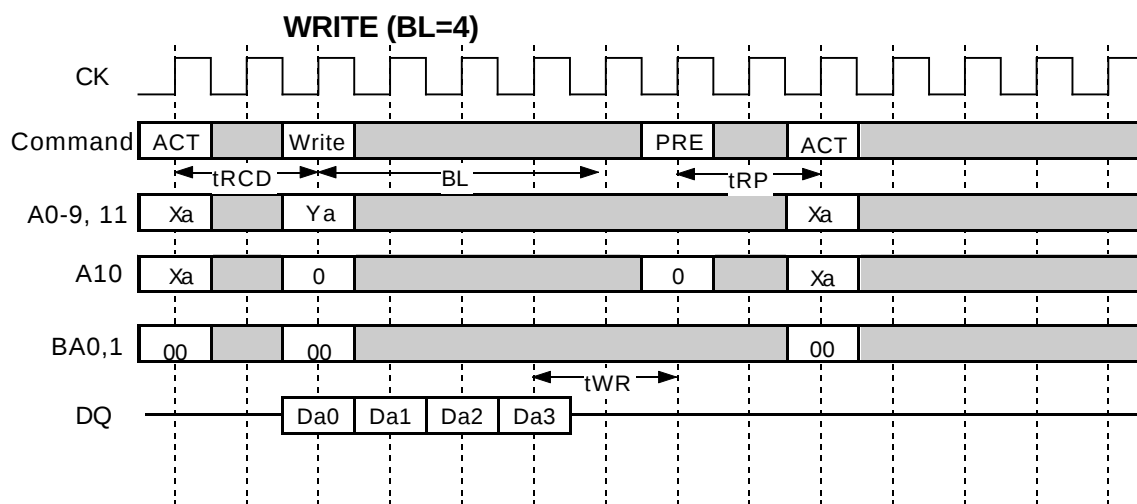


## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

**WRITE**

A WRITE command can be issued to any active bank. The start address is specified by A0-7 (x16). 1st input data is set at the same cycle as the WRITE. The consecutive data length to be written is defined by the Burst Length. The address sequence of burst data is defined by the Burst Type. Minimum delay time of a WRITE command after an ACT command to the same bank is  $t_{RCD}$ . From the last input data to the PRE command, the write recovery time ( $t_{WR}$ ) is required. When A10 is high at a WRITE command, auto-precharge (WRITEA) is performed. Any command (READ, WRITE, PRE, ACT, TBST) to the same bank is inhibited till the internal precharge is complete. The internal precharge starts at  $t_{WR}$  after the last input data cycle. The next ACT command can be issued after  $(BL + t_{WR} - 1 + t_{RP})$  from the previous WRITEA. In any case,  $t_{RCD} + BL + t_{WR} - 1 > t_{RASmin}$  must be met.

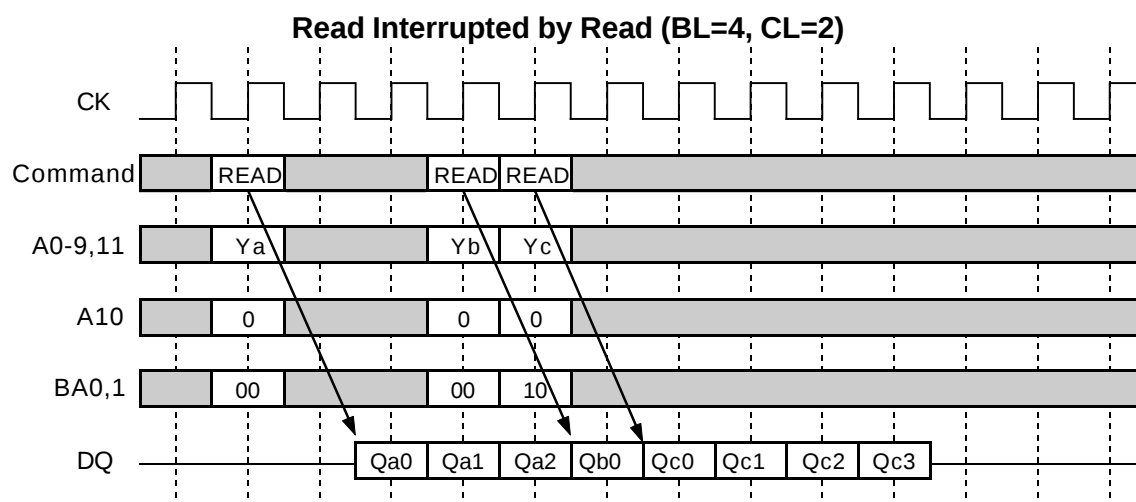


## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

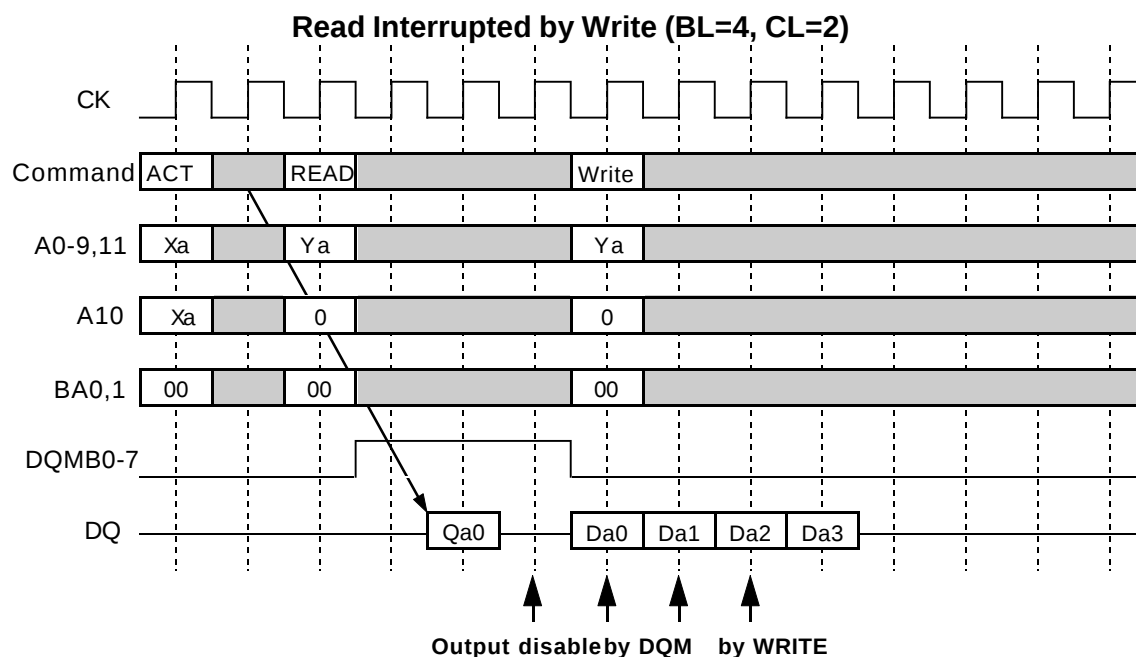
536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

**BURST INTERRUPTION****[ Read Interrupted by Read ]**

Burst read operation can be interrupted by new read of the same or the other bank. Random column access is allowed READ to READ interval is minimum 1 CK

**[ Read Interrupted by Write ]**

Burst read operation can be interrupted by write of any active bank. Random column access is allowed. In this case, the DQ should be controlled adequately by using the DQMB0-7 to prevent the bus contention. The output is disabled automatically 2 cycle after WRITE assertion.

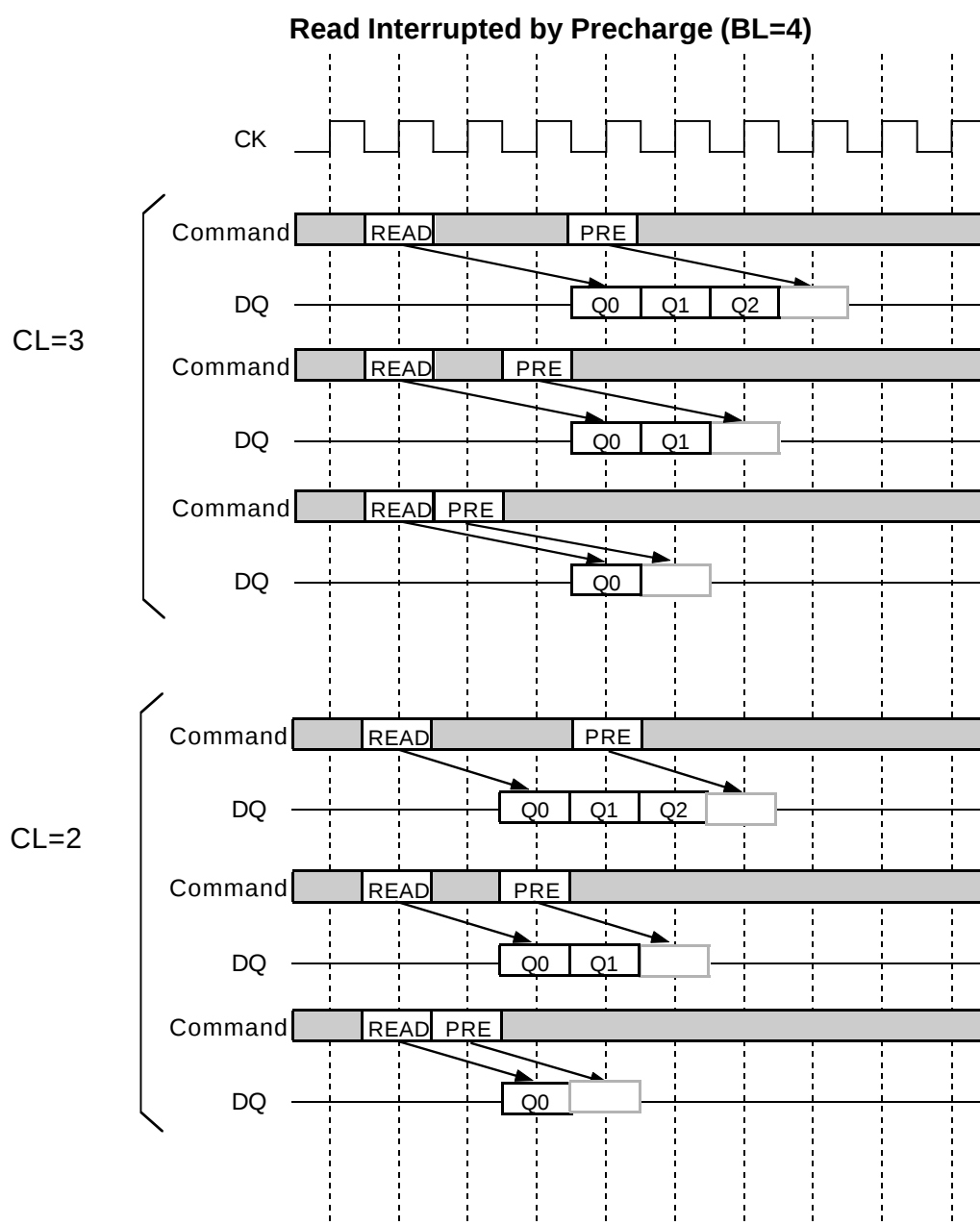


## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

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**[ Read Interrupted by Precharge ]**

A burst read operation can be interrupted by precharge of *the same bank*. READ to PRE interval is minimum 1 CK. A PRE command output disable latency is equivalent to the /CAS Latency.

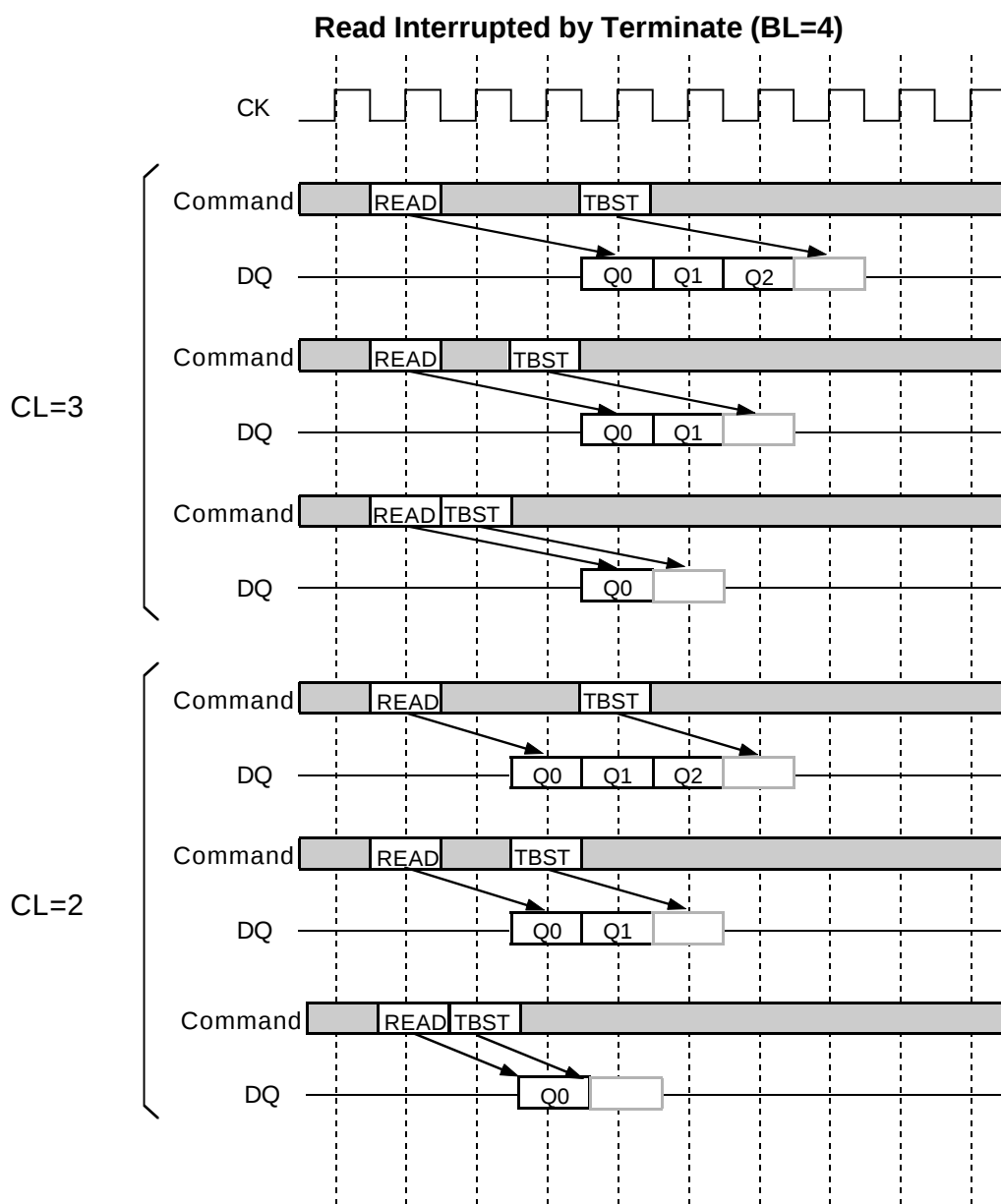


## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

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**[ Read Interrupted by Burst Terminate ]**

Similarly to the precharge, burst terminate command can interrupt burst read operation and disable the data output. The terminated bank remains active, READ to TBST interval is minimum of 1 CK. A TBST command to output disable latency is equivalent to the /CAS Latency.

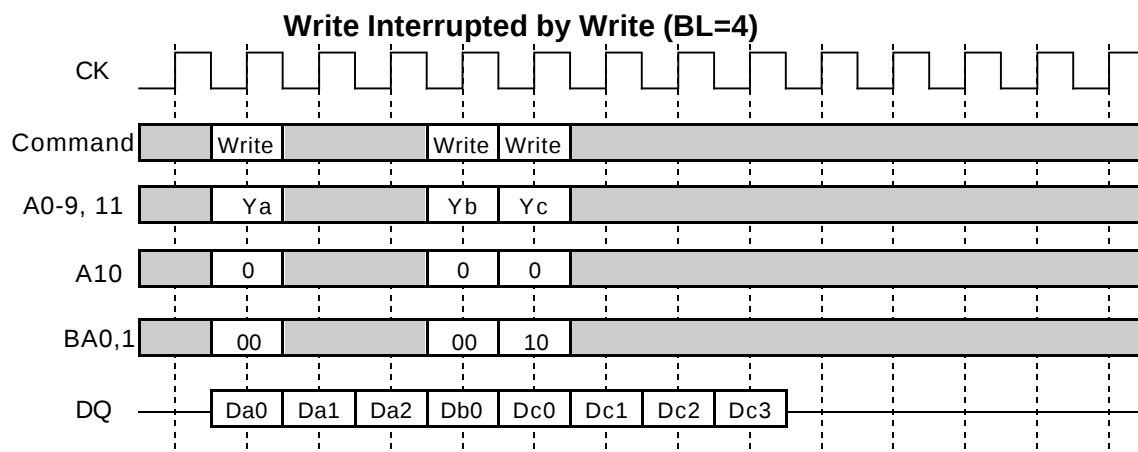


## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

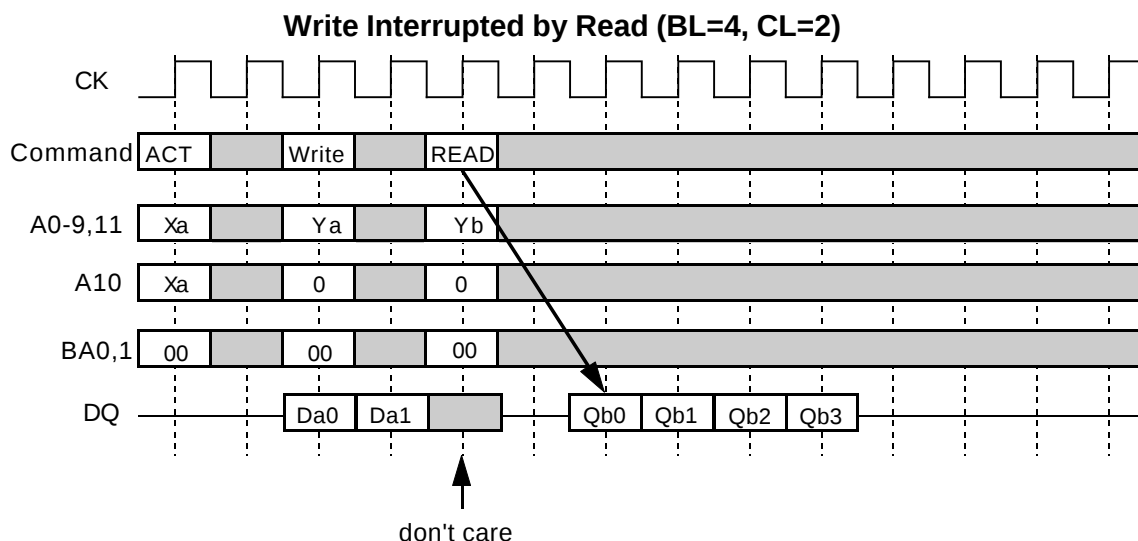
536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

**[ Write Interrupted by Write ]**

Burst write operation can be interrupted by new write of any active bank. Random column access is allowed. WRITE to WRITE interval is minimum 1 CK.

**[ Write Interrupted by Read ]**

Burst write operation can be interrupted by read of any active bank. Random column access is allowed. WRITE to READ interval is minimum 1 CK. The input data on DQ at the interrupting READ cycle is "don't care".

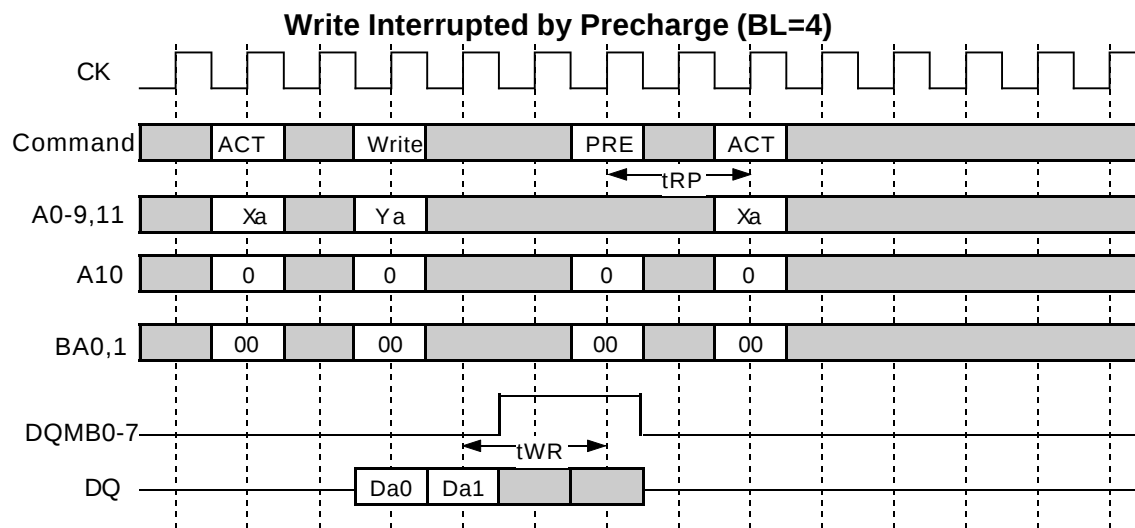


## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

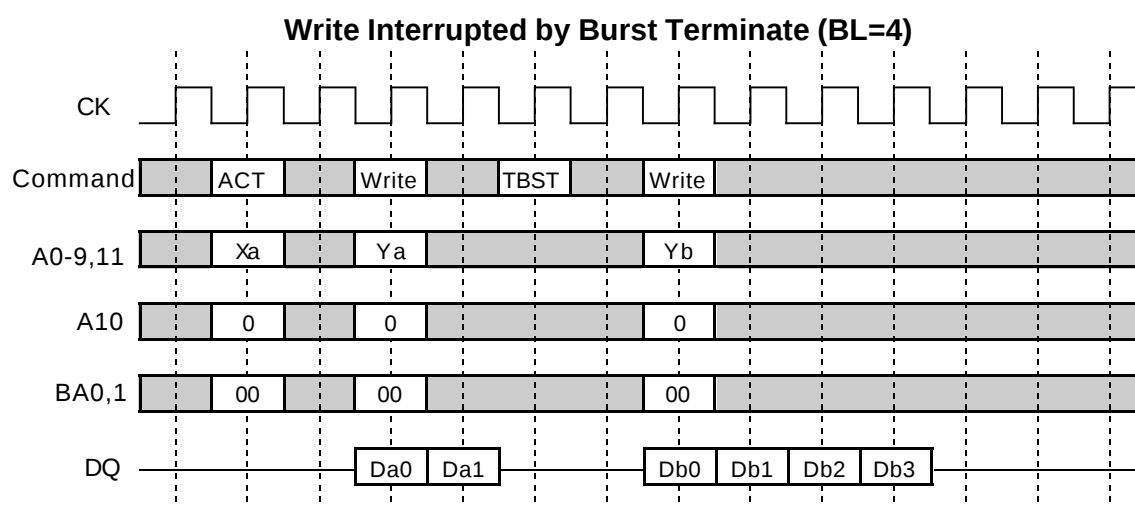
536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

**[ Write Interrupted by Precharge ]**

Burst write operation can be interrupted by precharge of *the same bank*. Write recovery time ( $t_{WR}$ ) is required from the last data to PRE command. During write recovery, data inputs must be masked by DQM.

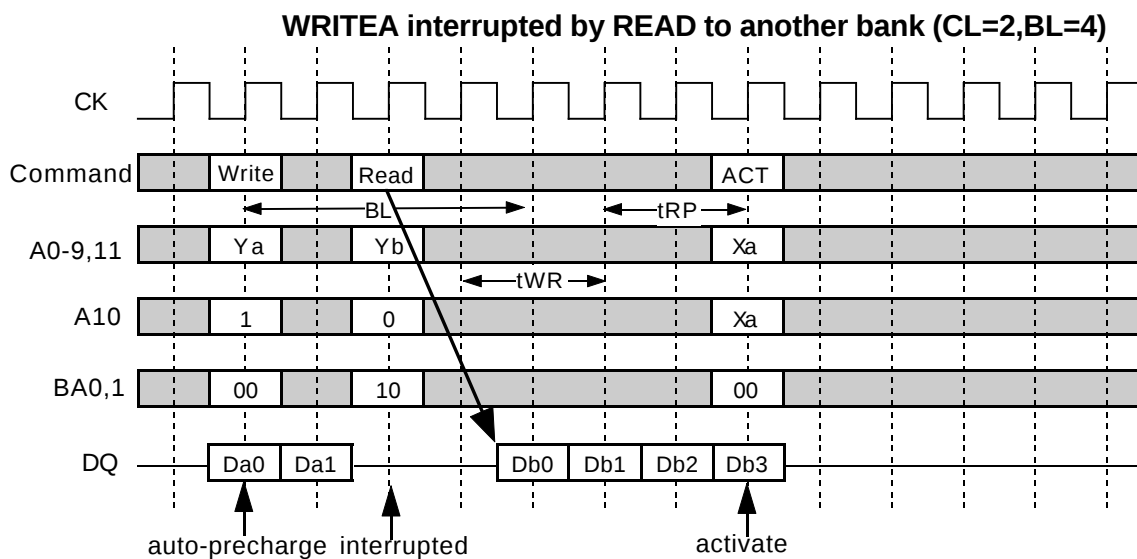
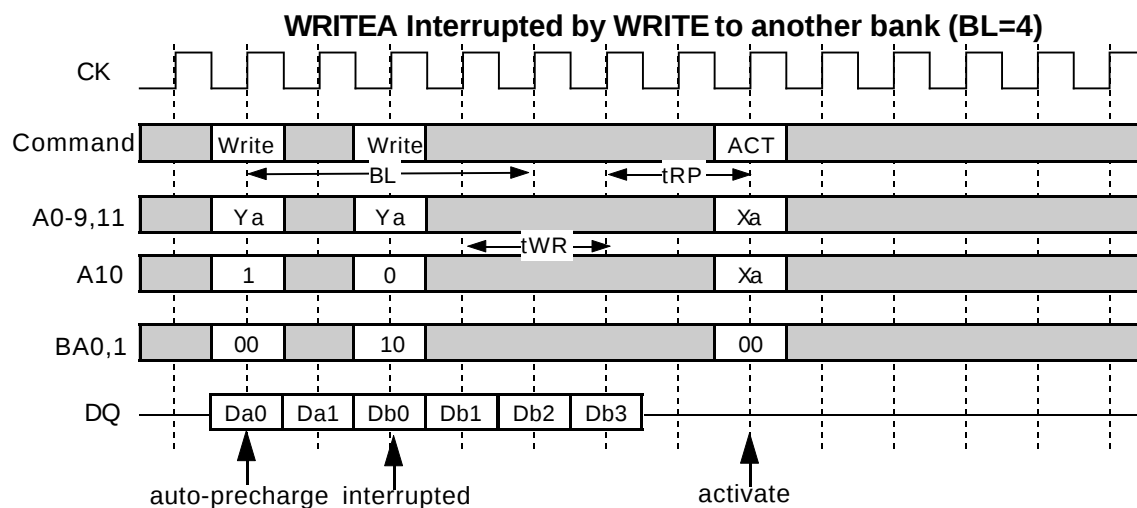
**[ Write Interrupted by Burst Terminate ]**

Burst terminate command can terminate burst write operation. In this case, the write recovery time is not required and the bank remains active. The WRITE to TBST minimum interval is 1CK.



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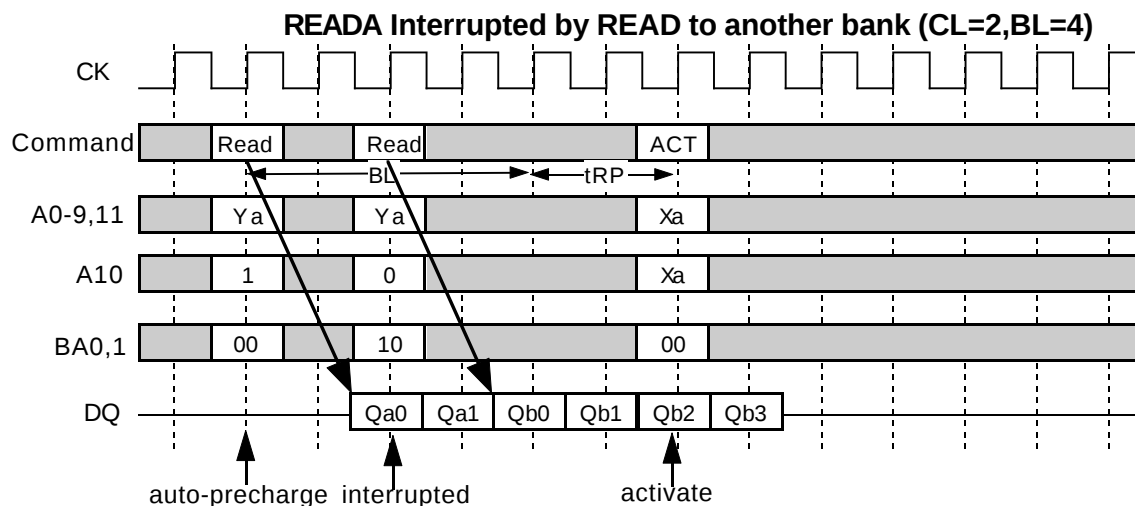
**[ Write with Auto-Precharge interrupted by Write or Read to another Bank ]**Burst write with auto-precharge can be interrupted by write or read to *another bank*.Next ACT command can be issued after  $(BL+tWR-1+tRP)$  from the WRITEA. Auto-precharge interrupted by a command to the same bank is inhibited.

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**[ Read with Auto-Precharge interrupted by Read to another Bank ]**

Burst read with auto-precharge can be interrupted by read to *another bank*. Next ACT command can be issued after (BL+tRP) from the READA. Auto-precharge interrupted by a command to the same bank is inhibited.

**Full Page Burst**

Full page burst length is available for only the sequential burst type. Full page burst read or write is repeated until a Precharge or a Burst Terminate command is issued. In case of the full page burst, a read or write with auto-precharge command is illegal.

**Single Write**

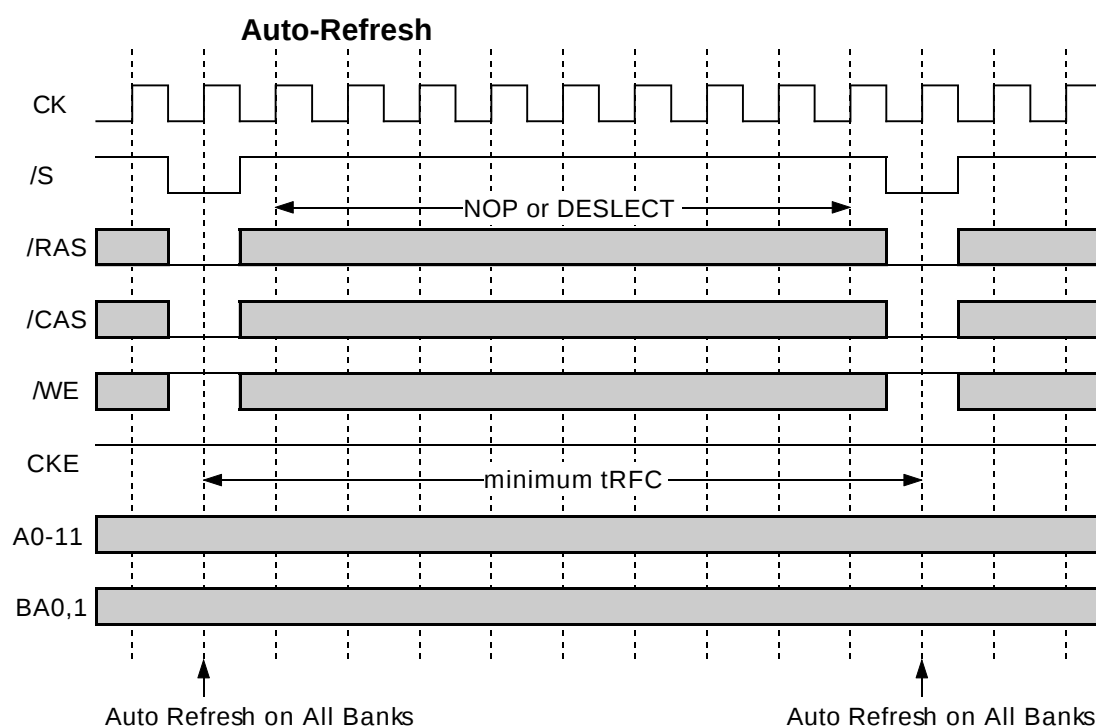
When single write mode is set, burst length for write is always one, independently of Burst Length defined by (A2-0).

**MH8S64DBKG -6,-6L-7,-7L,-8,-8L**

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

**AUTO REFRESH**

Single cycle of auto-refresh is initiated with a REFA(/CS=/RAS=/CAS=L, /WE=/CKE=H) command. The refresh address is generated internally. 4096 REFA cycle within 64ms refresh 64Mbit memory cells. The auto-refresh is performed on 4banks concurrently. Before performing an auto-refresh, all banks must be in the idle state. Auto-refresh to auto-refresh interval is minimum tRFC. Any command must not be issued before tRFC from the REFA command.

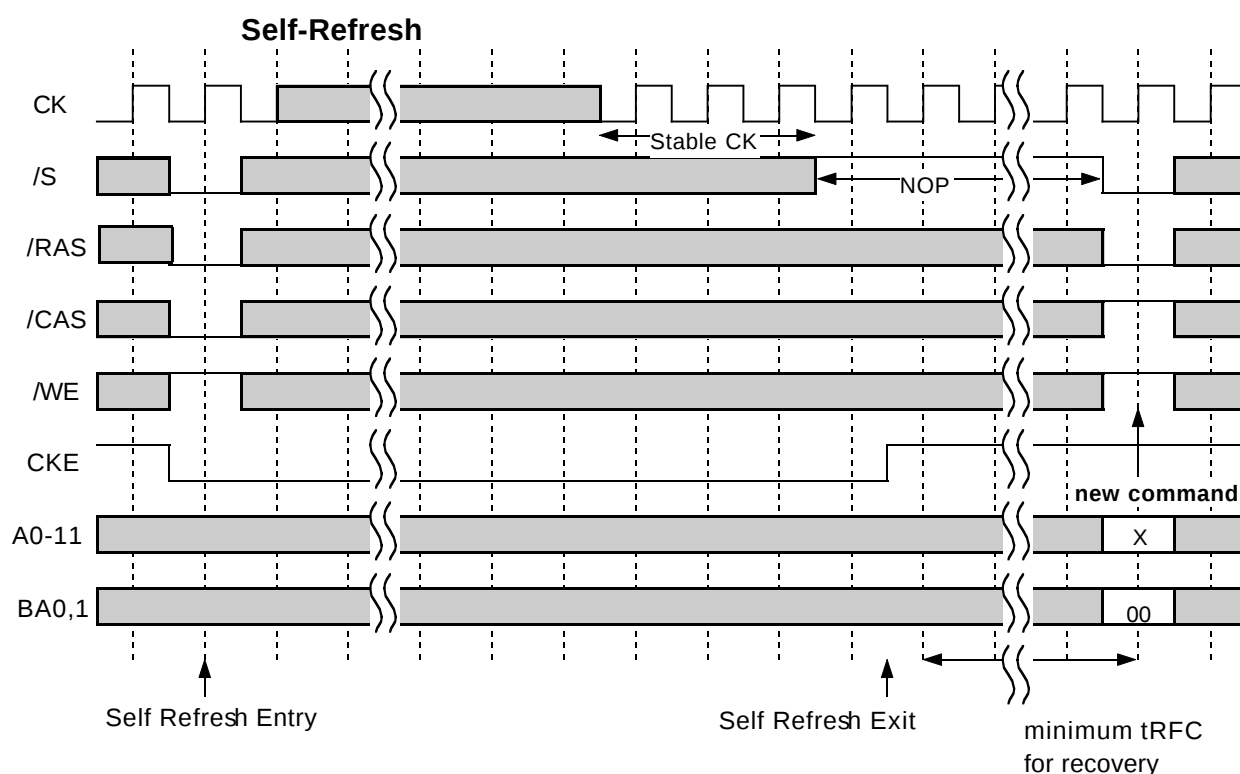


## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

**SELF REFRESH**

Self-refresh mode is entered by issuing a REFS command ( $/CS=/RAS=/CAS=L$ ,  $/WE=H$ ,  $CKE=L$ ). Once the self-refresh is initiated, it is maintained as long as  $CKE$  is kept low. During the self-refresh mode,  $CKE$  is asynchronous and the only enabled input, all other inputs including  $CK$  are disabled and ignored, so that power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable  $CK$  inputs, asserting  $DESEL$  or  $NOP$  command and then asserting  $CKE=H$ . After  $tRFC$  from the 1st  $CK$  edge following  $CKE=H$ , all banks are in the idle state and a new command can be issued after, but  $DESEL$  or  $NOP$  commands must be asserted till then.

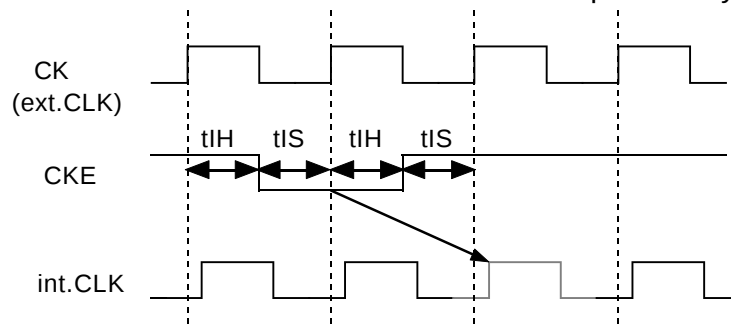
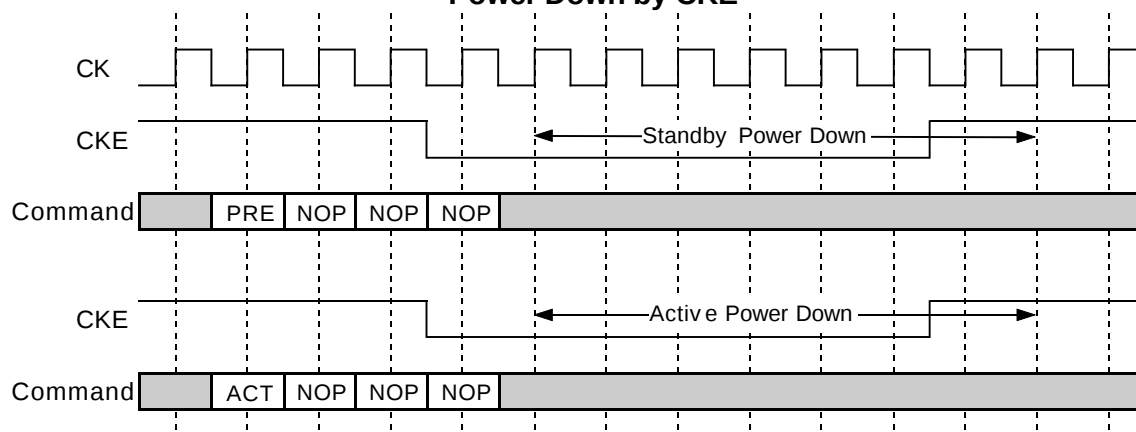
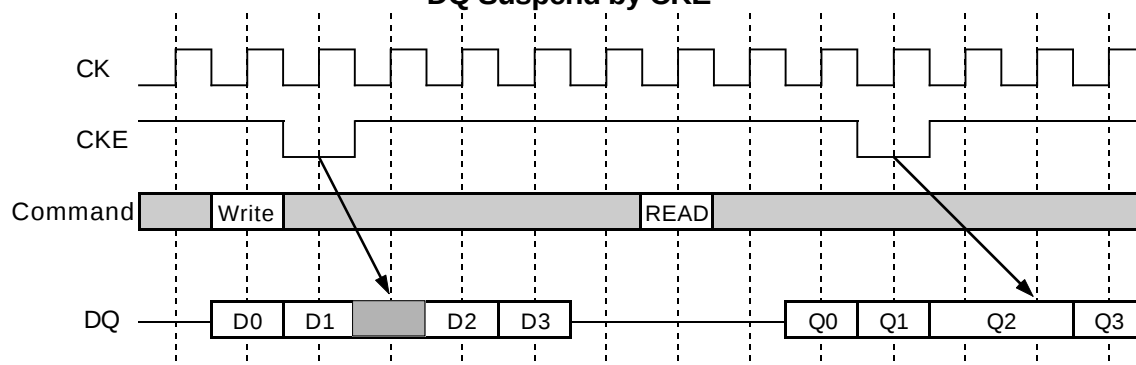


**MH8S64DBKG -6,-6L-7,-7L,-8,-8L**

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

**CLK SUSPEND and POWER DOWN**

CKE controls the internal CLK at the following cycle. Figure below shows how CKE works. By negating CKE, the next internal CLK is suspended. The purpose of CLK suspend is power down, output suspend or input suspend. CKE is a synchronous input except during the self-refresh mode. CLK suspend can be performed either when the banks are active or idle. A command at the suspended cycle is ignored.

**Power Down by CKE****DQ Suspend by CKE**

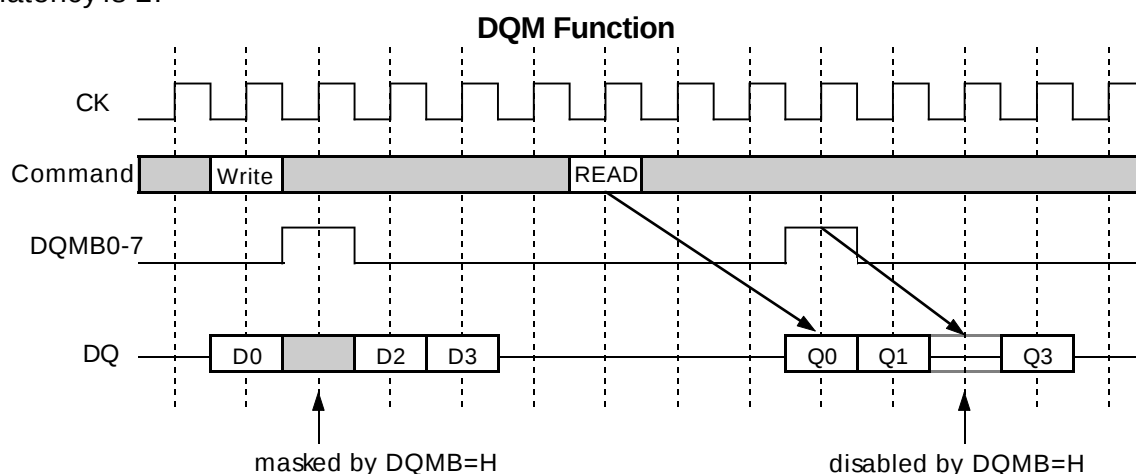
**MH8S64DBKG -6,-6L-7,-7L,-8,-8L**

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

**DQM CONTROL**

DQMB0-7 is a dual function signal defined as the data mask for writes and the output disable for reads. During writes, DQMB0-7 masks input data word by word. DQMB0-7 to Data In latency is 0.

During reads, DQMB0-7 forces output to Hi-Z word by word. DQMB0-7 to output Hi-Z latency is 2.



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536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

**ABSOLUTE MAXIMUM RATINGS**

| Symbol | Parameter             | Condition           | Ratings        | Unit |
|--------|-----------------------|---------------------|----------------|------|
| Vdd    | Supply Voltage        | with respect to Vss | -0.5 ~ 4.6     | V    |
| VI     | Input Voltage         | with respect to Vss | -0.5 ~ Vdd+0.5 | V    |
| VO     | Output Voltage        | with respect to Vss | -0.5 ~ Vdd+0.5 | V    |
| IO     | Output Current        |                     | 50             | mA   |
| Pd     | Power Dissipation     | Ta=25°C             | 8              | W    |
| Topr   | Operating Temperature |                     | 0 ~ 70         | °C   |
| Tstg   | Storage Temperature   |                     | -40 ~ 100      | °C   |

**RECOMMENDED OPERATING CONDITION**

(Ta=0 ~ 70°C, unless otherwise noted)

| Symbol | Parameter                           | Limits |      |         | Unit |
|--------|-------------------------------------|--------|------|---------|------|
|        |                                     | Min.   | Typ. | Max.    |      |
| Vdd    | Supply Voltage                      | 3.0    | 3.3  | 3.6     | V    |
| Vss    | Supply Voltage                      | 0      | 0    | 0       | V    |
| VIH    | High-Level Input Voltage all inputs | 2.0    |      | Vdd+0.3 | V    |
| VIL    | Low-Level Input Voltage all inputs  | -0.3   |      | 0.8     | V    |

Note)

1: VIH(max)=5.5V for pulse width less than 10ns.

2: VIL(min)=-1.0 for pulse width less than 10ns.

**CAPACITANCE**

(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

| Symbol | Parameter                      | Test Condition                     | Limits(max.) | Unit |
|--------|--------------------------------|------------------------------------|--------------|------|
| CI(A)  | Input Capacitance, address pin | VI = 1.4V<br>f=1MHz<br>Vi=200mVrms | 45           | pF   |
| CI(C)  | Input Capacitance, control pin |                                    | 45           | pF   |
| CI(K)  | Input Capacitance, CK pin      |                                    | 35           | pF   |
| CI/O   | Input Capacitance, I/O pin     |                                    | 22           | pF   |

**MH8S64DBKG -6,-6L-7,-7L,-8,-8L**

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

**AVERAGE SUPPLY CURRENT from Vdd**

(Ta=0 ~70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

| Parameter                                                                     | Symbol | Test Condition                                   | Limits<br>(max) |                   | Unit |
|-------------------------------------------------------------------------------|--------|--------------------------------------------------|-----------------|-------------------|------|
|                                                                               |        |                                                  | -6,-6L          | -7,-7L,<br>-8,-8L |      |
| operating current<br>one bank active (discrete)                               | Icc1   | tRC=min.tCLK=min, BL=1,CL=3                      | 460             | 440               | mA   |
| precharge stanby<br>current<br>in power-down mode                             | Icc2P  | CKE=L,tCLK=15ns, /CS>Vcc-0.2V                    | 16              | 16                | mA   |
|                                                                               | Icc2PS | CKE=CLK=L, /CS>Vcc-0.2V                          | 8               | 8                 | mA   |
| precharge stanby current<br>in non power-down mode                            | Icc2N  | CKE=H,tCLK=15ns, VIH>Vcc-0.2V, VIL<0.2V          | 160             | 160               | mA   |
|                                                                               | Icc2NS | CKE=H,CLK=L, VIH>Vcc-0.2V, VIL<0.2V(fixed)       | 120             | 120               | mA   |
| active stanby current<br>in non power-down mode<br>one bank active (discrete) | Icc3N  | CKE=H,tCLK=15ns                                  | 240             | 240               | mA   |
|                                                                               | Icc3NS | CKE=H,CLK=L                                      | 200             | 200               | mA   |
| burst current                                                                 | Icc4   | tCLK=min, BL=4, CL=3,all banks active (discerte) | 520             | 440               | mA   |
| auto-refresh current                                                          | Icc5   | tRC=min, tCLK=min                                | 1040            | 880               | mA   |
| self-refresh current                                                          | Icc6   | CKE <0.2V                                        | -6,-7,-8        | 8                 | mA   |
|                                                                               |        |                                                  | -6L,-7L,-8L     | 4                 | mA   |

Note)

1: Icc(max) is specified at the output open condition.

2: Input signals are changed one time during 30ns.

**AC OPERATING CONDITIONS AND CHARACTERISTICS**

(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

| Symbol  | Parameter                     | Test Condition        | Limits |      | Unit |
|---------|-------------------------------|-----------------------|--------|------|------|
|         |                               |                       | Min.   | Max. |      |
| VOH(DC) | High-Level Output Voltage(DC) | IOH=-2mA              | 2.4    |      | V    |
| VOL(DC) | Low-Level Output Voltage(DC)  | IOL=2mA               |        | 0.4  | V    |
| IOZ     | Off-state Output Current      | Q floating VO=0 ~ Vdd | -10    | 10   | uA   |
| Ii      | Input Current                 | VIH=0 ~ Vdd+0.3V      | -40    | 40   | uA   |

**MH8S64DBKG -6,-6L-7,-7L,-8,-8L**

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

**AC TIMING REQUIREMENTS (SDRAM Component)**

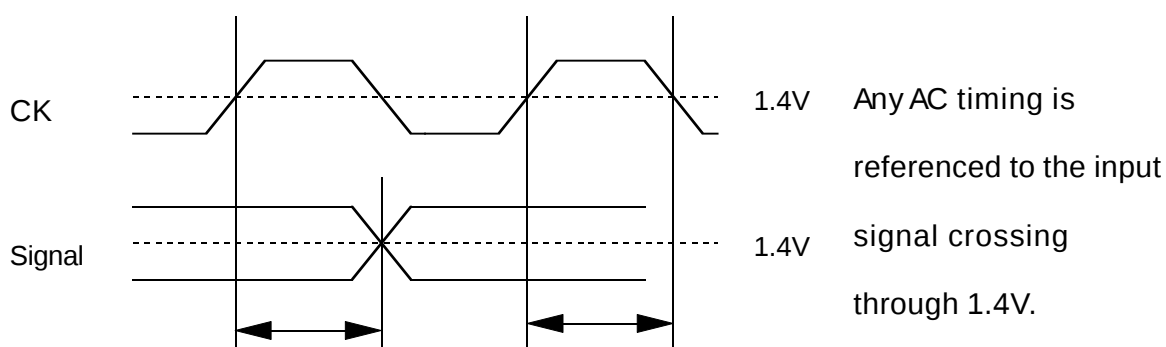
(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

Input Pulse Levels: 0.8V to 2.0V

Input Timing Measurement Level: 1.4V

| Symbol | Parameter                    |      | Limits |      |        |      |        |      | Unit |
|--------|------------------------------|------|--------|------|--------|------|--------|------|------|
|        |                              |      | -6,-6L |      | -7,-7L |      | -8,-8L |      |      |
|        |                              |      | Min.   | Max. | Min.   | Max. | Min.   | Max. |      |
| tCLK   | CK cycle time                | CL=2 | 10     |      | 10     |      | 13     |      | ns   |
|        |                              | CL=3 | 7.5    |      | 10     |      | 10     |      | ns   |
| tCH    | CK High pulse width          |      | 2.5    |      | 3      |      | 3      |      | ns   |
| tCL    | CK Low pilse width           |      | 2.5    |      | 3      |      | 3      |      | ns   |
| tT     | Transition time of CK        |      | 1      | 10   | 1      | 10   | 1      | 10   | ns   |
| tIS    | Input Setup time(all inputs) |      | 1.5    |      | 2      |      | 2      |      | ns   |
| tIH    | Input Hold time(all inputs)  |      | 0.8    |      | 1      |      | 1      |      | ns   |
| tRC    | Row cycle time               |      | 67.5   |      | 70     |      | 70     |      | ns   |
| tRFC   | Refresh Cycle time           |      | 75     |      | 80     |      | 80     |      | ns   |
| tRCD   | Row to Column Delay          |      | 20     |      | 20     |      | 20     |      | ns   |
| tRAS   | Row Active time              |      | 45     | 100K | 50     | 100K | 50     | 100K | ns   |
| tRP    | Row Precharge time           |      | 20     |      | 20     |      | 20     |      | ns   |
| tWR    | Write Recovery time          |      | 12     |      | 12     |      | 12     |      | ns   |
| tRRD   | Act to Act Deley time        |      | 15     |      | 20     |      | 20     |      | ns   |
| tRSC   | Mode Register Set Cycle time |      | 10     |      | 10     |      | 10     |      | ns   |
| tREF   | Refresh Interval time        |      |        | 64   |        | 64   |        | 64   | ms   |

Note:1 The timing requirements are assumed tT=1ns. If tT is longer than 1ns, (tT-1)ns should be added to the parameter.



**MH8S64DBKG -6,-6L-7,-7L,-8,-8L**

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

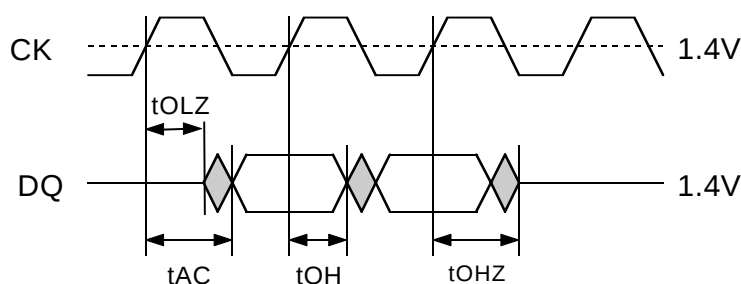
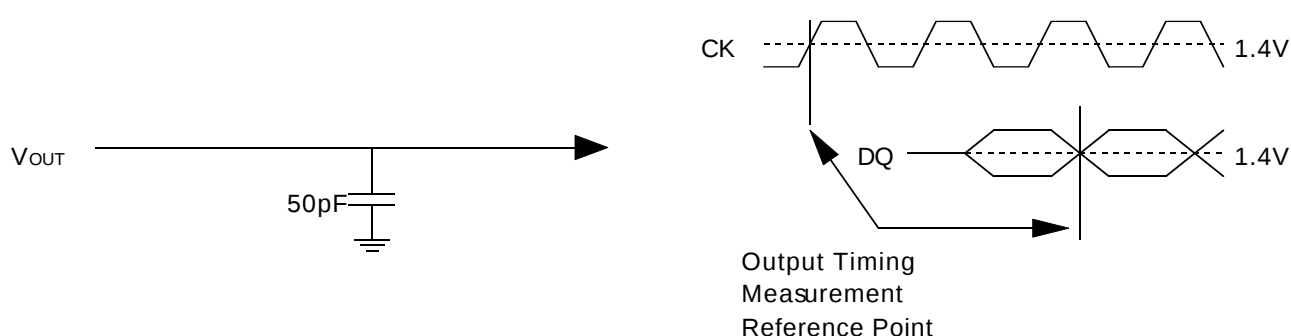
**SWITCHING CHARACTERISTICS (SDRAM Component)**

(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise note3)

| Symbol | Parameter                                 |      | Limits |      |        |      |        |      | Unit |
|--------|-------------------------------------------|------|--------|------|--------|------|--------|------|------|
|        |                                           |      | -6,-6L |      | -7,-7L |      | -8,-8L |      |      |
|        |                                           |      | Min.   | Max. | Min.   | Max. | Min.   | Max. |      |
| tAC    | Access time from CK                       | CL=2 |        | 6    |        | 6    |        | 7    | ns   |
|        |                                           | CL=3 |        | 5.4  |        | 6    |        | 6    | ns   |
| tOH    | Output Hold time from CK                  | CL=2 | 3      |      | 3      |      | 3      |      | ns   |
|        |                                           | CL=3 | 2.7    |      | 3      |      | 3      |      | ns   |
| tOLZ   | Delay time, output low impedance from CK  |      | 0      |      | 0      |      | 0      |      | ns   |
| tOHZ   | Delay time, output high impedance from CK |      | 2.7    | 5.4  | 3      | 6    | 3      | 6    | ns   |

Note)

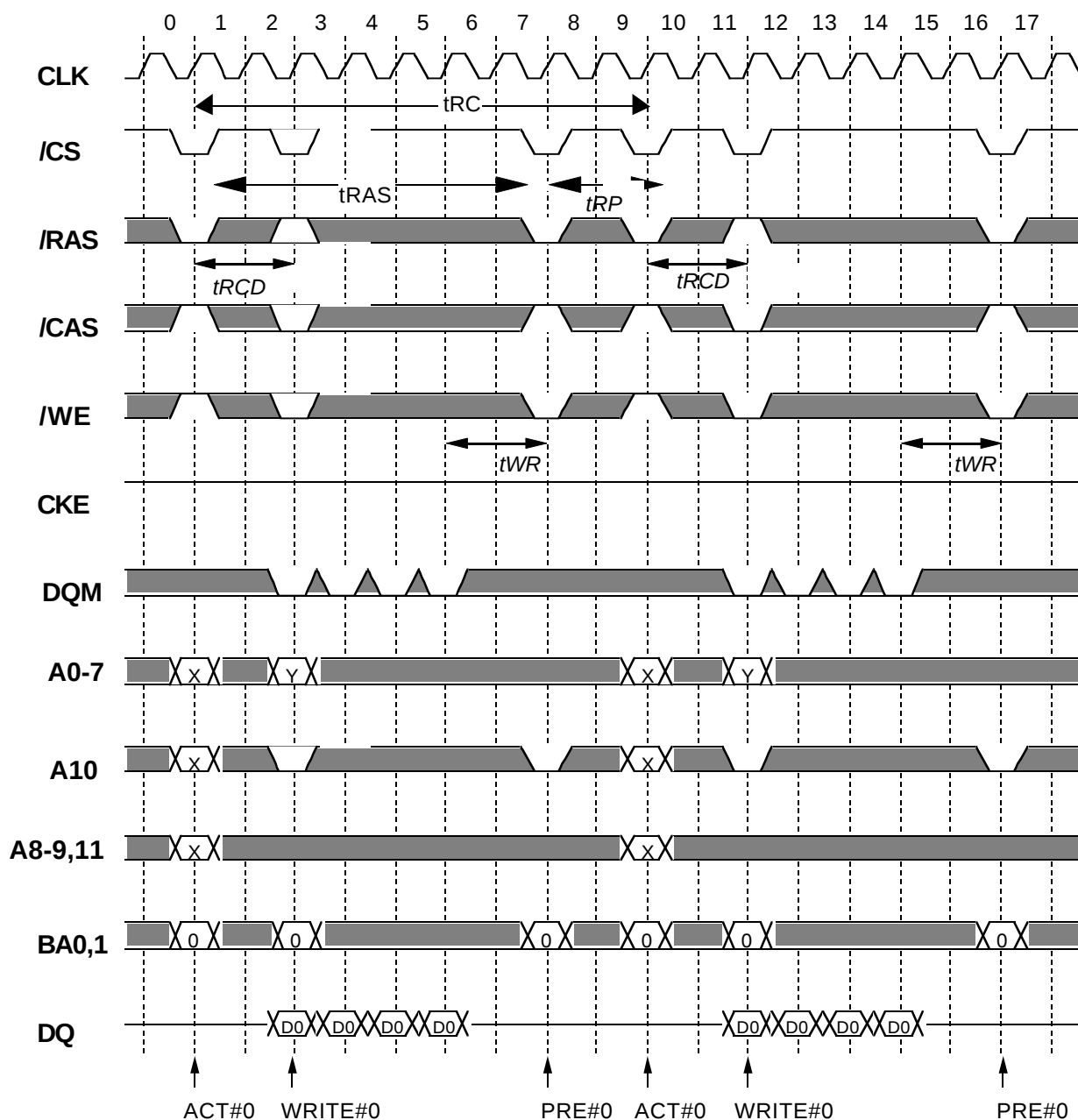
1 If clock rising time is longer than 1ns, (tT/2-0.5)ns should be added to parameter.

**Output Load Condition**

## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

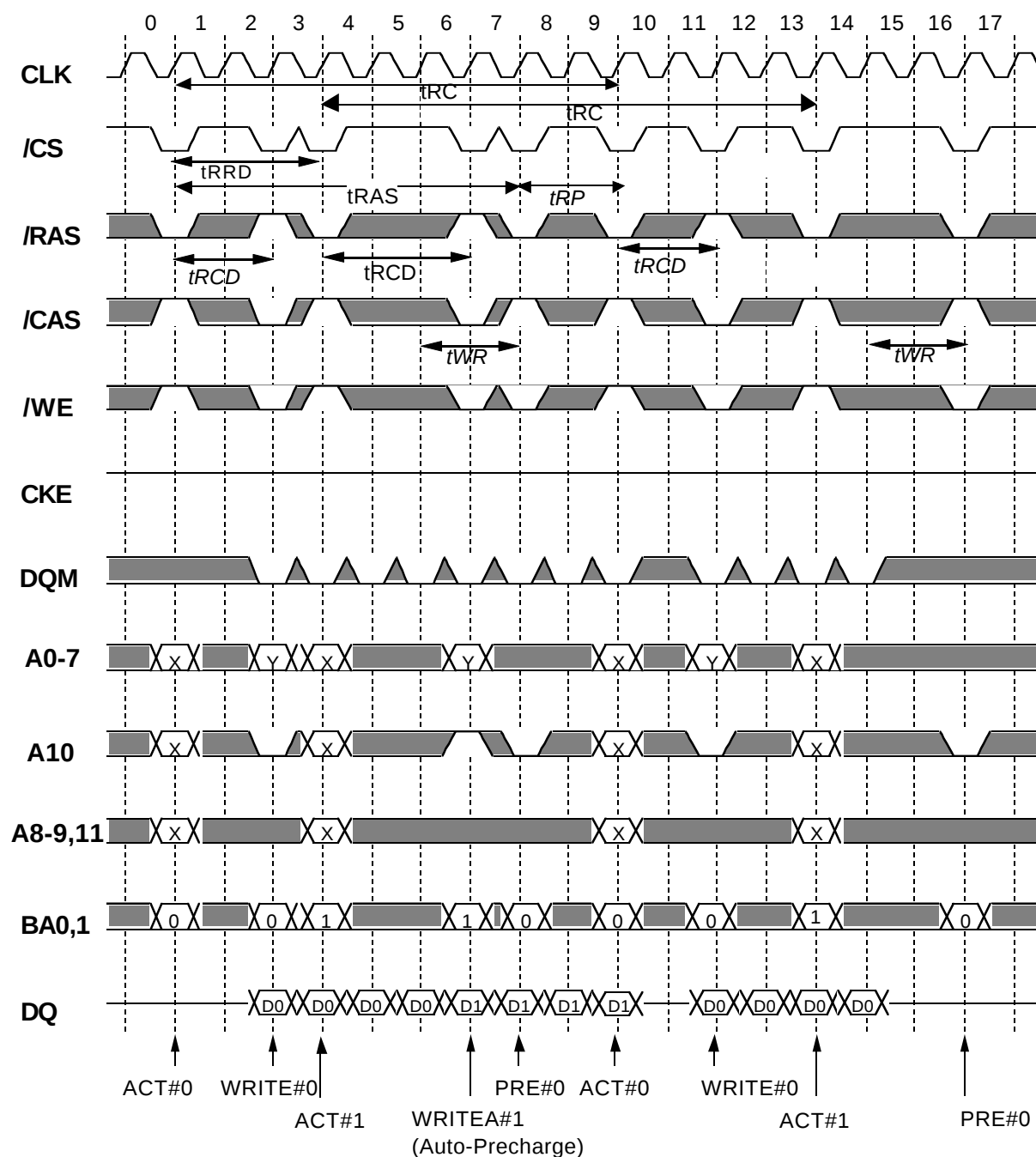
## Burst Write (single bank) @BL=4

*Italic parameter* indicates minimum case

## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

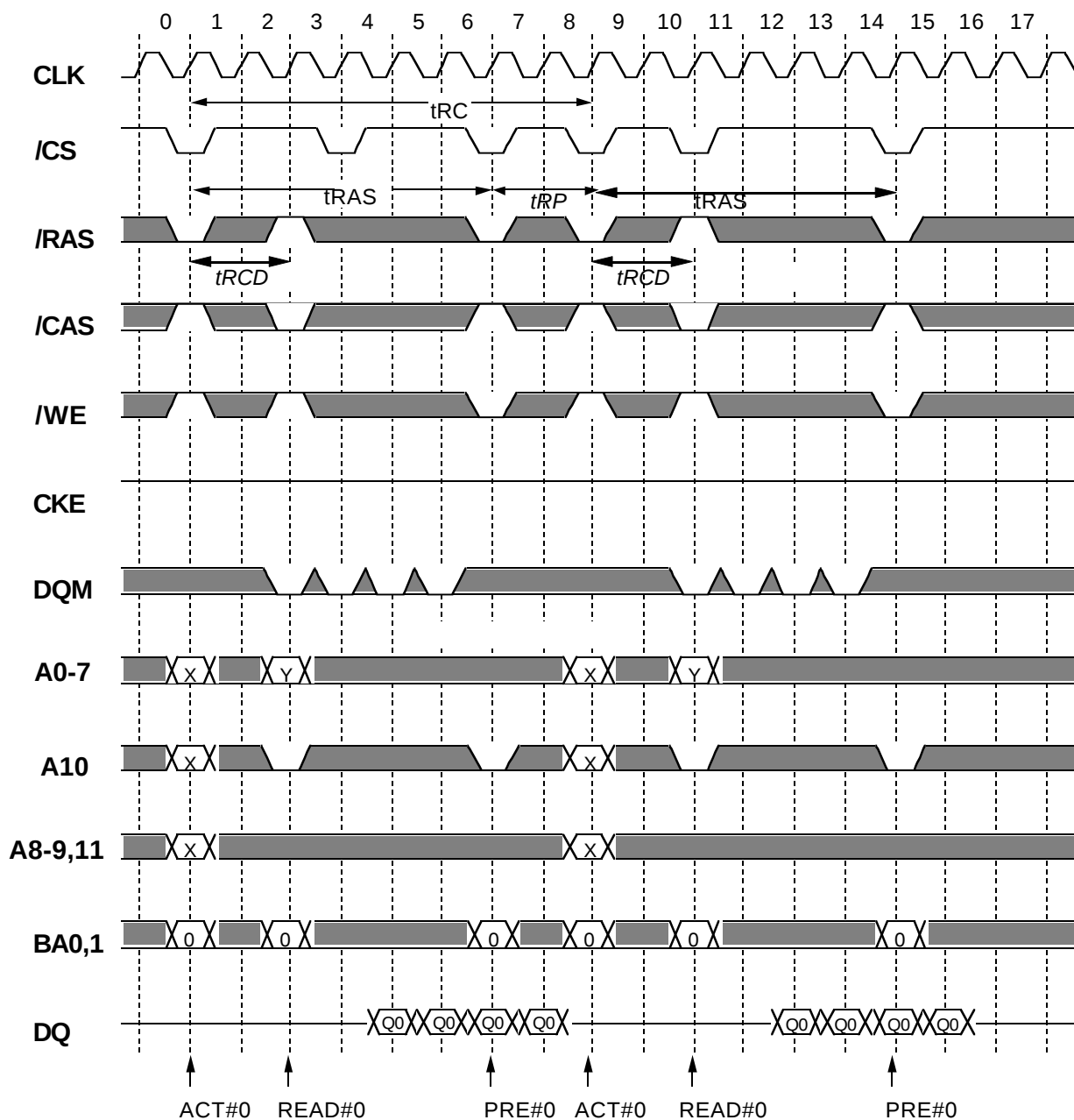
## Burst Write (multi bank) @BL=4

*Italic parameter* indicates minimum case

## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

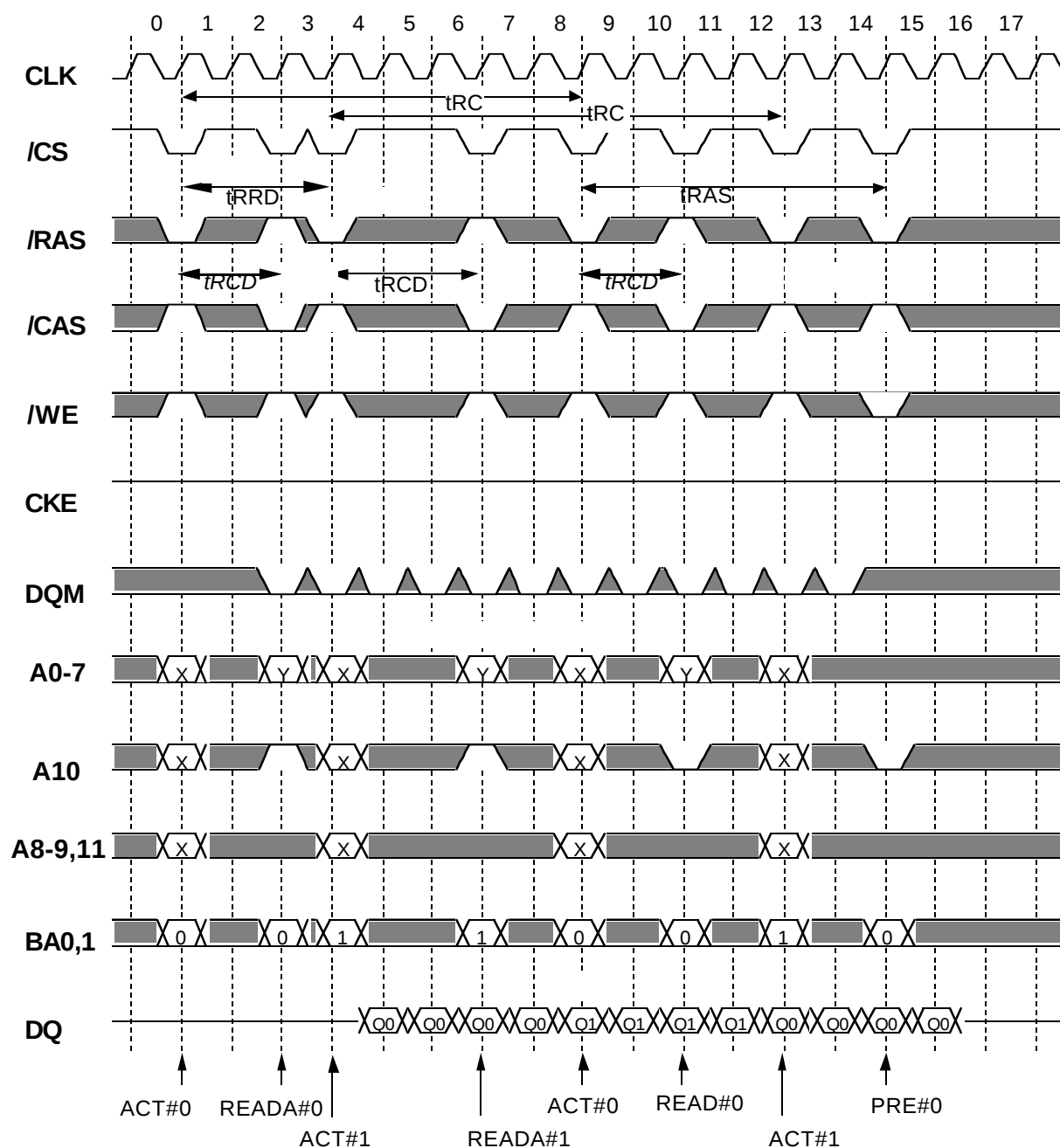
## Burst Read (single bank) @BL=4 CL=2

*Italic parameter* indicates minimum case

## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

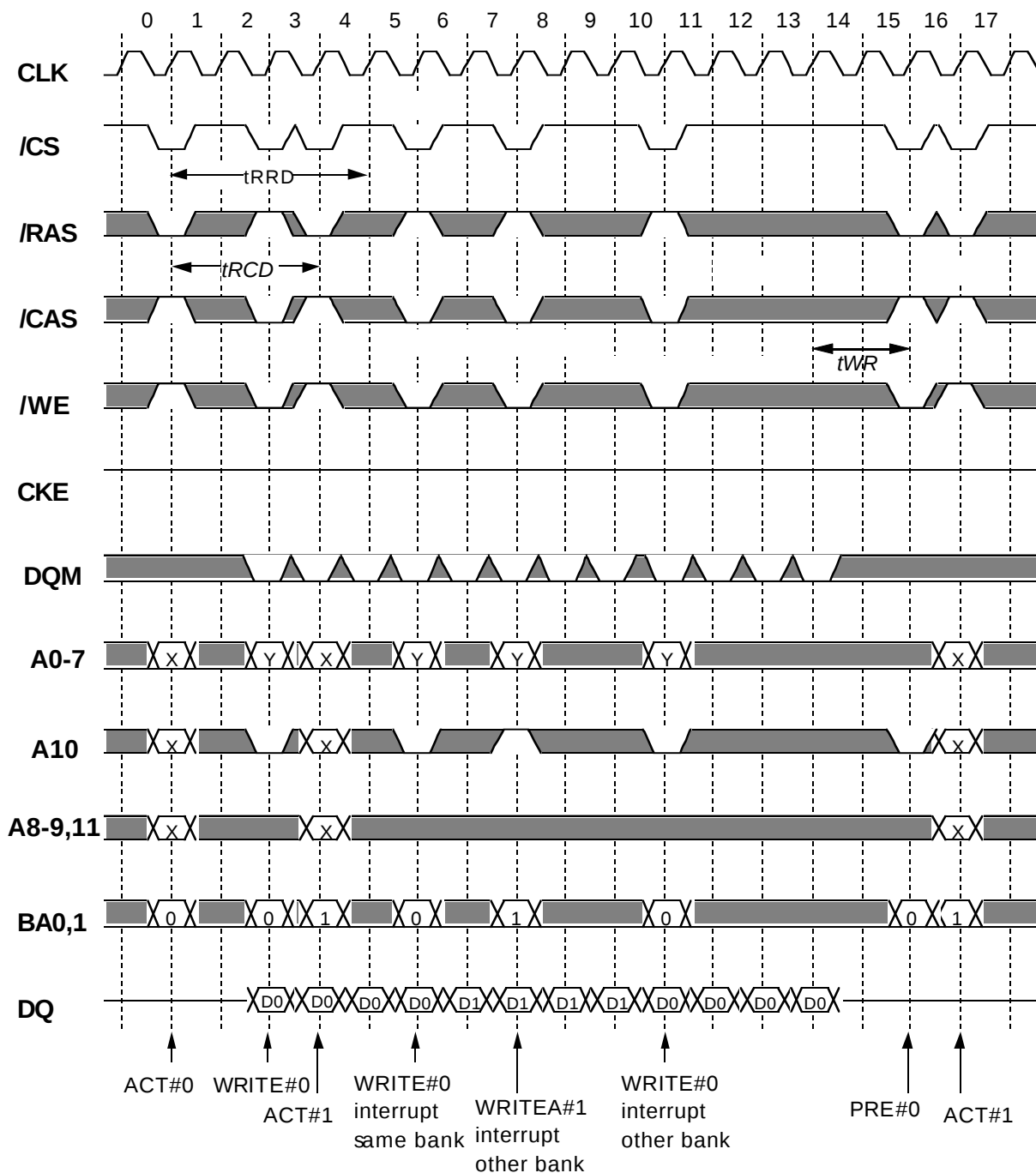
## Burst Read (multiple bank) @BL=4 CL=2

*Italic parameter* indicates minimum case

## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

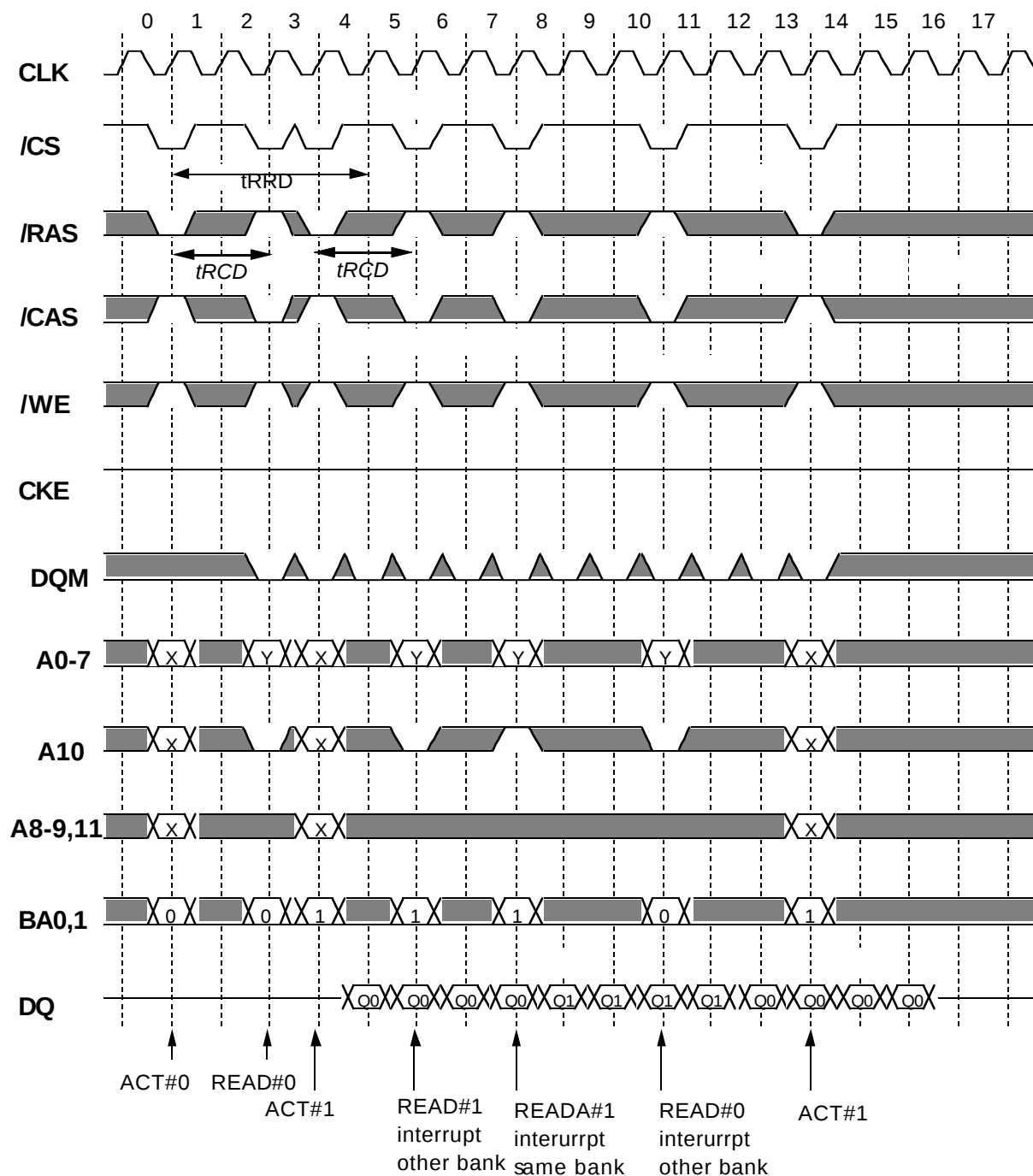
## Write Interrupted by Write @BL=4

*Italic parameter* indicates minimum case

# MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

## Read Interrupted by Read @BL=4 CL=2

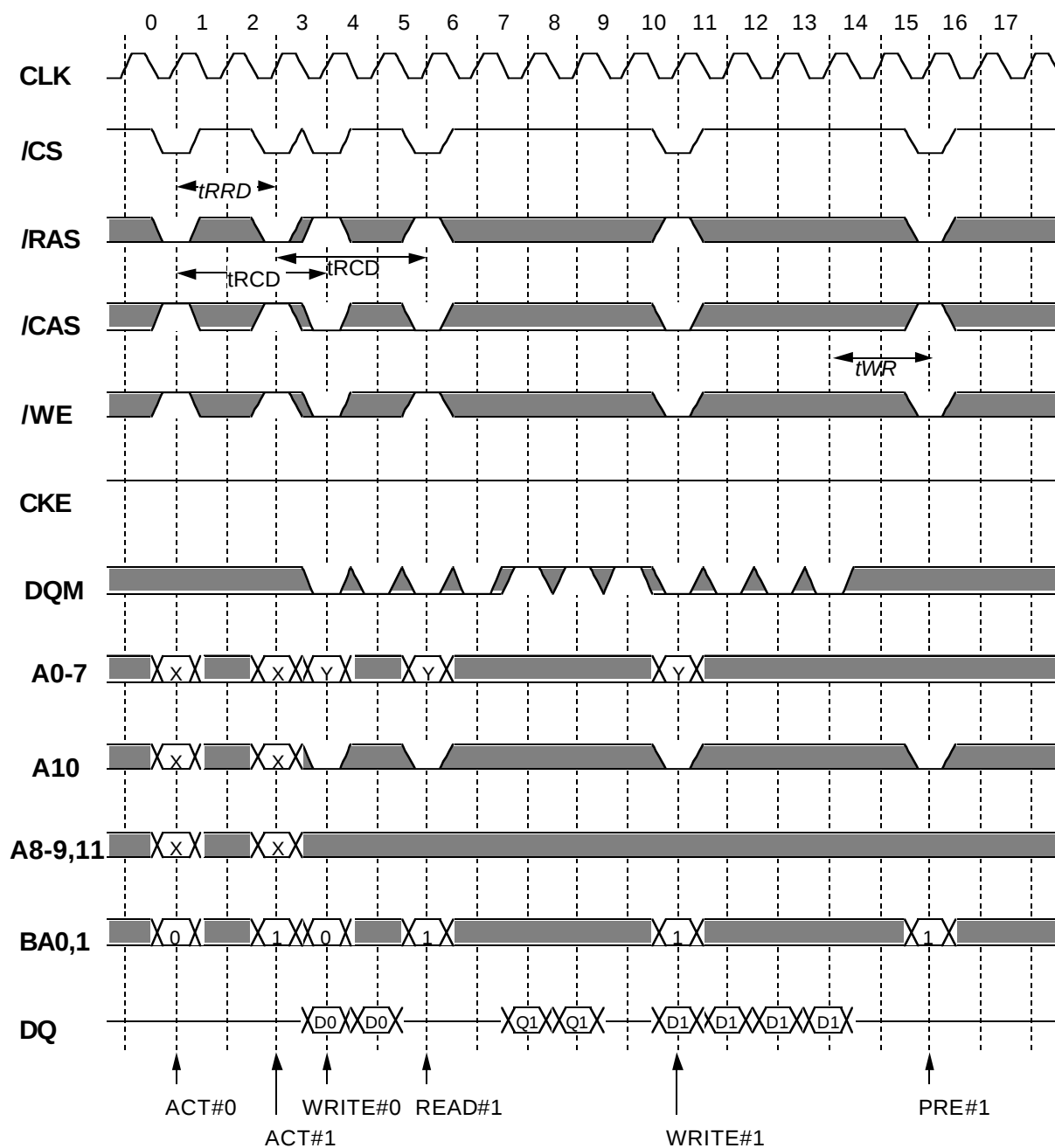


*Italic parameter* indicates minimum case

## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

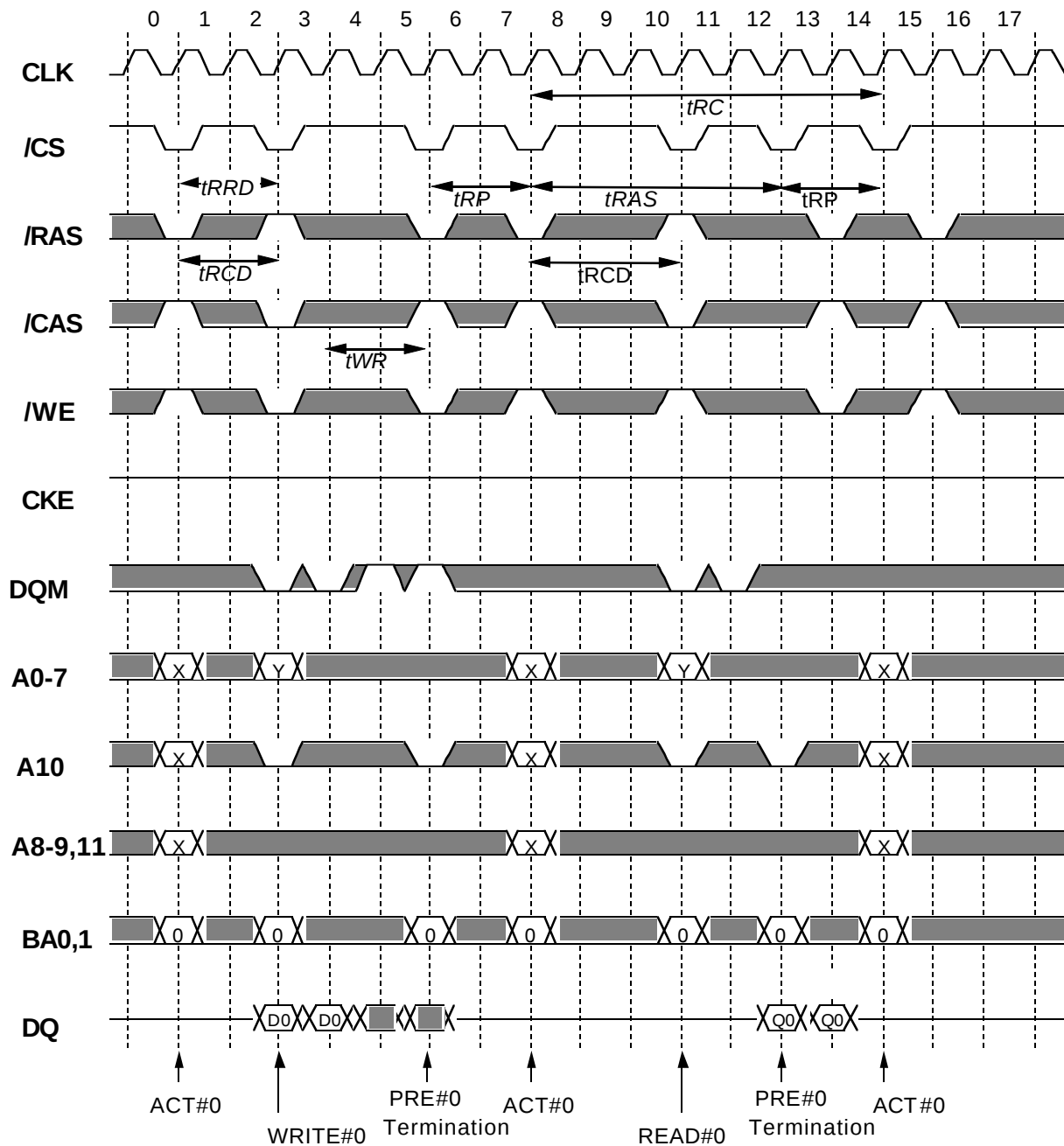
## Write Interrupted by Read, Read Interrupted by Write @BL=4,CL=2

*Italic parameter* indicates minimum case

## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

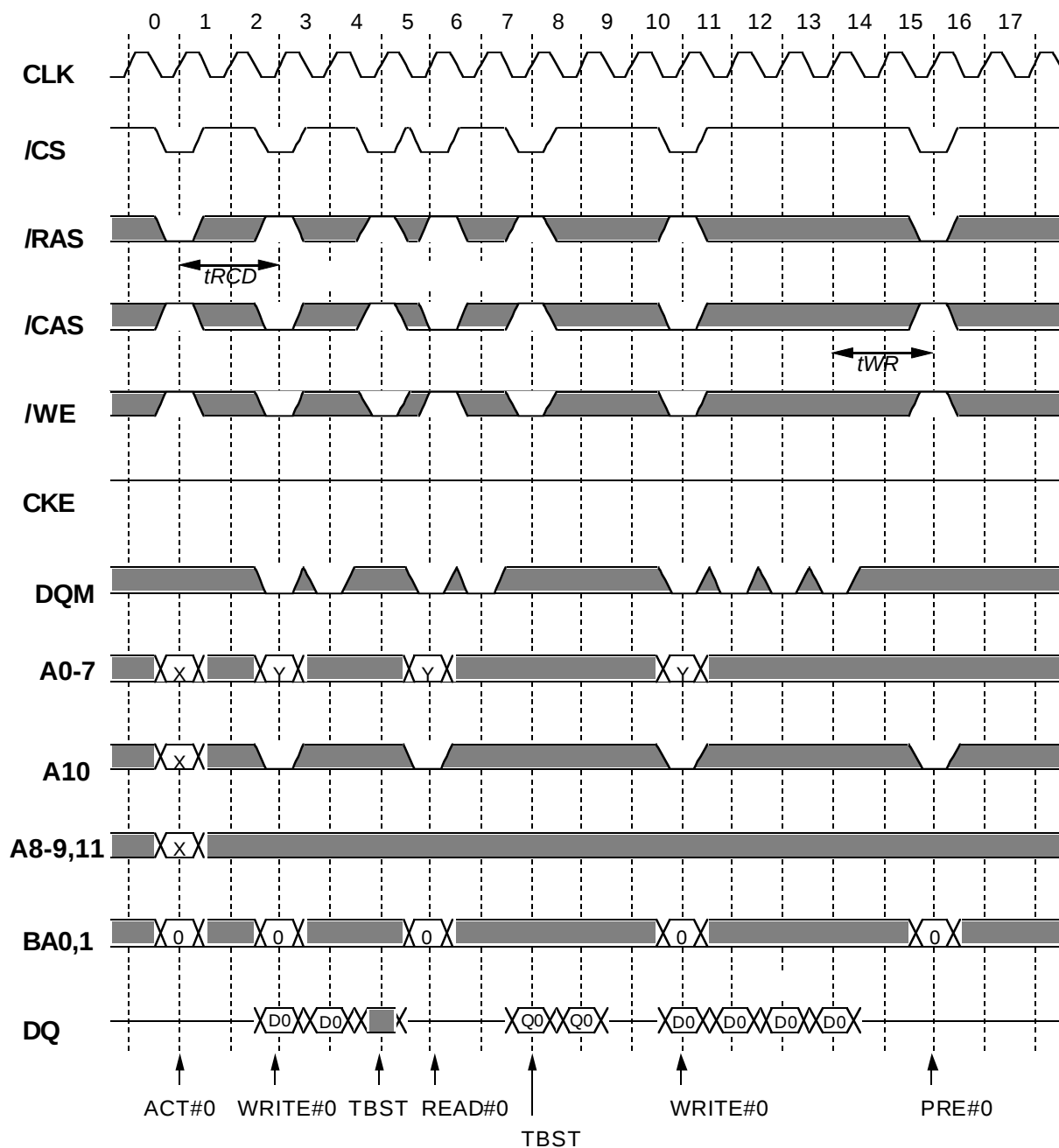
## Write/Read Terminated by Precharge @BL=4 CL=2

*Italic parameter* indicates minimum case

## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

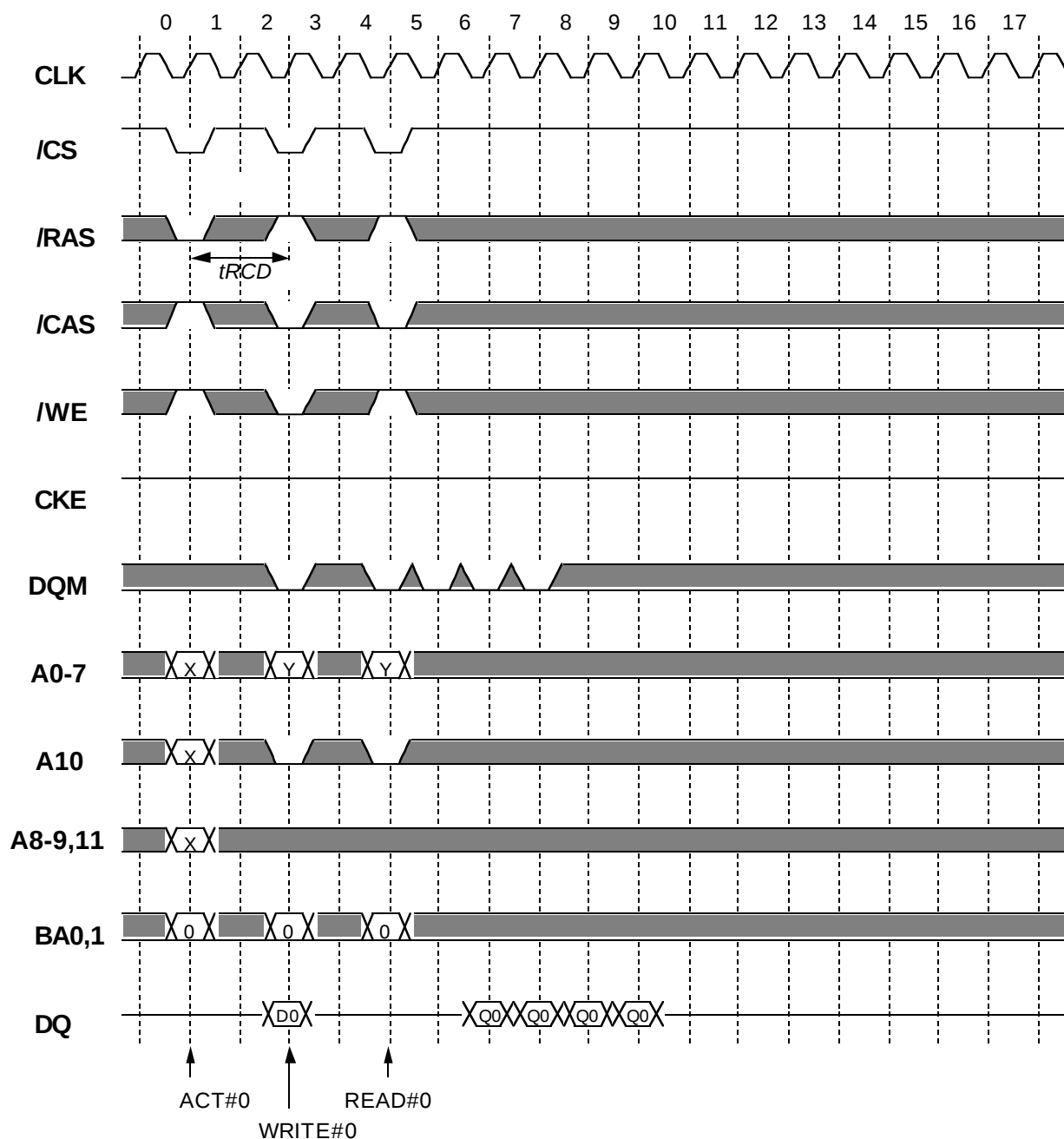
## Write/Read Terminated by Burst Terminate @BL=4,CL=2

*Italic parameter* indicates minimum case

# MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

## Single Write Burst Read @BL=4 CL=2

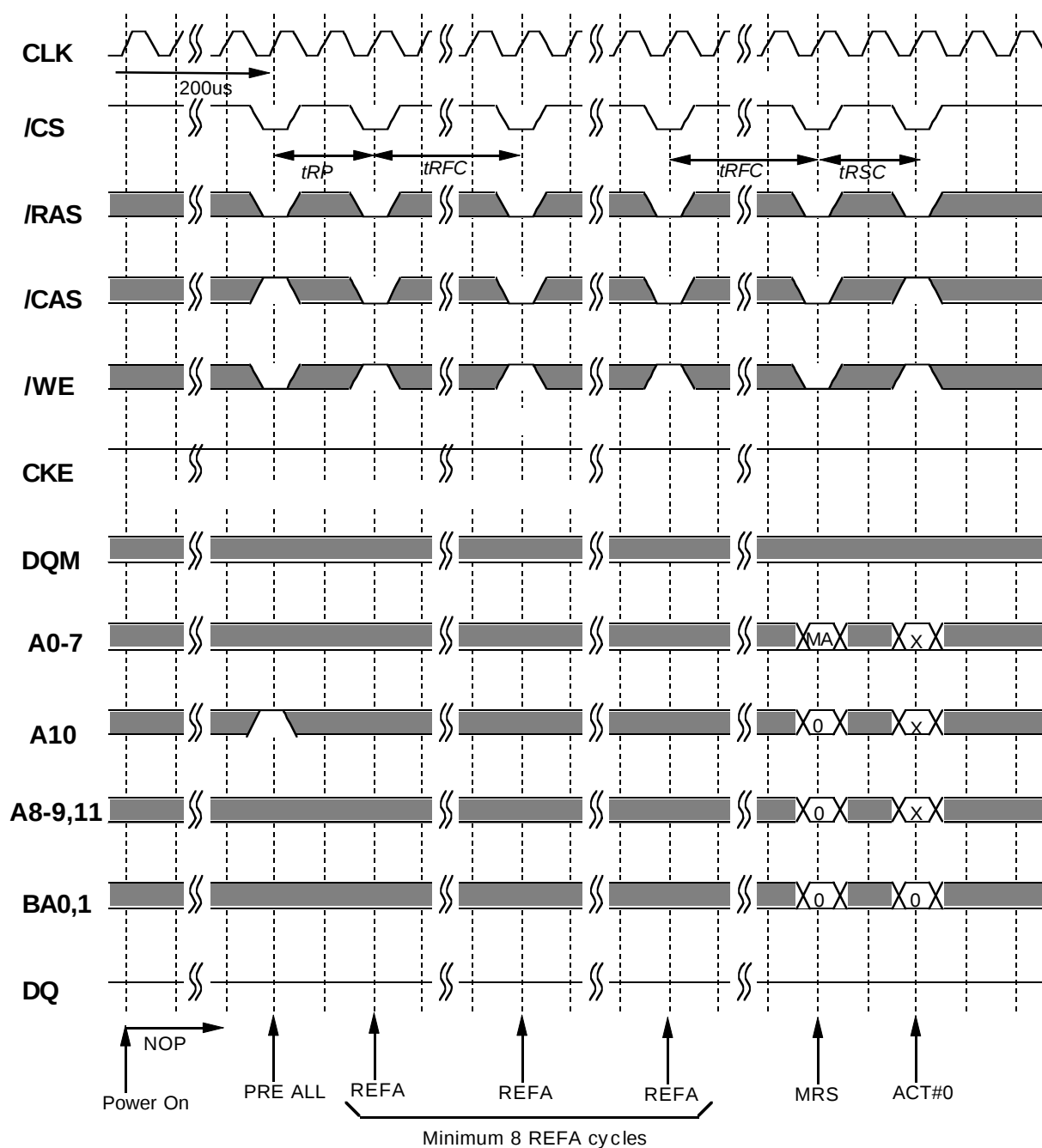


*Italic parameter* indicates minimum case

## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

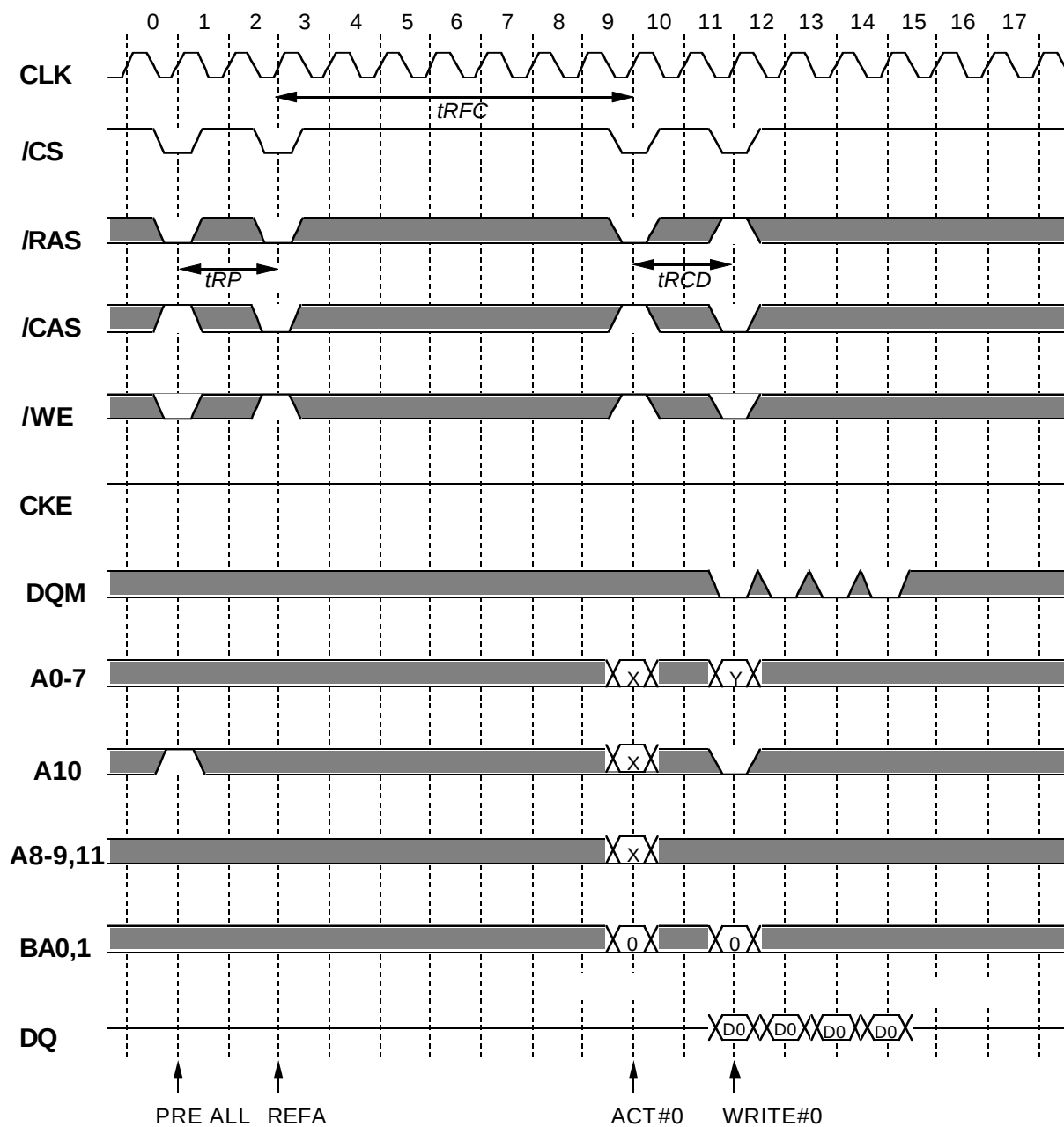
## Power-Up Sequence and Intialize



## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

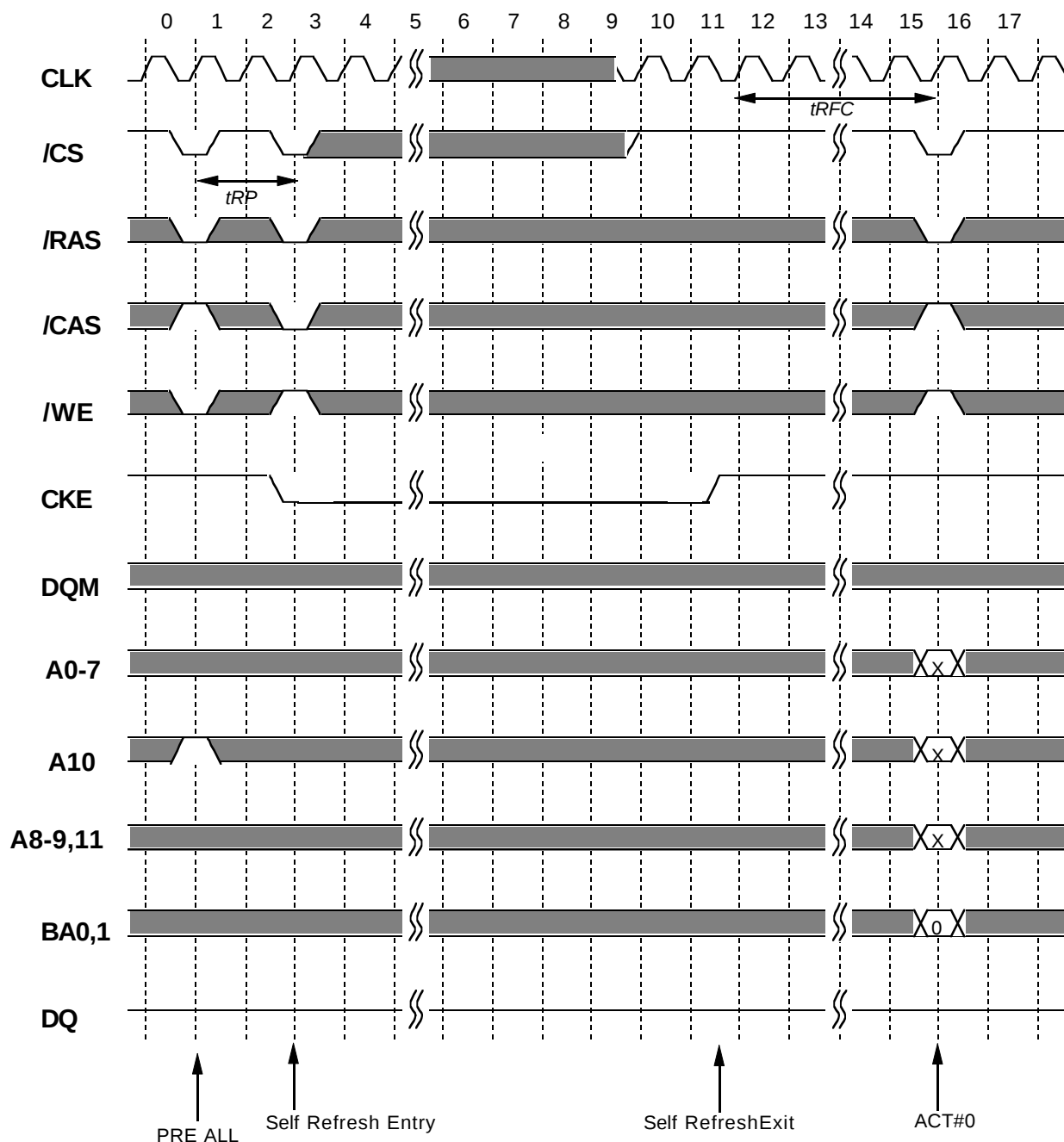
## Auto Refresh

*Italic parameter* indicates minimum case

# MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

## Self Refresh

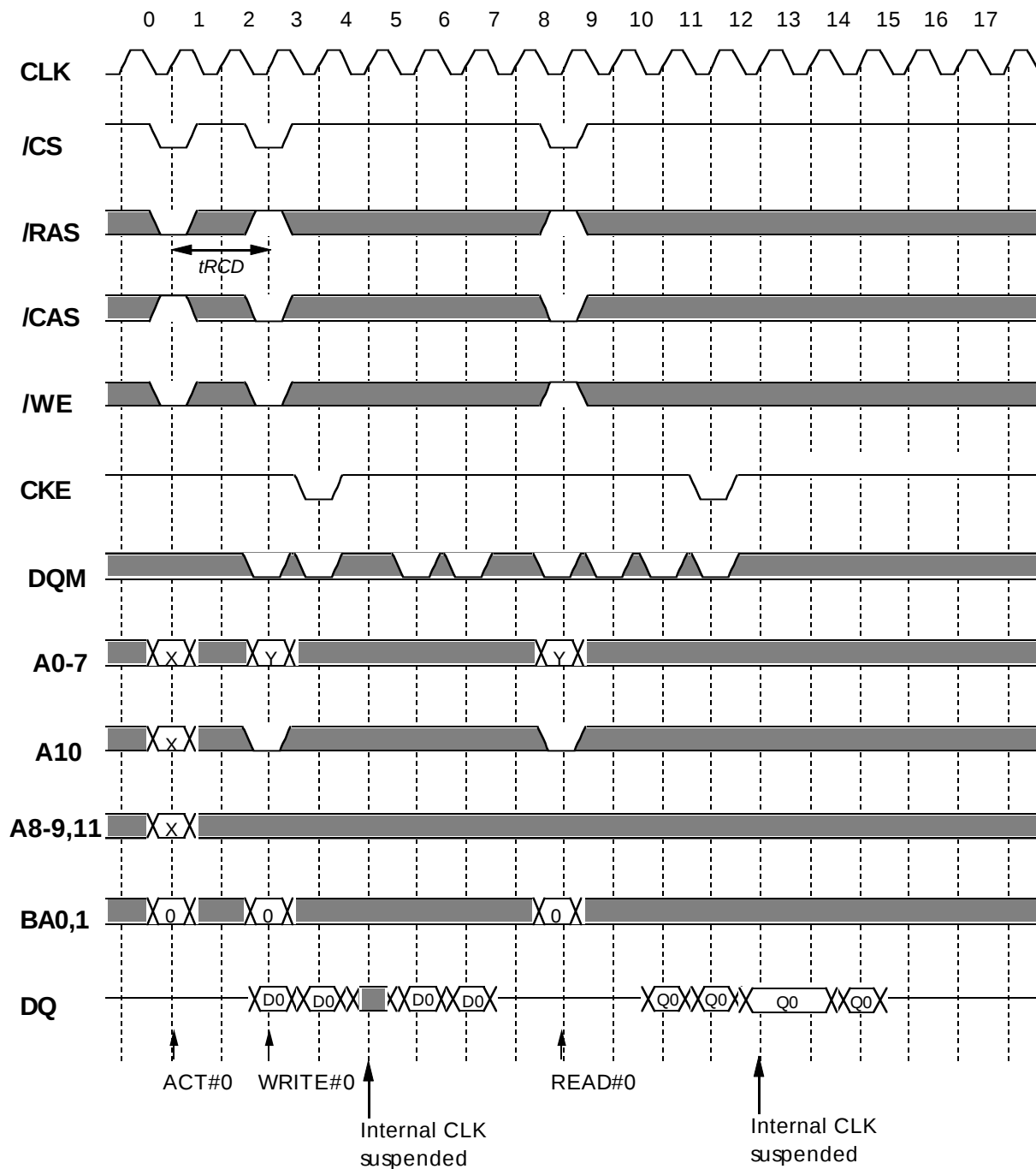


All banks must be idle before REFS is issued.

## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

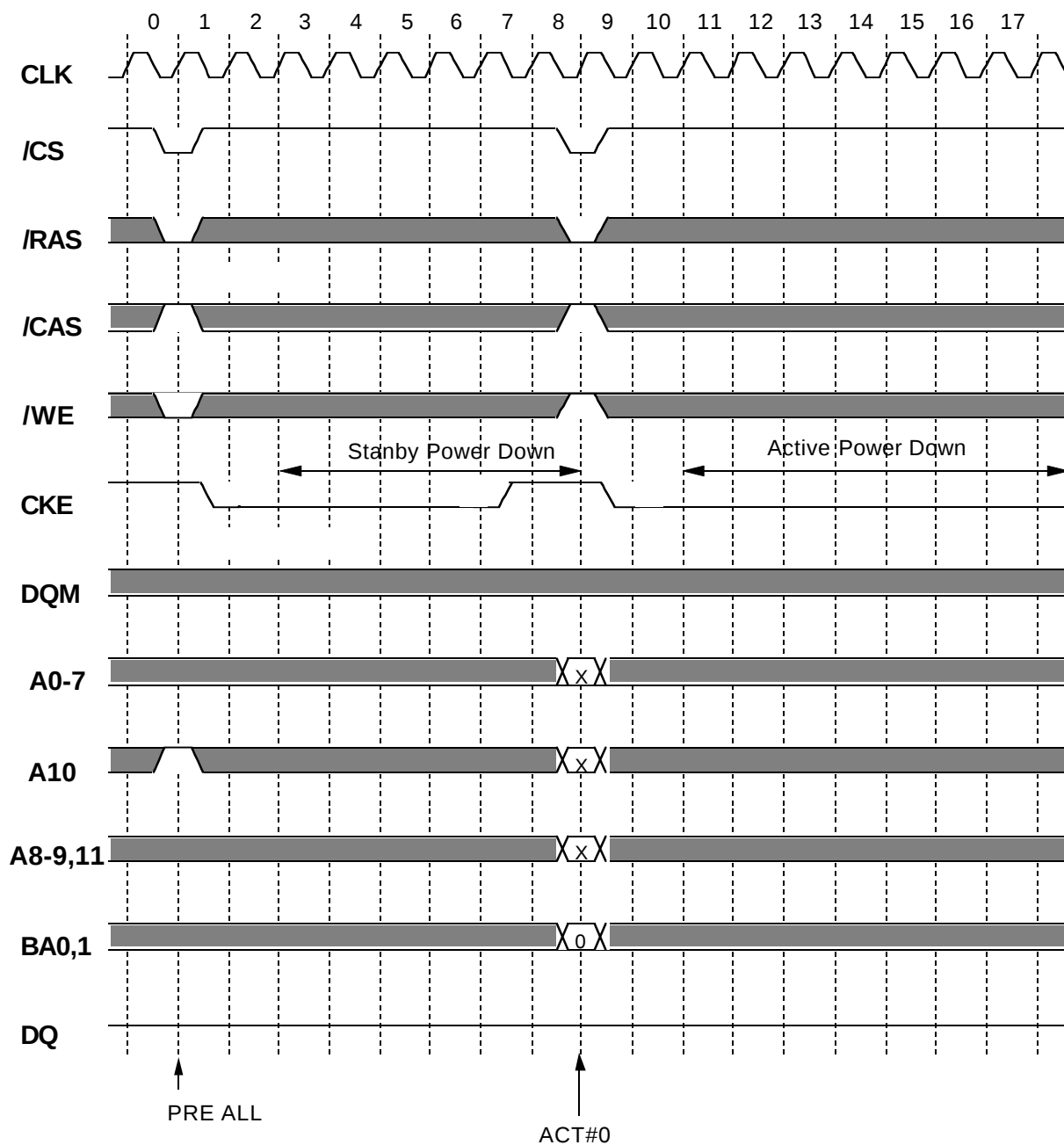
## CLK Suspension @BL=4 CL=2

*Italic parameter* indicates minimum case

# MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

## Power Down

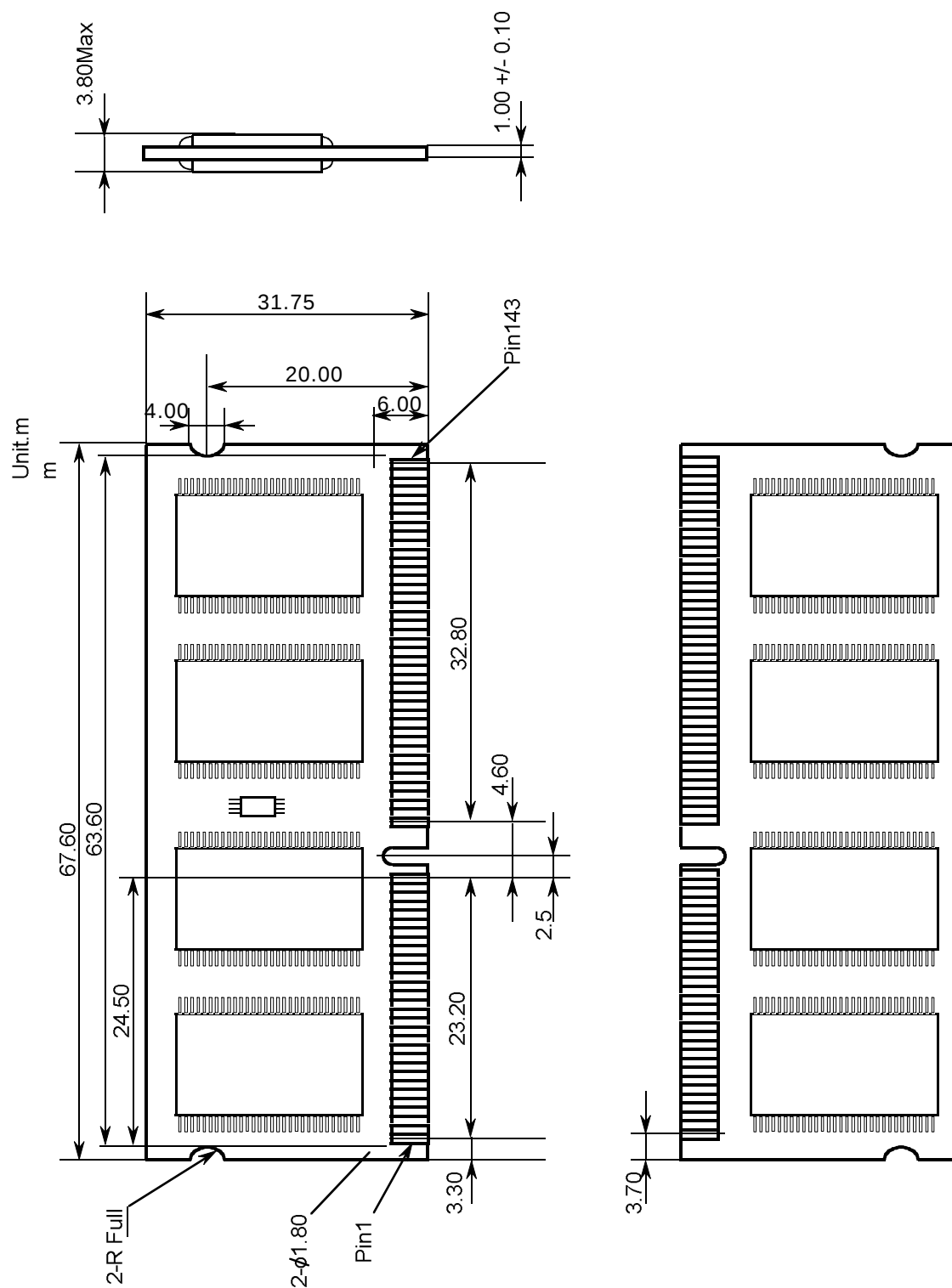


*Italic parameter* indicates minimum case

# MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

## OUTLINE



## MH8S64DBKG -6,-6L-7,-7L,-8,-8L

536870912-BIT (8388608 - WORD BY 64-BIT) Synchronous DRAM

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- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

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