DLP® 0.3 WVGA Series 220 DMD

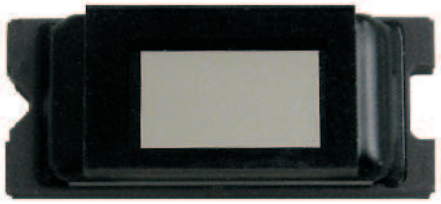
Check for Samples: DLP3000

FEATURES

- 0.3-Inch (7.62 mm) Diagonal Micromirror Array
  - 608 × 684 Array of Aluminum, Micrometer-Sized Mirrors
  - 7.6-µm Micromirror Pitch
  - ±12° Micromirror Tilt Angle (Relative to Flat State)
  - Side Illumination for Optimized Efficiency
  - 3-µs Micromirror Cross Over Time
- Highly Efficient in Visible Light (420 nm–700 nm):
  - Window Transmission 97% (Single Pass, Through Two Window Surfaces)
  - Micromirror Reflectivity 88%
  - Array Diffraction Efficiency 86%
  - Array Fill Factor 92%
  - Polarization Independent
- Up to WVGA Resolution (854x480) Wide Aspect Ratio Display
- Low Power Consumption, only 200 mW (Typical)
- 15-Bit, Double Data Rate (DDR) Input Data Bus
- 60-MHz to 80-MHz Input Data Clock Rate
- Integrated Micromirror Driver Circuitry
- Supports –10 °C to 70 °C
- 16.6-mm by 7-mm by 5-mm Package Footprint
- Dedicated DLPC300 Controller for Reliable Operation
- Package Mates to PANASONIC AXT550224 Socket

APPLICATIONS

- Machine Vision
- Industrial Inspection
- 3D Scanning
- 3D Optical Metrology
- Automated Fingerprint Identification
- Face Recognition
- Augmented Reality
- Embedded Display
- Interactive Display
- Information Overlay
- Spectroscopy
- Chemical Analyzers
- Medical Instruments
- Photo-Stimulation
- Virtual Gauges



DESCRIPTION

The DLP3000 digital micromirror device (DMD) is a digitally controlled MOEMS (micro-opto-electromechanical system) spatial light modulator (SLM). When coupled to an appropriate optical system, the DLP3000 can be used to modulate the amplitude and direction of incoming light. The DLP3000 creates light patterns with speed, precision, and efficiency.

Architecturally, the DLP3000 is a latchable, electrical-in/optical-out semiconductor device. This architecture makes the DLP3000 well suited for use in applications such as 3D scanning or metrology with structured light, augmented reality, microscopy, medical instruments, and spectroscopy. The compact physical size of the DLP3000 is well-suited for portable equipment where small form factor and lower cost are important. The compact package compliments the small size of LEDs to enable highly efficient, robust light engines.

The DLP3000 is one of two devices in the DLP 0.3 WVGA chipset (see Figure 1). Proper function and reliable operation of the DLP3000 requires that it be used in conjunction with the DLPC300 controller. See the DLP 0.3 WVGA Chip-set data sheet (TI literature number DLPZ005) for further details. Figure 2 shows a typical system application using the DLP 0.3-inch WVGA chipset.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

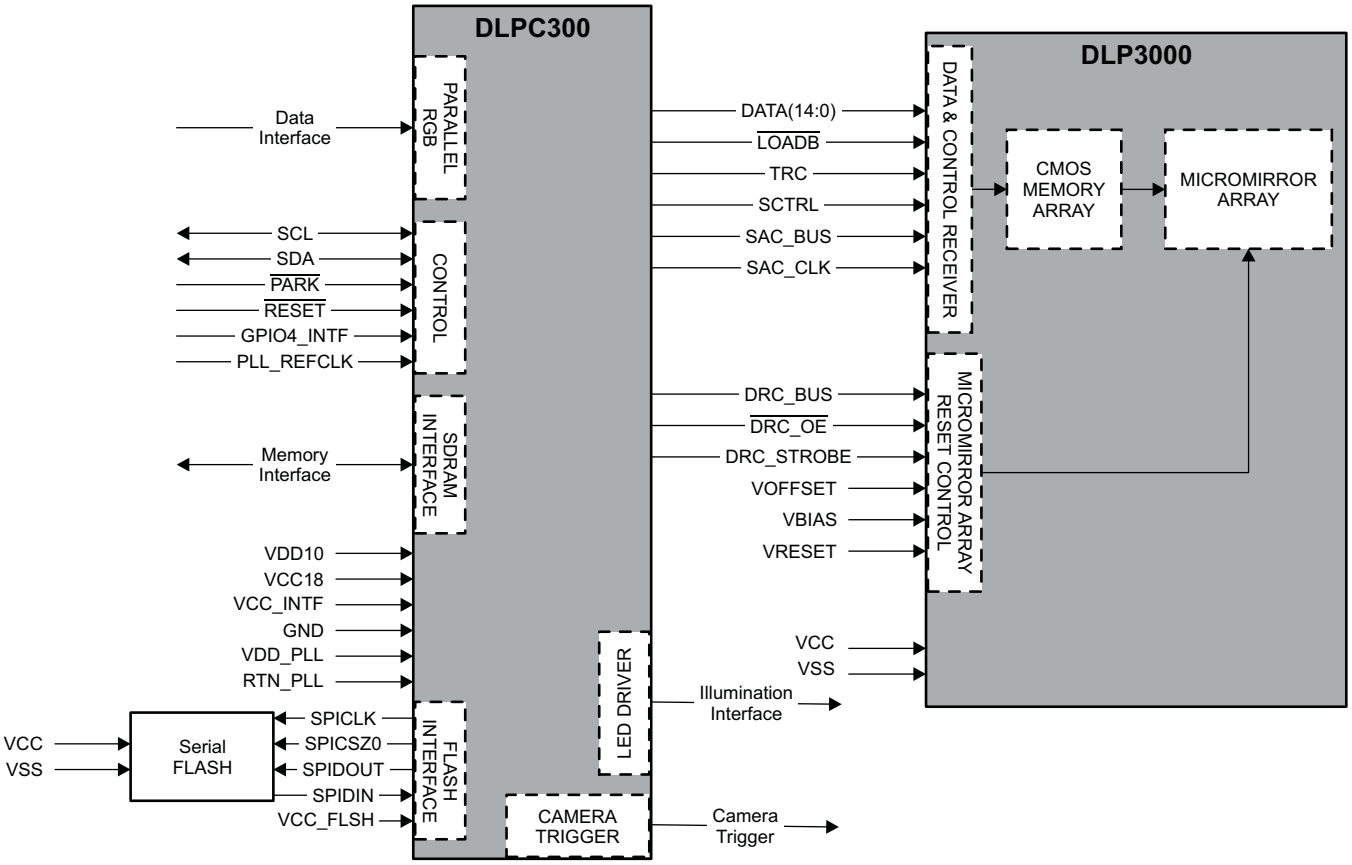


Figure 1. DLP 0.3 WVGA Chip Set

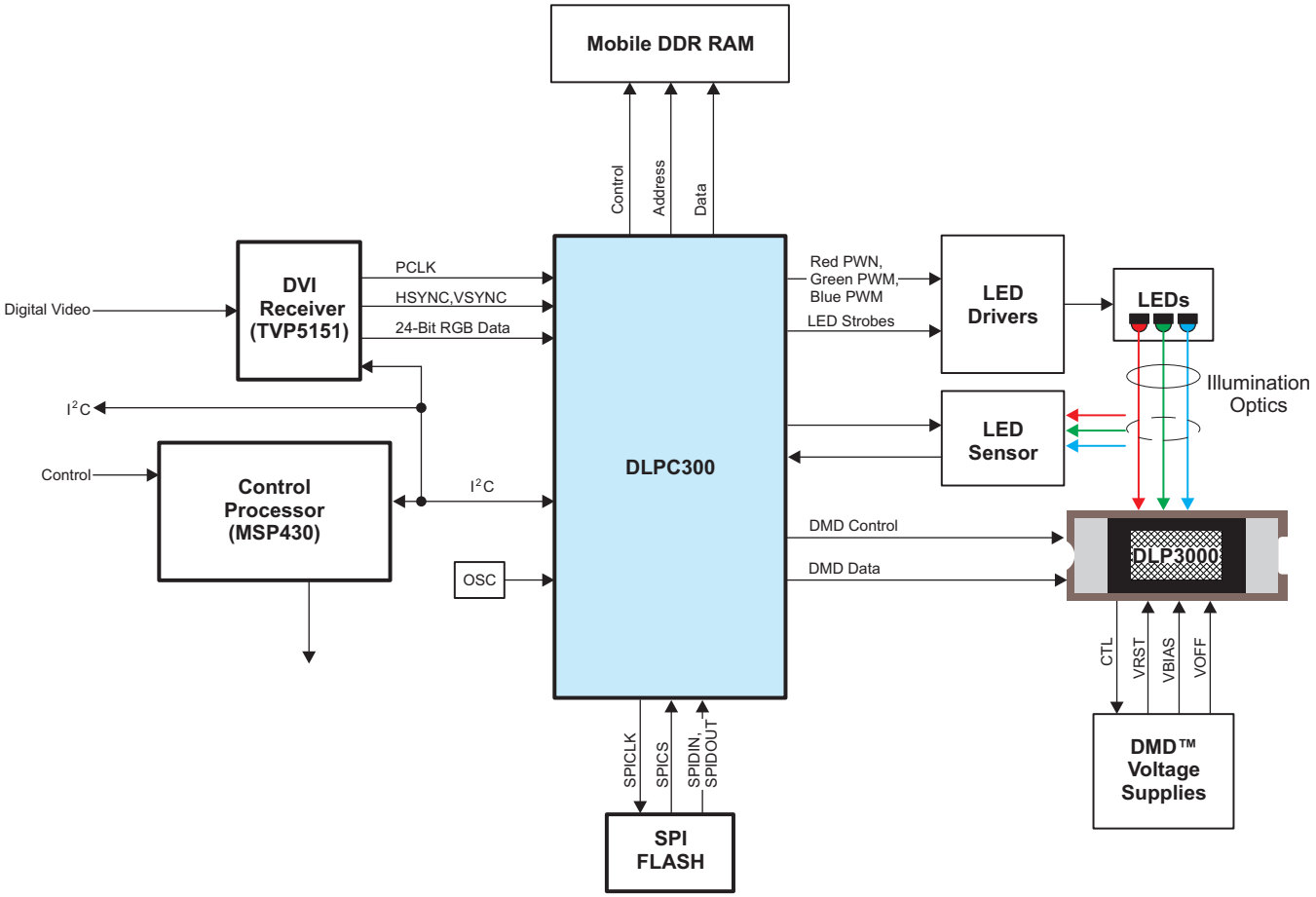


Figure 2. Typical Application

Electrically, the DLP3000 consists of a two-dimensional array of 1-bit CMOS memory cells, organized in a grid of 608 memory cell columns by 684 memory cell rows. The CMOS memory array is addressed on column-by-column basis, over a 15-bit double data rate (DDR) bus. Addressing is handled via a serial control bus. The specific CMOS memory access protocol is handled by the DLPC300 digital controller.

Optically, the DLP3000 consists of 415,872 highly reflective, digitally switchable, micrometer-sized mirrors (micromirrors) organized in a two-dimensional array. The micromirror array consists of 608 micromirror columns by 684 micromirror rows in diamond pixel configuration (Figure 3). Due to the diamond pixel configuration, the columns of each odd row are offset by half a pixel from the columns of the even row.

Each aluminum micromirror is approximately 7.6 microns in size (see *Micromirror Pitch* in Figure 3), and is switchable between two discrete angular positions: –12° and +12°. The angular positions are measured relative to a 0° *flat reference when the mirrors are parked in their inactive state*, parallel to the array plane (see Figure 4). The tilt direction is perpendicular to the hinge-axis. The on-state landed position is directed toward the left side of the package (see *DLP3000 Active Mirror Array*, *Micromirror Pitch*, and *Micromirror Hinge-Axis Orientation* in Figure 3).

Each individual micromirror is positioned over a corresponding CMOS memory cell. The angular position of a specific micromirror is determined by the binary state (logic 0 or 1) of the corresponding CMOS memory cell contents, after the mirror *clocking pulse* is applied. The angular position (–12° or +12°) of the individual micromirrors changes synchronously with a micromirror clocking pulse, rather than being coincident with the CMOS memory cell data update. Therefore, writing a logic 1 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a +12° position. Writing a logic 0 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a –12° position.

Updating the angular position of the micromirror array consists of two steps. First, updating the contents of the CMOS memory. Second, application of a mirror reset to all or a portion of the micromirror array (depending upon the configuration of the system). Mirror reset pulses are generated internally by the DLP3000 DMD, with application of the pulses being coordinated by the DLPC300 controller. See SWITCHING CHARACTERISTICS timing specifications.

Around the perimeter of the 608 × 684 array of micromirrors is a uniform band of *border* micromirrors. The border micromirrors are not user-addressable. The border micromirrors land in the –12° position once power has been applied to the device. There are 10 border micromirrors on each side of the 608 by 684 active array.

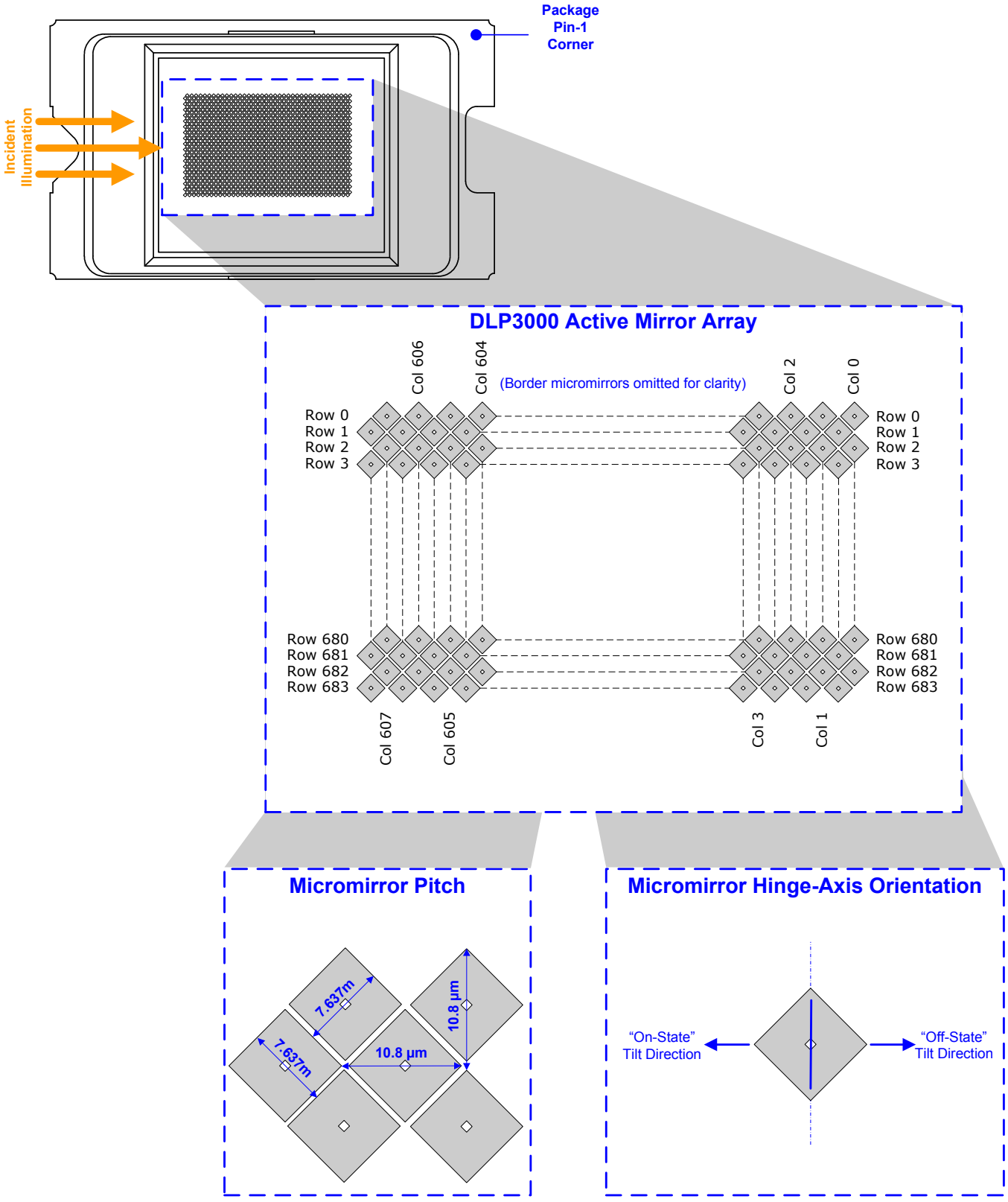


Figure 3. Micromirror Array, Pitch, and Hinge-Axis Orientation

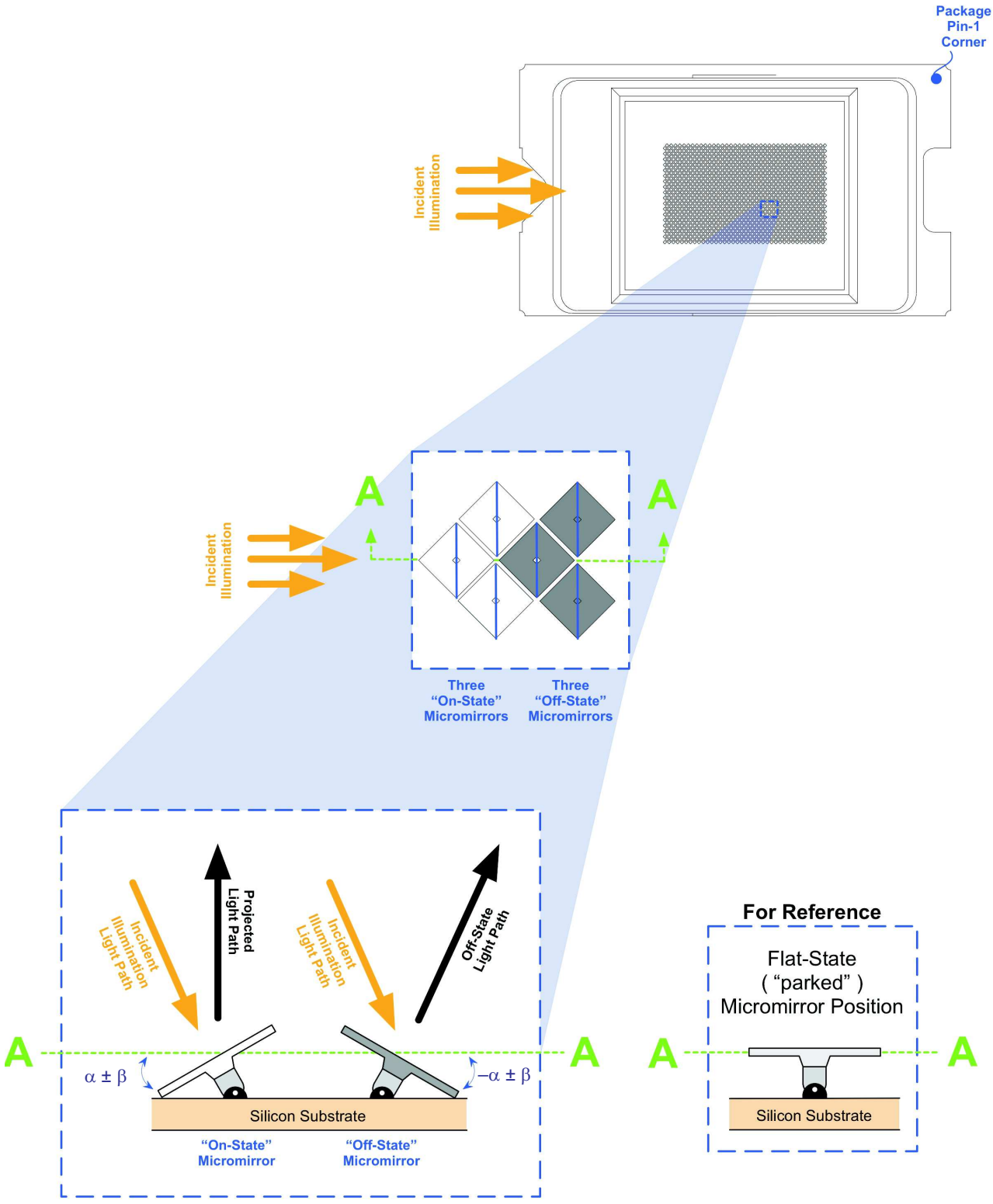


Figure 4. Micromirror Landed Positions and Light Paths

Related Documents

The following documents contain additional information related to the use of the DLP3000 device:

Table 1. Related Documents

DOCUMENT	TI LITERATURE NUMBER
DLP 0.3 WVGA Chipset data sheet	DLPZ005
DLPC300 Digital Controller data sheet	DLPS023
DLPC300 Software Programmer's Guide	DLPU004

Device Part Number Nomenclature

Figure 5 provides a legend for reading the complete device name for any DLP device.

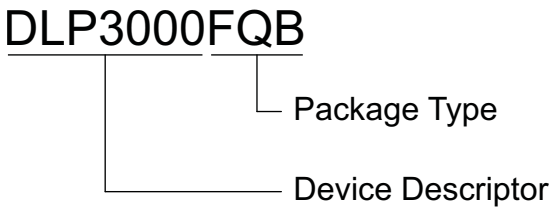


Figure 5. Device Nomenclature

Device Marking

The device marking consists of the fields shown in Figure 6.

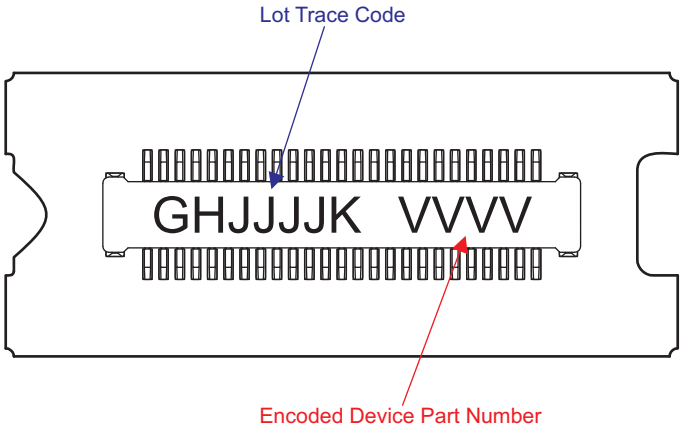


Figure 6. Device Marking

Device Terminals

This section describes the input/output characteristics of signals that interface to the DLP3000, organized by functional groups. Table 2 includes I/O, Type, Internal Termination, Clock Domain, and Data Rate characteristics which are further described in subsequent sections.

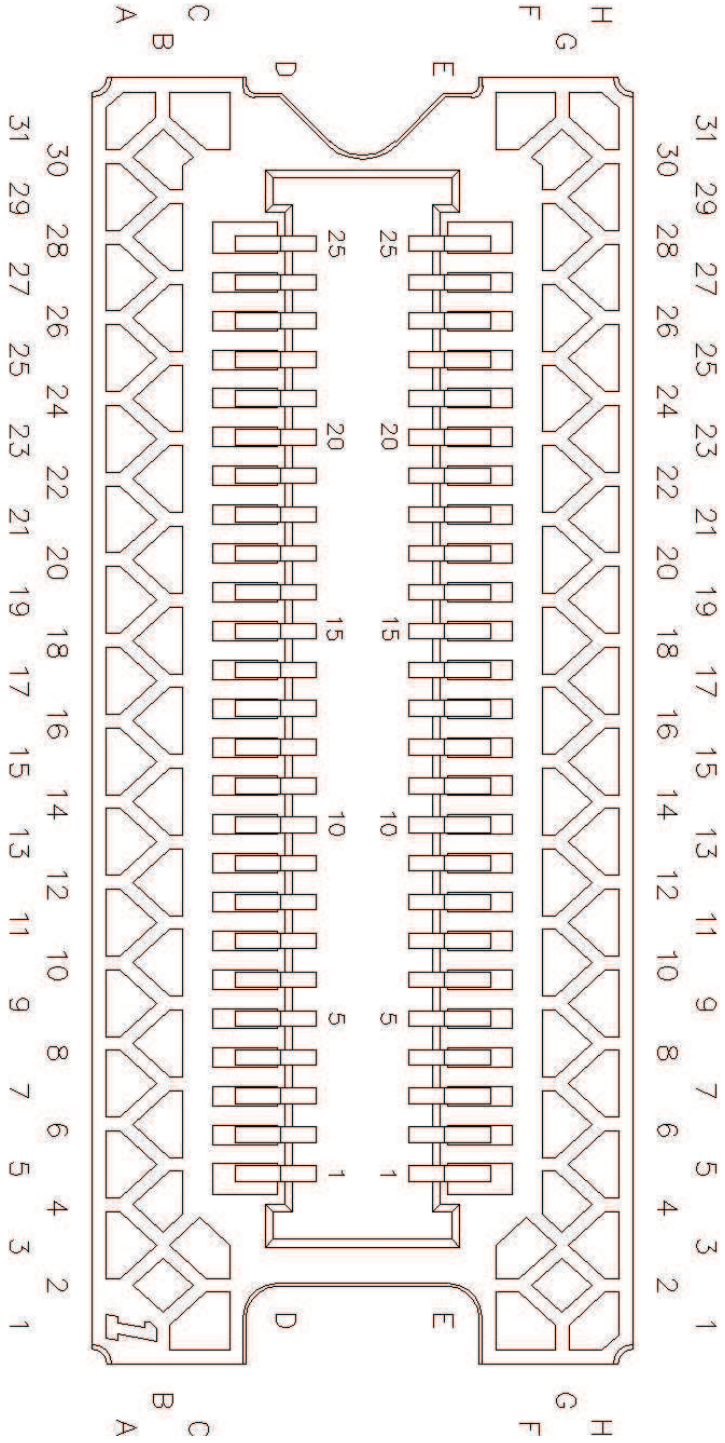


Figure 7. Package Connector Signal Names (Device Bottom View)

Table 2. Connector Pins

TERMINAL NAME	CONNECTOR PINS	I/O/P	TYPE	INTERNAL TERMINATION	CLOCKED BY	DATA RATE	DESCRIPTION
Data Inputs							
DATA(0)	D2	Input	LVCMOS	None	DCLK	DDR	Input data bus
DATA(1)	D4	Input	LVCMOS	None	DCLK	DDR	
DATA(2)	D5	Input	LVCMOS	None	DCLK	DDR	
DATA(3)	D6	Input	LVCMOS	None	DCLK	DDR	
DATA(4)	D8	Input	LVCMOS	None	DCLK	DDR	
DATA(5)	D10	Input	LVCMOS	None	DCLK	DDR	
DATA(6)	D12	Input	LVCMOS	None	DCLK	DDR	
DATA(7)	D14	Input	LVCMOS	None	DCLK	DDR	
DATA(8)	E16	Input	LVCMOS	None	DCLK	DDR	
DATA(9)	E14	Input	LVCMOS	None	DCLK	DDR	
DATA(10)	E12	Input	LVCMOS	None	DCLK	DDR	
DATA(11)	E10	Input	LVCMOS	None	DCLK	DDR	
DATA(12)	E5	Input	LVCMOS	None	DCLK	DDR	
DATA(13)	E6	Input	LVCMOS	None	DCLK	DDR	
DATA(14)	E8	Input	LVCMOS	None	DCLK	DDR	
DCLK	E18	Input	LVCMOS	None	–	–	Input data bus clock
Data Control Inputs							
$\overline{\text{LOADB}}$	E20	Input	LVCMOS	None	DCLK	DDR	Parallel data load enable
TRC	E4	Input	LVCMOS	None	DCLK	DDR	Input data toggle rate control
SCTRL	E2	Input	LVCMOS	None	DCLK	DDR	Serial control bus
SAC_BUS	E24	Input	LVCMOS	None	SAC_CLK	–	Stepped address control serial bus data
SAC_CLK	D24	Input	LVCMOS	None	–	–	Stepped address control serial bus clock
Mirror Reset Control Inputs							
DRC_BUS	D22	Input	LVCMOS	None	SAC_CLK		DMD reset-control serial bus
$\overline{\text{DRC\_OE}}$	D20	Input	LVCMOS	None	–	–	Active-low output enable signal for internal DMD Reset driver circuitry
DRC_STROBE	E22	Input	LVCMOS	None	SAC_CLK		Strobe signal for DMD Reset Control inputs
Power							
VBIAS	D16	Power	Analog	None	–	–	Mirror reset bias voltage
VOFFSET	D21	Power	Analog	None	–	–	Mirror reset offset voltage
VRESET	D18	Power	Analog	None	–	–	Mirror reset voltage
VREF	E21	Power	Analog	None	–	–	Power supply for double-data-rate low-voltage CMOS logic terminals
VCC	D1, D13, D25, E1, E13, E25	Power	Analog	None	–	–	Power supply for single-data-rate LVCMOS logic terminals
VSS	D3, D7, D9, D11, D15, D17, D19, D23, E3, E7, E9, E11, E15, E17, E19, E23	Power	Analog	None	–	–	Common return for all power inputs

Table 2. Connector Pins (continued)

TERMINAL NAME	CONNECTOR PINS	I/O/P	TYPE	INTERNAL TERMINATION	CLOCKED BY	DATA RATE	DESCRIPTION
No connect	A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A23, A25, A27, A29 A31, B2, B4, B6, B8, B10, B12, B14, B16, B18, B20, B22, B24, B26, B28, B30, C1, C3, C31, F1, F3, F31, G2, G4, G6, G8, G10, G12, G14, G16, G18, G20, G22, G24, G26, G28, G30, H1, H3, H5, H7, H9, H11, H13, H15, H17, H19, H21, H23, H25, H27, H29, H31	–	–	–	–	–	No connection (Any connection to these terminals may result in undesirable effects)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. The *Absolute Maximum Ratings* are stress ratings only, and functional performance of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PARAMETER		CONDITIONS	MIN	MAX	UNIT
Electrical					
V_{CC}	Voltage applied to V_{CC} (1)(2)		–0.5	4	V
V_{REF}	Voltage applied to V_{REF} (1)(2)		–0.5	4	V
V_{OFFSET}	Voltage applied to V_{OFFSET} (1)(2)(3)		–0.5	8.75	V
V_{BIAS}	Voltage applied to V_{BIAS} (1)(2)(3)		–0.5	17	V
V_{RESET}	Voltage applied to V_{RESET} (1)(2)		–11	0.5	V
	Supply voltage delta $\lvert V_{BIAS} - V_{OFFSET} \rvert$ (3)			8.75	V
	Voltage applied to all other input terminals (1)		–0.5	V_{REF} + 0.3	V
	Current required from a high-level output	V_{OH} = 2.4 V		–20	mA
	Current required from a low-level output	V_{OL} = 0.4 V		15	mA
Environmental					
	Storage temperature range (4)(5)		-40	80	°C
	Storage humidity (4)(5)	Non-condensing	0	95	% RH
	Illumination power density (4)(6)	< 420 nm		2	mW/cm^2
		420 nm to 700 nm	See (7)		
		> 700 nm		10	
	Electrostatic discharge immunity (8)	All pins		2000	V

(1) All voltages referenced to V_{SS} (ground).
(2) Voltages V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, and V_{RESET} are required for proper DMD operation.
(3) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw.
(4) Optimal, long-term performance of the Digital Micromirror Device (DMD) can be affected by various application parameters, including illumination spectrum, illumination power density, micromirror landed duty cycle, ambient temperature (both storage and operating), case temperature, ambient humidity (both storage and operating), and power on/off duty cycle. TI recommends that application-specific effects be considered as early as possible in the design cycle. Contact your local Texas Instruments representative for additional information related to optimizing the DMD performance.
(5) Simultaneous exposure to high storage temperature and high storage humidity may affect device reliability.
(6) Total integrated illumination power density, above or below the indicated wavelength threshold.
(7) Limited only by the resulting array temperature. Refer to the Thermal Characteristics for information related to calculating the micromirror array temperature.
(8) Tested in accordance with JESD22-A114-B electrostatic discharge (ESD) sensitivity testing, human-body model (HBM).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the *Recommended Operating Conditions*. No level of performance is implied when operating the device above or below the *Recommended Operating Conditions* limits.

			MIN	NOM	MAX	UNIT
ELECTRICAL						
V_{REF}	LVCMOS interface supply voltage (1)(2)		1.65	1.8	1.95	V
V_{CC}	LVCMOS logic supply voltage (1)(2)		2.375	2.5	2.625	V
V_{OFFSET}	Mirror electrode and HVCMOS supply voltage (1)(2)(3)		8.25	8.5	8.75	V
V_{BIAS}	Mirror electrode voltage (1)(2)(3)		15.5	16	16.5	V
V_{RESET}	Mirror electrode voltage (1)(2)		– 9.5	–10	–10.5	V
	Delta supply voltage $\lvert V_{BIAS} - V_{OFFSET} \rvert$ (3)				8.75	V
V_{T+}	Positive-going threshold voltage		0.4 × V_{REF}		0.7 × V_{REF}	V
$V_{T–}$	Negative-going threshold voltage		0.3 × V_{REF}		0.6 × V_{REF}	V
V_{hys}	Hysteresis voltage ($V_{T+} – V_{T–}$)		0.1 × V_{REF}		0.4 × V_{REF}	V
f_{DCLK}	DCLK clock frequency		60		80	MHz
MECHANICAL						
	Static load applied to the package electrical connector area (4) (5)				45	N
	Static load applied to the DMD mounting area (6) (5)				100	N
ENVIRONMENTAL						
	Operating Case Temperature (7)(8)			26		°C
	Operating Humidity (7)	non-condensing		60		% RH
	Operating Device Temperature Gradient (9)				10	°C
	Operating Landed Duty-Cycle (7)(10)			25		%

(1) All voltages referenced to V_{SS} (ground)
(2) Voltages V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, V_{RESET} are required for proper DMD operation.
(3) Exceeding the recommended voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw. See the *Absolute Maximum Ratings* for further details.
(4) Load should be uniformly distributed across the entire connector area.
(5) See Figure 8.
(6) Load should be uniformly distributed across the three datum-A surfaces.
(7) Optimal, long-term performance of the Digital Micromirror Device (DMD) can be affected by various application parameters, including illumination spectrum, illumination power density, micromirror landed duty cycle, ambient temperature (both storage and operating), case temperature, ambient humidity (both storage and operating), and power on/off duty cycle. TI recommends that application-specific effects be considered as early as possible in the design cycle. Contact your local Texas Instruments representative for additional information related to optimizing the DMD performance.
(8) Refer to the Thermal Characteristics for the calculation of the micromirror array temperature from the thermal test point TC3 shown in Figure 15.
(9) As measured between any two points on the exterior of the package, or as predicted between any two points inside the micromirror array cavity. Refer to the Thermal Characteristics for information related to calculating the micromirror array temperature.
(10) "Landed Duty-Cycle" refers to the percentage of time an individual micromirror spends landed in one state (+12 or -12 degrees) versus the other state (-12 or +12 degrees).

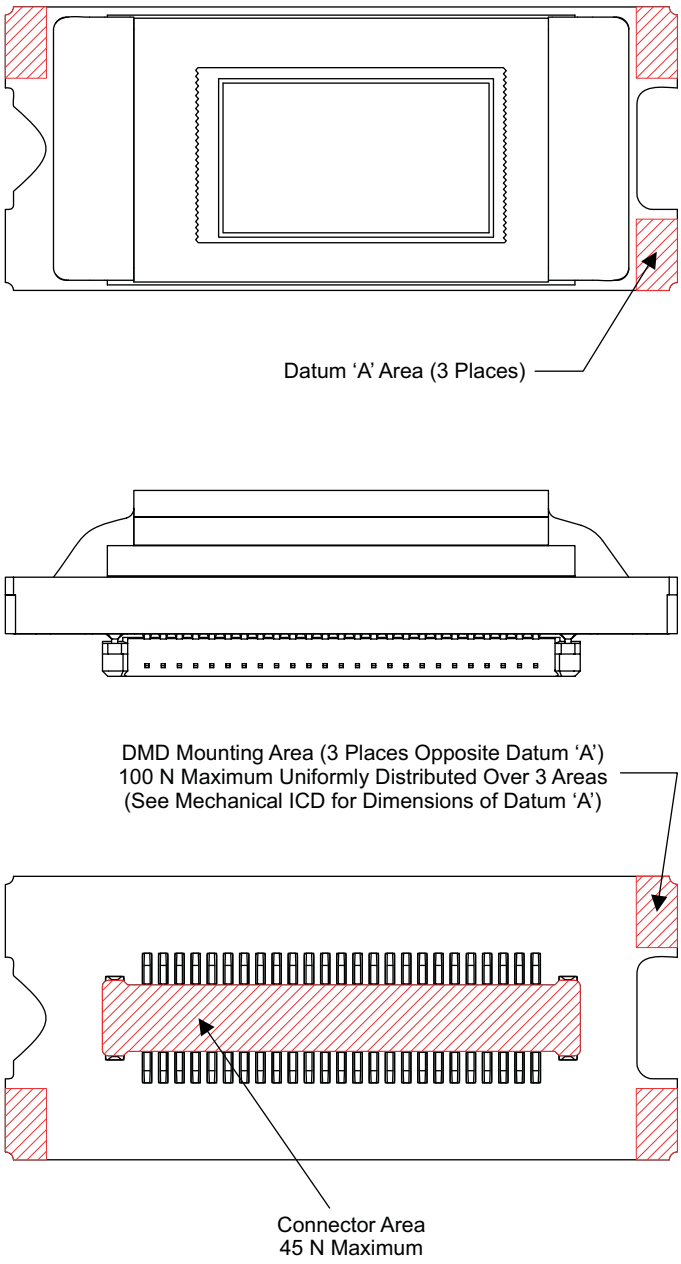


Figure 8. System Interface Loads

ELECTRICAL CHARACTERISTICS

over the range of recommended supply voltage and recommended case operating temperature (unless otherwise noted)

PARAMETER		CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage (1)	V_{CC} = 2.5 V,	I_{OH} = –21 mA	1.7		V
V_{OL}	Low-level output voltage (1)	V_{CC} = 2.5 V,	I_{OH} = 15 mA		0.4	V
I_{OH}	High-level output current	V_{OH} = 1.7 V			–15	mA
I_{OL}	Low-level output current	V_{OL} = 0.4 V			14	mA
I_{IL}	Low-level input current	V_{REF} = 1.95 V,	V_I = 0 V	–1.6		nA
I_{IH}	High-level input current	V_{REF} = 1.95 V,	V_I = V_{REF}		1.9	nA
I_{REF}	Current into V_{REF} terminal	V_{REF} = 1.95 V,	f_{DCLK} = 77 MHz		0.7	mA
I_{CC}	Current into V_{CC} terminal	V_{CC} = 2.625 V,	f_{DCLK} = 77 MHz		55	mA
I_{OFFSET}	Current into V_{OFFSET} terminal (2)	V_{OFFSET} = 8.75 V			1	mA
I_{BIAS}	Current into V_{BIAS} terminal (2)	V_{BIAS} = 17 V			1.6	mA
I_{RESET}	Current into V_{RESET} terminal (2)	V_{RESET} = –11 V			1.5	mA
P_{REF}	Power into V_{REF} terminal (3)	V_{REF} = 1.95 V,	f_{DCLK} = 77 MHz		1.5	mW
P_{CC}	Power into V_{CC} terminal (3)	V_{CC} = 2.625 V,	f_{DCLK} = 77 MHz		144	mW
P_{OFFSET}	Power into V_{OFFSET} terminal (3)	V_{OFFSET} = 8.75 V			9	mW
P_{BIAS}	Power into V_{BIAS} terminal (3)	V_{BIAS} = 17 V			27.2	mW
P_{RESET}	Power into V_{RESET} terminal (3)	V_{RESET} = –11 V			18	mW
C_I	Input capacitance	f = 1 MHz			10	pF
C_O	Output capacitance	f = 1 MHz			10	pF

(1) Applies to LVCMOS pins only
(2) Exceeding the maximum allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excesses current draw. (See *Absolute Maximum Ratings* for details.)
(3) In some applications, the total DMD heat load can be dominated by the amount of incident light energy absorbed. See the *Thermal Characteristics* for further details.

Measurement Conditions

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. *Figure 9* shows an equivalent test load circuit for the output under test. The load capacitance value stated is only for characterization and measurement of ac timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, V_{OL} MAX and V_{OH} MIN for output clocks.

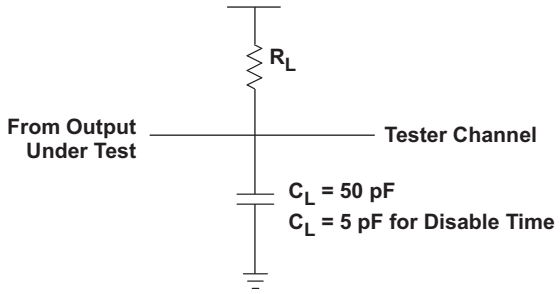


Figure 9. Test Load Circuit for AC Timing Measurements

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
t_{s1}	Setup time: DATA before rising or falling edge of DCLK	1			ns
	Setup time: TRC before rising or falling edge of DCLK	1			
	Setup time: SCTRL before rising or falling edge of DCLK	1			
t_{s2}	Setup time: $\overline{\text{LOADB}}$ low before rising edge of DCLK	1			ns
t_{s3}	Setup time: SAC_BUS low before rising edge of SAC_CLK	1			ns
t_{s4}	Setup time: DRC_BUS high before rising edge of SAC_CLK	1			ns
t_{s5}	Setup time: DRC_STROBE high before rising edge of SAC_CLK	1			ns
t_{h1}	Hold time: DATA after rising or falling edge of DCLK	1			ns
	Hold time: TRC after rising or falling edge of DCLK	1			
	Hold time: SCTRL after rising or falling edge of DCLK	1			
t_{h2}	Hold time: $\overline{\text{LOADB}}$ low after falling edge of DCLK	1			ns
t_{h3}	Hold time: SAC_BUS low after rising edge of SAC_CLK	1			ns
t_{h4}	Hold time: DRC_BUS after rising edge of SAC_CLK	1			ns
t_{h5}	Hold time: DRC_STROBE after rising edge of SAC_CLK	1			ns
t_{c1}	Clock cycle: DCLK	12.5		16.67	ns
t_{c3}	Clock cycle: SAC_CLK	12.5		16.67	ns
t_{w1}	Pulse width high or low: DCLK	5			ns
t_{w2}	Pulse width low: $\overline{\text{LOADB}}$	7			ns
t_{w3}	Pulse width high or low: SAC_CLK	5			ns
t_{w5}	Pulse width high: DRC_STROBE	7			ns
t_r	Rise time: DCLK / SAC_CLK			2.5	ns
	Rise time: DATA / TRC / SCTRL / $\overline{\text{LOADB}}$			2.5	
t_f	Fall time: DCLK / SAC_CLK			2.5	ns
	Fall time: DATA / TRC / SCTRL / $\overline{\text{LOADB}}$			2.5	

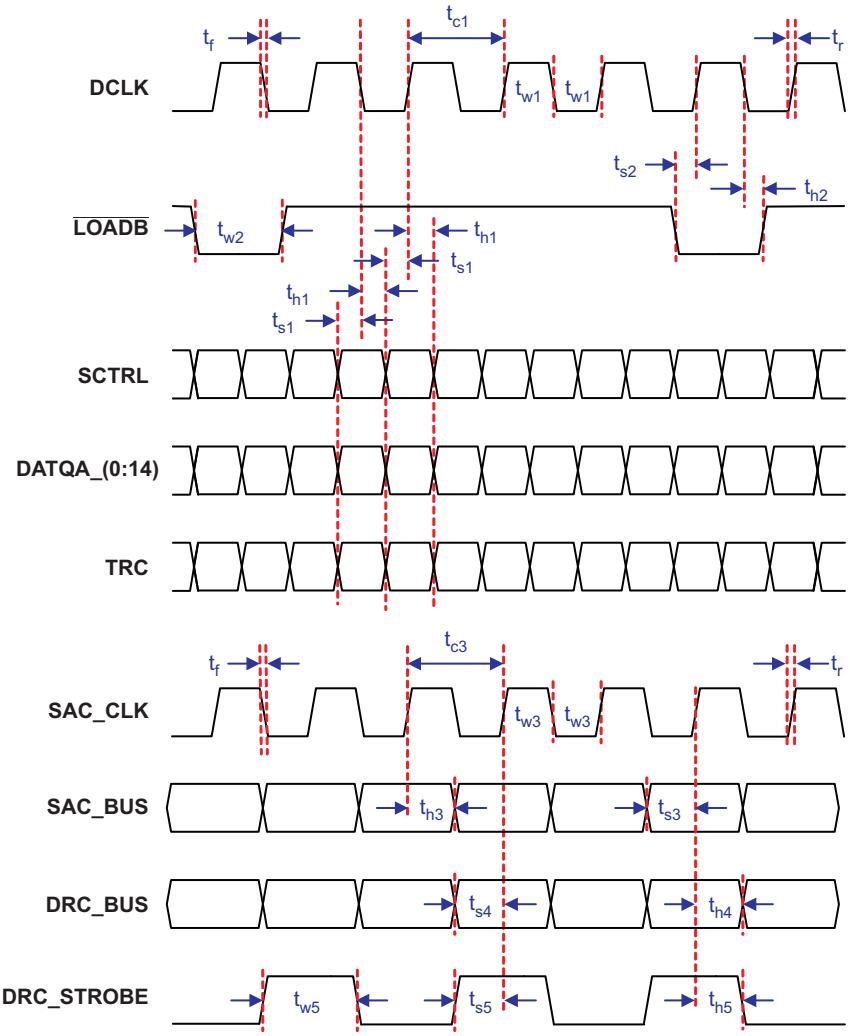


Figure 10. Switching Characteristics

POWER SUPPLY SEQUENCING REQUIREMENTS

DLP3000 includes four voltage-level supplies (V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, and V_{RESET}). For reliable operation of DLP3000, the following power supply sequencing requirements must be followed.

CAUTION

Reliable performance of the DMD requires that the following conditions be met:

1. That the V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, and V_{RESET} power supply inputs all be present during operation.
2. That the V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, and V_{RESET} power supplies be sequenced on and off in the manner prescribed below.

Repeated failure to adhere to the prescribed power-up and power-down procedures may affect device reliability

DMD Power Supply Power-Up Procedure

Step 1: Power up V_{CC} and V_{REF} in any order

Step 2: Wait for V_{CC} and V_{REF} to each reach a stable level within their respective recommended operating ranges.

Step 3: Power up V_{BIAS}, V_{OFFSET}, and V_{RESET} in any order, provided that the maximum delta-voltage between V_{BIAS} and V_{OFFSET} is not exceeded (see Absolute Maximum Ratings for details).

Note 1: ***During the power-up procedure, the DMD LVCMOS inputs should not be driven high until after Step 2 has been completed.***

Note 2: ***Power supply slew rates during power up are unrestricted, provided that all other conditions are met.***

DMD Power Supply Power-Down Procedure

Step 1: Command the chipset controller to execute a mirror-parking sequence. See the controller data sheet (listed in *Related Documents*) for details.

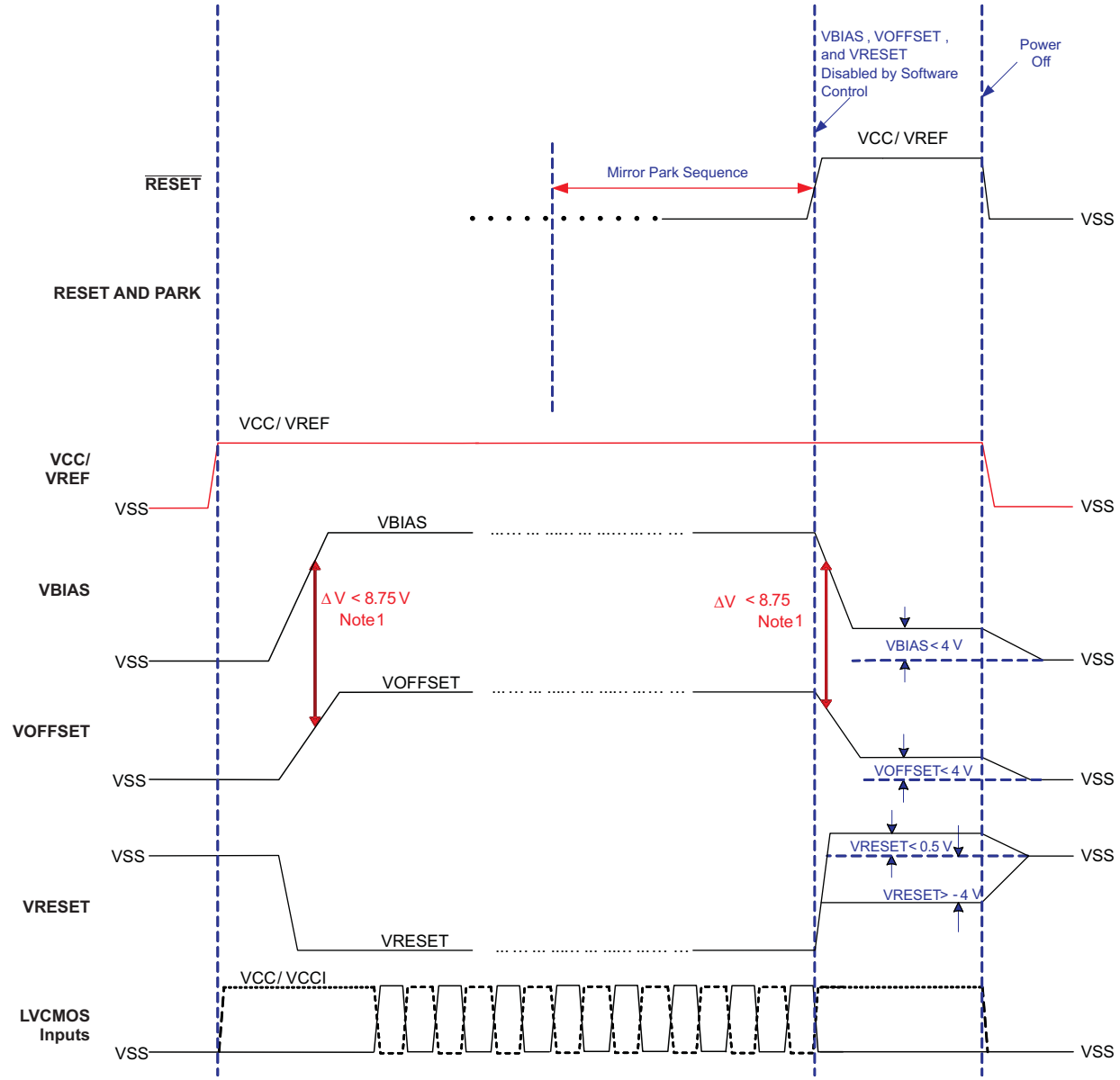
Step 2: Power down V_{BIAS}, V_{OFFSET}, and V_{RESET} in any order, provided that the maximum delta voltage between V_{BIAS} and V_{OFFSET} is not exceeded (see *Absolute Maximum Ratings* for details).

Step 3: Wait for V_{BIAS}, V_{OFFSET}, and V_{RESET} to each discharge to a stable level within 4 V of the reference ground.

Step 4: Power down V_{CC} and V_{REF} in any order.

Note 1: ***During the power-down procedure, the DMD LVCMOS inputs should be held at a level less than V_{REF} + 0.3 volts.***

Note 2: ***Power-supply slew rates during power down are unrestricted, provided that all other conditions are met.***



NOTE 1: Delta supply voltage |VBIAS – VOFFSET| < 8.75 V

Figure 11. Power-Up / Power-Down Timing

Micromirror Array Physical Characteristics

Physical characteristics of the micromirror array are provided in Table 3.

Table 3. Micromirror Array Physical Characteristics

PARAMETER	VALUE	UNITS
Number of active micromirror rows (1)	684	micromirrors
Number of active micromirror columns (1)	608	micromirrors
Micromirror pitch, diagonaL (2)	7.637	µm
Micromirror pitch, vertical and horizontal (2)	10.8	µm
Micromirror active array height (3)	684	micromirrors
	3.699	mm
Micromirror active array width (3)	604	micromirrors
	6.5718	mm
Micromirror array border (4)	10	mirrors/side

(1) See Figure 14
(2) See Figure 12
(3) SeeFigure 13
(4) The mirrors that form the array border are hard-wired to tilt in the –12° (“Off”) direction once power is applied to the DMD (see Figure 3 and Figure 4).

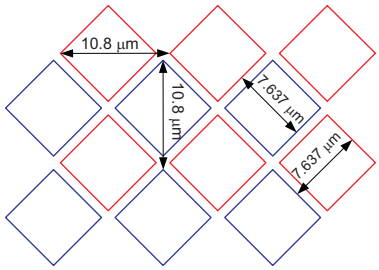


Figure 12. DLP3000 Pixel Pitch Dimensions

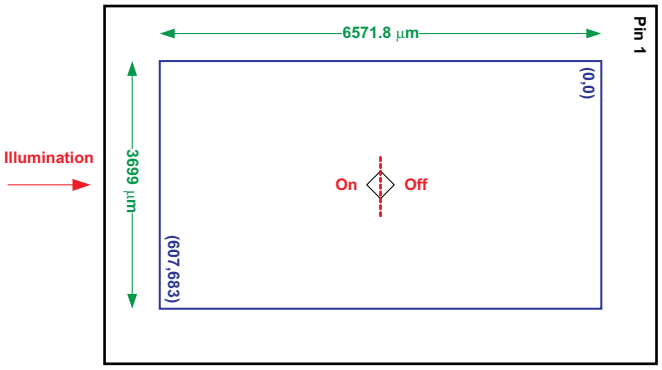


Figure 13. DLP3000 Micromirror Active Area

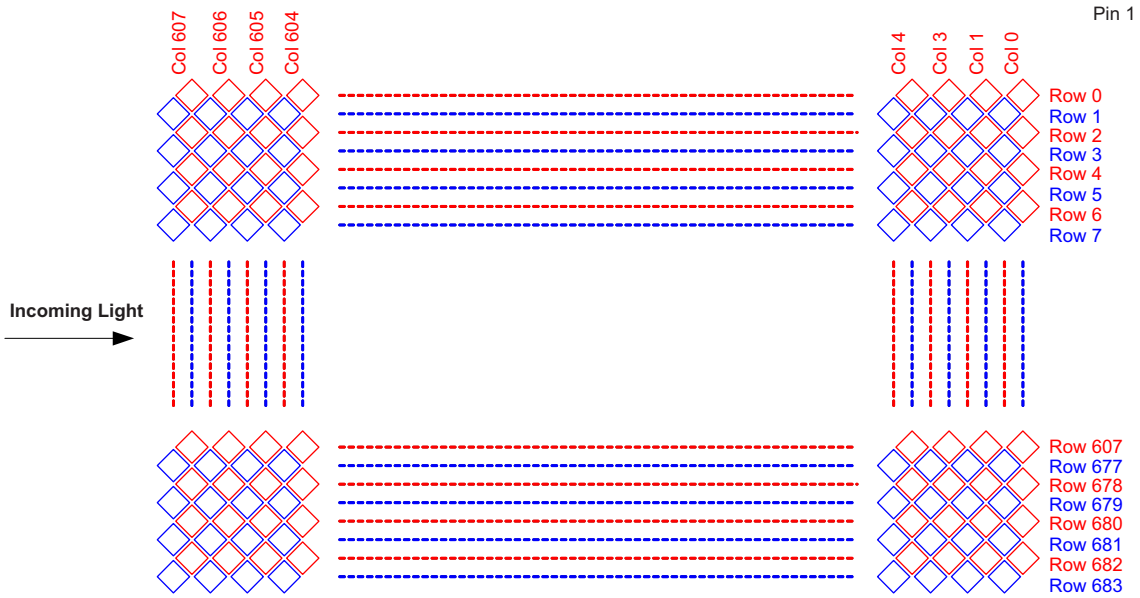


Figure 14. DLP3000 Pixel Arrangement

Micromirror Array Optical Characteristics

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. See the related application reports (listed in Related Documents) for guidelines.

Table 4. Optical Parameters

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
α	Micromirror tilt angle	DMD *parked* state(1)(2)(3), see Figure 4		0		degrees
		DMD "landed" state(1)(4)(5), see Figure 4		12		
β	Micromirror tilt angle variation (1)(4)(6)(7)(8)	See Figure 4	–1		1	degrees
	Micromirror crossover time(9)			5		µs
	Micromirror switching time(9)			16		µs
	Non-operating micromirrors(10)	Non-adjacent micromirrors			10	micromirrors
		Adjacent micromirrors			0	
	Orientation of the micromirror axis-of-rotation (11)		89	90	91	degrees
	Micromirror array optical efficiency(12)(13)	420 nm to 700 nm, with all micromirrors in the ON state		68%		
	Mirror metal specular reflectivity (420 nm – 700 nm)			89.4%		

(1) Measured relative to the plane formed by the overall micromirror array
(2) *Parking* the micromirror array returns all of the micromirrors to an essentially flat (0˚) state (as measured relative to the plane formed by the overall micromirror array).
(3) When the micromirror array is *parked*, the tilt angle of each individual micromirror is uncontrolled.
(4) Additional variation exists between the micromirror array and the package datums.
(5) When the micromirror array is *landed*, the tilt angle of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror *landing* in an nominal angular position of +12 degrees. A binary value of 0 results in a micromirror *landing* in an nominal angular position of –12 degrees.
(6) Represents the *landed* tilt angle variation relative to the nominal *landed* tilt angle
(7) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(8) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle varation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations and/or system contrast varations.
(9) Performance as measured at the start of life.
(10) Non-operating micromirror is defined as a micromirror that is unable to transition nominally from the –12 degree position to +12 degrees or vice versa.
(11) Measured relative to the package datums B and C, shown in the Package Mechanical Data section at the end of this document.
(12) The minimum or maximum DMD optical efficiency observed in a specific application depends on numerous application-specific design variables, such as:
  (a) Illumination wavelength, bandwidth/line-width, degree of coherence
  (b) Illumination angle, plus angle tolerance
  (c) Illumination and projection aperture size, and location in the system optical path
  (d) IIllumination overfill of the DMD micromirror array
  (e) Aberrations present in the illumination source and/or path
  (f) Aberrations present in the projection path
  (g) Etc.

  The specified nominal DMD optical efficiency is based on the following use conditions:
  (a) Visible illumination (420 nm–700 nm)
  (b) Input illumination optical axis oriented at 24° relative to the window normal
  (c) Projection optical axis oriented at 0° relative to the window normal
  (d) f/3 illumination aperture
  (e) f/2.4 projection aperture

  Based on these use conditions, the nominal DMD optical efficiency results from the following four components:
  (a) Micromirror array fill factor: nominally 92.5%
  (b) Micromirror array diffraction efficiency: nominally 86%
  (c) Micromirror surface reflectivity: nominally 88%
  (d) Window transmission: nominally 97% (single pass, through two surface transitions)
(13) Does not account for the effect of micromirror switching duty cycle, which is application dependant. Micromirror switching duty cycle represents the percentage of time that the micromirror is actually reflecting light from the optical illumination path to the optical projection path. This duty cycle depends on the illumination aperture size, the projection aperture size, and the micromirror array update rate.

Table 4. Optical Parameters (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Illumination overfill(14)			10%		
Window material			Corning Eagle XG		
Window refractive index	At 546.1 nm		1.5119		
Window aperture			See (15)		

(14) The active area of the DLP7000 is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can create artifacts from the mechanical features that surround the active array and other surface anomalies that may be visible on the projected image. The illumination optical system should be designed to limit light flux incident anywhere outside the active array less than 10% of the average flux level in the active area. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause visible artifacts.

(15) See the Package Mechanical Characteristics for details regarding the size and location of the window aperture.

Thermal Characteristics

Achieving optimal DMD performance requires proper management of the maximum DMD case temperature, the maximum temperature of any individual micromirror in the active array, the maximum temperature of the window aperture, and the temperature gradient between any two points on or within the package.

See the *Absolute Maximum Ratings* and *Recommended Operation Conditions* for applicable temperature limits.

Package Thermal Resistance

The DMD is designed to conduct the absorbed and dissipated heat back to the Series 220 package where it can be removed by an appropriate system thermal management. The system thermal management must be capable of maintaining the package within the specified operational temperatures at the Thermal Test Point location, see Figure 15. The total heat load on the DMD is typically driven by the incident light absorbed by the active area; although other contributions can include light energy absorbed by the window aperture, electrical power dissipation of the array, and/or parasitic heating.

Table 5. Package Thermal Resistance

	Min	Nom	Max	Units
Thermal resistance from active micromirror array to TC3			5	°C/W

Case Temperature

The temperature of the DMD case can be measured directly. For consistency, a thermal test point location is defined, as shown in Figure 15.

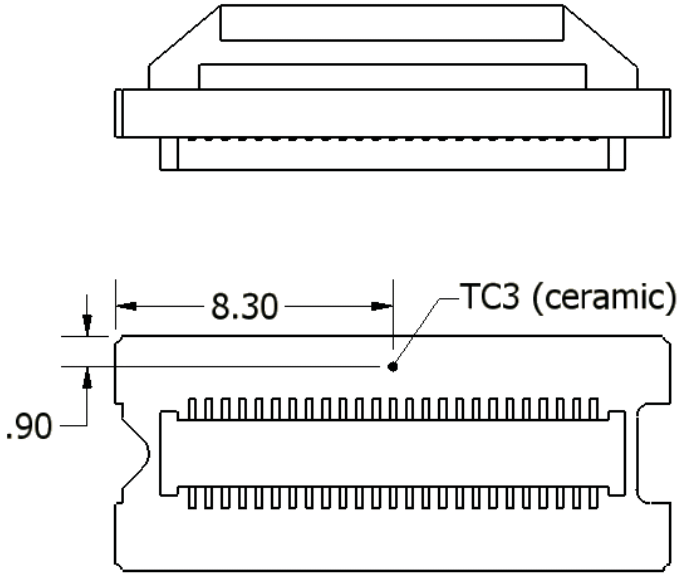


Figure 15. Thermal Test Point Location

Micromirror Array Temperature Calculation

Micromirror array temperature cannot be measured directly. Therefore, it must be computed analytically from:

- Thermal test point location (See Figure 15)
- Package thermal resistance
- Electrical power dissipation
- Illumination heat load

The relationship between the micromirror array and the case temperature is provided by the following equations:

$$T_{Array} = T_{Ceramic} + (Q_{Array} \times R_{Array\text{-}To\text{-}Ceramic})$$

$Q_{Array} = Q_{Elec} + Q_{Illum}$

$Q_{Illum} = C_{L2W} \times SL$

where the following elements are defined as:

T_{Array} = computed micromirror array temperature (°C)

$T_{Ceramic}$ = ceramic case temperature (°C) (TC3 location)

Q_{Array} = Total DMD array power (electrical + absorbed) (W)

$R_{Array\text{-}to\text{-}Ceramic}$ = thermal resistance of DMD package from array to TC3 (°C/W)

Q_{Elec} = nominal electrical power (W)

Q_{Illum} = absorbed illumination heat (W)

C_{L2W} = Lumens-to-watts constant, estimated at 0.00293 watt/lumen , based on array characteristics. It assumes a spectral efficiency of 300 lumens/watt for the projected light, illumination distribution of 83.7% on the active array, and 16.3% on the array border and window aperture.

SL = Screen lumens

These equations are based on traditional 1-chip DLP system with a total projection efficiency from the DMD to the screen of 87%. An example calculation is provided below. DMD electrical power dissipation varies and is dependent on the voltage, data rates, and operating frequencies. The nominal electrical power dissipation used in this calculation is 0.15 watts. Screen lumens is nominally 20 lumens. The ceramic case temperature at TC3 is 55 °C. Using these values in the above equations, the following values are computed:

$Q_{Array} = Q_{Elec} + C_{L2W} \times SL = 0.144\ W + (0.00293\ W/Lumen \times 20\ Lumen) = 0.2026\ W$

$T_{Array} = T_{Ceramic} + (Q_{Array} * R_{Array\text{-}To\text{-}Ceramic}) = 55°C + (0.2026\ W \times 5\ °C/W) = 56.01°C$

REVISION HISTORY

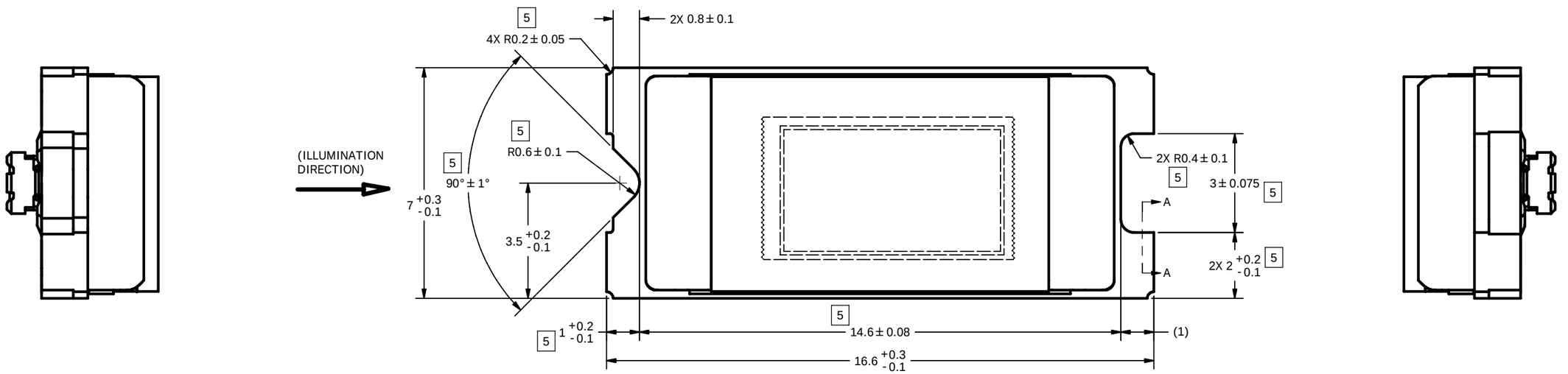
Changes from Original (January 2012) to Revision A **Page**

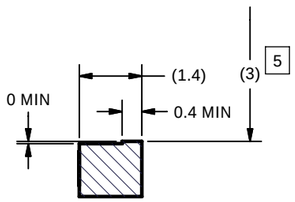
- Corrected the Operating Case Temperature Typ value From: 25 to 26°C 12
- Changed the Operating Humidity Typ value From: 50 to 60%RH 12
- Corrected the C_{L2W} constant value from: 0.00274 to 0.00293 watt/lumen 24

REVISIONS			
REV	DESCRIPTION	DATE	BY
A	ECO 2097098 INITIAL RELEASE	03/02/09	J. HOLM
B	ECO 2098984 TIGHTEN DIE ROTATION, NOTE 2; ADD 'DD1' SUFFIX TO CONNECTOR PART#; CHG DWG TO INVENTOR	08/27/09	BMH

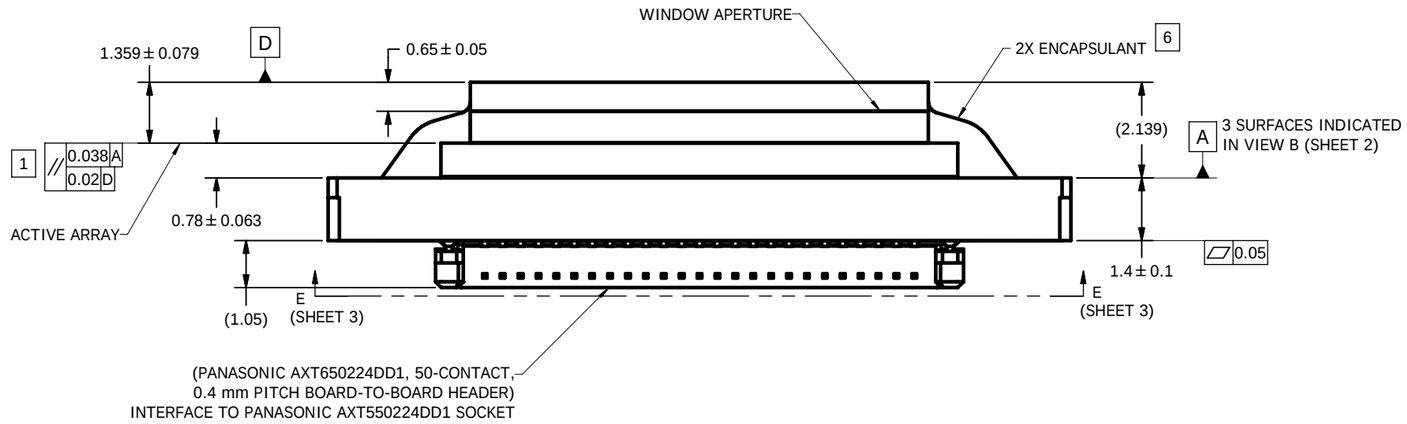
NOTES UNLESS OTHERWISE SPECIFIED:

1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. DMD MARKING TO APPEAR ON BOTTOM OF CONNECTOR.
5. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
6. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEWS C AND G (SHEET 2).





SECTION A-A
NOTCH OFFSETS



NONE	0314DA
NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1'
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- REMOVE ALL BURRS AND SHARP EDGES
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	J. HOLM	2/25/2009
ENGINEER	B. HASKETT	2/25/2009
QA/CE	P. KONRAD	3/9/2009
CM		
	J. GRIMMETT	3/9/2009
APPROVED		

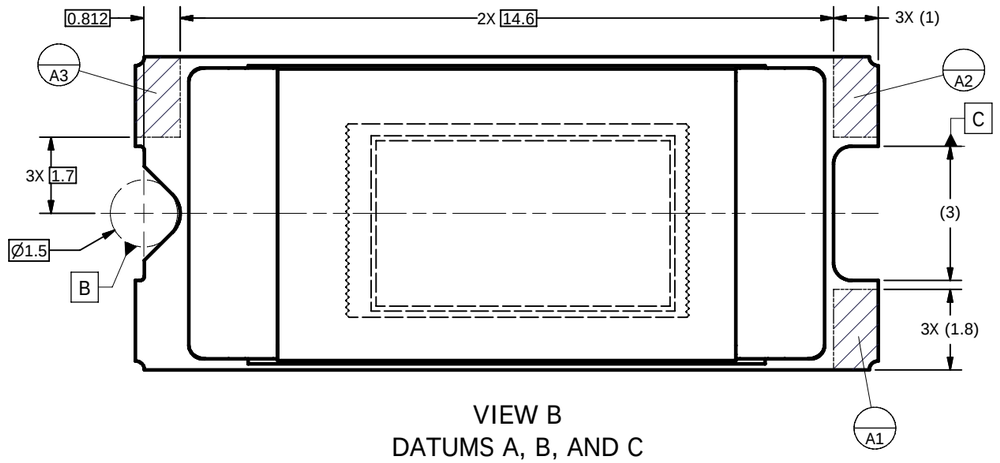
TEXAS INSTRUMENTS
Dallas Texas

TITLE
ICD, MECHANICAL, DMD,
.3 WVGA DDR SERIES 220
0.4 mm PITCH CONNECTOR

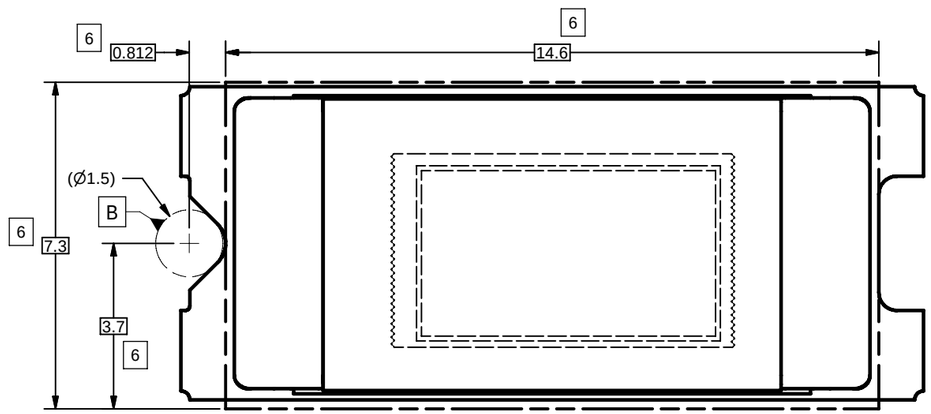
SIZE		DWG NO	REV
D		2510388	B

SCALE 15:1 SHEET 1 OF 3

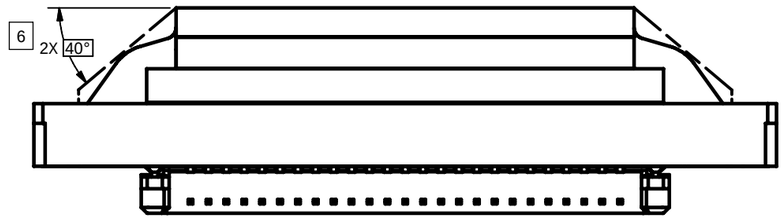
INV11-2006a



VIEW B
DATUMS A, B, AND C
(FROM SHEET 1)



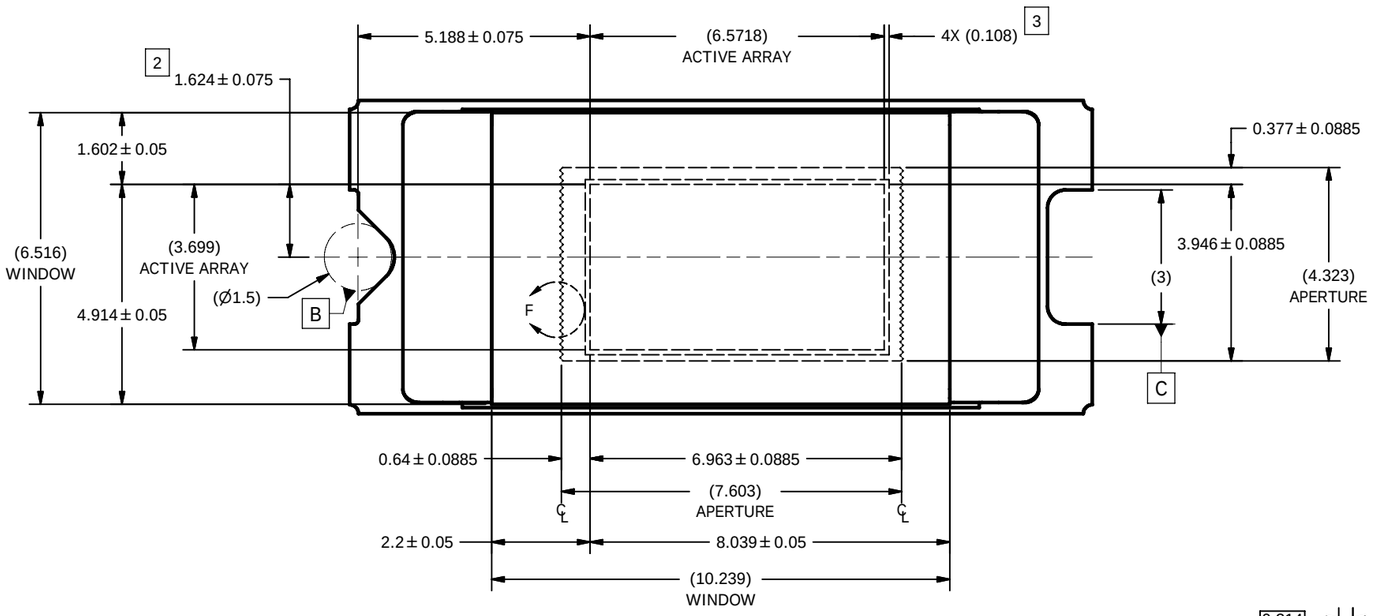
VIEW C
ENCAPSULANT MAXIMUM X/Y DIMENSIONS
(FROM SHEET 1)



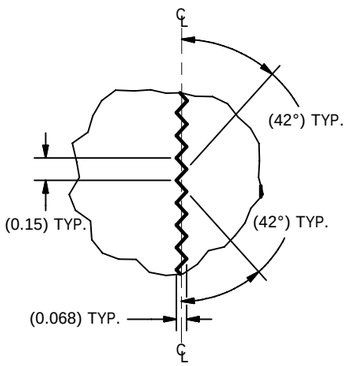
VIEW G
ENCAPSULANT HEIGHT LIMITS

TEXAS INSTRUMENTS Dallas Texas	DRAWN J. HOLM	DATE 2/25/2009	SIZE D	DWG NO 2510388	REV B
			SCALE	SHEET 2 OF 3	

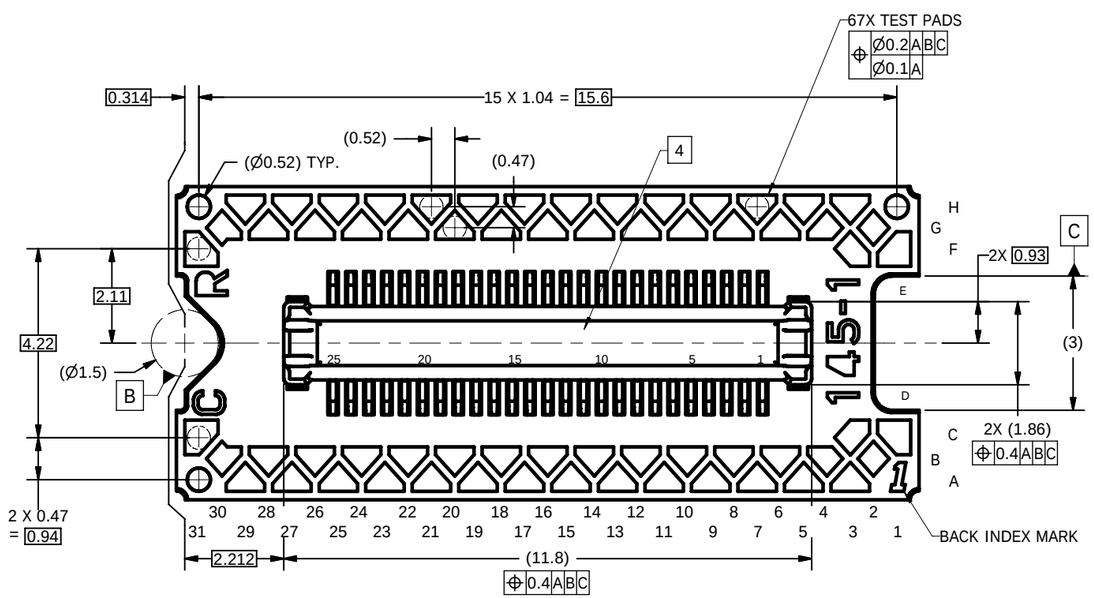
INV11-2006a



VIEW D
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



DETAIL F
APERTURE SHORT EDGES
SCALE 50 : 1



VIEW E-E
TEST PADS AND CONNECTOR
(FROM SHEET 1)

TEXAS INSTRUMENTS Dallas Texas	DRAWN J. HOLM	DATE 2/25/2009	SIZE D	DWG NO 2510388	REV B
			SCALE	SHEET 3 OF 3	

INV11-2006a

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DLP3000FQB	ACTIVE	LCCC	FQB	50	10	Green (RoHS & no Sb/Br)	Call TI	Level-1-NC-NC	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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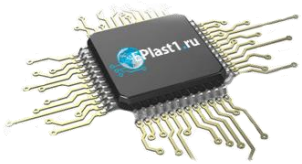
Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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