CY2SSTV855

Differential Clock Buffer/Driver

Features

- **Phase-locked loop (PLL) clock distribution for Double Data Rate Synchronous DRAM applications**
- **1:5 differential outputs**
- **External feedback pins (FBINT, FBINC) are used to synchronize the outputs to the clock input**
- **SSCG: Spread Aware™ for electromagnetic interference (EMI) reduction**
- **28-pin TSSOP package**
- **Conforms to JEDEC DDR specifications**

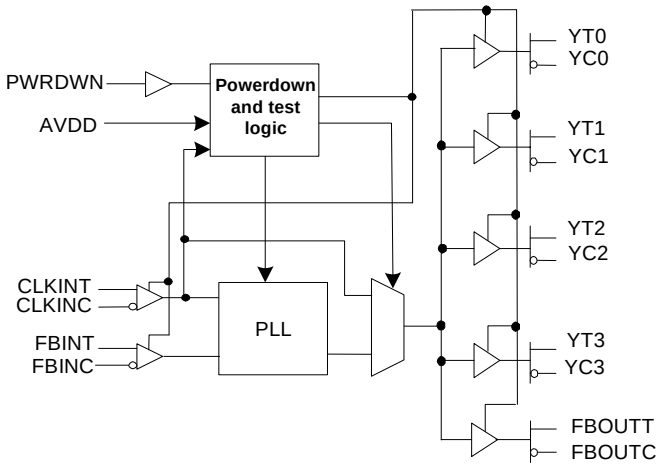
Functional Description

The CY2SSTV855 is a high-performance, very-low-skew, very-low-jitter zero-delay buffer that distributes a differential clock input pair (SSTL_2) to four differential (SSTL_2) pairs of clock outputs and one differential pair of feedback clock outputs. In support of low power requirements, when power-down is HIGH, the outputs switch in phase and frequency with the input clock. When power-down is LOW, all outputs are disabled to a high-impedance state and the PLL is shut down.

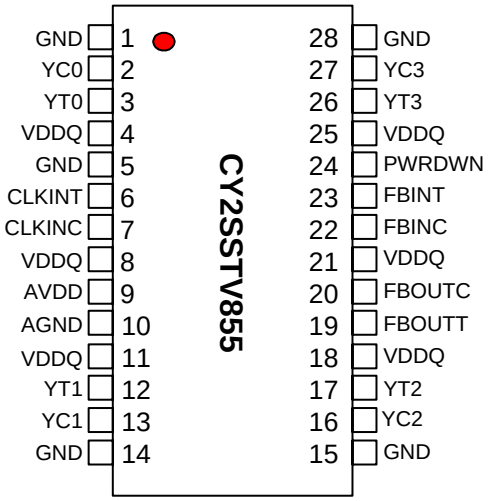
The device supports a low-frequency power-down mode. When the input is < 20 MHz, the PLL is disabled and the outputs are put in the Hi-Z state. When the input frequency is > 20 MHz, the PLL and outputs are enabled.

When AVDD is tied to ground, the PLL is turned off and bypassed with the input reference clock gated to the outputs. The Cypress CY2SSTV855 is Spread Aware and supports tracking of Spread Spectrum clock inputs to reduce EMI

Block Diagram



Pin Configuration



28-pin TSSOP

Pin Definition[1, 2]

Pin	Name	I/O	Description
6	CLKINT	I	**True Clock Input**. Low Voltage Differential True Clock Input.
7	CLKINC	I	**Complementary Clock Input**. Low Voltage Differential Complementary Clock Input.
22	FBINC	I	**Feedback Complementary Clock Input**. Differential Input Connect to FBOUTC for accessing the PLL.
23	FBINT	I	**Feedback True Clock Input**. Differential Input Connect to FBOUTT for accessing the PLL.
3,12,17,26	YT(0:3)	O	**True Clock Outputs**. Differential Outputs.
2,13,16,27	YC(0:3)	O	**Complementary Clock Outputs.** Differential Outputs.
19	FBOUTT	O	**Feedback True Clock Output**. Differential Outputs. Connect to FBINT for normal operation. A bypass delay capacitor at this output will control Input Reference/Output Clocks phase relationships.
20	FBOUTC	O	**Feedback Complementary Clock Output**. Differential Outputs. Connect to FBINC for normal operation. A bypass delay capacitor at this output will control Input Reference/Output Clocks phase relationships.
24	PWRDWN	I	**Control input to turn device in the power-down mode**.
4,8,11,18,21,25	VDDQ		**2.5V Power Supply for Output Clock Buffers**.2.5V Nominal.
9	AVDD		**2.5V Power Supply for PLL.** 2.5V Nominal.
1,5,14,15,28	GND		**Ground**
10	AGND		**Analog Ground**. 2.5V Analog Ground.

Zero-delay Buffer

When used as a zero-delay buffer the CY2SSTV855 will likely be in a nested clock tree application. For these applications the CY2SSTV855 offers a differential clock input pair as a PLL reference. The CY2SSTV855 then can lock onto the reference and translate with near zero delay to low-skew outputs. For normal operation, the external feedback differential input, FBINT/C, is connected to the feedback output, FBOUTT/C. By connecting the feedback output to the feedback input the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs.

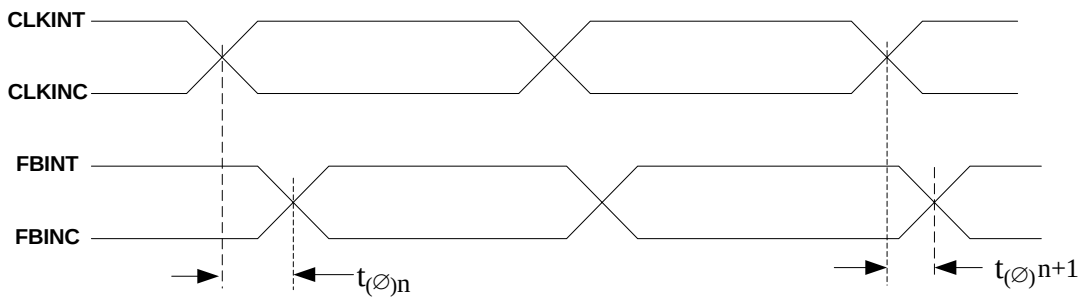
When AVDD is strapped LOW, the PLL is turned off and bypassed for test purposes.

Function Table

Inputs				Outputs				
AVDD	**PWRDWN**	**CLKINT**	**CLKINC**	**YT(0:3)**	**YC(0:3)**	**FBOUTT**	**FBOUTC**	**PLL**
GND	H	L	H	L	H	L	H	BYPASSED/OFF
GND	H	H	L	H	L	H	L	BYPASSED/OFF
2.5V	H	L	H	L	H	L	H	On
2.5V	H	H	L	H	L	H	L	On
2.5V	X	< 20 MHz	< 20 MHz	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Off

Notes:
1. PU = internal pull-up.
2. A bypass capacitor (0.1µF) should be placed as close as possible to each positive power pin (< 0.2”). If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductance of the traces.

Differential Parameter Measurement Information



$$t_{(\varnothing)n} = \frac{\sum_{1}^{n=N} t_{(\varnothing)n}}{N} \quad \text{N (is large number of samples)}$$

Figure 1. Static Phase Offset

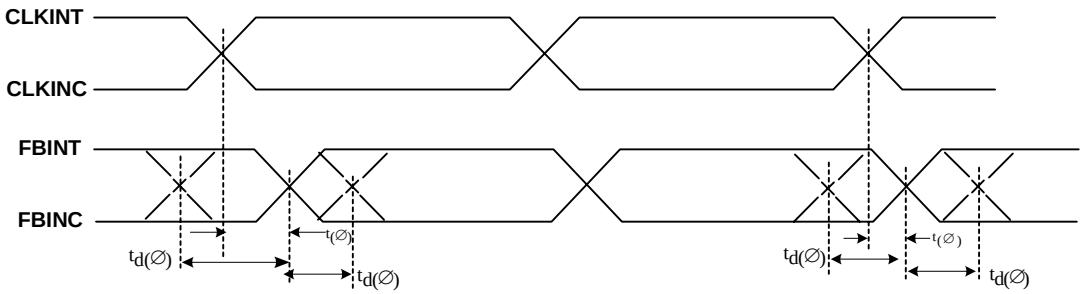


Figure 2. Dynamic Phase Offset

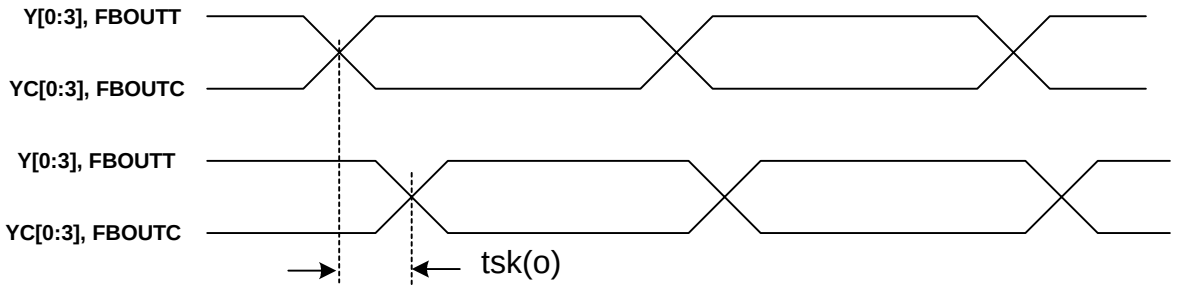


Figure 3. Output Skew

Differential Parameter Measurement Information (continued)

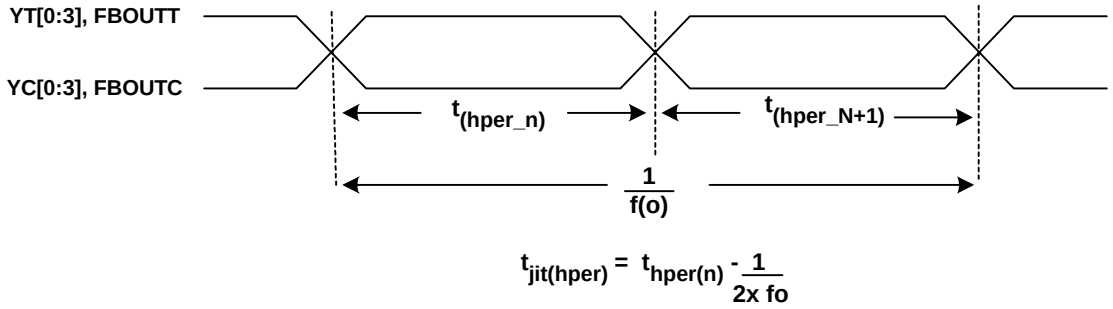


Figure 4. Half-period Jitter

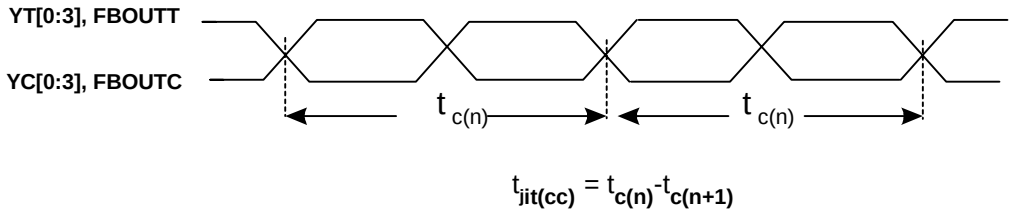


Figure 5. Cycle-to-cycle Jitter

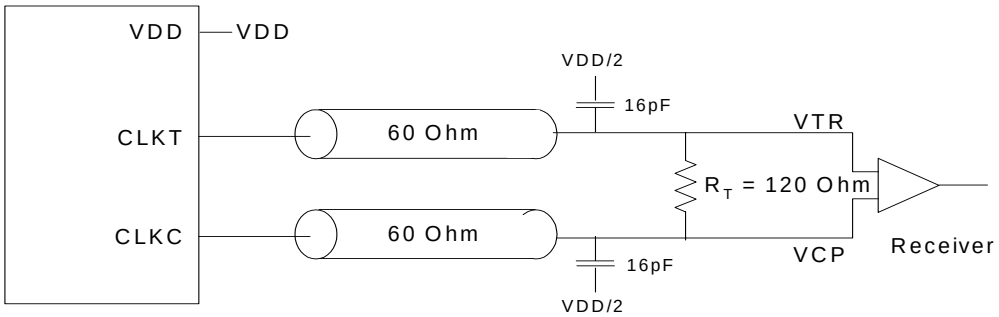


Figure 6. Differential Signal Using Direct Termination Resistor

Absolute Maximum Conditions[3]

Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V

Input Voltage Relative to V_{DDQ} or AV_{DD}: ..... V_{DD} + 0.3V

Storage Temperature: ..... –65°C to + 150°C

Operating Temperature: ..... –40°C to +85°C

Maximum Power Supply: 3.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in}$ or $V_{out}) < V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Electrical Specifications ($AV_{DD} = V_{DDQ} = 2.5V \pm 5\%$, T_A = –40°C to +85°C)[4]

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{ID}	Differential Input Voltage[5]	CLKINT, FBINT	0.36		V_{DDQ} + 0.6	V
V_{IX}	Differential Input Crossing Voltage[6]	CLKTIN, FBINT	(V_{DDQ}/2) – 0.2	V_{DDQ}/2	(V_{DDQ}/2) + 0.2	V
I_{IN}	Input Current	V_{IN} = 0V or $V_{IN} = V_{DDQ}$, CLKINT, FBINT	–10	–	10	µA
I_{OL}	Output Low Current	V_{DDQ} = 2.375V, V_{OUT} = 1.2V	26	35	–	mA
I_{OH}	Output High Current	V_{DDQ} = 2.375V, V_{OUT} = 1V	–18	–32	–	mA
V_{OL}	Output Low Voltage	V_{DDQ} = 2.375V, I_{OL} = 12 mA		–	0.6	V
V_{OH}	Output High Voltage	V_{DDQ} = 2.375V, I_{OH} = –12 mA	1.7	–	–	V
V_{OUT}	Output Voltage Swing[7]		1.1	–	V_{DDQ} – 0.4	V
V_{OC}	Output Crossing Voltage[8]		(V_{DDQ}/2) – 0.2	V_{DDQ}/2	(V_{DDQ}/2) + 0.2	V
I_{OZ}	High-Impedance Output Current	V_O = GND or $V_O = V_{DDQ}$	–10		10	µA
I_{DDQ}	Dynamic Supply Current[9]	V_{DDQ} = 170 MHz	–	235	300	mA
I_{DD}	PLL Supply Current	AV_{DD} only	–	9	12	mA
Cin	Input Pin Capacitance		–	4	–	pF

AC Electrical Specifications ($AV_{DD} = V_{DDQ} = 2.5V \pm 5\%$, T_A = –40°C to +85°C)[10, 11]

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
f_{CLK}	Operating Clock Frequency	$AV_{DD} = 2.5V \pm 0.2V$	60		170	MHz
t_{DC}	Input Clock Duty Cycle[12]		40		60	%
t_{LOCK}	Maximum PLL lock Time				100	µs
$t_{SL(O)}$	Output Clocks Slew Rate	20% to 80% of VOD	1		2	V/ns
t_{PZL}, t_{PZH}	Output Enable Time (all outputs)[13]			30		ns
t_{PLZ}, t_{PHZ}	Output Disable Time (all outputs)[13]			10		ns
t_{CCJ}	Cycle to Cycle Jitter	f > 66 MHz	–100		100	ps
$t_{JITT(H-PER)}$	Half-period jitter	f > 66 MHz	–100		100	ps

Notes:

3. **Multiple Supplies**: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
4. Unused inputs must be held HIGH or LOW to prevent them from floating.
5. Differential input signal voltage specifies the differential voltage |VTR – VCP| required for switching, where VTR is the true input level and VCP is the complementary input level.
6. Differential cross-point input voltage is expected to track V_{DDQ} and is the voltage at which the differential signals must be crossing.
7. For load conditions see *Figure 6*.
8. The value of V_{OC} is expected to be |VTR + VCP|/2. In case of each clock directly terminated by a 120Ω resistor. See *Figure 6*.
9. All outputs switching loaded with 16 pF in 60Ω environment. See *Figure 6*.
10. Parameters are guaranteed by design and characterization. Not 100% tested in production.
11. PLL is capable of meeting the specified parameters while supporting SSC synthesizers with modulation frequency between 30 kHz and 33.3 kHz with a downspread of –0.5%
12. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle = t_{WH}/t_C, where the cycle time (t_C) decreases as the frequency goes up.
13. Refers to transition of non-inverting output.
14. All differential input and output terminals are terminated with 120Ω/16 pF as shown in *Figure 6*.

AC Electrical Specifications (AV_{DD} = V_{DDQ} = 2.5V±5%, T_A = –40°C to +85°C)[10, 11] (continued)

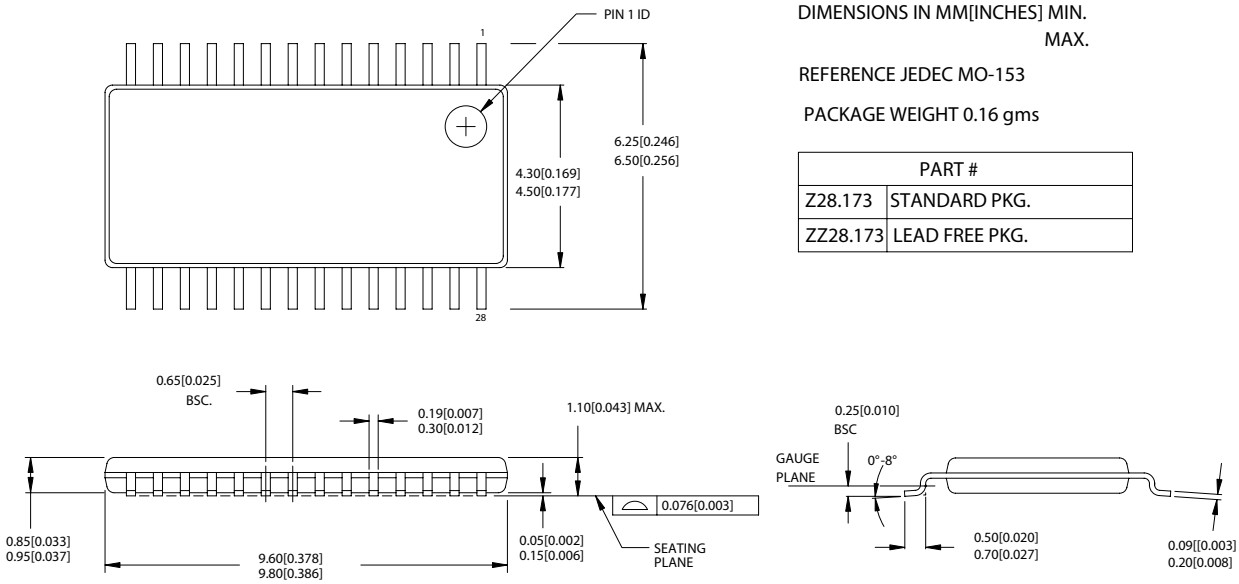
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
t_{PLH}	Low-to-High Propagation Delay, CLKINT to YT[0:3]		1.5	3.5	6	ns
t_{PHL}	High-to-Low Propagation Delay, CLKINT to YT[0:3]		1.5	3.5	6	ns
$t_{SK(0)}$	Any Output to Any Output Skew[14]		–	–	100	ps
$t_{(Ø)}$	Static Phase Offset[14]		–450	–	450	ps
$t_{D(Ø)}$	Dynamic Phase Offset	f > 66 MHz	–350	–	350	ps

Ordering Information

Part Number	Package Type	Product Flow
CY2SSTV855ZC	28-pin TSSOP	Commercial, 0° to 70°C
CY2SSTV855ZCT	28-pin TSSOP – Tape and Reel	Commercial, 0° to 70°C
CY2SSTV855ZI	28-pin TSSOP	Industrial, –40° to 85°C
CY2SSTV855ZIT	28-pin TSSOP – Tape and Reel	Industrial,–40° to 85°C
Lead Free		
CY2SSTV855ZXC	28-pin TSSOP	Commercial, 0° to 70°C
CY2SSTV855ZXCT	28-pin TSSOP – Tape and Reel	Commercial, 0° to 70°C
CY2SSTV855ZXI	28-pin TSSOP	Industrial, –40° to 85°C
CY2SSTV855ZXIT	28-pin TSSOP – Tape and Reel	Industrial,–40° to 85°C

Package Drawing and Dimensions

28-Lead Thin Shrunk Small Outline Package (4.40-mm Body) Z28.173



DIMENSIONS IN MM[INCHES] MIN.
MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.16 gms

PART #	
Z28.173	STANDARD PKG.
ZZ28.173	LEAD FREE PKG.

51-85120-*A

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Document History Page

Document Title: CY2SSTV855 Differential Clock Buffer/Driver Document #: 38-07459				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	117544	09/09/02	HWT	New data sheet
*A	122934	12/18/02	RBI	Add power up requirements to maximum ratings information
*B	124087	04/23/03	RGL	Changed the package drawing and dimension from Z28 to Z29 Corrected the block diagram Changed the Output Enable/Disable time from 3/3 to 30/10 ns Eliminated Dynamic Phase Offset spec. Changed the Phase Error Jitter spec. from ±50 to ±150 ps
*C	215389	See ECN	RGL	Added an Industrial Grade Devices (temp from –40°C to 85).
*D	224444	See ECN	RGL	Removed “PRELIMINARY”
*E	401500	See ECN	RGL	Added Lead Free Devices
*F	436956	See ECN	RGL	Changed the static and dynamic offset numbers

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