

SCSI Termpower Manager

FEATURES

- Integrated Circuit Breaker Function
- Integrated 0.2Ω Power FET
- SCSI, SCSI-2, SCSI-3 Compliant
- $1\mu\text{A}$ ICC When Disabled
- Programmable On Time
- Accurate 1.65A Trip Current and 2.0A Max Current
- Fixed 3% Duty Cycle
- Uni-Directional Switch
- Thermal Shutdown

DESCRIPTION

The UCC3916 SCSI termpower manager provides complete power management, hot swap capability, and circuit breaker functions with minimal external components. For most applications, the only external component required to operate the device, other than supply bypassing, is a timing capacitor which sets the fault time.

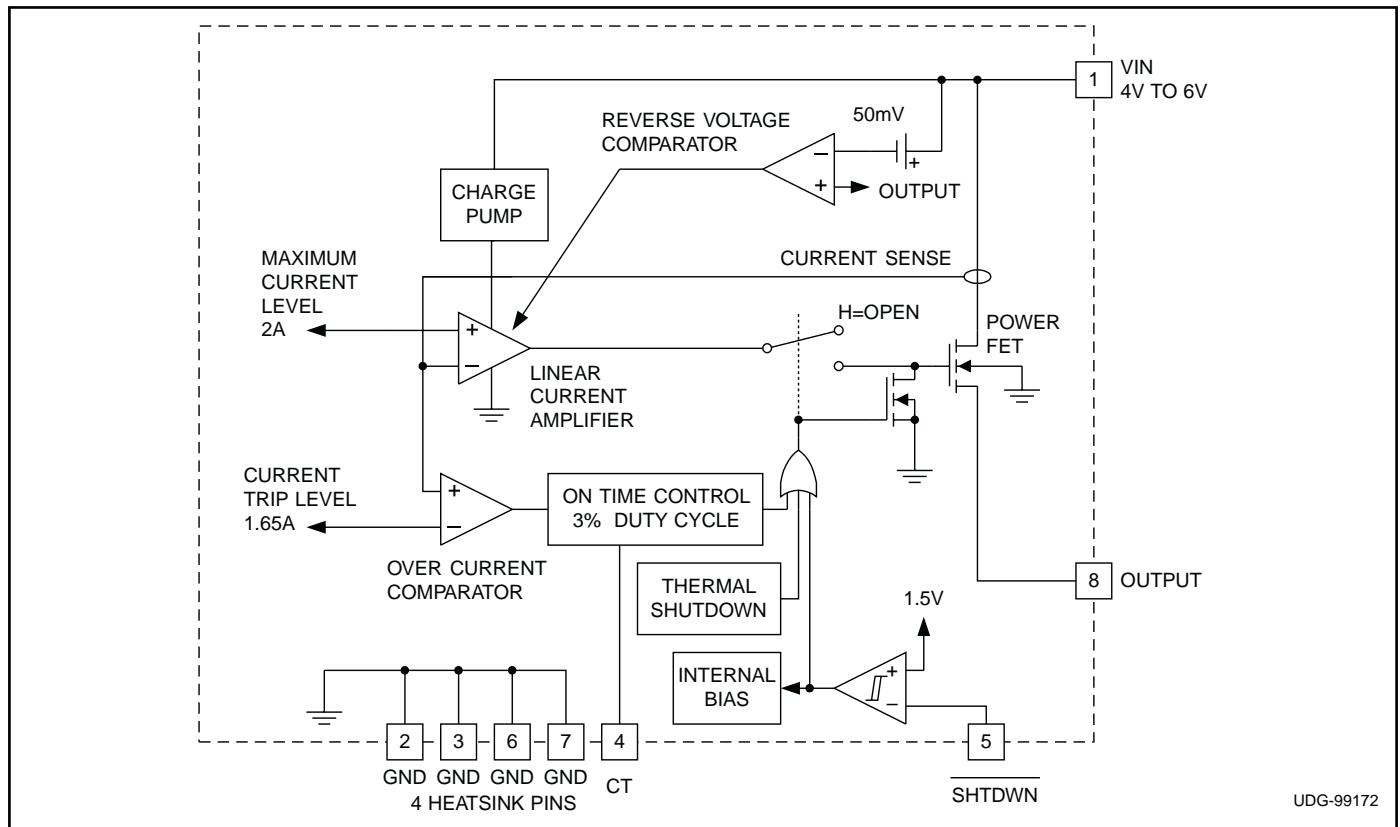
The current trip level is internally set at 1.65A, and the maximum current level is also internally programmed for 2A. While the output current is below the trip level of 1.65A, the internal power MOSFET is switched on at a nominal $220\text{m}\Omega$. When the output current exceeds the trip level but remains less than the maximum current level, the MOSFET remains switched on, but the fault timer starts charging CT. Once the fault time is reached, the circuit will shut off for a time which equates to a 3% duty cycle. Finally, when the output current reaches the maximum current level, the MOSFET transitions from a switch to a constant current source.

The UCC3916 is designed for uni-directional current flow, emulating a diode in series with the power MOSFET.

The UCC3916 can be put in a sleep mode, drawing only $1\mu\text{A}$ of supply current.

Other features include thermal shutdown and low thermal resistance Small Outline Power package.

BLOCK DIAGRAM

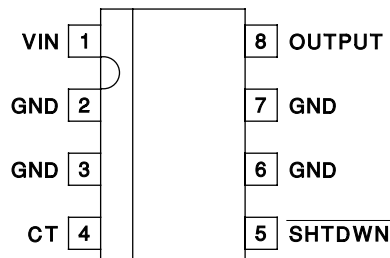


UDG-99172

ABSOLUTE MAXIMUM RATINGS

VIN +6V
 Output Current
 DC Self Limiting
 Pulse (Less than 100ns) 20A
 Storage Temperature -65°C to +150°C
 Junction Temperature -55°C to +150°C
 Lead Temperature (Soldering, 10 sec.) +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM**SOIC-8 (Top View)
DP Package**

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for $T_J = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{IN} = 5\text{V}$, $SHTDWN = 2.4\text{V}$, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
ICC			1.00	2.00	mA
ICC - Sleep Mode	$SHTDWN = 0.2\text{V}$		0.50	5	μA
Output Section					
Voltage Drop	$I_{OUT} = 1\text{A}$		0.22	0.33	V
	$I_{OUT} = 1.5\text{A}$		0.33	0.50	V
	$I_{OUT} = 1.65\text{A}$		0.40	0.60	V
Trip Current		-1.8	-1.65	-1.5	A
Max Current		-2.4	-2	-1.65	A
Reverse Leakage	$V_{IN} = 4.5\text{V}$, $V_{OUT} = 5\text{V}$		6	20	μA
	$V_{IN} = 0\text{V}$, $V_{OUT} = 5\text{V}$		0.50	9	μA
Soft Start Time	Initial Startup		50		μs
Short Circuit Response			100		ns
Fault Section					
CT Charge Current	$V_{CT} = 1.0\text{V}$	-45	-36.0	-27	μA
CT Discharge Current	$V_{CT} = 1.0\text{V}$	0.90	1.0	1.50	μA
Output Duty Cycle	$V_{OUT} = 0\text{V}$	2.00	3.00	6.00	%
CT Charge Threshold		0.4	0.5	0.6	V
CT Discharge Threshold		1.2	1.4	1.8	V
Thermal Shutdown			170		$^\circ\text{C}$
Thermal Hysteresis			10		$^\circ\text{C}$
Shutdown Section					
Shutdown Threshold			1.5	3.0	V
Shutdown Hysteresis			150	300	mV
Shutdown Bias Current	$SHTDWN = 1.0\text{V}$		100	500	nA

Note 1: All voltages are with respect to ground.

PIN DESCRIPTIONS

CT: A capacitor is applied between this pin and ground to set the maximum fault time. The maximum fault time must be more than the time to charge external capacitance. The maximum fault time is defined as:

$$T_{\text{FAULT}} = 28 \cdot 10^3 \cdot CT.$$

Once the fault time is reached the output will shutdown for a time given by:

$$T_{\text{SD}} = 1 \cdot 10^6 \cdot CT$$

this results in a 3% duty cycle. 0.1μF is recommended for SCSI applications to achieve the normal maximum capacitance on the Tempwr line.

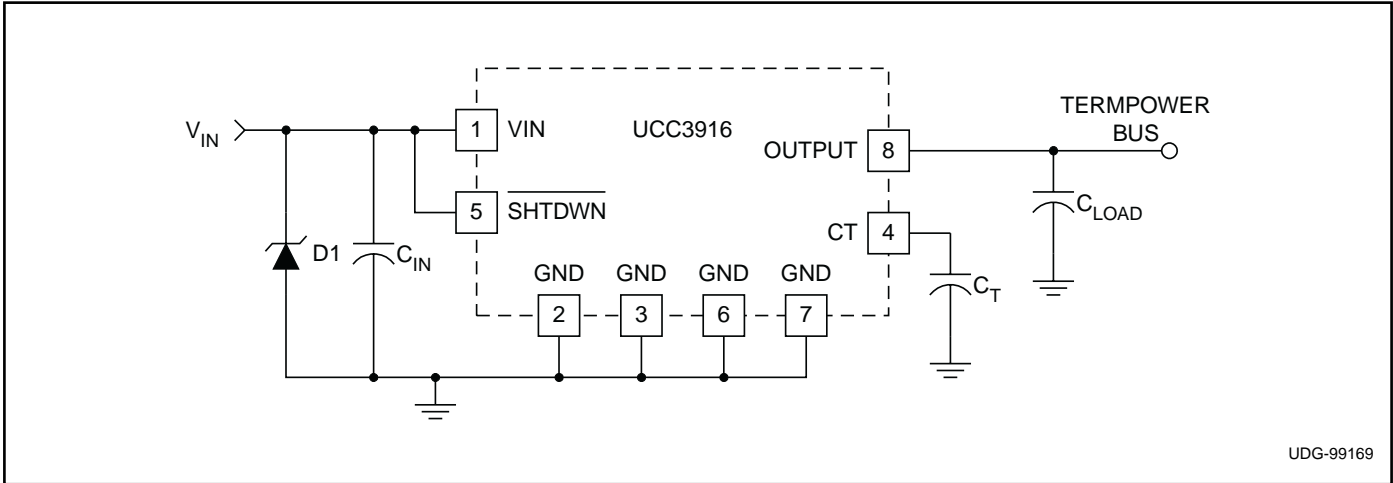
SHTDWN: The IC enters a low-power sleep mode when this pin is low and exits the sleep mode when this pin is high.

VIN: Input voltage to the circuit breaker, ranging from 4V to 6V.

VOUT: Output voltage of the circuit breaker. When switched, the output voltage is approximately:

$$V_{\text{OUT}} = V_{\text{IN}} - (220\text{m}\Omega) \cdot I_{\text{OUT}}.$$

TYPICAL APPLICATION



APPLICATION INFORMATION

Protecting The UCC3916 From Voltage Transients

The parasitic inductance associated with the power distribution can cause a voltage spike at VIN if the load current is suddenly interrupted by the UCC3916. *It is important to limit the peak of this spike to less than 6V to prevent damage to the UCC3916.* This voltage spike can be minimized by:

- Reducing the power distribution inductance (e.g., twist the positive (+) and negative (-) leads of the power supply feeding VIN, locate the power supply close to the UCC3916 or use a PCB ground plane).
- Decoupling VIN with a capacitor, CIN, located close to the VIN. This capacitor is typically less than 1μF to limit the inrush current.
- Clamping the voltage at VIN below 6V with a Zener diode, D1, located close to the VIN pin.

SAFETY RECOMMENDATIONS

Although the UCC3916 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3916 is intended for use in safety critical applications where UL[®] or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3916 will prevent the fuse from blowing virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
UCC3916DP	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3916DPG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3916DPTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3916DPTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

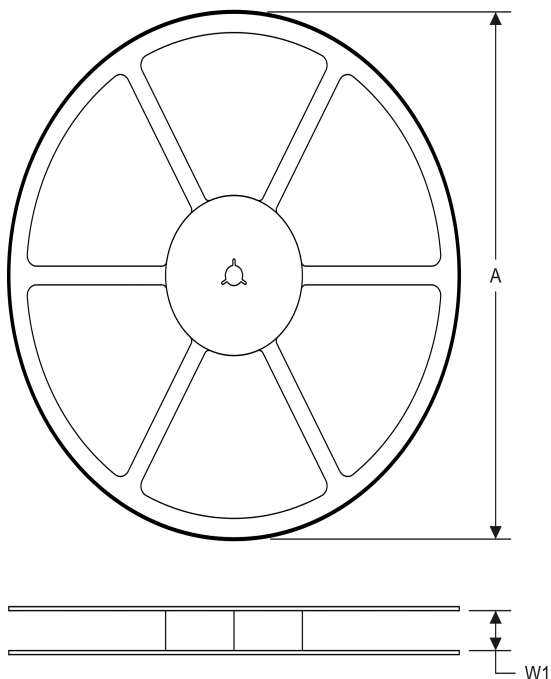
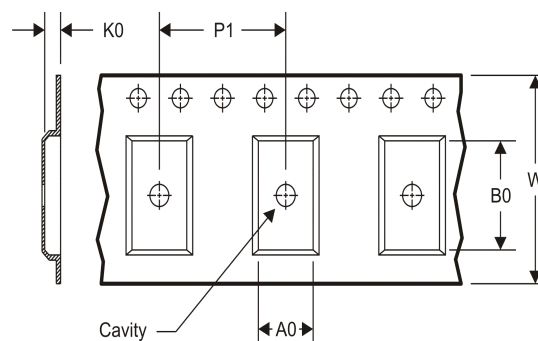
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


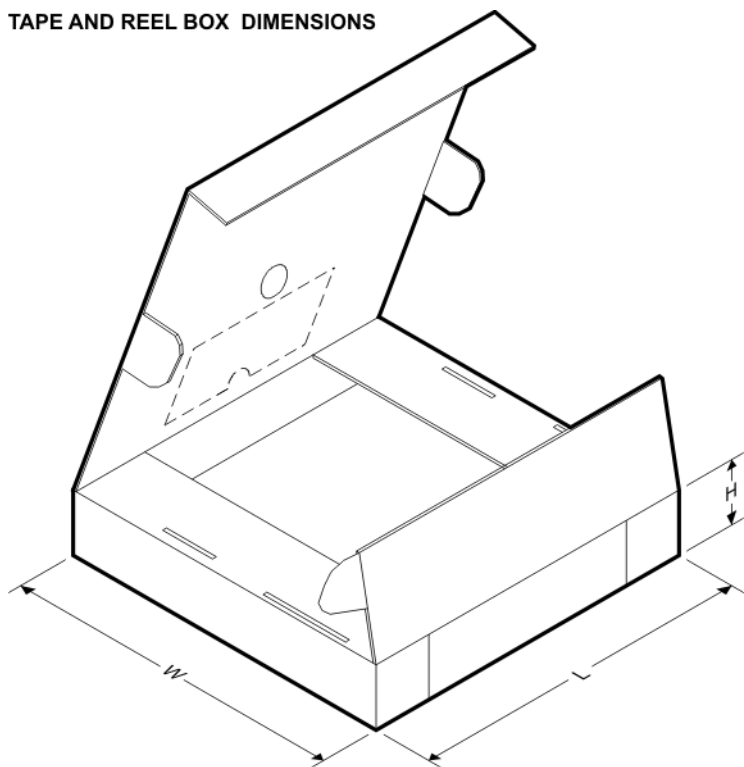
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC3916DPTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC3916DPTR	SOIC	D	8	2500	367.0	367.0	35.0

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Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.