

## Low Power, High Voltage SPST Analog Switches

### DESCRIPTION

The DG447, DG448 are dual supply single-pole/single-throw (SPST) switches. On resistance is 25  $\Omega$  maximum and flatness is 2.2  $\Omega$  max over the specified analog signal range. These analog switches were designed to provide high speed, low error switching of precision analog signals. The primary application areas are in the routing and switching in telecommunications and test equipment. Combining low power, low leakages, low on-resistance and small physical size, the DG477, DG448 are also ideally suited for portable and battery powered industrial and military equipment.

The DG477 has one normally closed switch, while the DG448 switch is normally open. They operate either from a single + 7 V to 36 V supply or from dual  $\pm 4.5$  V to  $\pm 20$  V supplies. They are offered in the very popular, small TSOP6 package.

### FEATURES

- $\pm 15$  V analog signal range
- On-resistance -  $R_{DS(on)}$ : 25  $\Omega$  max.
- Fast switching action -  $t_{ON}$ : 100 ns
- $V_L$  logic supply not required
- TTL CMOS input compatible
- Rail to rail signal handling
- Dual or single supply operation
- Compliant to RoHS Directive 2002/95/EC


**RoHS**  
COMPLIANT

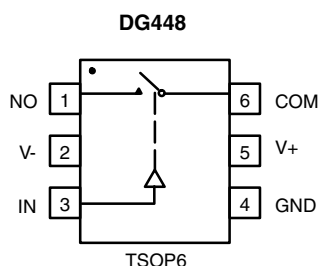
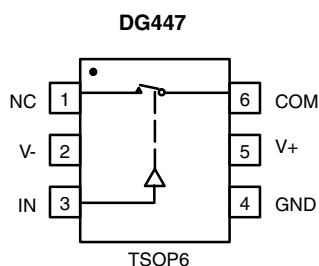
### BENEFITS

- Wide dynamic range
- Low signal errors and distortion
- Break-before-make switching action
- Simple interfacing
- Reduced board space
- Improved reliability

### APPLICATIONS

- Precision test equipment
- Precision instrumentation
- Communications systems
- PBX, PABX systems
- Audio equipment
- Redundant systems
- PC multimedia boards
- Hard disc drives

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



#### TRUTH TABLE

| Logic | DG447 | DG448 |
|-------|-------|-------|
| 0     | ON    | OFF   |
| 1     | OFF   | ON    |

Logic "0"  $\leq 0.8$  V

Logic "1"  $\geq 2.4$  V

Device Marking:

DG447DV = G5xxx

DG448DV = G6xxx

**ORDERING INFORMATION**

| Temp. Range         | Package    | Part Number   |
|---------------------|------------|---------------|
| <b>DG447, DG448</b> |            |               |
| - 40 °C to 85 °C    | 6-pin TSOP | DG447DV-T1-E3 |
|                     |            | DG448DV-T1-E3 |

**ABSOLUTE MAXIMUM RATINGS** ( $T_A = 25\text{ °C}$ , unless otherwise noted)

| Parameter Referenced to V-                                | Limit  | Unit |
|---|--|------|
| V+  | 44   | V    |
| GND   | 25   |      |
| Digital Inputs <sup>a</sup> , $V_{no/nc}$ , $V_{COM}$     | (V-) - 2 V to (V+) + 2 V<br>or 30 mA, whichever occurs first |      |
| Current, (Any Terminal) Continuous                        | 30   | mA   |
| Current (NO or NC or COM) Pulsed at 1 ms, 10 % Duty Cycle | 100  |      |
| Storage Temperature                                       | - 65 to 150  | °C   |
| Power Dissipation (Package) <sup>b</sup>                  | 6-pin TSOP <sup>c</sup>                                      | 570  |
|   |  | mW   |

Notes:

a. Signals on NO, NC, COM, or IN exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC board.

c. Derate 7 mW/°C above 70 °C.

**SPECIFICATIONS<sup>a</sup>**

| Parameter                           | Symbol                      | Test Conditions<br>Unless Otherwise Specified<br>V+ = 15 V, V- = - 15 V<br>VIN = 2.4 V, 0.8 V <sup>f</sup> | Temp. <sup>b</sup> | D Suffix<br>- 40 °C to 85 °C |                   |                   | Unit |
|-------------------------------------|-----------------------------|--|--------------------|------------------------------|-------------------|-------------------|------|
|                                     |                             |  |                    | Min. <sup>d</sup>            | Typ. <sup>c</sup> | Max. <sup>d</sup> |      |
| Analog Switch                       |                             |  |                    |                              |                   |                   |      |
| Analog Signal Range <sup>e</sup>    | V <sub>ANALOG</sub>         |  | Full               | - 15                         |                   | 15                | V    |
| Drain-Source<br>On-Resistance       | R <sub>ON</sub>             | I <sub>no/nc</sub> = 10 mA, V <sub>COM</sub> = 10 V<br>V+ = 13.5 V, V- = - 13.5 V                          | Room<br>Full       |                              | 17                | 25<br>30          | Ω    |
| On-Resistance Flatness              | R <sub>ON</sub><br>Flatness | I <sub>no/nc</sub> = 10 mA, V <sub>COM</sub> = ± 5 V, 0 V<br>V+ = 13.5 V, V- = - 13.5 V                    | Room<br>Full       |                              | 0.8               | 2.2<br>3          |      |
| Switch Off Leakage Current          | I <sub>no/nc(off)</sub>     | V+ = 16.5, V- = - 16.5 V<br>V <sub>COM</sub> = ± 15.5 V<br>V <sub>no/nc</sub> = -/+ 15.5 V                 | Room<br>Full       | - 1<br>- 10                  | - 0.1             | 1<br>10           | nA   |
|                                     | I <sub>COM(off)</sub>       |  | Room<br>Full       | - 1<br>- 10                  | - 0.1             | 1<br>10           |      |
| Channel On Leakage Current          | I <sub>COM(on)</sub>        | V+ = 16.5 V, V- = - 16.5<br>V <sub>COM</sub> = V <sub>no/nc</sub> = ± 15.5 V                               | Room<br>Full       | - 1<br>- 10                  | - 0.1             | 1<br>10           |      |
| Digital Control                     |                             |  |                    |                              |                   |                   |      |
| Input, High Voltage                 | I <sub>INH</sub>            |  | Full               | 2.4                          |                   |                   | V    |
| Input, Low Voltage                  | I <sub>INL</sub>            |  | Full               |                              |                   | 0.8               |      |
| Input Capacitance <sup>e</sup>      | C <sub>IN</sub>             |  | Room               |                              | 5                 |                   | pF   |
| Input Current                       | I <sub>IN</sub>             | V <sub>IN</sub> = 0 or 5 V   |                    | - 1                          |                   | 1                 | μA   |
| Dynamic Characteristics             |                             |  |                    |                              |                   |                   |      |
| Turn-On Time                        | t <sub>ON</sub>             | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF<br>V <sub>no/nc</sub> = ± 10 V                              | Room<br>Full       |                              | 100               | 130<br>140        | ns   |
| Turn-Off Time                       | t <sub>OFF</sub>            |  | Room<br>Full       |                              | 50                | 95<br>110         |      |
| Charge Injection <sup>e</sup>       | Q                           | C <sub>L</sub> = 10 nF, V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω                                     | Room               |                              | 10                |                   | pC   |
| Off-Isolation <sup>e</sup>          | OIRR                        | C <sub>L</sub> = 5 pF, R <sub>L</sub> = 50 Ω, f = 1 MHz  | Room               |                              | - 72              |                   | dB   |
| Source Off Capacitance <sup>e</sup> | C <sub>S(off)</sub>         | f = 1 MHz  | Room               |                              | 19                |                   | pF   |
| Drain Off Capacitance <sup>e</sup>  | C <sub>D(off)</sub>         |  | Room               |                              | 8                 |                   |      |
| Channel On Capacitance <sup>e</sup> | C <sub>D(on)</sub>          | f = 1 MHz  | Room               |                              | 30                |                   |      |
| Power Supplies                      |                             |  |                    |                              |                   |                   |      |
| Positive Supply Current             | I+                          | V+ = 16.5 V, V- = - 16.5 V<br>VIN = 0 or 5 V   | Room<br>Full       |                              | 16                | 30<br>50          | μA   |
| Negative Supply Current             | I-                          |  | Room<br>Full       | - 1<br>- 10                  | - 0.02            |                   |      |

**SPECIFICATIONS<sup>a</sup>**

| Parameter                        | Symbol                      | Test Conditions<br>Unless Otherwise Specified<br>V+ = 12 V, V- = 0 V<br>VIN = 2.4 V, 0.8 V <sup>f</sup> | Temp. <sup>b</sup> | D Suffix<br>- 40 °C to 85 °C |                   |                   | Unit |
|----------------------------------|-----------------------------|---|--------------------|------------------------------|-------------------|-------------------|------|
|                                  |                             |   |                    | Min. <sup>d</sup>            | Typ. <sup>c</sup> | Max. <sup>d</sup> |      |
| Analog Switch                    |                             |   |                    |                              |                   |                   |      |
| Analog Signal Range <sup>e</sup> | V <sub>ANALOG</sub>         |   | Full               | 0                            |                   | 12                | V    |
| Drain-Source On-Resistance       | R <sub>ON</sub>             | I <sub>no/nc</sub> = - 10 mA, V <sub>COM</sub> = 8 V<br>V+ = 10.8 V                                     | Room<br>Full       |                              | 32                | 45<br>60          | Ω    |
| On-Resistance Flatness           | R <sub>ON</sub><br>Flatness | I <sub>no/nc</sub> = 10 mA, V <sub>COM</sub> = 2, 6, 8 V<br>V+ = 10.8 V                                 | Room<br>Full       |                              | 2                 | 6<br>8            | Ω    |
| Dynamic Characteristics          |                             |   |                    |                              |                   |                   |      |
| Turn-On Time                     | t <sub>ON</sub>             | V <sub>NO, NC</sub> = ± 10 V, R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF                            | Room<br>Full       |                              | 140               | 175<br>225        | nS   |
| Turn-Off Time                    | t <sub>OFF</sub>            |   | Room<br>Full       |                              | 50                | 120<br>150        |      |
| Charge Injection <sup>e</sup>    | Q                           | C <sub>L</sub> = 10 nF, V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω                                  | Room               |                              | 12                |                   | pC   |
| Power Supplies                   |                             |   |                    |                              |                   |                   |      |
| Positive Supply Current          | I+                          | V+ = 13.2 V, VIN = 0 V, 5 V   | Room<br>Full       |                              | 22                | 50<br>75          | μA   |

Notes:

a. Refer to PROCESS OPTION FLOWCHART.

b. Room = 25 °C, full = as determined by the operating temperature suffix.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

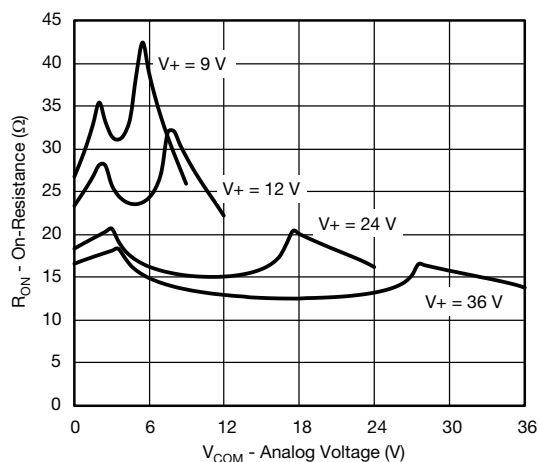
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

e. Guaranteed by design, not subject to production test.

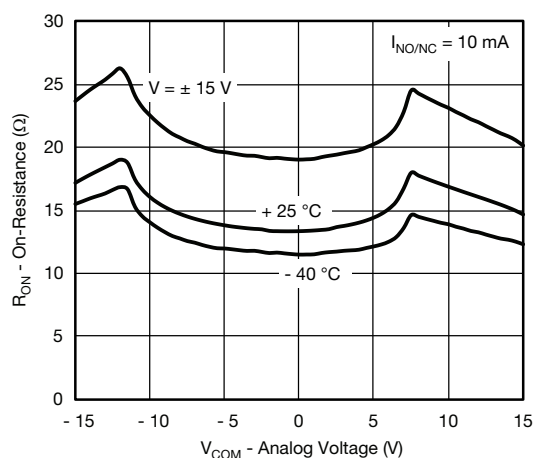
f.  $V_{IN}$  = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

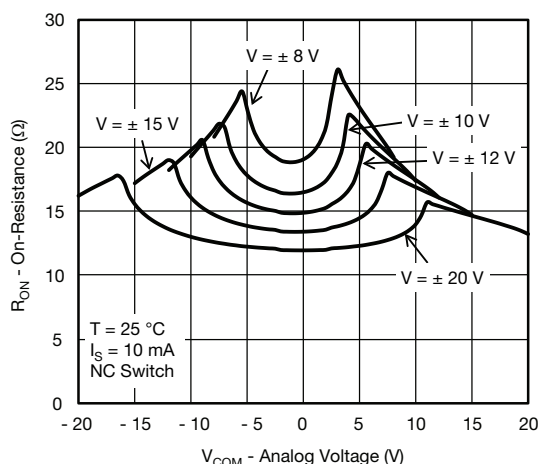
## TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



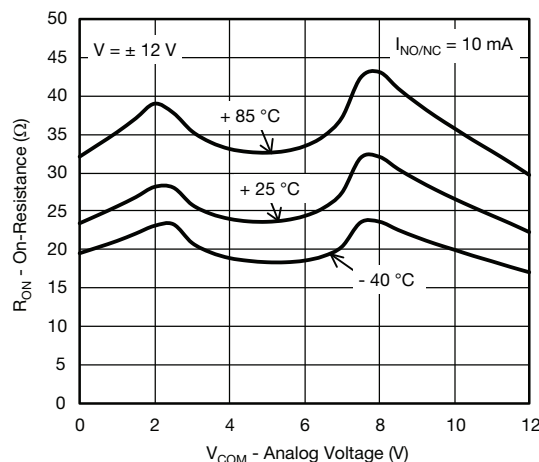
$R_{ON}$  vs.  $V_{COM}$  and Single Supply Voltage



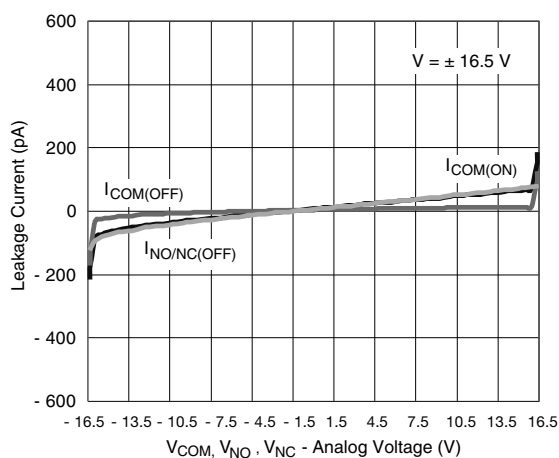
$R_{ON}$  vs. Analog Voltage and Temperature



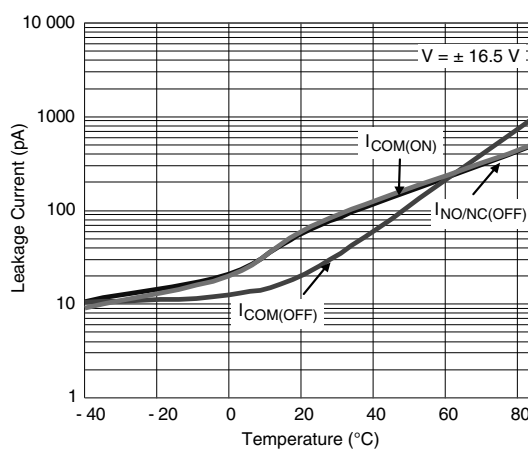
$R_{ON}$  vs.  $V_{COM}$  and Dual Supply Voltage



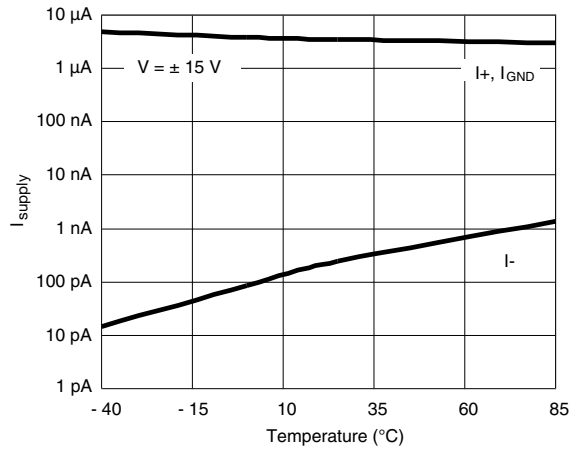
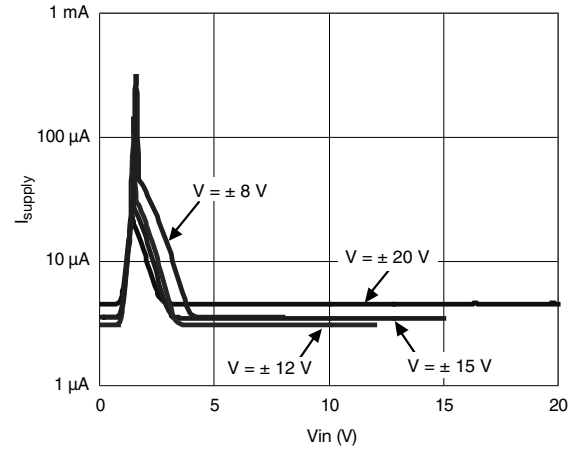
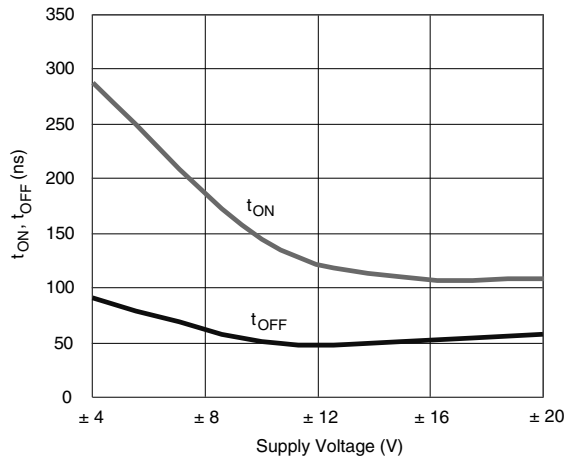
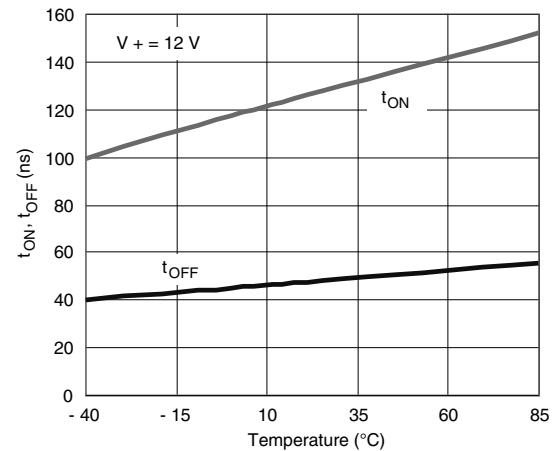
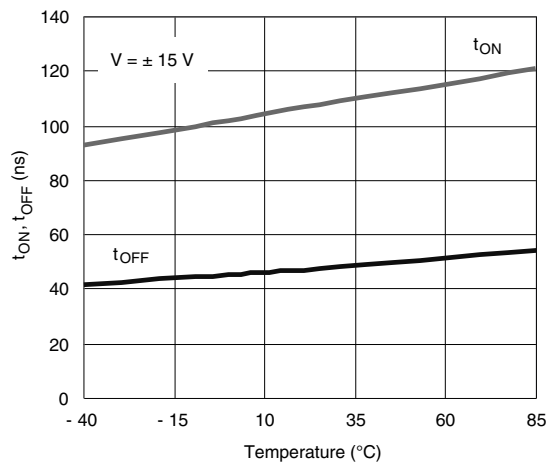
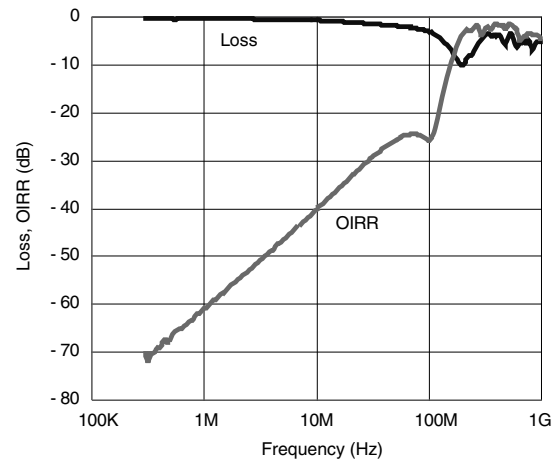
$R_{ON}$  vs. Analog Voltage and Temperature



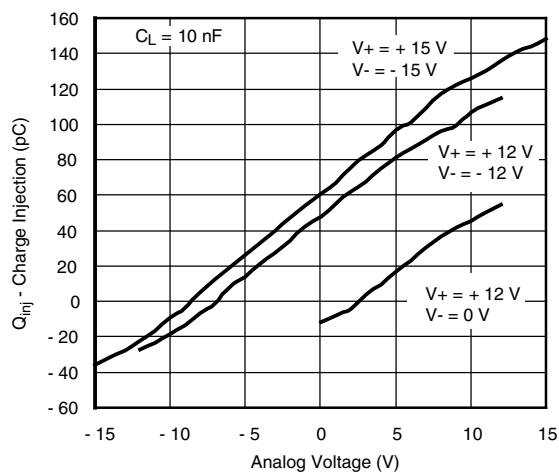
Leakage vs. Analog Voltage



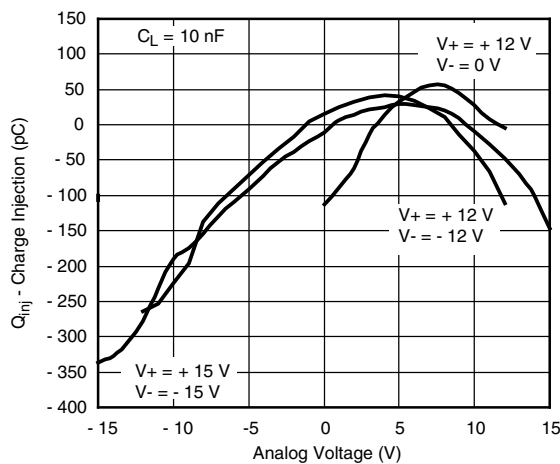
Leakage Current vs. Temperature

**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

**Supply Current vs. Temperature**

**Supply Current vs.  $V_{\text{IN}}$** 

**Switching Time vs. Supply Voltages**

**Switching Time vs. Temperature**

**Switching Time vs. Temperature**

**Off Isolation and Insertion Loss vs. Frequency**

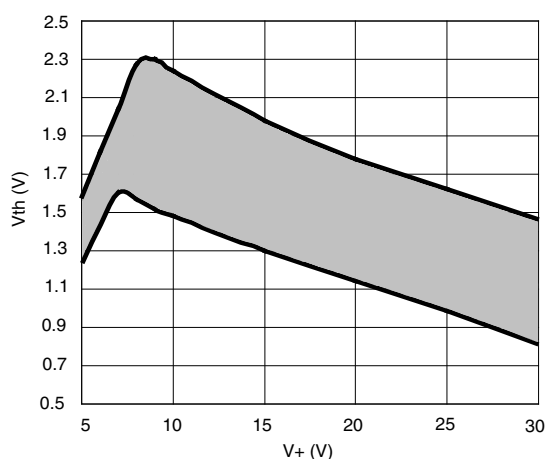
## TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



Charge Injection vs. Analog Voltage  
(Measured at COM pin)



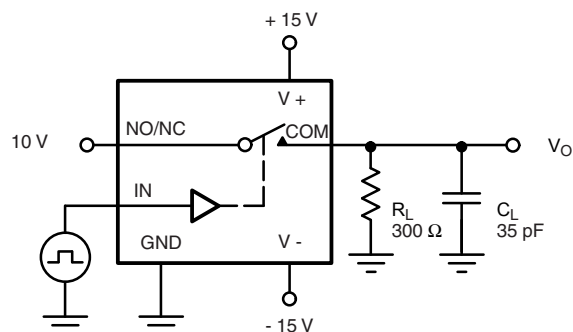
Charge Injection vs. Analog Voltage  
(Measured at NC or NO pin)



Input Switching Threshold vs. Supply Voltage

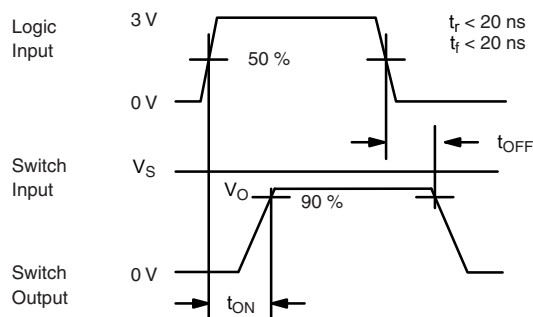
## TEST CIRCUITS

$V_O$  is the steady state output with the switch on.



$C_L$  (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{ON}}$$



Note: Logic input waveform is inverted for switches that have the opposite logic sense.

Figure 1. Switching Time

## TEST CIRCUITS

$V_O$  is the steady state output with the switch on.

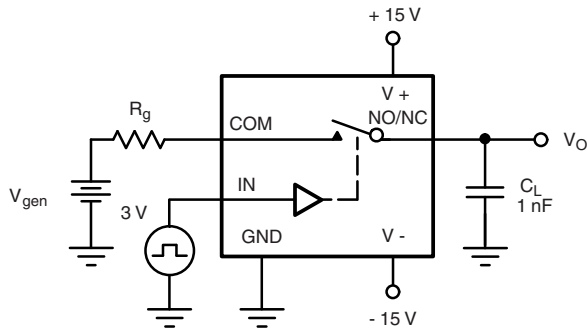


Figure 2. Charge Injection

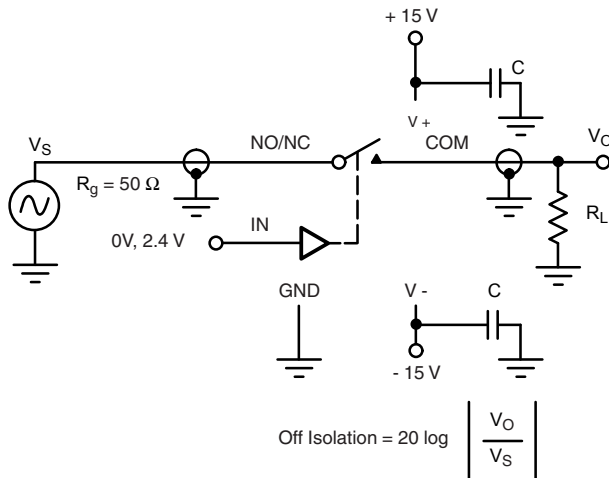
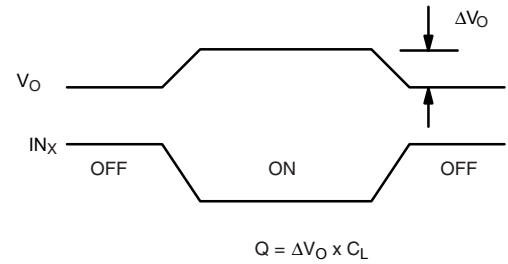


Figure 3. Off Isolation

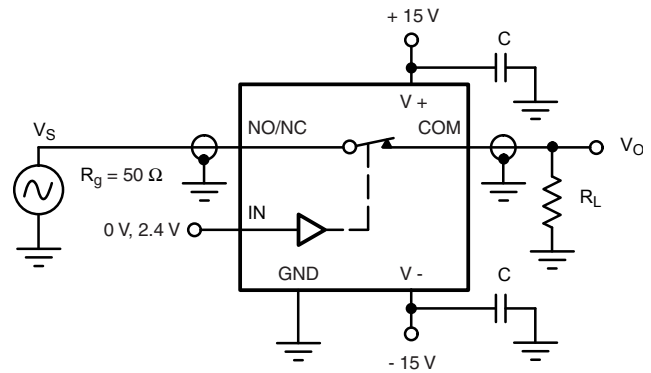


Figure 4. Insertion Loss

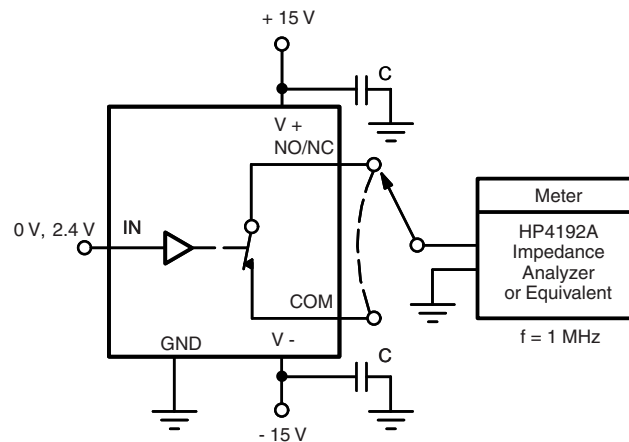
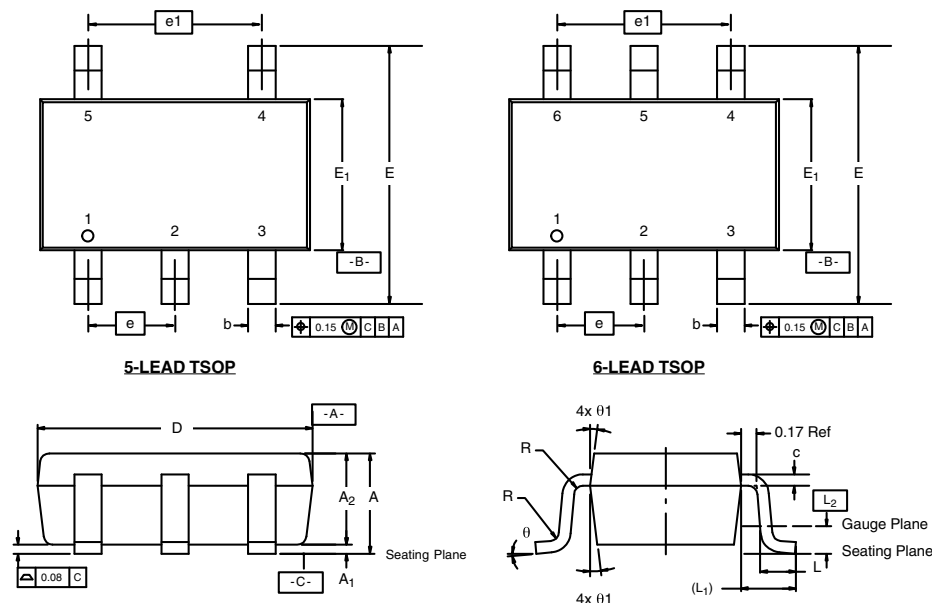


Figure 5. Source/Drain Capacitances

**TSOP: 5/6-LEAD**  
JEDEC Part Number: MO-193C



| DIM.           | MILLIMETERS |      |      | INCHES     |       |       |
|----------------|-------------|------|------|------------|-------|-------|
|                | MIN.        | NOM. | MAX. | MIN.       | NOM.  | MAX.  |
| A              | 0.91        | -    | 1.10 | 0.036      | -     | 0.043 |
| A <sub>1</sub> | 0.01        | -    | 0.10 | 0.0004     | -     | 0.004 |
| A <sub>2</sub> | 0.90        | -    | 1.00 | 0.035      | 0.038 | 0.039 |
| b              | 0.30        | 0.32 | 0.45 | 0.012      | 0.013 | 0.018 |
| c              | 0.10        | 0.15 | 0.20 | 0.004      | 0.006 | 0.008 |
| D              | 2.95        | 3.05 | 3.10 | 0.116      | 0.120 | 0.122 |
| E              | 2.70        | 2.85 | 2.98 | 0.106      | 0.112 | 0.117 |
| E <sub>1</sub> | 1.55        | 1.65 | 1.70 | 0.061      | 0.065 | 0.067 |
| e              | 0.95 BSC    |      |      | 0.0374 BSC |       |       |
| e <sub>1</sub> | 1.80        | 1.90 | 2.00 | 0.071      | 0.075 | 0.079 |
| L              | 0.32        | -    | 0.50 | 0.012      | -     | 0.020 |
| L <sub>1</sub> | 0.60 Ref.   |      |      | 0.024 Ref. |       |       |
| L <sub>2</sub> | 0.25 BSC    |      |      | 0.010 BSC  |       |       |
| R              | 0.10        | -    | -    | 0.004      | -     | -     |
| θ              | 0°          | 4°   | 8°   | 0°         | 4°    | 8°    |
| θ <sub>1</sub> | 7° Nom.     |      |      | 7° Nom.    |       |       |

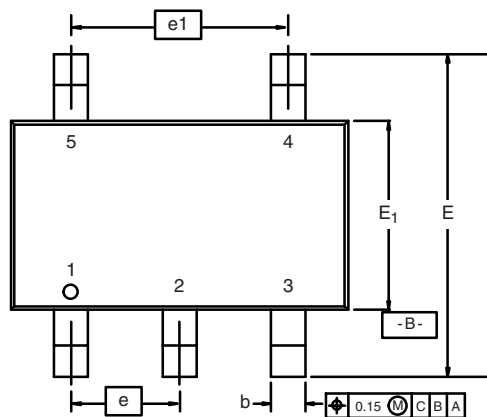
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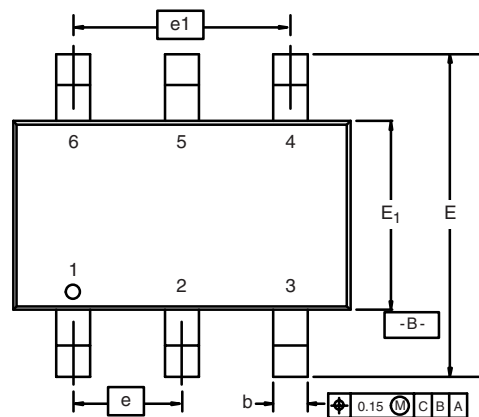


## TSOP: 5/6-LEAD

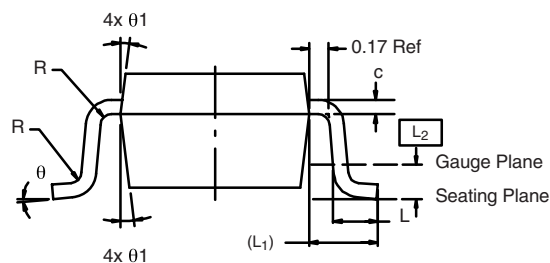
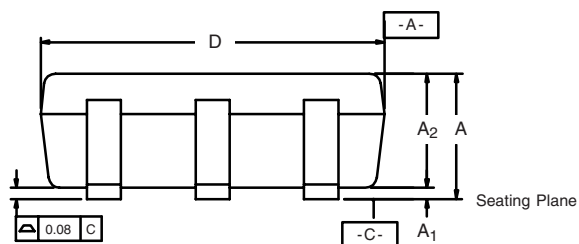
JEDEC Part Number: MO-193C



5-LEAD TSOP



6-LEAD TSOP



|                                | MILLIMETERS |      |      | INCHES     |       |       |
|--------------------------------|-------------|------|------|------------|-------|-------|
| Dim                            | Min         | Nom  | Max  | Min        | Nom   | Max   |
| A                              | 0.91        | -    | 1.10 | 0.036      | -     | 0.043 |
| A <sub>1</sub>                 | 0.01        | -    | 0.10 | 0.0004     | -     | 0.004 |
| A <sub>2</sub>                 | 0.90        | -    | 1.00 | 0.035      | 0.038 | 0.039 |
| b                              | 0.30        | 0.32 | 0.45 | 0.012      | 0.013 | 0.018 |
| c                              | 0.10        | 0.15 | 0.20 | 0.004      | 0.006 | 0.008 |
| D                              | 2.95        | 3.05 | 3.10 | 0.116      | 0.120 | 0.122 |
| E                              | 2.70        | 2.85 | 2.98 | 0.106      | 0.112 | 0.117 |
| E <sub>1</sub>                 | 1.55        | 1.65 | 1.70 | 0.061      | 0.065 | 0.067 |
| e                              | 0.95 BSC    |      |      | 0.0374 BSC |       |       |
| e <sub>1</sub>                 | 1.80        | 1.90 | 2.00 | 0.071      | 0.075 | 0.079 |
| L                              | 0.32        | -    | 0.50 | 0.012      | -     | 0.020 |
| L <sub>1</sub>                 | 0.60 Ref    |      |      | 0.024 Ref  |       |       |
| L <sub>2</sub>                 | 0.25 BSC    |      |      | 0.010 BSC  |       |       |
| R                              | 0.10        | -    | -    | 0.004      | -     | -     |
| θ                              | 0°          | 4°   | 8°   | 0°         | 4°    | 8°    |
| θ <sub>1</sub>                 | 7° Nom      |      |      | 7° Nom     |       |       |
| ECN: C-06593-Rev. I, 18-Dec-06 |             |      |      |            |       |       |
| DWG: 5540                      |             |      |      |            |       |       |

## Mounting LITTLE FOOT® TSOP-6 Power MOSFETs

Surface mounted power MOSFET packaging has been based on integrated circuit and small signal packages. Those packages have been modified to provide the improvements in heat transfer required by power MOSFETs. Leadframe materials and design, molding compounds, and die attach materials have been changed. What has remained the same is the footprint of the packages.

The basis of the pad design for surface mounted power MOSFET is the basic footprint for the package. For the TSOP-6 package outline drawing see <http://www.vishay.com/doc?71200> and see <http://www.vishay.com/doc?72610> for the minimum pad footprint. In converting the footprint to the pad set for a power MOSFET, you must remember that not only do you want to make electrical connection to the package, but you must make thermal connection and provide a means to draw heat from the package, and move it away from the package.

In the case of the TSOP-6 package, the electrical connections are very simple. Pins 1, 2, 5, and 6 are the drain of the MOSFET and are connected together. For a small signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.

Figure 1 shows the copper spreading recommended footprint for the TSOP-6 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlays the basic pattern on pins 1,2,5, and 6. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. Notice that the planar copper is shaped like a "T" to move heat away from the drain leads in all directions. This pattern uses all the available area underneath the body for this purpose.

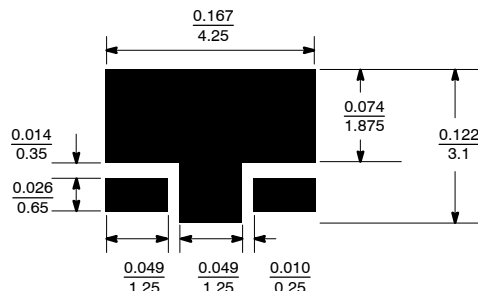


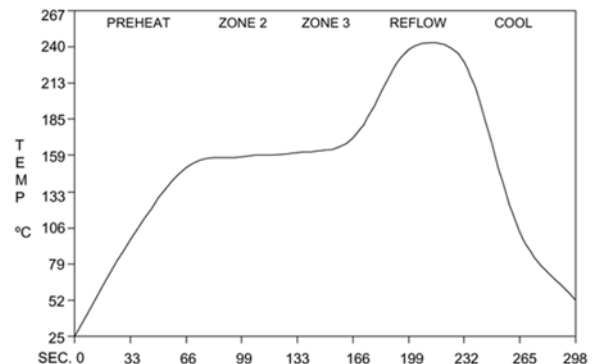
FIGURE 1. Recommended Copper Spreading Footprint

Since surface mounted packages are small, and reflow soldering is the most common form of soldering for surface mount components, "thermal" connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

### REFLOW SOLDERING

Vishay Siliconix surface-mount packages meet solder reflow reliability requirements. Devices are subjected to solder reflow as a test preconditioning and are then reliability-tested using temperature cycle, bias humidity, HAST, or pressure pot. The solder reflow temperature profile used, and the temperatures and time duration, are shown in Figures 2 and 3.



|                             |                     |
|-----------------------------|---------------------|
| Ramp-Up Rate                | +6°C/Second Maximum |
| Temperature @ 155 ± 15°C    | 120 Seconds Maximum |
| Temperature Above 180°C     | 70 – 180 Seconds    |
| Maximum Temperature         | 240 +5/-0°C         |
| Time at Maximum Temperature | 20 – 40 Seconds     |
| Ramp-Down Rate              | +6°C/Second Maximum |

FIGURE 2. Solder Reflow Temperature Profile

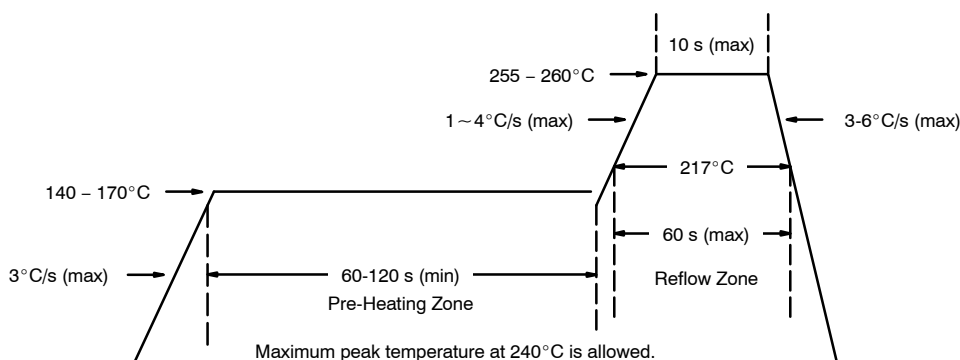


FIGURE 3. Solder Reflow Temperature and Time Durations

## THERMAL PERFORMANCE

A basic measure of a device's thermal performance is the junction-to-case thermal resistance,  $R\theta_{JC}$ , or the junction-to-foot thermal resistance,  $R\theta_{JF}$ . This parameter is measured for the device mounted to an infinite heat sink and is therefore a characterization of the device only, in other words, independent of the properties of the object to which the device is mounted. Table 1 shows the thermal performance of the TSOP-6.

| TABLE 1.                                   |        |
|--|--------|
| Equivalent Steady State Performance—TSOP-6 |        |
| Thermal Resistance $R\theta_{JF}$          | 30°C/W |

## SYSTEM AND ELECTRICAL IMPACT OF TSOP-6

In any design, one must take into account the change in MOSFET  $r_{DS(on)}$  with temperature (Figure 4).

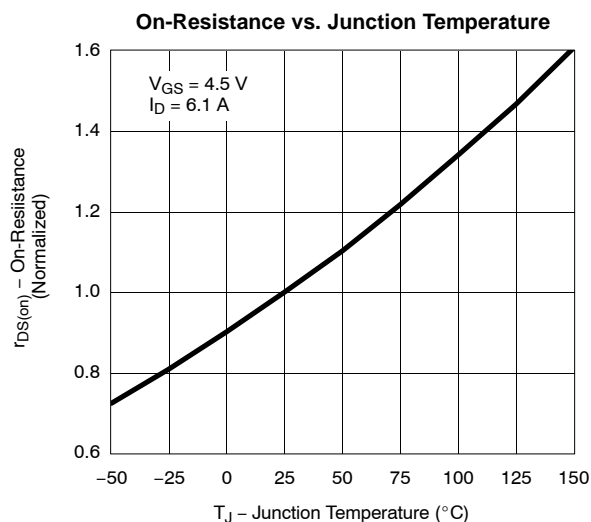
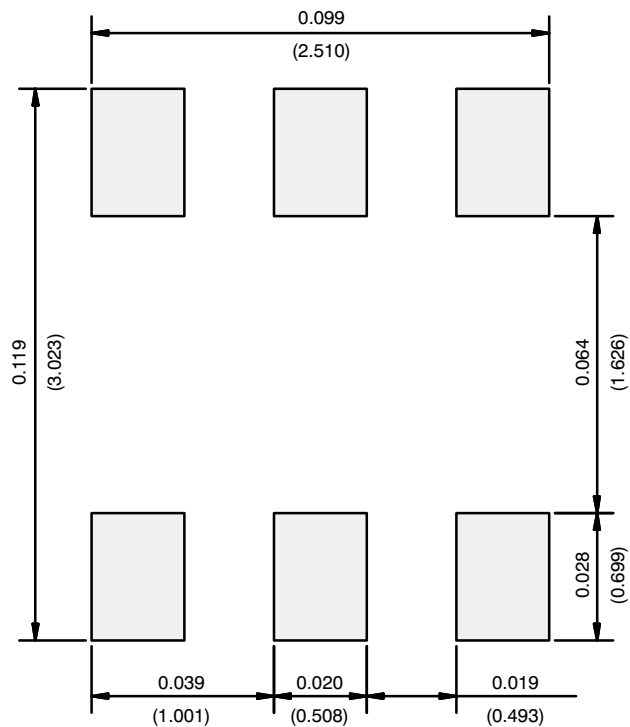


FIGURE 4. Si3434DV

## RECOMMENDED MINIMUM PADS FOR TSOP-6



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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