National Semiconductor

PRELIMINARY
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PC87108AVHG/PC87108AVJE
Advanced UART and Infrared Controller

General Description

The PC87108A is a serial communications device with infrared capability. It supports 6 modes of operation and is backward compatible with the 16550 and 16450. The operational modes are: UART, Sharp-IR, IrDA 1.0 SIR, IrDA 1.1 MIR and FIR, and Consumer Electronics IR (also referred to as TV Remote or Consumer Remote Control).

The device provides two methods to allow its internal registers to be accessed. It can either directly decode a 16-bit address, or it can accept an externally generated chip select in combination with a 4-bit address. When a 16-bit address is used, any one of four PC COMM port legacy addresses can be selected as the base address.

In order to support existing legacy software based upon the 16550 UART, the PC87108A provides a special fallback mechanism that automatically switches the device to 16550 compatibility mode when the baud generator divisor is accessed through the legacy ports in bank 1.

The device architecture has been optimized to meet the requirements of a variety of UART and infrared based applications. DMA support for all operational modes has been incorporated into the architecture. Routing for interrupt and DMA handshake signals is provided to meet Plug-and-Play as well as PC' 95 requirements.

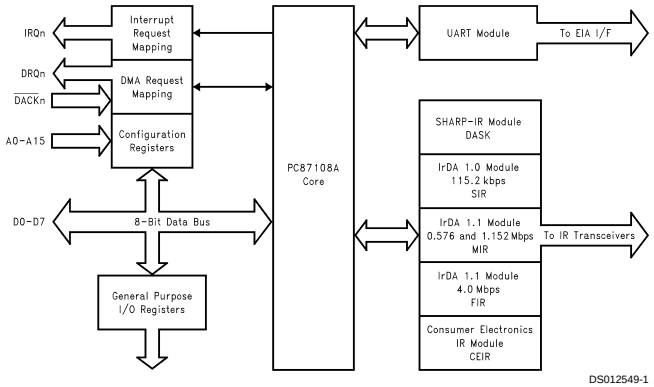
The device can use either 1 or 2 DMA channels. One channel is required for infrared based applications, since infrared communications work in half duplex fashion. Two channels would normally be needed to handle high-speed full duplex UART based applications.

To further ease driver design and simplify the implementation of infrared protocols, a 12-bit timer with 125 µs resolution has also been included.

Features

- Fully compatible with 16550 and 16450 devices
- Extended UART mode
- Sharp-IR with selectable internal or external modulation/ demodulation
- IrDA 1.0 SIR with up to 115.2 kbaud data rate
- IrDA 1.1 MIR and FIR with 0.576, 1.152 and 4.0 Mbps data rates
- CEIR mode
- UART mode data rates up to 1.5 Mbps
- Back-to-Back infrared frame transmission and reception
- Full duplex infrared frame transmission and reception
- Transmit deferral
- Automatic fallback to 16550 compatibility mode
- IrDA modes pipelining
- Selectable 16 or 32 level FIFOs
- Support for Plug-n-Play infrared adapters
- Automatic or manual transceiver configuration
- 12-bit timer for infrared protocol support
- 4 general purpose I/O pins
- Interrupt signal routing to 1 of 7 output pins
- DMA handshake signal routing for either 1 or 2 channels
- Full 16-bit address decode
- Selectable base address or chip select mode
- Support for power management
- 5V or 3.3V operation
- ISA compatible interface
- 80-pin PQFP or TQFP package

Block Diagram



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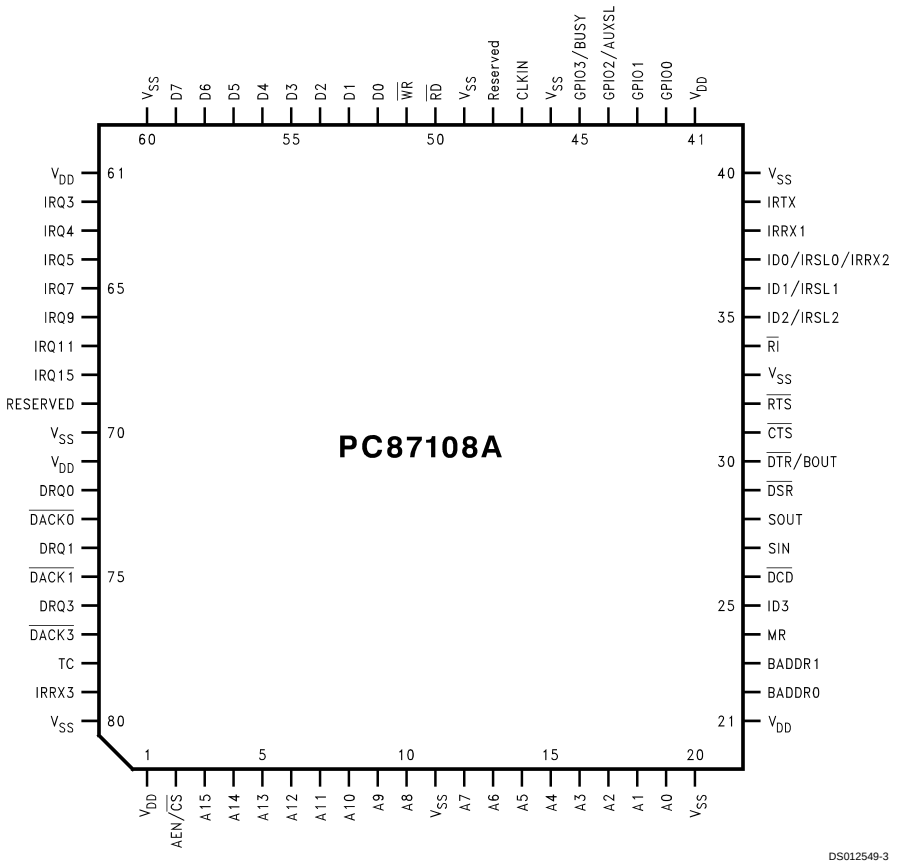
CONNECTION DIAGRAM



Top View

FIGURE 1. 80-Pin PQFP or TQFP Package

Symbol	Pin(s)	Type	Description
SUPPLIES			
V_{DD}	1, 21, 41, 61, 71		**5V or 3.3V Power Supply.**
V_{SS}	11, 20, 33, 40, 46, 49, 60, 70, 80		**Ground.**
BUS INTERFACE SIGNALS			
A0–A15	19–12, 10–3	I	**Address.** Input signals used to determine which internal register is accessed. In the chip select accessing mode, only A0–A3 are used (Section 4.2). A0–A15 are ignored during a DMA access.
AEN/$\overline{CS}$	2	I	**Address Enable or Chip Select.** Dual function pin. The pin function is selected by the levels of BADDR[0–1] during reset (Section 4.2). AEN is used to disable the internal address decoder when it is high. $\overline{CS}$ is used in conjunction with A0–A3 to select the internal registers.
D7–D0	59–52	I/O	**Data Bus.** 8-bit bi-directional data lines used to transfer data between the PC87108A and the CPU or DMA controller. D0 is the LSB and D7 is the MSB.

1.0 Pin Description (Continued)

Symbol	Pin(s)	Type	Description
BUS INTERFACE SIGNALS			
$\overline{DACK0}$, $\overline{DACK1}$, $\overline{DACK3}$	73, 75, 77	I	**DMA Acknowledge.** Active low inputs to acknowledge the corresponding DMA requests and enable the $\overline{RD}$ or $\overline{WR}$ signals during a DMA access cycle.
DRQ0, DRQ1, DRQ3	72, 74, 76	O	**DMA Request.** Active high outputs to signal the DMA controller that a data transfer from the PC87108A is required.
IRQ3–5, IRQ7, IRQ9, IRQ11, IRQ15	62–68	O	**Interrupt Request.** These outputs are used to signal an interrupt condition to the CPU. Only one signal can be selected at any one time, the others are disabled (Section 4.2.2). The selected IRQ signal can be configured to be either open-drain or totem-pole. Its polarity is also programmable.
MR	24	I	**Master Reset.** A high level on this input resets the PC87108A. This signal asynchronously terminates any activity and places the device in the Disable state. Upon MR deassertion, the BADDR[0–1] inputs are sampled to select the accessing mode and/or the base address.
$\overline{RD}$	50	I	**Read.** Active low input asserted by the CPU or DMA controller to read data or status information from the PC87108A.
TC	78	I	**Terminal Count.** This input is asserted by the DMA controller to indicate the end of a DMA transfer. The signal is only effective during a DMA access cycle.
	51	I	**Write.** Active low input asserted by the CPU or DMA controller to write data or control information to the PC87108A.
UART INTERFACE SIGNALS			
$\overline{CTS}$	31	I	**Clear to Send.** When low, indicates that the MODEM or Data Set is ready to accept data. The $\overline{CTS}$ signal is a MODEM status input whose condition can be tested by reading the MSR register.
$\overline{DCD}$	26	I	**Data Carrier Detect.** When low, indicates that the MODEM or Data Set has detected a carrier. The $\overline{DCD}$ signal is a MODEM status input whose condition can be tested by reading the MSR register.
$\overline{DSR}$	29	I	**Data Set Ready.** When low, indicates that the MODEM or Data Set is ready to establish a communications link. The $\overline{DSR}$ signal is a MODEM status input whose condition can be tested by reading the MSR register.
$\overline{DTR}$ /BOUT	30	O	**Data Terminal Ready or Baud Generator Clock.** Dual function pin. $\overline{DTR}$ is the normal pin function. It is used to indicate to the MODEM or Data Set that the device is ready to exchange data. $\overline{DTR}$ is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, $\overline{DTR}$ is set to its inactive state. The BOUT function is enabled by the BTEST bit in the EXCR1 register. When enabled, the baud generator output clock is driven on this pin.
$\overline{RI}$	34	I	**Ring Indicator.** When low, indicates that a telephone ring signal has been received by the MODEM. The $\overline{RI}$ signal is a MODEM status input whose condition can be tested by reading the MSR register.
$\overline{RTS}$	32	O	**Request to Send.** When low, this output indicates to the MODEM or Data Set that the device is ready to send data. $\overline{RTS}$ is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, $\overline{RTS}$ is set to its inactive state.
SIN	27	I	**Serial Data In.** This input receives serial data from the communications link.
SOUT	28	O	**Serial Data Out.** This output sends serial data to the communications link. This signal is set to a Marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes.

1.0 Pin Description (Continued)

Symbol	Pin(s)	Type	Description
INFRARED INTERFACE SIGNALS			
ID0/IRSL0/IRRX2	37	I/O	**Transceiver Identification/Control or Secondary Infrared Receive.** Multi function pin implementing the following functions: — ID0, to read identification data to support Plug-n-Play infrared adapters. — IRSL0, to select the transceiver operational mode. — IRRX2, used either as a high-speed receiver input (for MIR and FIR) to support transceiver modules with two receive data outputs, or as an auxiliary input to support two transceiver modules.
ID1/IRSL1, ID2/IRSL2	36, 35	I/O	**Transceiver Identification or Control.** Used to read identification data to support Plug-n-Play infrared adapters, as well as to select the transceiver operational mode.
ID3	25	I	**Transceiver Identification.** Used to read identification data to support Plug-n-Play infrared adapters.
IRRX1	38	I	**Infrared Receiver.** Primary input to receive serial data from the infrared transceiver module. If the infrared transceiver provides two receive data output, the low-speed output should be connected to this pin.
IRRX3	79	I	**Auxiliary Infrared Receiver.** This pin can be used as an auxiliary infrared receiver input when two infrared transceiver modules are used in the system.
IRTX	39	O	**Infrared Transmit.** This output sends serial data to the transceiver module(s).
MISCELLANEOUS SIGNALS			
BADDR0, 1	22, 23	I	**Base Address.** These inputs are sampled during reset to select the device accessing mode and/or the address of the Index register (Section 4.2). An internal 30 kΩ pull-down resistor is used on these pins. External 10 kΩ resistors can be used to pull these pins to V_{DD}.
CLKIN	47	I	**Clock.** 48 MHz clock input.
GPIO0, GPIO1	42, 43	I/O	**General Purpose I/O.** These pins are programmable as input or output, and can be used to control external devices. They have open-drain outputs and weak internal pull-ups.
GPIO2/AUXSL	44	I/O	**General Purpose I/O or Auxiliary Infrared Input Select.** Dual function pin. The pin function is controlled by the AUXIR__SL bit in the MCTL register (Section 4.2.3). This pin has an open-drain output and a weak internal pull-up.
GPIO3/BUSY	45	I/O	**General Purpose I/O or Busy Status.** Dual function pin. The pin function is controlled by the BUSY__SL bit in the MCTL register (Section 4.2.3). This pin has an open-drain output and a weak internal pull-up.
RESERVED	48, 69		**Reserved.** No connections should be made to these pins.

1.0 Pin Description (Continued)

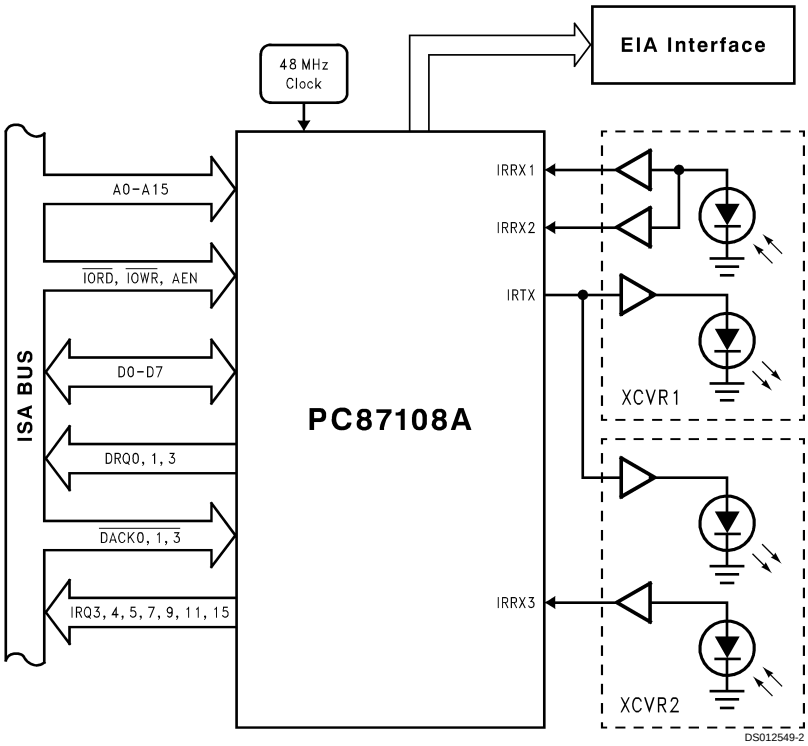


FIGURE 2. Basic Configuration

2.0 Functional Description

2.1 DEVICE OVERVIEW

The PC87108A is a serial communications element that implements the most common infrared communications protocols.

In addition to the infrared modes, the device provides a UART mode of operation that is backward compatible to the 16550 to support existing communications software.

The device includes two basic modules: the UIR (universal infrared) module and the configuration module. The UIR module implements all the communications functions, while the configuration module controls the enabling of the device as well as the selection of the base address and the routing of the interrupt and DMA control signals. The general purpose I/O pins are also controlled by the configuration module. The UIR module uses a register banking scheme similar to the one used by the 16550.

This minimizes the number of I/O addresses needed to access the internal registers. Most of the communications features are programmed via configuration registers placed in banks 0 through 7. The main control and status information has been consolidated into bank 0 to eliminate unnecessary bank switchings. A description of the device operation is provided in the following sections.

2.2 UART MODE

This mode is designed to support serial data communications with a remote peripheral device or modem using a wired interface. The device provides transmit and receive channels that can operate concurrently to handle full-duplex operation. They perform parallel-to-serial conversion on data characters received from the CPU or a DMA controller, and serial-to-parallel conversion on data characters received from the serial interface. The format of the serial data stream is shown in *Figure 3*. A data character contains 5 to 8 data bits. It is preceded by a start bit and is followed by an optional parity bit and a stop bit. Data is transferred in Little Endian order (least significant bit first).

The UART mode is the default mode of operation after power up or reset. In fact, after reset, the device enters the 16450 compatibility mode. In addition to the 16450 and 16550 compatibility modes, an extended mode of operation is also available. When the extended mode is selected, the device architecture changes slightly and a variety of additional features are made available. The interrupt sources are no longer prioritized, and an auxiliary status and control register replaces the scratch pad register. The additional features include: transmitter FIFO thresholding, DMA capability, and interrupts on transmitter empty and DMA event.

2.0 Functional Description (Continued)

The clock for both transmit and receive channels is provided by an internal baud generator that divides its input clock by any divisor value from 1 to $2^{16} - 1$. The output clock frequency of the baud generator must be programmed to be sixteen times the baud rate value. The baud generator input clock is derived from a 24 MHz clock through a programmable prescaler. The prescaler value is determined by the PRESL bits in the EXCR2 register. Its default value is 13. This allows all the standard baud rates, up to 115.2 kbaud to be obtained. Smaller prescaler values will allow baud rates up to 921.6 kbaud (standard) and 1.5 Mbaud (non standard).

Before operation can begin, both the communications format and baud rate must be programmed by the software. The communications format is programmed by loading a control byte into the LCR register, while the baud rate is selected by loading an appropriate value into the baud generator divisor register. The software can read the status of the device at any time during operation. The status information includes FULL/EMPTY state for both transmit and receive channels, and any other condition detected on the received data stream, like a parity error, framing error, data overrun, or break event.

FIGURE 3. Serial Data Stream Format

2.3 SHARP-IR MODE

This mode supports bi-directional data communication with a remote device using infrared radiation as the transmission medium. Sharp-IR uses Digital Amplitude Shift Keying (DASK) and allows serial communication at baud rates up to 38.4 kbaud. The format of the serial data is similar to the UART data format. Each data word is sent serially beginning with a zero value start bit, an optional parity bit, and ending with at least one stop bit with a binary value of one. A zero is signalled by sending a 500 kHz continuous pulse train of infrared radiation. A one is signaled by the absence of any infrared signal. The PC87108A can perform the modulation and demodulation operations internally, or it can rely on the external optical module to perform them.

Operation in Sharp-IR is similar to the operation in UART mode. The main difference being that data transfer operations are normally performed in half duplex fashion, and the modem control and status signals are not used. Selection of the Sharp-IR mode is controlled by the MDSL bits in the MCR register when the device is in extended mode, or by the IR__SL bits in the IRCR1 register when the device is in non-extended mode. This prevents legacy software, running in non-extended mode, from spuriously switching the device to UART mode, when the software writes to the MCR register.

2.4 IrDA 1.0 SIR MODE

This is the first operational mode that has been defined by the IrDA committee and, similarly to Sharp-IR, it also supports bi-directional data communication with a remote device using infrared radiation as the transmission medium. IrDA 1.0 SIR allows serial communication at baud rates up to 115.2 kbaud. The format of the serial data is similar to the UART data format. Each data word is sent serially beginning with a zero value start bit, followed by 8 data bits, and ending with at least one stop bit with a binary value of one. A zero is signaled by sending a single infrared pulse. A one is signaled by not sending any pulse. The width of each pulse can be either 1.6 µs or 3/16ths of a single bit time. (1.6 µs equals 3/16ths of a bit time at 115.2 kbaud). This way, each word begins with a pulse for the start bit.

Operation in IrDA 1.0 SIR is similar to the operation in UART mode. The main difference being that data transfer operations are normally performed in half duplex fashion, and the modem control and status signals are not used. Selection of the IrDA 1.0 SIR mode is controlled by the MDSL bits in the MCR register when the device is in extended mode, or by the IR__SL bits in the IRCR1 register when the device is in non-extended mode. This prevents legacy software, running in non-extended mode, from spuriously switching the device to UART mode, when the software writes to the MCR register.

2.5 IrDA 1.1 MIR AND FIR MODES

The PC87108A supports both IrDA 1.1 MIR and FIR modes, with data rates of 576 kbps, 1.152 Mbps and 4.0 Mbps. Details on the frame format, encoding schemes, CRC sequences, etc. are provided in the appropriate IrDA documents. The MIR transmitter front-end section performs bit stuffing on the outbound data stream and places the Start and Stop flags at the beginning and end of MIR frames. The MIR receiver front-end section removes flags and “de-stuffs” the inbound bit stream, and checks for abort conditions.

The FIR transmitter front-end section adds the Preamble as well as Start and Stop flags to each frame and encodes the transmit data into a 4PPM (Four Pulse Position Modulation) data stream. The FIR receiver front-end section strips the Preamble and flags from the inbound data stream and decodes the 4PPM data while also checking for coding violations.

Both MIR and FIR front-ends also automatically append CRC sequences to transmitted frames and check for CRC errors on received frames.

2.5.1 High Speed Infrared Transmit Operation

When the transmitter is empty, if either the CPU or the DMA controller writes data into the TX__FIFO, transmission of a frame will begin. Frame transmission can be normally completed by using one of the following methods:

2.0 Functional Description (Continued)

1. **S__EOT bit (Set End of Transmission).** This method is used when data transfers are performed in PIO mode. When the CPU sets the S__EOT bit before writing the last byte into the TX__FIFO, the byte will be tagged with an EOF indication. When this byte reaches the TX__FIFO bottom, and is read by the transmitter front-end, a CRC is appended to the transmitted DATA and the frame is normally terminated.
2. **DMA TC Signal (DMA Terminal Count).** This method is used when data transfers are performed in DMA mode. It works similarly to the previous method except that the tagging of the last byte of a frame occurs when the DMA controller asserts the TC signal during the write of the last byte to the TX__FIFO.
3. **Frame Length Counter.** This method can be used when data transfers are performed in either PIO or DMA mode. The value of the FEND__MD bit in the IRCR2 register determines whether the Frame Length Counter is effective in the PIO or DMA mode. The counter is loaded from the Frame Length Register (TFRL) at the beginning of each frame, and it is decremented as each byte is transmitted. An EOF is generated when the counter reaches zero. When used in DMA mode with an 8237 type DMA controller, this method allows a large data block to be automatically split into equal-size back-to-back frames, plus a shorter frame that is terminated by the DMA TC signal, if the block size is not an exact multiple of the frame size.

   An option is also provided to stop transmission at the end of each frame. This happens when the transmitter Frame-End stop mode is enabled (TX__MS bit in the IRCR2 register set to 1). By using this option, the software can send frames of different sizes without re-initializing the DMA controller for each frame. After transmission of each frame, the transmitter stops and generates an interrupt. The software loads the length of the next frame into the TFRL register and restarts the transmitter by clearing the TXHFE bit in the ASCR register.

Note: PIO or DMA mode is only controlled by the setting of the DMA__EN bit in the extended-mode MCR register. The device treats CPU and DMA access cycles the same except that DMA cycles always access the TX__ or RX__FIFO, regardless of the selected bank. When DMA__EN is set to 1, the CPU can still access the TX__FIFO and RX__FIFO. The CPU accesses will, however, be treated as DMA accesses as far as the function of the FEND__MD bit is concerned.

While a frame is being transmitted, data must be written to the TX__FIFO at a rate dictated by the transmission speed. If the CPU or DMA controller fails to meet this requirement, a transmitter underrun will occur, an inverted CRC is appended to the frame being transmitted, and the frame is terminated with a Stop flag. Data transmission will then stop. Transmission of the inverted CRC will guarantee that the remote receiving device will receive the frame with a CRC error and will discard it.

Following an underrun condition, data transmission always stops at the next frame boundary. The frame bytes from the point where the underrun occurred to the end of the frame will not be sent out to the external infrared interface. Nonetheless, they will be removed from the TX__FIFO by the transmitter and discarded. The underrun indication will be reported only when the transmitter detects the end of frame via one of the methods described above. The software can do various things to recover from an underrun condition. For example, it can simply clear the underrun condition by writing a 1 into bit 6 of ASCR and re-transmit the underrun frame later, or it can re-transmit it immediately, before transmitting other frames.

If it chooses to re-transmit the frame immediately, it needs to perform the following steps:

1. Disable DMA controller, if DMA mode was selected.
2. Read the TXFLV register to determine the number of bytes in the TX__FIFO. (This is needed to determine the exact point where the underrun occurred, and whether or not the first byte of a new frame is in the TX__FIFO).
3. Reset TX__FIFO.
4. Backup DMA controller registers.
5. Clear Transmitter underrun bit.
6. Re-enable DMA controller.

2.5.2 High Speed Infrared Receive Operation

When the receiver front-end detects an incoming frame, it will start de-serializing the infrared bit stream and load the resulting data bytes into the RX__FIFO. When the EOF is detected, two or four CRC bytes are appended to the received data, and an EOF flag is written into the tag section of the RX__FIFO along with the last byte. In the present implementation, the CRC bytes are always transferred to the RX__FIFO following the data. Additional status information, related to the received frame, is also written into the RX__FIFO tag section at this time. The status information will be loaded into the LSR register when the last frame byte reaches the RX__FIFO bottom.

The receiver keeps track of the number of received bytes from the beginning of the current frame. It will only transfer to the RX__FIFO a number of bytes not exceeding the maximum frame length value which is programmed via the RFRML register in bank 4. Any additional frame bytes will be discarded. When the maximum frame length value is exceeded, the MAX__LEN error flag will be set.

Although data transfers from the RX__FIFO to memory can be performed either in PIO or DMA mode, DMA mode should be used due to the high data rates.

In order to handle back-to-back incoming frames, when DMA mode is selected and an 8237 type DMA controller is used, an 8-level ST__FIFO (Status FIFO) is provided. When an EOF is detected, in 8237 DMA mode, the status and byte count information for the frame is written into the ST__FIFO. An interrupt is generated when the ST__FIFO level reaches a programmed threshold or an ST__FIFO time-out occurs.

The CPU uses this information to locate the frame boundaries in the memory buffer where the data, belonging to the received frames, has been transferred by the 8237 type DMA controller.

During reception of multiple frames, if the RX__FIFO and/or the ST__FIFO fills up, due to the DMA controller or CPU not serving them in time, one or more frames can be crushed and lost. This means that no bytes belonging to these frames were written to

2.0 Functional Description (Continued)

the RX__FIFO. In fact, a frame will be lost in 8237 mode when the ST__FIFO is full for the entire time during which the frame is being received, even though there were empty locations in the RX__FIFO. This is because no data bytes can be loaded into the RX__FIFO and then transferred to memory by the DMA controller, unless there is at least one available entry in the ST__FIFO to store the number of received bytes. This information, as mentioned before, is needed by the software to locate the frame boundaries in the DMA memory buffer.

In the event that a number of frames are lost, for any of the reasons mentioned above, one or more lost-frame indications including the number of lost frames, are loaded into the ST__FIFO.

Frames can also be lost in PIO mode, but only when the RX__FIFO is full. The reason being that, in these cases, the ST__FIFO is only used to store lost-frame indications. It will not store frame status and byte count.

2.6 CONSUMER ELECTRONICS IR (CEIR) MODE

The Consumer Electronics IR circuitry is designed to optimally support all the major protocols presently used in remote-controlled home entertainment equipment. The main protocols currently in use are: RC-5, RC-6, RECS 80, NEC and RCA. The PC87108, in conjunction with an external optical module, provides the physical layer functions necessary to support these protocols. These functions include modulation, demodulation, serialization, de-serialization, data buffering, status reporting, interrupt generation, etc. The software is responsible for the generation of the infrared code to be transmitted, and for the interpretation of the received code.

2.6.1 CEIR Transmit Operation

The code to be transmitted consists of a sequence of bytes that represent either a bit string or a set of run-length codes. The number of bits or run-length codes usually needed to represent each infrared code bit depends on the infrared protocol used. The RC-5 protocol, for example, needs two bits or between one and two run-length codes to represent each infrared code bit.

CEIR transmission starts when the transmitter is empty and either the CPU or the DMA controller writes code bytes into the TX__FIFO. The transmission is normally completed when the CPU sets the S__EOT bit in the ASCR register before writing the last byte, or when the DMA controller activates the TC signal. Transmission is also completed if the CPU simply stops transferring data and the transmitter becomes empty. In this case however, a transmitter underrun condition will be generated. The underrun must be cleared before the next transmission can occur. The code bytes written into the TX__FIFO are either de-serialized or run-length decoded, and the resulting bit string is modulated by a subcarrier signal and sent to the transmitter LED. The bit rate of this bit string, like in the UART mode, is determined by the value programmed in the baud generator divisor register. Unlike a UART transmission, start, stop and parity bits are not included in the transmitted data stream. A logic 1 in the bit string will keep the LED off, so no infrared signal is transmitted. A logic 0 will generate a sequence of modulating pulses which will turn on the transmitter LED. Frequency and pulse width of the modulating pulses are programmed by the MCFR and MCPW bits in the IRTXMC register as well as the TXHSC bit in the RCCFG register.

The RC__MMD bits select the transmitter modulation mode. If C__PLS mode is selected, modulation pulses are generated continuously for the entire time in which one or more logic 0 bits are being transmitted. If 6__PLS or 8__PLS modes are selected, 6 or 8 pulses are generated each time one or more logic 0 bits are transmitted following a logic 1 bit. C__PLS modulation mode is used for RC-5, RC-6, NEC and RCA protocols. 8__PLS or 6__PLS modulation mode is used for the RECS 80 protocol. The 8__PLS or 6__PLS mode allows minimization of the number of bits needed to represent the RECS 80 infrared code sequence. The current transmitter implementation supports only the modulated modes of the RECS 80 protocol. The flash mode is not supported since it is not popular and is becoming less frequently used.

Note: The total transmission time for the logic 0 bits must be equal or greater than 6 or 8 times the period of the modulation subcarrier, otherwise fewer pulses will be transmitted.

2.6.2 CEIR Receive Operation

The CEIR receiver is significantly different from a UART receiver for two basic reasons. First, the incoming infrared signals are DASK modulated. Therefore, a demodulation operation may be necessary. Second, there are no start bits in the incoming data stream.

Whenever an infrared signal is detected, the operations performed by the receiver are slightly different depending on whether or not receiver demodulation is enabled. If the demodulator is not enabled, the receiver will immediately switch to the active state. If the demodulator is enabled, the receiver checks the subcarrier frequency of the incoming signal, and it switches to the active state only if the frequency falls within the programmed range. If this is not the case, the signal is ignored and no other action is taken.

When the receiver active state is entered, the RXACT bit in the ASCR register is set to 1. Once in the active state, the receiver keeps sampling the infrared input signal and generates a bit stream where a logic 1 indicates an idle condition and a logic 0 indicates the presence of infrared energy. The infrared input is sampled regardless of the presence of infrared pulses at a rate determined by the value loaded into the baud generator divisor register. The received bit string is either de-serialized and assembled into 8-bit characters, or it is converted to run-length encoding values. The resulting data bytes are then transferred to the RX__FIFO.

The receiver also sets the RXWDG bit in the ASCR register each time an infrared pulse signal is detected. This bit is automatically cleared when the ASCR register is read, and it is intended to assist the software in determining when the infrared link has been idle for a certain time. The software can then stop the data reception by writing a 1 into the RXACT bit to clear it and return the receiver to the inactive state.

2.0 Functional Description (Continued)

The frequency bandwidth for the incoming modulated infrared signal is selected by DFR and DBW bits in the IRRXDC register. There are two CEIR receiver data modes: “Over-sampled” and “Programmed-T-Period” mode. For either mode the sampling rate is determined by the setting of the baud generator divisor register.

The “Over-sampled” mode can be used with the receiver demodulator either enabled or disabled. It should be used with the demodulator disabled when a detailed snapshot of the incoming signal is needed, for example to determine the period of the subcarrier signal. If the demodulator is enabled, the stream of samples can be used to reconstruct the incoming bit string. To obtain a good resolution, a fairly high sampling rate should be selected.

The “Programmed-T-Period” mode should be used with the receiver demodulator enabled. The T Period represents one half bit time, for protocols using bi-phase encoding, or the basic unit of pulse distance, for protocols using pulse distance encoding. The baud rate is usually programmed to match the T Period. For long periods of logic low or high, the receiver samples the demodulated signal at the programmed sampling rate.

Whenever a new infrared energy pulse is detected, the receiver will re-synchronize the sampling process to the incoming signal timing. This reduces timing related errors and eliminates the possibility of missing short infrared pulse sequences, especially when dealing with the RECS 80 protocol. In addition, the “Programmed-T-Period” sampling minimizes the amount of data used to represent the incoming infrared signal, therefore reducing the processing overhead in the host CPU.

2.7 FIFO TIME-OUTS

In order to prevent received data from sitting in the RX __FIFO and/or the ST__FIFO indefinitely, if the programmed interrupt or DMA thresholds are not reached, time-out mechanisms are provided.

An RX__FIFO time-out generates a receiver High-Data-Level interrupt and/or a Receiver DMA request if bit 0 of IER and/or bit 2 of MCR (in extended mode) are set to 1 respectively. An RX__FIFO time-out also sets bit 0 of ASCR to 1 if the RX__FIFO is below the threshold. This bit is tested by the software, when a receiver High-Data-Level interrupt occurs, to decide whether a number of bytes, as indicated by the RX__FIFO threshold, can be read without checking bit 0 of the LSR register. An ST__FIFO time-out is enabled only in MIR and FIR modes, and generates an interrupt if bit 6 of IER is set to 1.

The conditions that must exist for a time-out to occur in the various modes of operation, are described below. When a time-out has occurred, it can only be reset when the FIFO that caused the time-out is read by the CPU or DMA controller.

MIR or FIR Modes

RX__FIFO Time-out Conditions:

1. At least one byte is in the RX__FIFO, and
2. More than 64 µs have elapsed since the last byte was loaded into the RX__FIFO from the receiver logic, and
3. More than 64 µs have elapsed since the last byte was read from the RX__FIFO by the CPU or DMA controller.

ST__FIFO Time-out Conditions:

1. At least one entry is in the ST__FIFO, and
2. More than 1 ms has elapsed since the last byte was loaded into the RX__FIFO by the receiver logic, and
3. More than 1 ms has elapsed since the last entry was read from the ST__FIFO by the CPU.

UART, Sharp-IR, SIR Modes

RX__FIFO Time-out Conditions:

1. At least one byte is in the RX__FIFO, and
2. More than four character times have elapsed since the last byte was loaded into the RX__FIFO from the receiver logic, and
3. More than four character times have elapsed since the last byte was read from the RX__FIFO by the CPU or DMA controller.

CEIR Mode

RX__FIFO Time-out Conditions:

The RX__FIFO Time-out, in CEIR mode, is disabled while the receiver is active. The conditions for this time-out to occur are as follows:

1. At least one byte has been in the RX__FIFO for 64 µs or more, and
2. The receiver has been inactive (RXACT=0) for 64 µs or more, and
3. More than 64 µs have elapsed since the last byte was read from the RX__FIFO by the CPU or DMA controller.

2.8 TRANSMIT DEFERRAL

This feature allows the software to send short high-speed data frames in PIO mode without the risk of a transmitter underrun being generated. Even though this feature is available and works the same way in all modes, it will most likely be used in MIR and FIR modes to support high-speed negotiations. This is because in other modes, either the transmit data rate is relatively low and thus the CPU can keep up with it without letting an underrun occur, as in the case CEIR Mode, or transmit underruns are allowed and are not considered to be error conditions.

Transmit deferral is available only in extended mode and when the TX__FIFO is enabled. When transmit deferral is enabled (TX__DFR bit of MCR set to 1) and the transmitter becomes empty, an internal flag will be set that locks the transmitter. If the CPU

2.0 Functional Description (Continued)

now writes data into the TX__FIFO, the transmitter will not start sending the data until the TX__FIFO level reaches either 14 for a 16-level TX__FIFO, or 30 for a 32-level TX__FIFO, at which time the internal flag is cleared. The internal flag is also cleared and the transmitter starts transmitting when a time-out condition is reached. This prevents some bytes from being in the TX__FIFO indefinitely if the threshold is not reached.

The time-out mechanism is implemented by a timer that is enabled when the internal flag is set and there is at least one byte in the TX__FIFO. Whenever a byte is loaded into the TX__FIFO the timer gets reloaded with the initial value. If no bytes are loaded for a 64-µs time, the timer times out and the internal flag gets cleared, thus enabling the transmitter.

2.9 AUTOMATIC FALLBACK TO 16550 COMPATIBILITY MODE

This feature is designed to support existing legacy software packages using the 16550 UART.

For proper operation, many of these software packages require that the device look identical to a plain 16550 since they access the UART registers directly.

Due to the fact that several extended features as well as new operational modes are provided, the user must make sure that the device is in the proper state before a legacy program can be executed.

The fallback mechanism is designed for this purpose. It eliminates the need for user intervention to change the state of the device, when a legacy program must be executed following completion of a program that used any of the device's extended features.

This mechanism automatically switches the device to 16550 compatibility mode and turns off any extended features whenever the baud generator divisor register is accessed through the LBGD(L) or LBGD(H) ports in register bank 1.

In order to avoid spurious fallbacks, baud generator divisor ports are provided in bank 2. Accesses of the baud generator divisor through these ports will change the baud rate setting but will not cause a fall back.

New programs, designed to take advantage of the extended features, should not use LBGD(L) and LBGD(H) to change the baud rate. They should use BGD(L) and BGD(H) instead.

A fallback can occur from either extended or non-extended modes. If extended mode is selected, fallback is always enabled. In this case, when a fallback occurs, the following happens:

1. Transmitter and receiver FIFOs will switch to 16 levels.
2. A value of 13 will be selected for the baud generator prescaler.
3. The ETDLBK and BTEST bits in the EXCR1 Register will be cleared.
4. UART mode will be selected.
5. A switch to non-extended mode will occur.

When a fallback occurs from non-extended mode, only the first three of the above actions will take place. No switching to UART mode occurs if either Sharp__IR or SIR infrared modes were selected. This prevents spurious switchings to UART mode when a legacy program, running in infrared mode, accesses the baud generator divisor register from bank 1.

Fallback from non-extended mode can be disabled by setting the LOCK bit in the EXCR2 register. When Lock is set to 1 and the device is in non-extended mode, two scratchpad registers overlayed with LBGD(L) and LBGD(H) are enabled. Any attempted CPU access of the baud generator divisor register through LBGD(L) and LBGD(H) will access the scratchpad registers, and the baud rate setting will not be affected. This feature allows existing legacy programs to run faster than 115.2 kbaud without their being aware of it.

2.10 PIPELINING

This feature is designed to support the IrDA infrared modes and it allows minimization of the time delay from the end of a negotiation phase to the subsequent data transfer phase.

The device accomplishes this objective by automatically selecting a new mode and/or loading new values into the baud generator divisor register as soon as the current data transmission completes and the transmitter becomes empty. The new operational mode and the baud divisor value are programmed into special pipeline registers.

Pipelining is automatically disabled after a pipeline operation takes place. It should be re-enabled by the software after the special pipeline registers have been reloaded.

Even though there are no other restrictions between source and target modes, aside from having to be IrDA modes, pipelining will most likely be used from SIR as the source mode, since SIR is the mode used by the negotiation procedures in the presently defined IrDA protocols.

Following a pipeline operation, the transmitter will be halted for 250 µs to allow the newly selected receive filter in the remote optical transceiver to stabilize. If a switch from either MIR or FIR to SIR occurred as a result of pipelining, the transmitter will be halted for 250 µs or a character time (at the newly selected baud rate), whichever is greater. This is to guarantee that reception at a remote station of any character triggered by an interaction pulse is complete before the next SIR data transmission begins.

Since a pipelining operation is performed without software intervention, automatic transceiver configuration must be enabled.

2.11 OPTICAL TRANSCEIVER INTERFACE

The PC87108A implements a very flexible interface for the external infrared transceiver. Several signals are provided for this purpose. A transceiver module with one or two receive signals, or two transceiver modules can be directly interfaced without any additional logic.

2.0 Functional Description (Continued)

Since various operational modes are supported, the transmitter power as well as the receiver filter in the transceiver module must be configured according to the selected mode.

The PC87108A provides four special interface pins (ID/IRSL[2–0] and ID3) to control the infrared transceiver. The logic levels of the ID/IRSL[2–0] pins can be either directly controlled by the software (through the setting of bits 2–0 in the IRCFG1 register), or can be automatically selected by the device whenever a new mode is entered.

The automatic transceiver configuration is enabled by setting the AMCFG bit in the IRCFG4 register to 1. One of its advantages is that it allows the low-level functional details of the transceiver module being used to be hidden from the software drivers. It also speeds up the transceiver mode selection, and it must be enabled if the pipelining feature is to be used.

The operational mode settings for the automatic configuration are determined by various bit fields in the IRCFGn registers that must be programmed when the device is initialized.

The ID/IRSL[2–0] pins will power up as inputs and can be driven by an external source. When in input mode, they can be used to read the identification data of Plug-n-Play infrared adapters. The ID3 pin is input-only and is also used for this purpose.

The ID0/IRSL0/IRRX2 pin can also function as an input to support an additional infrared receive signal. In this case, however, only two configuration pins will be available. The IRSL0__DS and IRSL21__DS bits in the IRCFG4 register determine the direction of the ID/IRSL[2–0] pins.

3.0 Architectural Description

Eight register banks are provided to control the operation of the UIR module. These banks are mapped into the same address range, and only the selected bank is directly accessible by the software. The address range spans 8 byte locations. The BSR register is used to select the bank and is common to all banks. Therefore, each bank defines seven new registers. The register banks can be divided into two sets. Banks 0–3 are used to control both UART and infrared modes of operation; banks 4–7 are used to control and configure the infrared modes only. The register bank main functions are listed in *Table 1*. Descriptions of the various registers are given in the following sections.

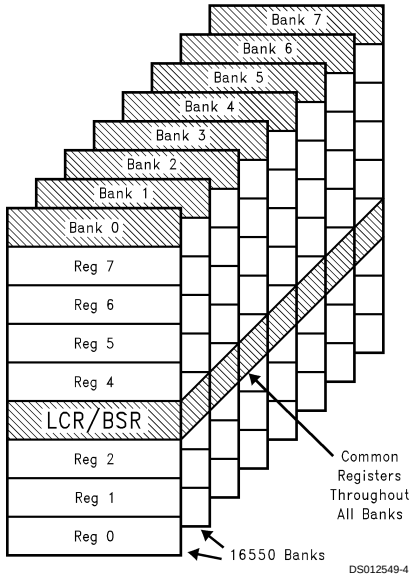


FIGURE 4. Register Bank Architecture

TABLE 1. Register Banks Summary

Bank	UART Mode	IR Mode	Description
0	✓	✓	Global Control and Status Registers
1	✓	✓	Legacy Bank
2	✓	✓	Baud Generator Divisor and Extended Control
3	✓	✓	Identification and Shadow Registers
4		✓	Timer and Counters
5		✓	Infrared Control and Status FIFO

3.0 Architectural Description (Continued)

TABLE 1. Register Banks Summary (Continued)

Bank	UART Mode	IR Mode	Description
6		✓	Infrared Physical Layer Configuration
7		✓	Consumer-IR and Optical Transceiver Configuration

3.1 BANK 0

TABLE 2. Bank 0 Register Set

Address Offset	Register Name	Description
0	**TXD/RXD**	Transmit/Receive Data Ports
1	**IER**	Interrupt Enable Register
2	**EIR/FCR**	Event Identification/FIFO Control Registers
3	**LCR/BSR**	Link Control/Bank Select Registers
4	**MCR**	Modem/Mode Control Register
5	**LSR**	Link Status Register
6	**MSR**	Modem Status Register
7	**SPR/ASCR**	Scratchpad/Auxiliary Status and Control Register

3.1.1 TXD/RXD – Transmit/Receive Data Ports

These ports share the same address.

TXD is accessed during CPU write cycles. It provides the write data path to the transmitter holding register when the FIFOs are disabled, or to the TX__FIFO top location when the FIFOs are enabled.

RXD is accessed during CPU read cycles. It provides the read data path from the receiver holding register when the FIFOs are disabled, or from the RX__FIFO bottom location when the FIFOs are enabled.

DMA cycles always access the transmitter and receiver holding registers or FIFOs, regardless of the selected bank.

3.1.2 IER – Interrupt Enable Register

This register controls the enabling of the various interrupts. Some interrupts are common to all operating modes, while others are only available with specific modes. Bits 4 to 7 can be set in extended mode only. They are cleared in non-extended mode. When a bit is set to 1, an interrupt is generated when the corresponding event occurs. In the non-extended mode most events can be identified by reading the LSR and MSR registers. The receiver high-data-level event can only be identified by reading the EIR register after the corresponding interrupt has been generated. In the extended mode events are identified by event flags in the EIR register. Upon reset, all bits are set to 0.

Note 1: If the interrupt signal drives an edge-sensitive interrupt controller input, it is advisable to disable all interrupts by clearing all the IER bits upon entering the interrupt routine, and re-enable them just before exiting it. This will guarantee proper interrupt triggering in the interrupt controller in case one or more interrupt events occur during execution of the interrupt routine.

Note 2: If an interrupt source must be disabled, the CPU can do so by clearing the corresponding bit in the IER register. However, if an interrupt event occurs just before the corresponding enable bit in the IER register is cleared, a spurious interrupt may be generated. To avoid this problem, the clearing of any IER bit should be done during execution of the interrupt service routine. If the interrupt controller is programmed for level-sensitive interrupts, the clearing of IER bits can also be performed outside the interrupt service routine, but with the CPU interrupt disabled.

Note 3: If the LSR, MSR or EIR registers are to be polled, the interrupt sources which are identified via self-clearing bits should have their corresponding IER bits set to 0. This will prevent spurious pulses on the interrupt output pin.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	TMR__IE	SFIF__IE	TXEMP__IE/ PLD__IE	DMA__IE	MS__IE	LS__IE/ TXHLT__IE	TXLDL__IE	RXHDL__IE
Reset State	0	0	0	0	0	0	0	0

FIGURE 5. Interrupt Enable Register

B0 RXHDL__IE – Receiver High-Data-Level Interrupt Enable.

B1 TXLDL__IE – Transmitter Low-Data-Level Interrupt Enable.

B2 *UART, Sharp-IR, SIR Modes*

LS__IE – Link Status Interrupt Enable.

MIR, FIR, CEIR Modes

LS__IE/TXHLT__IE – Link Status/Transmitter Halted Interrupt Enable.

3.0 Architectural Description (Continued)

B3 MS__IE – Modem Status Interrupt Enable.

B4 DMA__IE – DMA Interrupt Enable.

B5 *UART, Sharp-IR, CEIR Modes*

TXEMP__IE – Transmitter Empty Interrupt Enable.

SIR, MIR, FIR Modes

TXEMP__IE/PLD__IE – Transmitter Empty/Pipeline Load Interrupt Enable.

B6 *MIR, FIR Modes*

SFIF__IE – ST__FIFO Interrupt Enable.

B7 TMR__IE – Timer Interrupt Enable.

3.1.3 EIR/FCR – Event Identification/FIFO Control Registers

These registers share the same address.

EIR is accessed during CPU read cycles while FCR is accessed during CPU write cycles.

EIR– Event Identification Register, Read-Only.

The function of this register changes depending upon whether the device is in extended or non-extended mode.

Non-Extended Mode

The function of EIR is the same as in the 16550. It returns an encoded value representing the highest priority pending interrupt. While a CPU access is occurring, the device records new interrupts, but it does not change the currently encoded value until the access is complete. *Table 3* shows the interrupt priorities and the EIR encoded values.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	FEN1	FEN0	0	0	RXFT	IPR1	IPR0	IPF
Reset State	0	0	0	0	0	0	0	1

FIGURE 6. Event Identification Register, Non-Extended Mode

B0 IPF – Interrupt Pending Flag.

When this bit is 0, an interrupt is pending.

When it is 1, no interrupt is pending.

B2–1 IPR [1–0] – Interrupt Priority.

When bit 0 is 0, these bits identify the highest priority pending interrupt.

B3 RXFT – RX__FIFO Time-out.

In the 16450 mode this bit is always 0.

In the 16550 mode (FIFOs enabled), this bit is set when an RX__FIFO time-out occurred and the associated interrupt is currently the highest priority pending interrupt.

B5–4 These bits always return 0.

B7–6 FEN [1–0] – FIFOs Enabled.

These bits are set to 1 when the FIFOs are enabled (bit 0 of FCR set to 1).

3.0 Architectural Description (Continued)

TABLE 3. Non-Extended Mode Interrupt Priorities

EIR Bits 3210	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0001	N/A	None	None	N/A
0110	Highest	Link Status	Parity error, or Framing error, or Data overrun, or Break event	Reading the LSR Register
0100	Second	Receiver High-Data-Level Event	Receiver holding register full, or RX__FIFO level equal to or above threshold	Reading the RXD port, or RX__FIFO level drops below threshold
1100	Second	RX__FIFO Timeout	At least 1 character in RX__FIFO, and no character input to or read from the RX__FIFO for 4 character times	Reading the RXD port
0010	Third	Transmitter Low-Data-Level Event	Transmitter holding register or TX__FIFO empty	Reading the EIR register if this interrupt is currently the highest priority pending interrupt, or writing into the TXD port
0000	Fourth	Modem Status	Any transition on $\overline{CTS}$, $\overline{DSR}$, or $\overline{DCD}$, or low-to-high transition on $\overline{RI}$	Reading the MSR register

Extended Mode

The EIR register does not return an encoded value like in the non-extended mode. Each bit represents an event flag and is set to 1 when the corresponding event occurred or is pending, regardless of the setting of the corresponding bit in the IER register. Bit 4 is cleared when this register is read if an 8237 type DMA controller is used. All other bits are cleared when the corresponding interrupts are acknowledged.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	TMR__EV	SFIF__EV	TXEMP__EV/ PLD__EV	DMA__EV	MS__EV	LS__EV/ TXHLT__EV	TXLDL__EV	RXHDL__EV
Reset State	0	0	1	0	0	0	1	0

FIGURE 7. Event Identification Register, Extended Mode

B0 RXHDL__EV – Receiver High-Data-Level Event.

FIFOs Disabled: Set to 1 when one character is in the receiver holding register.

FIFOs Enabled: Set to 1 when the RX__FIFO level is equal to or above the threshold level, or an RX__FIFO time-out has occurred.

B1 TXLDL__EV – Transmitter Low-Data-Level Event.

FIFOs Disabled: Set to 1 when the transmitter holding register is empty.

FIFOs Enabled: Set to 1 when the TX__FIFO level is below the threshold level.

B2 *UART, Sharp-IR, SIR Modes*

LS__EV – Link Status Event.

Set to 1 when a receiver error or break condition is reported.

Note that, when the FIFOs are enabled, the PE, FE and BRK conditions are only reported when the associated character reaches the bottom of the RX__FIFO. An overrun error (OE) is reported as soon as it occurs.

MIR, FIR Modes

LS__EV/TXHLT__EV – Link Status/Transmitter Halted Event.

Set to 1 when any of the following conditions occur:

1. Last byte of received frame reaches the bottom of the RX__FIFO
2. Receiver overrun
3. Transmitter underrun
4. Transmitted halted on frame end

CEIR Mode

LS__EV/TXHLT__EV – Link Status/Transmitter Halted.

Set to 1 when a receiver overrun or a transmitter underrun condition occurs.

Note: A high speed CPU can service the interrupt generated by the last frame byte reaching the RX_FIFO bottom before that byte is transferred to memory by the DMA controller. This can happen when the CPU interrupt latency is shorter than the RX_FIFO time-out (Refer to the "FIFO Time-out" section). A DMA request is generated only when the RX_FIFO level reaches the DMA threshold or when a FIFO time-out occurs, in order to minimize the performance degradation due

3.0 Architectural Description (Continued)

to DMA signal handshake sequences. If the DMA controller must be set up before receiving each frame, the software in the interrupt routine should make sure that the last byte of the frame just received has been transferred to memory before re-initializing the DMA controller, otherwise that byte could appear as the first byte of the next received frame.

B3 *UART Mode*

MS__EV – Modem Status Event.

Set to 1 when any of the bits 0 to 3 in the MSR register is set to 1.

Any Infrared Mode

MS__EV/Unused – Modem Status Event.

The function of this bit depends on the setting of the IRMSSL bit in the IRCR2 register.

IRMSSL Value	Bit Function
0	Modem Status interrupt event
1	Forced to 0

B4 DMA__EV – DMA Event.

When an 8237 type DMA controller is used, this bit is set to 1 when a DMA terminal count (TC) is signaled. It is cleared upon read.

B5 *UART, Sharp-IR, CEIR Modes*

TXEMP__EV – Transmitter Empty.

This bit is the same as bit 6 of the LSR register. It is set to 1 when the transmitter is empty.

MIR, FIR, SIR Modes

TXEMP__EV/PLD__EV – Transmitter Empty/Pipeline Load Event.

Set to 1 when the transmitter is empty or a pipeline operation occurs.

B6 *MIR, FIR Modes*

SFIF__EV – ST__FIFO Event.

Set to 1 when the ST__FIFO level is equal to or above the threshold, or an ST__FIFO time-out occurs. This bit is cleared when the CPU reads the ST__FIFO and its level drops below the threshold.

B7 TMR__EV – Timer Event.

Set to 1 when the timer reaches 0.

Cleared by writing 1 into bit 7 of the ASCR register.

FCR – FIFO Control Register, Write-Only

Used to enable the FIFOs, clear the FIFOs and set the interrupt threshold levels.

Upon reset, all bits are set to 0.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	RXFTH1	RXFTH0	TXFTH1	TXFTH0	res	TXSR	RXSR	FIFO__EN
Reset State	0	0	0	0	0	0	0	0

FIGURE 8. FIFO Control Register

B0 FIFO__EN – Enable FIFOs.

When set to 1, both TX__FIFO and RX__FIFO are enabled.

In MIR, FIR and CEIR modes, the FIFOs are always enabled, and the setting of this bit is ignored.

B1 RXSR – Receiver Soft Reset.

Writing a 1 to this bit position generates a receiver soft reset, whereby the receiver logic as well as the RX__FIFO are both cleared.

This bit is automatically cleared by the hardware.

B2 TXSR – Transmitter Soft Reset.

Writing a 1 to this bit position generates a transmitter soft reset, whereby the transmitter logic as well as the TX__FIFO are both cleared.

This bit is automatically cleared by the hardware.

B3 Reserved.

Write 0.

B5–4 TXFTH [1–0] – TX__FIFO Interrupt Threshold.

In non-extended mode, these bits have no effect, regardless of the values written into them.

In extended mode, these bits select the TX__FIFO interrupt threshold level.

3.0 Architectural Description (Continued)

An interrupt is generated when the TX__FIFO level drops below the threshold.

Bits 5–4	TX__FIFO Thresh. (16 Levels)	TX__FIFO Thresh. (32 Levels)
00	1	1
01	3	7
10	9	17
11	13	25

B7–6 RXFTH [1–0] – RX__FIFO Interrupt Threshold.

These bits select the RX__FIFO interrupt threshold level.

An interrupt is generated when the RX__FIFO level is equal to or above the threshold.

Bits 7–6	RX__FIFO Thresh. (16 Levels)	RX__FIFO Thresh. (32 Levels)
00	1	1
01	4	8
10	8	16
11	14	26

3.1.4 LCR/BSR – Link Control/Bank Select Register

These registers share the same address.

The Link Control Register (LCR) is used to select the communications format for data transfers in UART, Sharp-IR and SIR modes.

The Bank select register (BSR) is used to select the register bank to be accessed next.

When the CPU performs a read cycle from this address location, the BSR content is returned. The content of LCR is returned when the CPU reads the SH__LCR register in bank 3.

During CPU write cycles, the setting of bit 7 (BKSE, bank select enable) determines the register to be accessed.

If bit 7 is 0, both LCR and BSR are written into. If bit 7 is 1, only BSR is written into, and LCR is not affected. This prevents the communications format from being spuriously affected when a bank other than bank 0 is accessed. Upon reset, all bits are set to 0.

LCR – Link Control Register

The Format of LCR is shown in *Figure 9.*

Bits 0 to 6 are only effective in UART, Sharp-IR and SIR modes.

They are ignored in MIR, FIR and CEIR modes.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1	WLS0
Reset State	0	0	0	0	0	0	0	0

FIGURE 9. Link Control Register

B1–0 WLS [1–0] – Character Length.

These bits specify the length of each transmitted or received serial character.

Bits 10	Character Length
00	5 Bits
01	6 Bits
10	7 Bits
11	8 Bits

B2 STB – Stop Bits.

Number of stop bits in each transmitted serial character. If this bit is 0, 1 stop bit is generated in the transmitted data. If it is 1 and a 5-bit character length is selected via bits 0 and 1, 1.5 stop bits are generated. If it is 1 and a 6, 7 or 8-bit character length is selected, 2 stop bits are generated. The receiver checks 1 stop bit only, regardless of the number of stop bits selected.

B3 PEN – Parity Enable.

When set to 1, parity bits are generated and checked by the transmitter and receiver channels respectively.

B4 EPS – Even Parity.

3.0 Architectural Description (Continued)

Used in conjunction with the STKP bit to determine the parity bit. See encodings below.

B5 STKP – Stick Parity.

The encodings of this and the previous two bits, for control of the parity bit, are as follows:

PEN	EPS	STKP	Selected Parity
0	x	x	none
1	0	0	odd
1	1	0	even
1	0	1	logic 1
1	1	1	logic 0

B6 SBRK – Set Break.

When set to 1, the following occurs:

— If UART mode is selected, the SOUT pin is forced to a logic 0 state.

— If SIR mode is selected, pulses are issued continuously on the IRTX pin.

— If Sharp-IR mode is selected and internal modulation is enabled, pulses are issued continuously on the IRTX pin.

— If Sharp-IR mode is selected and internal modulation is disabled, the IRTX pin is forced to a logic 1 state.

The break is disabled by setting this bit to 0. This bit acts only on the transmitter front-end and has no effect on the rest of the transmitter logic.

The following sequence should be followed to avoid transmission of erroneous characters because of the break.

1. Wait for the transmitter to be empty (TXEMP = 1).
2. Set SBRK to 1
3. Wait for the transmitter to be empty, and clear SBRK when normal transmission has to be restored.

During the break, the transmitter can be used as a character timer to accurately establish the break duration.

B7 BKSE – Bank Select Enable.

In the LCR register this bit is always 0.

BSR – Bank Select Register

When bit 7 is 1, bits 0–6 of BSR are used to select the bank. The encodings are shown in *Table 4.*

TABLE 4. Bank Selection Encodings

BSR Bits								Selected Bank
7	6	5	4	3	2	1	0	
0	x	x	x	x	x	x	x	0
1	0	x	x	x	x	x	x	1
1	1	x	x	x	x	1	x	1
1	1	x	x	x	x	x	1	1
1	1	1	0	0	0	0	0	2
1	1	1	0	0	1	0	0	3
1	1	1	0	1	0	0	0	4
1	1	1	0	1	1	0	0	5
1	1	1	1	0	0	0	0	6
1	1	1	1	0	1	0	0	7
1	1	1	1	1	x	0	0	Reserved
1	1	0	x	x	x	0	0	Reserved

3.1.5 MCR – Modem/Mode Control Register

Used to control the interface with the modem or data set, as well as the device operational mode. The function of this register changes depending upon whether the device is in extended or non-extended mode. In extended mode the interrupt output signal is always enabled and loopback can be selected by setting bit 4 of the EXCR1 register. Upon reset, all bits are set to 0.

3.0 Architectural Description (Continued)

Non-Extended Mode

The format of the non-extended mode MCR is shown in *Figure 10*.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	—	—	—	LOOP	ISEN/ DCDLP	RILP	RTS	$\overline{DTR}$
Reset State	0	0	0	0	0	0	0	0

FIGURE 10. Modem Control Register, Non-Extended Mode

B0 DTR – Data Terminal Ready.

This bit controls the $\overline{DTR}$ signal output.

When it is set to 1, $\overline{DTR}$ is driven low.

In loopback mode this bit internally drives DSR.

B1 RTS – Request to Send.

This bit controls the $\overline{RTS}$ signal output.

When it is set to 1, $\overline{RTS}$ is driven low.

In loopback mode this bit internally drives CTS.

B2 RILP – Loopback RI.

In normal operation this bit is unused.

In loopback mode this bit internally drives RI.

B3 ISEN/DCDL – Interrupt Signal Enable/Loopback DCD.

In normal operation this bit controls the interrupt signal, and it must be set to 1 in order to enable it.

In loopback mode, this bit internally drives DCD, and the interrupt signal is always enabled.

Note: New programs should always keep this bit set to 1 during normal operation. The interrupt signal should be controlled through the Plug-n-Play logic.

B4 LOOP – Loopback Enable.

When set to 1, loopback mode is selected.

This bit accesses the same internal register as bit 4 of the EXCR1 register.

Refer to the section describing the EXCR1 register for more information on the loopback mode.

B7–5 Reserved.

Forced to 0.

Extended Mode

The format of the extended mode MCR is shown in *Figure 11*.

Note: Bits 2 to 7 should always be initialized after the operational mode is changed from non-extended to extended.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	MDSL2	MDSL1	MDSL0	IR__PLS	TX__DFR	DMA__EN	RTS	DTR
Reset State	0	0	0	0	0	0	0	0

FIGURE 11. Modem Control Register, Extended Mode

B0 DTR – Data Terminal Ready.

This bit controls the $\overline{DTR}$ signal output.

When it is set to 1, $\overline{DTR}$ is driven low.

In loopback mode this bit internally drives both DSR and RI.

B1 RTS – Request to Send.

This bit controls the $\overline{RTS}$ signal output.

When it is set to 1, $\overline{RTS}$ is driven low.

In loopback mode this bit internally drives both CTS and DCD.

B2 DMA__EN – DMA Mode Enable.

When set to 1, DMA mode of operation is enabled.

When data transfers are performed by a DMA controller, the transmit and/or receive data interrupts should be disabled to avoid spurious interrupts.

Note that DMA cycles always access the data holding registers or FIFOs, regardless of the selected bank.

B3 TX__DFR – Transmit Deferral.

When set to 1, transmit deferral is enabled.

Effective only when the TX__FIFO is enabled.

B4 IR__PLS – Send Interaction Pulse.

This bit is effective only in MIR and FIR Modes.

It is set to 1 by writing 1 into it.

Writing 0 into it has no effect.

When set to 1, a 2 µs infrared interaction pulse is transmitted at the end of the frame and the bit is automatically cleared by the hardware.

This bit is also cleared when the transmitter is soft reset.

Note: The interaction pulse must be emitted at least once every 500 ms, as long as the high-speed connection lasts, in order to quiet slower (115.2 kbps or below) systems that might otherwise interfere with the link.

B7–5 MDSL [2–0] – Mode Select.

These bits are used to select the operational mode as shown in *Table 5*.

When the mode is changed, the transmitter and receiver are soft reset, and the modem status events are cleared.

TABLE 5. UIR Module Operational Modes

Bits 7 6 5	Operational Mode
000	UART
001	Reserved
010	Sharp-IR
011	SIR
100	MIR
101	FIR
110	CEIR
111	Reserved

3.1.6 LSR – Link Status Register

This register provides status information to the CPU concerning the data transfer.

Bits 1 through 4 (and 7 when in MIR or FIR mode) indicate link status events.

These bits are sticky, and accumulate any conditions occurred since the last time the register was read.

These bits are cleared when any of the following events occurs:

1. Hardware reset.
2. The receiver is soft reset.
3. The LSR register is read.

Note: This register is intended for read operations only. Writing to this register is not recommended as it may cause indeterminate results.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	ER__INF/ FR__END	TXEMP	TXRDY	BRK/ MAX__LEN	FE/ PHY__ERR	PE/ BAD__CRC	OE	RXDA
Reset State	0	1	1	0	0	0	0	0

FIGURE 12. Link Status Register

B0 RXDA – Receiver Data Available.

Set to 1 when the Receiver Holding Register is full.

If the FIFOs are enabled, this bit is set when at least one character is in the RX__FIFO.

Cleared when the CPU reads all the data in the Holding Register or in the RX__FIFO.

B1 *UART, Sharp-IR, SIR, CEIR Modes*

OE – Overrun Error.

This bit is set to 1 as soon as an overrun condition is detected by the receiver.

Cleared upon read.

FIFOs Disabled: An overrun occurs when a new character is completely received into the receiver front-end section and the CPU has not yet read the previous character in the receiver holding register. The new character is discarded, and the receiver holding register is not affected.

3.0 Architectural Description (Continued)

FIFOs Enabled: An overrun occurs when a new character is completely received into the receiver front-end section and the RX__FIFO is full.

The new character is discarded, and the RX__FIFO is not affected.

MIR, FIR Modes

OE – Overrun Error.

An overrun occurs when a new character is completely received into the receiver front-end section and the RX__FIFO or the ST__FIFO is full.

The new character is discarded, and the RX__FIFO is not affected.

Cleared upon read.

B2 *UART, Sharp-IR, SIR Modes*

PE – Parity Error.

This bit is set to 1 if the received character did not have the correct parity, as selected by the parity control bits in the LCR register.

If the FIFOs are enabled, the Parity Error condition will be associated with the particular character in the RX__FIFO it applies to.

In which case, the PE bit is set when the character reaches the bottom of the RX__FIFO.

Cleared upon read.

MIR, FIR Modes

BAD__CRC – CRC Error.

Set to 1 when a mismatch between the received CRC and the receiver-generated CRC is detected, and the last byte of the received frame has reached the bottom of the RX__FIFO.

Cleared upon read.

B3 *UART, Sharp-IR, SIR Modes*

FE – Framing Error.

This bit indicates that the received character did not have a valid stop bit.

It is set to 1 when the stop bit is detected as a logic 0.

If the FIFOs are enabled, the Framing Error condition will be associated with the particular character in the RX__FIFO it applies to.

In which case, the FE bit is set when the character reaches the bottom of the RX__FIFO.

After a Framing Error is detected, the receiver will try to resynchronize.

If the bit following the stop bit position is 0, the receiver assumes it to be a valid start bit and the next character is shifted in.

If that bit is 1, the receiver will enter the idle state looking for the next start bit.

Cleared upon read.

MIR Mode

PHY__ERR – Physical Layer Error.

Set to 1 when an abort condition is detected during the reception of a frame, and the last byte of the frame has reached the bottom of the RX__FIFO.

Cleared upon read.

FIR Mode

PHY__ERR – Physical Layer Error.

Set to 1 when an encoding error or the sequence BOF-data-BOF is detected (missing EOF) during the reception of a frame, and the last byte of the frame has reached the bottom of the RX__FIFO.

Cleared upon read.

B4 *UART, Sharp-IR, SIR Modes*

BRK – Break Event Detected.

Set to 1 when a sequence of logic 0 bits, equal or longer than a full character transmission, is received.

If the FIFOs are enabled, the Break condition will be associated with the particular character in the RX__FIFO it applies to.

In which case, the BRK bit is set when the character reaches the bottom of the RX__FIFO. When a Break occurs only one zero character is transferred to the receiver holding register or to the RX__FIFO.

The next character transfer takes place after at least one logic 1 bit is received followed by a valid start bit.

Cleared upon read.

MIR, FIR Modes

MAX__LEN – Maximum Length.

Set to 1 when a frame exceeding the maximum length has been received, and the last byte of the frame has reached the bottom of the RX__FIFO.

3.0 Architectural Description (Continued)

Cleared upon read.

B5 TXRDY – Transmitter Ready.

This bit is set to 1 when the Transmitter Holding Register or the TX__FIFO is empty.

It is cleared when a data character is written to the TXD port.

B6 TXEMP – Transmitter Empty.

Set to 1 when the Transmitter is empty. The transmitter empty condition occurs when the Holding Register or the TX__FIFO is empty, and the transmitter front-end is idle.

B7 *UART, Sharp-IR, SIR Modes*

ER__INF – Error in RX__FIFO.

Set to 1 when at least one character with a PE, FE or BRK condition is in the RX__FIFO.

This bit is always 0 in 16450 mode.

MIR, FIR Modes

FR__END – Frame End.

Set to 1 when the last byte (Frame End Byte) of a received frame reaches the bottom of the RX__FIFO.

Cleared upon read.

3.1.7 MSR – Modem Status Register

The function of this register depends on the selected operational mode. When UART Mode is selected, this register provides the current-state as well as state-change information of the status lines from the MODEM or Data Set. When any one of the Infrared Modes is selected, the register function is controlled by the setting of the IRMSSL bit in the IRCR2 register. If IRMSSL is 0, the MSR register works the same as in UART mode. If IRMSSL is 1, the MSR register returns the value 30h, regardless of the state of the MODEM input lines.

In Loopback mode, the MSR register works similarly except that its status inputs are internally driven by appropriate bits in the MCR register since the MODEM input lines are internally disconnected. Refer to the sections describing the MCR and EXCR1 register for more information.

A description of the various bits of MSR, with Loopback disabled and UART Mode selected, is provided below. When any of the bits 0 to 3 is set to 1, a Modem Status Interrupt is generated. Bits 0 to 3 are set to 0 when any of the following events occurs.

1. Hardware reset.
2. The MSR register is read.
3. The operational mode is changed and the IRMSSL bit is 0.

Note: The modem status lines have no effect on transmitter and receiver operation. They can be used as general purpose inputs.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS
Reset State	X	X	X	X	0	0	0	0

FIGURE 13. Modem Status Register

B0 DCTS – Delta Clear to Send.

Set to 1 when the $\overline{\text{CTS}}$ input changes state.

Cleared upon read.

B1 DDSR – Delta Data Set Ready.

Set to 1 when the $\overline{\text{DSR}}$ input changes state.

Cleared upon read.

B2 TERI – Ring Indicator Trailing Edge.

Set to 1 when the $\overline{\text{RI}}$ input changes from a low state to a high state.

Cleared upon read.

B3 DDCD – Delta Data Carrier Detect.

Set to 1 when the $\overline{\text{DCD}}$ input changes state.

Cleared upon read.

B4 CTS – Clear to Send.

This bit returns the complement of the $\overline{\text{CTS}}$ input.

B5 DSR – Data Set Ready.

This bit returns the complement of the $\overline{\text{DSR}}$ input.

B6 RI – Ring Indicator.

This bit returns the complement of the $\overline{\text{RI}}$ input.

3.0 Architectural Description (Continued)

B7 DCD – Data Carrier Detect.

This bit returns the complement of the $\overline{DCD}$ input.

3.1.8 SPR/ASCR – Scratchpad/Auxiliary Status and Control Register

These registers share the same address.

SPR– Scratchpad Register.

This register is accessed when the device is in non-extended mode.

It does not control the device in any way, and is intended to be used by the programmer to hold data temporarily.

ASCR– Auxiliary Status and Control Register.

This register is accessed when the extended mode of operation is selected.

All the ASCR bits are cleared when a hardware reset occurs or when the operational mode changes.

Bits 2 and 6 are cleared when the transmitter is soft reset.

Bits 0, 1, 4 and 5 are cleared when the receiver is soft reset.

The format of ASCR is shown in *Figure 14*.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	PLD/ CTE	TXUR	RXBSY/ RXACT	LOST__FR/ RXWDG	TXHFE	S__EOT	FEND__INF	RXF__TOUT
Reset State	0	0	0	0	0	0	0	0

FIGURE 14. Auxiliary Status and Control Register

B0 **RXF__TOUT – RX__FIFO Time-out.**

This bit is read-only, and is set to 1 when an RX__FIFO time-out occurs.

In MIR or FIR modes this bit can be used in conjunction with bit 1 to determine whether a number of bytes, as determined by the RX__FIFO threshold, can be read without checking the RXDA bit in the LSR register for each byte. Cleared when a character is read from the RX__FIFO.

B1 *MIR, FIR Modes*

FEND__INF – Frame End Bytes in RX__FIFO.

This bit is read-only, and is set to 1 when one or more Frame End bytes are in the RX__FIFO.

Cleared when no Frame End byte is in the RX__FIFO.

B2 *MIR, FIR Modes*

S__EOT – Set End of Transmission.

When a 1 is written into this bit position before writing the last character into the TX__FIFO, frame transmission is completed and a CRC + EOF is sent. This bit can be used as an alternative to the Transmitter Frame Length register. If this method is to be used, the FEND__MD bit in the IRCR2 register should be set to 1, or the Transmitter Frame Length register should be set to maximum count.

This bit is automatically cleared by the hardware when a character is written into the TX__FIFO.

CEIR Mode

S__EOT – Set End of Transmission.

When a 1 is written into this bit position before writing the last character into the TX__FIFO, data transmission is gracefully completed. If the CPU simply stops writing data into the TX__FIFO at the end of the data stream, a transmitter underrun is generated and the transmitter stops. In this case, this is not an error, however the software needs to clear the underrun before the next transmission can occur.

This bit is automatically cleared by the hardware when a character is written into the TX__FIFO.

B3 *MIR, FIR Modes*

TXHFE – Transmitter Halted on Frame End.

This bit is used only when the transmitter frame-end stop mode is selected (TX__MS bit in IRCR2 set to 1). It is set to 1 by the hardware when transmission of a frame is complete and the *end-of-frame* condition was generated by the TFRCC counter reaching 0.

This bit must be cleared, by writing 1 into it, to re-enable transmission.

B4 *MIR, FIR Modes*

LOST__FR – Lost Frame Flag.

This bit is read-only, and reflects the setting of the lost-frame indicator flag at the bottom of the ST__FIFO.

CEIR Mode

RXWDG – Receiver Watch Dog.

3.0 Architectural Description (Continued)

Set to 1 each time an infrared pulse or pulse-train is detected by the receiver.

Can be used by the software to detect a receiver idle condition.

Cleared upon read.

B5 *MIR, FIR Modes*

RXBSY – Receiver Busy.

This bit is read-only, and returns a 1 when reception of a frame is in progress.

CEIR Mode

RXACT – Receiver Active.

Set to 1 when an infrared pulse or pulse-train is received. If a 1 is written into this bit position, the bit is cleared and the receiver is deactivated. When this bit is set, the receiver samples the infrared input continuously at the programmed baud rate and transfers the data to the RX__FIFO.

B6 *MIR, FIR, CEIR Modes*

TXUR – Transmitter Underrun.

This bit is set to 1 when a transmitter underrun occurs.

It is always cleared when a mode other than MIR, FIR or CEIR is selected.

This bit must be cleared, by writing 1 into it, to re-enable transmission.

B7 *UART, Sharp-IR, CEIR Modes*

CTE - Clear Timer Event

Writing 1 into this bit position clears the TMR_EV bit in the EIR register. Writing 0 into it has no effect.

MIR, FIR, SIR Modes

PLD/CTE – Pipeline Load Status/Clear Timer Event.

Reading this bit returns the pipeline load status. It is set to 1 by the hardware when a pipeline load operation occurs. It is cleared upon read.

Writing 1 into this bit position clears the TMR__EV bit in the EIR register. Writing 0 into it has no effect. The write operation has no effect on the Pipeline Load Status.

3.2 BANK 1

TABLE 6. Bank 1 Register Set

Address Offset	Register Name	Description
0	**LBGD(L)**	Legacy Baud Generator Divisor Port (Low-Byte)
1	**LBGD(H)**	Legacy Baud Generator Divisor Port (High-Byte)
2	**Reserved**	
3	**LCR/BSR**	Link Control/Bank Select Registers
4-7	**Reserved**	

3.2.1 LBGD – Legacy Baud Generator Divisor Port

This port provides an alternate data path to the baud generator divisor register. It is implemented for compatibility with the 16550 and to support existing legacy software packages. New software should use the BGD port in bank 2 to access the baud generator devisor register. Like the BGD port, LBGD is 16 bits wide and is split into two 8-bit parts, LBGD(L) and LBGD(H), occupying consecutive address locations. A CPU read or write access of the divisor register, through either LBGD(L) or LBGD(H), will affect the device operational mode as follows.

If the device is in extended mode, the device is switched back to 16550 compatibility mode.

In addition to the EXT__SL bit, the following bits are also cleared.

1. Bits 2 to 7 of extended-mode MCR.
2. Bit 5 and 7 of EXCR1.
3. Bits 0 to 5 of EXCR2.
4. Bits 2 and 3 of IRCR1.

If the device is in non-extended mode and the LOCK bit is 0, the following bits will be cleared.

1. Bits 5 and 7 of EXCR1.
2. Bits 0 to 5 of EXCR2.

If the device is in non-extended mode and the LOCK bit is 1, the content of the divisor register will not be affected and no other action is taken.

3.0 Architectural Description (Continued)

3.2.2 LCR/BSR – Link Control/Bank Select Registers

These registers are the same as in bank 0.

3.3 BANK 2

TABLE 7. Bank 2 Register Set

Address Offset	Register Name	Description
0	**BGD(L)**	Baud Generator Divisor Port (Low-Byte)
1	**BGD(H)**	Baud Generator Divisor Port (High-Byte)
2	**EXCR1**	Extended Control Register 1
3	**LCR/BSR**	Link Control/Bank Select Registers
4	**EXCR2**	Extended Control Register 2
5	**Reserved**	
6	**TXFLV**	TX__FIFO Level
7	**RXFLV**	RX__FIFO Level

3.3.1 BGD – Baud Generator Divisor Port

This port provides the data path to the baud generator divisor register that holds the reload value for the baud generator counter. Divisor values from 1 to $2^{16} - 1$ can be used. See *Table 8.* The zero value is reserved and must not be used. The programmed value must be such that the baud generator output clock frequency is sixteen times the desired baud rate value. The baud generator divisor register is 16 bits wide and is split into two independently accessible 8-bit parts. Correspondingly, the BGD port is also 16 bits wide and is split into two 8-bit parts, occupying consecutive address locations. BGD(L) is located at the lower address and accesses the least significant part of the baud generator divisor register, whereas BGD(H) is located at the higher address and accesses the most significant part. The baud generator divisor register must be loaded during initialization to ensure proper operation of the baud generator. Upon loading either part of it, the baud generator counter is immediately loaded.

After reset, the content of the baud generator divisor register is indeterminate.

TABLE 8. Baud Generator Divisor Settings

Prescaler Value	13		1.625		1	
Baud Rate	**Divisor**	**% Error**	**Divisor**	**% Error**	**Divisor**	**% Error**
50	2304	0.16%	18461	0.00%	30000	0.00%
75	1536	0.16%	12307	0.01%	20000	0.00%
110	1047	0.19%	8391	0.01%	13636	0.00%
134.5	857	0.10%	6863	0.00%	11150	0.02%
150	768	0.16%	6153	0.01%	10000	0.00%
300	384	0.16%	3076	0.03%	5000	0.00%
600	192	0.16%	1538	0.03%	2500	0.00%
1200	96	0.16%	769	0.03%	1250	0.00%
1800	64	0.16%	512	0.16%	833	0.04%
2000	58	0.53%	461	0.12%	750	0.00%
2400	48	0.16%	384	0.16%	625	0.00%
3600	32	0.16%	256	0.16%	416	0.16%
4800	24	0.16%	192	0.16%	312	0.16%
7200	16	0.16%	128	0.16%	208	0.16%
9600	12	0.16%	96	0.16%	156	0.16%
14400	8	0.16%	64	0.16%	104	0.16%
19200	6	0.16%	48	0.16%	78	0.16%
28800	4	0.16%	32	0.16%	52	0.16%
31250	—	—	—	—	48	0.00
38400	3	0.16%	24	0.16%	39	0.16%

3.0 Architectural Description (Continued)

TABLE 8. Baud Generator Divisor Settings (Continued)

Prescaler Value	13		1.625		1	
Baud Rate	**Divisor**	**% Error**	**Divisor**	**% Error**	**Divisor**	**% Error**
57600	2	0.16%	16	0.16%	26	0.16%
115200	1	0.16%	8	0.16%	13	0.16%
230400	—	—	4	0.16%	—	—
460800	—	—	2	0.16%	—	—
750000	—	—	—	—	2	0.00%
921600	—	—	1	0.16%	—	—
1500000	—	—	—	—	1	0.00%

3.3.2 EXCR1 – Extended Control Register 1

Used to control the extended mode of operation.

Upon reset all bits are set to 0.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	BTEST	res	ETDLBK	LOOP	DMASWP	DMATH	DMANF	EXT__SL
Reset State	0	0	0	0	0	0	0	0

FIGURE 15. Extended Control Register 1

B0 EXT__SL – Extended Mode Select.

When set to 1, extended mode is selected.

B1 DMANF – DMA Fairness Control.

This bit controls the maximum duration of DMA burst transfers.

0 → DMA requests are forced inactive after approximately 10.5 µs of continuous transmitter and/or receiver DMA operation.

1 → A TX__DMA request is deactivated when the TX__FIFO is full.

An RX__DMA request is deactivated when the RX__FIFO is empty.

B2 DMATH – DMA Threshold Levels Select.

This bit selects the TX__FIFO and RX__FIFO threshold levels used by the DMA request logic to support demand transfer mode.

A TX__DMA request is generated when the TX__FIFO level is below the threshold.

An RX__DMA request is generated when the RX__FIFO level reaches the threshold or when an RX__FIFO time-out occurs.

Bit Value	RX__FIFO DMA Thresh.	TX__FIFO DMA Thresh. (16-Levels)	TX__FIFO DMA Thresh. (32-Levels)
0	4	13	29
1	10	7	23

B3 DMASWP – DMA Swap.

This bit selects the routing of the DMA control signals between the internal DMA logic and the configuration module. When this bit is 0, the transmitter and receiver DMA control signals are not swapped. When it is 1, they are swapped. A block diagram illustrating the control signals routing is given in *Figure 16*.

The swap feature is particularly useful when only one 8237 DMA channel is used to serve both transmitter and receiver. In this case only one external DRQ/$\overline{\text{DACK}}$ signal pair will be interconnected to the swap logic by the configuration module. Routing the external DMA channel to either the transmitter or the receiver DMA logic is then simply controlled by the DMASWP bit. This way, the infrared device drivers do not need to know the details of the configuration module.

B4 LOOP – Loopback Enable.

When set to 1, loopback mode is selected.

This bit accesses the same internal register as bit 4 in the MCR register, when the device is in non-extended mode.

Loopback mode behaves similarly in both non-extended and extended modes.

When extended mode is selected, the DTR bit in the MCR register internally drives both $\overline{\text{DSR}}$ and $\overline{\text{RI}}$, and the $\overline{\text{RTS}}$ bit drives $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$.

During loopback the following occur:

3.0 Architectural Description (Continued)

1. The transmitter and receiver interrupts are fully operational. The modem status interrupts are also fully operational, but the interrupts' sources are now the lower bits of the MCR register. Modem interrupts in infrared modes are disabled unless the IRMSSL bit in the IRCR2 register is 0. Individual interrupts are still controlled by the IER register bits.
2. The DMA control signals are fully operational.
3. UART and infrared receiver serial input pins are disconnected. The internal receiver serial inputs are connected to the corresponding internal transmitter serial outputs.
4. The UART transmitter serial output pin is forced high and the infrared transmitter serial output pin is forced low, unless the ETDLBK bit is set to 1. In which case they will function normally.
5. The modem status input pins ($\overline{DSR}$, $\overline{CTS}$, $\overline{RI}$ and $\overline{DCD}$) are disconnected. The internal modem status signals, are driven by the lower bits of the MCR register.

B5 ETDLBK – Enable Transmitter Output During Loopback.

When set to 1, the transmitter serial output is enabled and functions normally when loopback is selected.

B6 Reserved.

Write 1.

B7 BTEST – Baud Generator Test.

When set to 1, the output of the baud generator is routed to the DTR pin.

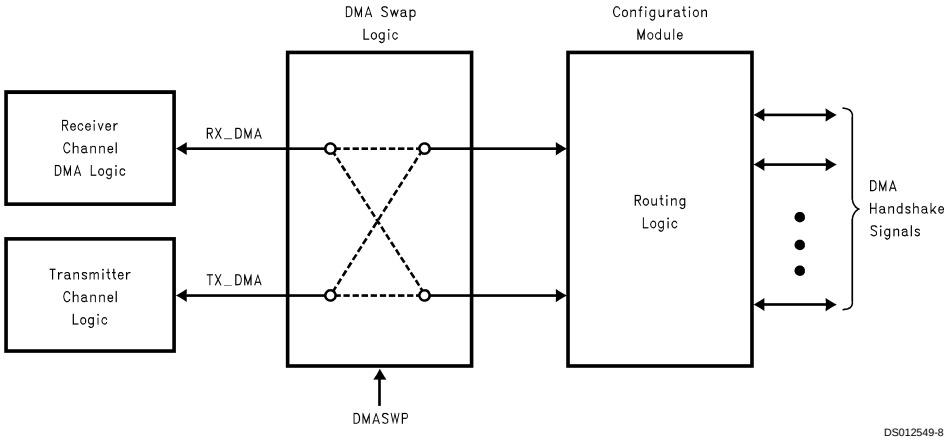


FIGURE 16. DMA Control Signals Routing

3.3.3 LCR/BSR – Link Control/Bank Select Registers

These registers are the same as in bank 0.

3.3.4 EXCR2 – Extended Control Register 2

This register is used to configure the transmitter and receiver FIFOs, and the baud generator prescaler.

Upon reset all bits are set to 0.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	LOCK	res	PRESL1	PRESL0	RF__SIZ1	RF__SIZ0	TF__SIZ1	TF__SIZ0
Reset State	0	0	0	0	0	0	0	0

FIGURE 17. Extended Control Register 2

B1–0 TF__SIZ [1–0] – TX__FIFO Levels Select.

These bits select the number of levels for the TX__FIFO.

They are effective only when the FIFOs are enabled.

Bits 1–0	TX__FIFO Levels
00	16
01	32
1x	Reserved

3.0 Architectural Description (Continued)

B3–2 RF__SIZ [1–0] – RX__FIFO Levels Select.

These bits select the number of levels for the RX__FIFO.

They are effective only when the FIFOs are enabled.

Bits 3–2	RX__FIFO Levels
00	16
01	32
1x	Reserved

B5–4 PRESL [1–0] – Prescaler Select.

The prescaler divides the 24 MHz input clock frequency to provide the clock for the baud generator.

Bits 5–4	Prescaler Value
0 0	13.0
0 1	1.625
1 0	Reserved
1 1	1.0

B6 Reserved.

Read/write 0.

B7 LOCK – Lock Bit.

When set to 1, accesses to the baud generator divisor register through LBGD(L) and LBGD(H) as well as fallback are disabled from non-extended mode.

In this case two scratchpad registers overlayed with LBGD(L) and LBGD(H) are enabled, and any attempted CPU access of the baud generator divisor register through LBGD(L) and LBGD(H) will access the scratchpad registers instead. This bit must be set to 0 when extended mode is selected.

3.3.5 TXFLV – TX__FIFO Level, Read-Only

This register returns the number of bytes in the TX__FIFO. It can be used for software debugging, or during recovery from a transmitter underrun condition in one of the high-speed infrared modes.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	res	TFL5	TFL4	TFL3	TFL2	TFL1	TFL0
Reset State	0	0	0	0	0	0	0	0

FIGURE 18. Transmit FIFO Level

B5–0 TFL [5–0] – Number of bytes in TX__FIFO.

B7–6 Reserved.

Return 0's.

3.3.6 RXFLV – RX__FIFO Level, Read-Only

This register returns the number of bytes in the RX__FIFO. It can be used for software debugging.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	res	RFL5	RFL4	RFL3	RFL2	RFL1	RFL0
Reset State	0	0	0	0	0	0	0	0

FIGURE 19. Receive FIFO Level

B5–0 RFL [5–0] – Number of bytes in RX__FIFO.

B7–6 Reserved.

Return 0's.

Note: The contents of TXFLV and RXFLV are not frozen during CPU reads. Therefore, invalid data could be returned if the CPU reads these registers during normal transmitter and receiver operation. To obtain correct data, the software should perform three consecutive reads and then take the data from the second read, if first and second read yield the same result, or from the third read, if first and second read yield different results.

3.0 Architectural Description (Continued)

3.4 BANK 3

TABLE 9. Bank 3 Register Set

Address Offset	Register Name	Description
0	**MID**	Module Identification Register
1	**SH__LCR**	Link Control Register Shadow
2	**SH__FCR**	FIFO Control Register Shadow
3	**LCR/BSR**	Link Control/Bank Select Registers
4–7	**Reserved**	

3.4.1 MID – Module Identification Register, Read Only

When read, it returns the module revision.

The returned value is 2Xh.

3.4.2 SH__LCR – Link Control Register Shadow, Read Only

This register returns the value of the LCR register.

The LCR register is written into when a byte value with bit 7 set to 0 is written to the LCR/BSR registers location (at offset 3) from any bank.

3.4.3 SH__FCR – FIFO Control Register Shadow, Read-Only

This register returns the value written into the FCR register in bank 0.

3.4.4 LCR/BSR – Link Control/Bank Select Registers

These registers are the same as in bank 0.

3.5 BANK 4

TABLE 10. Bank 4 Register Set

Address Offset	Register Name	Description
0	**TMR(L)**	Timer Register (Low-Byte)
1	**TMR(H)**	Timer Register (High-Byte)
2	**IRCR1**	Infrared Control Register 1
3	**LCR/BSR**	Link Control/Bank Select Registers
4	**TFRL(L)/ TFRCC(L)**	Transmitter Frame Length/ Current Count (Low Byte)
5	**TFRL(H)/ TFRCC(H)**	Transmitter Frame Length/ Current Count (High Byte)
6	**RFRML(L)/ RFRCC(L)**	Receive Frame Maximum Length/ Current Count (Low Byte)
7	**RFRML(H)/ RFRCC(H)**	Receive Frame Maximum Length/ Current Count (High Byte)

3.5.1 TMR – Timer Register

This register is used to program the reload value for the internal down-counter as well as to read the current counter value. TMR is 12 bits wide and is split into two independently accessible parts occupying consecutive address locations. TMR(L) is located at the lower address and accesses the least significant 8 bits, whereas TMR(H) is located at the higher address and accesses the most significant 4 bits. Values from 1 to $2^{12} - 1$ can be used. The zero value is reserved and must not be used. The upper 4 bits of TMR(H) are reserved and must be written with 0's. The timer resolution is 125 µs, providing a maximum time-out interval of approximately 0.5 seconds. To properly program the timer, the CPU must always write the lower value into TMR(L) first, and then the upper value into TMR(H). Writing into TMR(H) causes the counter to be loaded. A read of TMR returns the current counter value if the CTEST bit is 0, or the programmed reload value if CTEST is 1. In order for a read access to return an accurate value, the CPU should always read TMR(L) first, and then TMR(H). This is because a read of TMR(H) returns the content of an internal latch that is loaded with the 4 most significant bits of the current counter value when TMR(L) is read. After reset, the content of this register is indeterminate.

3.0 Architectural Description (Continued)

3.5.2 IRCR1 – Infrared Control Register 1

Used to control the timer and counters as well as enable the Sharp-IR or SIR infrared mode in the non-extended mode of operation.

Upon reset, all bits are set to 0.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	res	res	res	IR__SL1	IR__SL0	CTEST	TMR__EN
Reset State	0	0	0	0	0	0	0	0

FIGURE 20. Infrared Control Register 1

B0 TMR__EN – Timer Enable, Extended Mode Only.

When this bit is 1, the timer is enabled.

When it is 0, the timer is frozen.

B1 CTEST – Counters Test.

When this bit is set to 1, the TMR register reload value, as well as the TFRL and RFRML register contents are returned during CPU reads.

B3–2 IR__SL [1–0] – SIR or Sharp-IR Select, Non-Extended Mode Only.

These bits are used to select the appropriate infrared mode when the device is in non-extended mode.

They are ignored when extended mode is selected.

Bits 3–2	Selected Mode
00	UART
01	Reserved
10	Sharp-IR
11	SIR

B7–4 Reserved.

Write as 0's.

3.5.3 LCR/BSR – Link Control/Bank Select Registers

These Registers are the same as in bank 0.

3.5.4 TFRL/TFRCC – Transmitter Frame-Length/Current-Count

These registers share the same addresses. TFRL is always accessed during write cycles and is used to program the frame length, in bytes, for the frames to be transmitted. The frame length value does not include any appended CRC bytes. TFRL is accessed during read cycles if the CTEST bit is set to 1, and returns the previously programmed value. Values from 1 to $2^{13} - 1$ can be used. The zero value is reserved and must not be used. TFRCC is loaded with the content of TFRL when transmission of a frame begins, and decrements after each byte is transmitted. It is read-only and is accessed during CPU read cycles when the CTEST bit is 0. It returns the number of currently remaining bytes of the frame being transmitted. These registers are 13 bits wide and are split into two independently accessible parts occupying consecutive address locations. TFRL(L) and TFRCC(L) are located at the lower address and access the least significant 8 bits, whereas TFRL(H) and TFRCC(H) are located at the higher address and access the most significant 5 bits. To properly program TFRL, the CPU must always write the lower value into TFRL(L) first, and then the upper value into TFRL (H). The upper 3 bits of TFRL(H) are reserved and must be written with 0's. In order for a read access of TFRCC to return an accurate value, the CPU should always read TFRCC(L) first, and then TFRCC(H). After reset, the content of the TFRL register is 800h.

3.5.5 RFRML/RFRCC – Receiver Frame Maximum-Length/Current-Count

These registers share the same addresses. RFRML is always accessed during write cycles and is used to program the maximum frame length, in bytes, for the frames to be received. The maximum frame length value includes the CRC bytes. RFRML is accessed during read cycles if the CTEST bit is set to 1, and returns the previously programmed value. Values from 4 to $2^{13} - 1$ can be used. The values from 0 to 3 are reserved and must not be used. RFRCC holds the current byte count of the incoming frame, and increments after each byte is received. It is read-only and is accessed during CPU read cycles when the CTEST bit is 0. These registers are 13 bits wide and are split into two independently accessible parts occupying consecutive address locations. RFRML(L) and RFRCC(L) are located at the lower address and access the least significant 8 bits, whereas RFRML(H) and RFRCC(H) are located at the higher address and access the most significant 5 bits. To properly program RFRML, the CPU must always write the lower value into RFRML(L) first, and then the upper value into RFRML(H). The upper 3 bits of RFRML(H) are reserved and must be written with 0's. In order for a read access of RFRCC to return an accurate value, the CPU should always read RFRCC(L) first, and then RFRCC(H). After reset, the content of the RFRML register is 800h.

Note: TFRCC and RFRCC are intended for testing purposes only. Use of these registers for any other purpose is not recommended.

3.0 Architectural Description (Continued)

3.6 BANK 5

TABLE 11. Bank 5 Register Set

Address Offset	Register Name	Description
0	**P__BGD(L)**	Pipelined Baud Generator Divisor Register (Low-Byte)
1	**P__BGD(H)**	Pipelined Baud Generator Divisor Register (High-Byte)
2	**P__MDR**	Pipeline Mode Register
3	**LCR/BSR**	Link Control/Bank Select Registers
4	**IRCR2**	Infrared Control Register 2
5	**FRM__ST**	Frame Status
6	**RFRL(L)/LSTFRC**	Received Frame Length (Low-Byte)/Lost Frame Count
7	**RFRL(H)**	Received Frame Length (High-Byte)

3.6.1 P__BGD – Pipelined Baud Generator Divisor Register

This register holds the value that determines the new baud rate following a pipeline operation. It is a 16-bit wide register and is split into two 8-bit parts, P__BGD(L) and P__BGD(H), occupying consecutive address locations. The value written into these registers will be loaded into the least and most significant parts of the baud generator divisor register when the transmitter becomes empty and both the MD__PEN and BR__PEN bits in the P__MDR register are set to 1. Upon reset, the content of this register is indeterminate.

3.6.2 P__MDR – Pipelined Mode Register

This register can be read or written in any mode. However, a pipeline operation will only take place if the presently selected mode and the target mode are both IrDA modes.

Furthermore, SIR must be selected in extended mode and the TX__FIFO must be enabled.

When a pipeline operation takes place, the following occurs:

1. If the target mode is MIR or FIR, the transmitter is halted for 250 µs.
2. If the target mode is SIR, the transmitter is halted for 250 µs or a character time (at the newly selected baud rate), whichever is greater.
3. Bits 7, 6, 5 and 2 will be loaded into the corresponding bit positions in the MCR register in bank 0, bit 3 will be loaded into bit position 3 of EXCR1.

Upon reset, all bits are set to 0.

Bits	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Function	P__MDSL2	P__MDSL1	P__MDSL0	res	P__DMASWP	P__DMA__EN	BR__PEN	MD__PEN
Reset State	0	0	0	0	0	0	0	0

FIGURE 21. Pipelined Mode Register

B0 MD__PEN – Mode Bits Pipelining Enable.

When this bit is set to 1 and the transmitter becomes empty, a pipeline load operation takes place.

This bit is automatically cleared after the load has occurred.

B1 BR__PEN – Baud Rate Pipelining Enable.

This bit is effective only when the MD__PEN bit is set to 1.

When it is set to 1 and a pipeline load operation takes place, the P__BGD register will be loaded into the baud generator divisor register.

B2 P__DMA__EN – Pipelined DMA Enable Bit

B3 P__DMASWP – Pipelined DMA Swap Bit

B4 Reserved.

Write 0.

B7–5 P__MDSL [2–0] – Pipelined Mode Select Bits

3.6.3 LCR/BSR – Link Control/Bank Select Registers

These registers are the same as in bank 0.

3.0 Architectural Description (Continued)

3.6.4 IRCR2 – Infrared Control Register 2

Upon reset, the content of this register is 02h.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	SFTSL	FEND__MD	AUX__IRRX	TX__MS	MDRS	IRMSSL	IR__FDPLX
Reset State	0	0	0	0	0	0	1	0

FIGURE 22. Infrared Control Register 2

B0 IR__FDPLX – Infrared Full Duplex Mode.

When set to 1, the infrared receiver is not masked during transmission.

B1 IRMSSL – MSR Register Function Select in Infrared Mode.

This bit selects the behavior of the modem status register/interrupt when any infrared mode is selected. When UART mode is selected, the modem status register and interrupt function normally, and this bit is ignored.

0 → MSR register and modem status interrupt work as in UART mode.

1 → MSR register returns 30h and the modem status interrupt is disabled.

B2 MDRS – MIR Data Rate Select.

This bit determines the data rate in MIR mode.

0 → 1.152 Mbps

1 → 0.576 Mbps

B3 TX__MS – Transmitter Mode Select.

This bit is used in MIR and FIR modes only. When it is set to 1, transmitter frame-end stop mode is selected. In this case the transmitter stops after transmission of a frame is complete, if the *end-of-frame* condition was generated by the TFRCC counter reaching 0. The transmitter can be restarted by clearing the TXHFE bit in the ASCR register.

B4 AUX__IRRX – Auxiliary Infrared Input Select.

When set to 1, the infrared signal is received from the auxiliary input. See *Table 17*.

B5 FEND__MD – Frame End Control.

This bit selects whether a terminal-count condition from the

TFRCC register will generate an EOF in PIO mode or DMA mode.

0 → TFRCC terminal count effective in PIO mode.

1 → TFRCC terminal count effective in DMA mode.

B6 SFTSL – ST__FIFO Threshold Select.

An interrupt request is generated when the ST__FIFO level reaches the threshold or when an ST__FIFO time-out occurs.

Bit Value	Threshold Level
0	2
1	4

B7 Reserved.

Read/write 0.

3.6.5 ST__FIFO – Status FIFO

The ST__FIFO is used in MIR and FIR Modes.

It is an 8-level FIFO and is intended to support back-to-back incoming frames in DMA mode, when an 8237-type DMA controller is used. Each ST__FIFO entry contains either status information and frame length for a single frame, or the number of lost frames. The bottom entry spans three address locations, and is accessed via the FRM__ST, RFRL(L)/LSTFRC and RFRL(H) registers. The ST__FIFO is flushed when a hardware reset occurs or when the receiver is soft reset.

Note: The status and length information of received frames is loaded into the ST__FIFO whenever the DMA__EN bit in the extended-mode MCR register is set to 1 and an 8237 type DMA controller is used, regardless of whether the CPU or the DMA controller is transferring the data from the RX__FIFO to memory. This implies that, during testing, if full duplex is enabled and a DMA channel is servicing the transmitter while the CPU is servicing the receiver, the CPU must still read the ST__FIFO. Otherwise, it fills up and incoming frames will be rejected.

3.0 Architectural Description (Continued)

3.6.5.1 FRM__ST – Frame Status Byte at ST__FIFO Bottom, Read-Only

This register returns the status byte at the bottom of the ST__FIFO. If the LOST__FR bit is 0, bits 0 to 4 indicate if any error condition occurred during reception of the corresponding frame. Error conditions will also affect the error flags in the LSR register.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	VLD	LOST__FR	res.	MAX__LEN	PHY__ERR	BAD__CRC	OVR1	OVR2
Reset State	0	0	0	0	0	0	0	0

FIGURE 23. Frame Status Byte

B0 OVR2 – Overrun Error 2.

This bit is set to 1 when incoming characters or entire frames have been discarded due to the ST__FIFO being full.

B1 OVR1 – Overrun Error 1.

This bit is set to 1 when incoming characters or entire frames have been discarded due to the RX__FIFO being full.

B2 BAD__CRC – CRC Error.

Set to 1 when a mismatch between the received CRC and the receiver-generated CRC is detected.

B3 PHY__ERR – Physical Layer Error.

Set to 1 when an encoding error or the sequence BOF-data-BOF is detected in FIR mode, or an abort condition is detected in MIR mode.

B4 MAX__LEN – Maximum Frame Length Exceeded.

Set to 1 when a frame exceeding the maximum length has been received.

B5 Reserved.

Returned data is indeterminate.

B6 LOST__FR – Lost Frame Indicator Flag.

Indicates the type of information provided by this ST__FIFO entry.

0 → Entry provides status information and length for a received frame.

1 → Entry provides overrun indications and number of lost frames.

B7 VLD – ST__FIFO Entry Valid.

When set to 1, the bottom ST__FIFO entry contains valid data.

3.6.5.2 RFRL(L)/LSTFRC – Received Frame Length /Lost-Frame-Count at ST__FIFO Bottom, Read-Only

This register should be read only when the VLD bit in FRM__ST is 1. The information returned depends on the setting of the LOST__FR bit. Upon reset, all bits are set to 0.

LOST__FR = 0 → Least significant 8 bits of the received frame length.

LOST__FR = 1 → Number of lost frames

3.6.5.3 RFRL(H) – Received-Frame-Length at ST__FIFO Bottom, Read-Only

This register should be read only when the VLD bit in FRM__ST is 1. The information returned depends on the setting of the LOST__FR bit. Upon reset, all bits are set to 0.

LOST__FR = 0 → Most significant 5 bits of the received frame length.

LOST__FR = 1 → All 0's

Reading this register removes the bottom ST__FIFO entry.

3.7 BANK 6

TABLE 12. Bank 6 Register Set

Address Offset	Register Name	Description
0	**IRCR3**	Infrared Control Register 3
1	**MIR__PW**	MIR Pulse Width Register
2	**SIR__PW**	SIR Pulse Width Register
3	**LCR/BSR**	Link Control/Bank Select Registers
4	**BFPL**	Beginning Flags/Preamble Length Register
5–7	**Reserved**	

3.0 Architectural Description (Continued)

3.7.1 IRCR3 – Infrared Control Register 3

Used to select the operating mode of the infrared interface.

Upon reset, the content of this register is 20h.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	SHDM__DS	SHMD__DS	FIR__CRC	MIR__CRC	res	TXCRC__INV	TXCRC__DS	res
Reset State	0	0	1	0	0	0	0	0

FIGURE 24. Infrared Control Register 3

B0 Reserved.

Write 0.

B1 TXCRC__DS – Disable Transmitter CRC.

When set to 1, a CRC is not transmitted.

B2 TXCRC__INV – Invert Transmitter CRC.

When set to 1, an inverted CRC is transmitted. This bit can be used to force a bad CRC for testing purposes.

B3 Reserved.

Write 0.

B4 MIR__CRC – MIR Mode CRC Select.

Determines the length of the CRC in MIR mode.

0 → 16-bit CRC

1 → 32-bit CRC

B5 FIR__CRC – FIR Mode CRC Select.

Determines the length of the CRC in FIR mode.

0 → 16-bit CRC

1 → 32-bit CRC

B6 SHMD__DS – Sharp-IR Modulation Disable.

When set to 1, internal 500 kHz transmitter modulation is disabled.

B7 SHDM__DS – Sharp-IR Demodulation Disable.

When set to 1, internal 500 kHz receiver demodulation is disabled.

3.7.2 MIR__PW – MIR Pulse Width Register

This register is used to program the width of the transmitted MIR infrared pulses in increments of either 20.833 ns or 41.666 ns depending on the setting of the MDSR bit in the IRCR2 register. The programmed value has no effect on the MIR receiver. After reset, the content of this register is 0Ah.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	res	res	res	MPW3	MPW2	MPW1	MPW0
Reset State	0	0	0	0	1	0	1	0

FIGURE 25. MIR Pulse Width Register

B3-0 MPW [3–0] – MIR Signal Pulse Width

Encoding	Pulse Width, MDRS = 0	Pulse Width, MDRS = 1
00XX	Reserved	Reserved
0100	83.33 ns	166.66 ns
0101	104.16 ns	208.33 ns
0110	125 ns	250 ns
0111	145.83 ns	291.66 ns
1000	166.66 ns	333.33 ns
1001	187.50 ns	374.99 ns
1010	208.33 ns	416.66 ns
1011	229.16 ns	458.33 ns
1100	250 ns	500 ns
1101	270.83 ns	541.66 ns

Encoding	Pulse Width, MDRS = 0	Pulse Width, MDRS = 1
1110	291.66 ns	583.32 ns
1111	312.5 ns	625 ns

B7-4 Reserved.
Write 0's.

3.7.3 SIR__PW – SIR Pulse Width Register

This register determines the width of the transmitted SIR infrared pulses.
The programmed value has no effect on the SIR receiver. After reset, the content of this register is 0.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	res	res	res	SPW3	SPW2	SPW1	SPW0
Reset State	0	0	0	0	0	0	0	0

FIGURE 26. SIR Pulse Width Register

B3-0 SPW [3-0] – SIR Signal Pulse Width.

Encoding	Pulse Width
0000	3/16 of bit time
1101	1.6 µs

Other encodings are reserved and will select a pulse width of 1.6 µs.

B7-4 Reserved.
Write 0's.

3.7.4 LCR/BSR – Link Control/Bank Select Registers

These registers are the same as in bank 0.

3.7.5 BFPL – Beginning Flags/Preamble Length Register

Used to program the number of beginning flags and preamble symbols for MIR and FIR modes respectively.
After reset, the content of this register is 2Ah, selecting 2 beginning flags and 16 preamble symbols.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	MBF3	MBF2	MBF1	MBF0	FPL3	FPL2	FPL1	FPL0
Reset State	0	0	1	0	1	0	1	0

FIGURE 27. Beginning Flags/Preamble Length Register

B3–0 FPL [3–0] – FIR Preamble Length.
Selects the number of preamble symbols for FIR frames.

Encoding	Preamble Length
0000	Reserved
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	8
1000	10
1001	12
1010	16
1011	20
1100	24
1101	28

Encoding	Preamble Length
1110	32
1111	Reserved

B7–4 MBF [3–0] – MIR Beginning Flags.

Selects the number of beginning flags for MIR frames.

Encoding	Beginning Flags
0000	Reserved
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	8
1000	10
1001	12
1010	16
1011	20
1100	24
1101	28
1110	32
1111	Reserved

3.8 BANK 7

TABLE 13. Bank 7 Register Set

Address Offset	Register Name	Description
0	IRRXDC	Infrared Receiver Demodulator Control
1	IRTXMC	Infrared Transmitter Modulator Control
2	RCCFG	Consumer-IR Configuration
3	LCR/BSR	Link Control/Bank Select Registers
4	IRCFG1	Infrared Interface Configuration Register 1
5	IRCFG2	Infrared Interface Configuration Register 2
6	IRCFG3	Infrared Interface Configuration Register 3
7	IRCFG4	Infrared Interface Configuration Register 4

3.8.1 IRRXDC – Infrared Receiver Demodulator Control Register

After reset, the content of this register is 29h, selecting a frequency range from 34.61 kHz to 38.26 kHz for the CEIR mode, and from 480.0 kHz to 533.3 kHz for Sharp-IR mode. The value of this register is ignored if receiver demodulation for both Sharp-IR and CEIR mode is disabled. The available frequency ranges for CEIR and Sharp-IR modes are given in *Table 14* through *Table 16.*

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	DBW2	DBW1	DBW0	DFR4	DFR3	DFR2	DFR1	DFR0
Reset State	0	0	1	0	1	0	0	1

FIGURE 28. Infrared Receiver Demodulator Control Register

B4–0 DFR [4–0] – Demodulator Frequency.

These bits determine the subcarrier's center frequency for the CEIR mode.

B7–5 DBW [2–0] – Demodulator Bandwidth.

3.0 Architectural Description (Continued)

These bits determine the demodulator bandwidth within which the subcarrier signal frequency has to fall in order for the signal to be accepted.

Used for both Sharp-IR and CEIR modes.

TABLE 14. CEIR Low-Speed Demodulator Frequency Ranges in kHz (RXHSC = 0)

	DBW [2–0] Bits											
	001		010		011		100		101		110	
DFR [4–0]	min	max	min	max	min	max	min	max	min	max	min	max
00011	28.6	31.6	27.3	33.3	26.1	35.3	25.0	37.5	24.0	40.0	23.1	42.9
00100	29.3	32.4	28.0	34.2	26.7	36.2	25.6	38.4	24.6	41.0	23.7	43.9
00101	30.1	33.2	28.7	35.1	27.4	37.1	26.3	39.4	25.2	42.1	24.3	45.1
00110	31.7	35.1	30.3	37.0	29.0	39.2	27.8	41.7	26.7	44.4	25.6	47.6
00111	32.6	36.0	31.1	38.1	29.8	40.3	28.5	42.8	27.4	45.7	26.3	48.9
01000	33.6	37.1	32.0	39.2	30.7	41.5	29.4	44.1	28.2	47.0	27.1	50.4
01001	34.6	38.3	33.0	40.4	31.6	42.8	30.3	45.4	29.1	48.5	28.0	51.9
01011	35.7	39.5	34.1	41.7	32.6	44.1	31.3	46.9	30.0	50.0	28.8	53.6
01100	36.9	40.7	35.2	43.0	33.7	45.5	32.3	48.4	31.0	51.6	29.8	55.3
01101	38.1	42.1	36.4	44.4	34.8	47.1	33.3	50.0	32.0	53.3	30.8	57.1
01111	39.4	43.6	37.6	45.9	36.0	48.6	34.5	51.7	33.1	55.1	31.8	59.1
10000	40.8	45.1	39.0	47.6	37.3	50.4	35.7	53.6	34.3	57.1	33.0	61.2
10010	42.3	46.8	40.4	49.4	38.6	52.3	37.0	55.6	35.6	59.3	34.2	63.5
10011	44.0	48.6	42.0	51.3	40.1	54.3	38.5	57.7	36.9	61.5	35.5	65.9
10101	45.7	50.5	43.6	53.3	41.7	56.5	40.0	60.0	38.4	64.0	36.9	68.6
10111	47.6	52.6	45.5	55.6	43.5	58.8	41.7	62.5	40.0	66.7	38.5	71.4
11010	49.7	54.9	47.4	57.9	45.3	61.4	43.5	65.2	41.7	69.5	40.1	74.5
11011	51.9	57.4	49.5	60.6	47.4	64.1	45.4	68.1	43.6	72.7	41.9	77.9
11101	54.4	60.1	51.9	63.4	49.7	67.2	47.6	71.4	45.7	76.1	43.9	81.6

TABLE 15. CEIR High-Speed Demodulator Frequency Ranges in kHz (RXHSC = 1)

	DBW [2–0] Bits											
	001		010		011		100		101		110	
DFR [4–0]	min	max	min	max	min	max	min	max	min	max	min	max
00011	381.0	421.1	363.6	444.4	347.8	470.6	333.3	500.0	320.0	533.3	307.7	571.4
01000	436.4	480.0	417.4	505.3	400.0	533.3	384.0	564.7	369.2	600.0	355.6	640.0
01011	457.7	505.3	436.4	533.3	417.4	564.7	400.0	600.0	384.0	640.0	369.9	685.6

TABLE 16. Sharp-IR Demodulator Frequency Ranges in kHz

	DBW [2–0] Bits											
	001		010		011		100		101		110	
DFR [4–0]	min	max	min	max	min	max	min	max	min	max	min	max
xxxxx	480.0	533.3	457.1	564.7	436.4	600.0	417.4	640.0	400.0	685.6	384.0	738.5

3.8.2 IRTXMC – Infrared Transmitter Modulator Control Register

Used to select the modulation subcarrier parameters for CEIR and Sharp-IR modes. For Sharp-IR, only the subcarrier pulse width is controlled by this register, the subcarrier frequency is fixed at 500 kHz.

After reset, the content of this register is 69h, selecting a subcarrier frequency of 36 kHz and a pulse width of 7 µs for CEIR, or a pulse width of 0.8 µs for Sharp-IR.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	MCPW2	MCPW1	MCFW0	MCFR4	MCFR3	MCFR2	MCFR1	MCFR0
Reset State	0	1	1	0	1	0	0	1

FIGURE 29. Infrared Transmitter Modulator Control Register

B4–0 MCFR [4–0] – Modulation Subcarrier Frequency.

Selects the frequency for the CEIR modulation subcarrier.

Encoding	Low Frequency, TXHSC = 0	High Frequency, TXHSC = 1
00000	Reserved	Reserved
00001	Reserved	Reserved
00010	Reserved	Reserved
00011	30 kHz	400 kHz
00100	31 kHz	Reserved
00101	32 kHz	Reserved
00110	33 kHz	Reserved
00111	34 kHz	Reserved
01000	35 kHz	450 kHz
01001	36 kHz	Reserved
01010	37 kHz	Reserved
01011	38 kHz	480 kHz
01100	39 kHz	Reserved
01101	40 kHz	Reserved
01110	41 kHz	Reserved
01111	42 kHz	Reserved
10000	43 kHz	Reserved
10001	44 kHz	Reserved
10010	45 kHz	Reserved
10011	46 kHz	Reserved
10100	47 kHz	Reserved
10101	48 kHz	Reserved
10110	49 kHz	Reserved
10111	50 kHz	Reserved
11000	51 kHz	Reserved
11001	52 kHz	Reserved
11010	53 kHz	Reserved
11011	54 kHz	Reserved
11100	55 kHz	Reserved
11101	56 kHz	Reserved
11110	56.9 kHz	Reserved
11111	Reserved	Reserved

B7–5 MCPW [2–0] – Modulation Subcarrier Pulse Width.

Encoding	Low Frequency, TXHSC = 0 (Consumer-IR only)	High Frequency, TXHSC = 1 (Consumer-IR or Sharp-IR)
000	Reserved	Reserved
001	Reserved	Reserved
010	6 µs	0.7 µs
011	7 µs	0.8 µs
100	9 µs	0.9 µs
101	10.6 µs	Reserved

Encoding	Low Frequency, TXHSC = 0 (Consumer-IR only)	High Frequency, TXHSC = 1 (Consumer-IR or Sharp-IR)
110	Reserved	Reserved
111	Reserved	Reserved

3.8.3 RCCFG – CEIR Configuration Register

This register controls the basic operation of the CEIR mode.

After reset, all bits are set to 0.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	R__LEN	T__OV	RXHSC	RCDM__DS	res	TXHSC	RC__MMD1	RC__MMD0
Reset State	0	0	0	0	0	0	0	0

FIGURE 30. CEIR Configuration Register

B1–0 RC__MMD [1–0] – Transmitter Modulation Mode.

Determines how infrared pulses are generated from the transmitted bit string.

00 → C__PLS Modulation Mode.

Pulses are generated continuously for the entire logic 0 bit time.

01 → 8__PLS Modulation Mode.

8 pulses are generated each time one or more logic 0 bits are transmitted following a logic 1 bit.

10 → 6__PLS Modulation Mode.

6 pulses are generated each time one or more logic 0 bits are transmitted following a logic 1 bit.

11 → Reserved.

Result is indeterminate.

B2 TXHSC – Transmitter Subcarrier Frequency Select.

Selects the frequency range for the modulation subcarrier.

0 → 30–56.9 kHz

1 → 400–480 kHz

B3 Reserved.

Write 0.

B4 RCDM__DS – Receiver Demodulation Disable.

When this bit is 1, the internal demodulator is disabled. The internal demodulator, when enabled, performs subcarrier frequency checking and envelope generation.

It must be disabled when demodulation is done externally, or when oversampling mode is used to determine the subcarrier frequency.

B5 RXHSC – Receiver Subcarrier Frequency Select.

Selects the frequency range for the receiver demodulator.

0 → 30–56.9 kHz

1 → 400–480 kHz

B6 T__0V – Receiver Sampling Mode.

0 → Programmed-T-period sampling.

1 → Oversampling Mode.

B7 R__LEN – Run-Length Control.

When set to 1, run-length encoding/decoding is enabled.

The format of a run-length code is YXXXXXXX, where:

Y - Bit value

XXXXXXX — Number of bits minus 1.

(Selects 1 to 128 bits).

3.0 Architectural Description (Continued)

3.8.4 LCR/BSR – Link Control/Bank Select Registers

These registers are the same as in bank 0.

3.8.5 IRCFG [1–4] – Infrared Interface Configuration Registers

Four registers are provided to configure the infrared interface. These registers are used to select the infrared receiver inputs as well as the transceiver operational mode. Selection of the transceiver mode is accomplished by up to three special output signals (ID/IRSL [2–0]). When these signals are programmed as outputs, they will be forced low when automatic configuration is enabled (AMCFG bit set to 1) and UART mode is selected.

3.8.5.1 IRCFG1 – Infrared Interface Configuration Register 1

This register holds the transceiver configuration data for Sharp-IR and SIR Modes.

When automatic configuration is not enabled, it is used to directly control the transceiver operational mode. The least significant four bits are also used to read the identification data of a Plug-n-Play infrared adapter.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	STRV__MS	SIRC2	SIRC1	SIRC0	IRID3	IRIC2	IRIC1	IRIC0
Reset State	0	0	0	0	X	X	X	X

FIGURE 31. Infrared Configuration Register 1

B0 IRIC0 – Transceiver Identification/Control.

The function of this bit depends on whether the ID0/IRSL0/IRRX2 pin is programmed as an input or as an output.

ID0/IRSL0/IRRX2 Pin Programmed as Input (IRSL0__DS = 0).

Upon read, this bit returns the logic level of the pin.

Data written into this bit position is ignored.

ID0/IRSL0/IRRX2 Pin Programmed as Output (IRSL0__DS = 1).

If AMCFG is set to 1, this bit will drive the ID0/IRSL0/IRRX2 pin when Sharp-IR Mode is selected.

If AMCFG is 0, this bit will drive the ID0/IRSL0/IRRX2 pin regardless of the selected mode.

Upon read, this bit returns the value previously written.

B2–1 IRIC[2–1] – Transceiver Identification/Control

The function of these bits depends on whether the ID/IRSL[2–1] pins are programmed as inputs or as outputs.

ID/IRSL[2–1] Pins Programmed as Inputs (IRSL21__DS = 0).

Upon read, these bits return the logic levels of the pins.

Data written into these bit positions is ignored.

ID/IRSL[2–1] Pins Programmed as Outputs (IRSL21__DS = 1).

If AMCFG is set to 1, these bits will drive the ID/IRSL[2–1] pins when Sharp-IR Mode is selected.

If AMCFG is 0, these bits will drive the ID/IRSL[2–1] pins regardless of the selected mode.

Upon read, these bits return the values previously written.

B3 IRID3 – Transceiver Identification.

Upon read, it returns the logic level of the ID3 pin.

Data written into this bit position is ignored.

B6–4 SIRC [2–0] – SIR Mode Transceiver Configuration.

These bits will drive the ID/IRSL[2–0] pins when AMCFG is 1 and SIR Mode is selected.

They are unused when AMCFG is 0 or when the ID/IRSL[2–0] pins are programmed as inputs.

Upon read, these bits return the values previously written.

B7 STRV__MS – Special Transceiver Mode Select.

This bit is used to select the operational mode in some optical transceiver modules. When this bit is set to 1, the IRTX output is forced high and a timer is started.

The timer times out after approximately 64 µs, at which time the bit is reset and IRTX returns low. The timer is restarted every time a 1 is written into this bit position. Therefore, the time in which IRTX is forced high can be extended beyond 64 µs.

This should be avoided, however, to prevent damage to the transmitter LED.

Writing 0 into this bit position has no effect.

3.0 Architectural Description (Continued)

3.8.5.2 IRCFG2 – Infrared Interface Configuration Register 2

This register holds the transceiver configuration data for MIR and FIR Modes.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	FIRC2	FIRC1	FIRC0	res	MIRC2	MIRC1	MIRC0
Reset State	0	0	0	0	0	0	0	0

FIGURE 32. Infrared Configuration Register 2

B2–0 MIRC [2–0] – MIR Mode Transceiver Configuration.

These bits will drive the ID/IRSL[2–0] pins when AMCFG is 1 and MIR Mode is selected.

They are unused when AMCFG is 0 or when the ID/IRSL [2–0] pins are programmed as inputs.

Upon read, these bits return the values previously written.

B3 Reserved.

Write 0.

B6–4 FIRC [2–0] – FIR Mode Transceiver Configuration.

These bits will drive the ID/IRSL [2–0] pins when AMCFG is 1 and FIR Mode is selected.

They are unused when AMCFG is 0 or when the ID/IRSL [2–0] pins are programmed as inputs.

Upon read, these bits return the values previously written.

B7 Reserved.

Write 0.

3.8.5.3 IRCFG3 — Infrared Interface Configuration 3

This register holds the transceiver configuration data for Low-Speed and High-Speed Consumer-IR Modes.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	RHCH2	RHCH1	RHCH0	res	RCLC2	RCLC1	RCLC0
Reset State	0	0	0	0	0	0	0	0

FIGURE 33. Infrared Configuration Register 3

B2–0 RCLC [2–0] – Consumer-IR Mode Transceiver Configuration, Low-Speed.

These bits will drive the ID/IRSL[2–0] pins when AMCFG is 1 and Consumer-IR Mode with 30 kHz–56 kHz receiver subcarrier frequency is selected.

They are unused when AMCFG is 0 or when the ID/IRSL[2–0] pins are programmed as inputs.

Upon read, these bits return the values previously written.

B3 Reserved.

Write 0.

B6–4 RCHC [2–0] – Consumer-IR Mode Transceiver Configuration, High-Speed.

These bits will drive the ID/IRSL[2–0] pins when AMCFG is 1 and Consumer-IR Mode with 400 kHz–480 kHz receiver subcarrier frequency is selected.

They are unused when AMCFG is 0 or when the ID/IRSL[2–0] pins are programmed as inputs.

Upon read, these bits return the values previously written.

B7 Reserved.

Write 0.

3.8.5.4 IRCFG4 – Infrared Interface Configuration 4

This register is used to configure the receiver data path and enable the automatic selection of the configuration pins. After reset, the content of this register is 0.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	AMCFG	IRRX__MD	IRSL0__DS	RXINV	IRSL21__DS	res	res	res
Reset State	0	0	0	0	0	0	0	0

FIGURE 34. Infrared Configuration Register 4

B2–0 Reserved.

3.0 Architectural Description (Continued)

Read/write 0's.

B3 IRSL21__DS – ID/IRSL[2–1] Pins' Direction Select.

This bit determines the direction of the ID/IRSL[2–1] pins.

0 → Pins' direction is input.

1 → Pins' direction is ouput.

B4 RXINV – IRRX Signal Invert.

This bit is provided to support optical transceivers with receive signals of opposite polarity (active high instead of active low).

When set to 1, an inverter is placed on the receiver input signal path.

B5 IRSL0__DS – ID0/IRSL0/IRRX2 Pin Direction Select.

This bit determines the direction of the ID0/IRSL0/IRRX2 pin.

0 → Pin's direction is input.

1 → Pin's direction is output.

B6 IRRX__MD – IRRX Mode Select.

Determines whether a single input or two separate inputs are used for Low-Speed and High-Speed IrDA modes.

0 → One input is used for both SIR and MIR/FIR.

1 → Separate inputs are used for SIR and MIR/FIR.

Table 17 shows the IRRXn pins used in the PC87108A for the low-speed and high-speed infrared modes, and for the various combinations of IRSL0__DS, IRRX__MD and AUX__IRRX.

B7 AMCFG – Automatic Module Configuration Enable.

When set to 1, automatic infrared transceiver configuration is enabled.

TABLE 17. Infrared Receiver Input Selection (HIS__IR = 1 When Selected Mode is MIR or FIR)

IRSL0__DS	IRRX__MD	AUX__IRRX	HIS__IR	IRRXn
0	0	0	x	IRRX1
0	0	1	x	IRRX2
0	1	X	0	IRRX1
0	1	X	1	IRRX2
1	0	0	X	IRRX1
1	0	1	X	IRRX3
1	1	X	0	IRRX1
1	1	X	1	IRRX3

4.0 Device Configuration

4.1 OVERVIEW

On power-up or after a hardware reset, the PC87108A will have all of its modules and functions disabled.

The GPIO and ID/IRSL [2–0] pins are in input mode. The IRTX and the UART output pins are set to their inactive state. Before normal operation can be started, the device must be enabled and several items must be configured. These include the routing of the interrupt and DMA control signals, as well as the setting of direction and output data for the GPIO pins.

Routing of interrupt and DMA control signals is provided to support plug-and-play, and is usually handled by the system plug-and-play BIOS.

Additional items, related to the communications protocols and the infrared transceiver interface, are configured via appropriate registers in the UIR module register set.

4.2 CONFIGURATION AND GPIO REGISTERS

Five registers are provided to control the basic configuration and the GPIO pins. One additional register is provided for device identification. The way these registers are accessed is determined by the levels of the BADDR0 and BADDR1 pins during reset. Two accessing modes are provided: Index/Data register mode, and CS (chip select) mode.

In the Index/Data register mode, two registers occupying consecutive address locations, are used. An index value is first loaded into the Index register. The desired register is then read or written by accessing the Data register. As *Table 18* shows, one of three different addresses for the Index register can be selected.

4.0 Device Configuration (Continued)

After reset, the Index register can be located by performing a read from each of these addresses. A successful read will return a value of 5Ah. This value is only returned once after reset. Subsequent reads will return 00h or any value previously written to the Index register. To prevent false identification due to a floating bus, it is recommended to read twice and check for both values 5Ah and 00h.

The CS mode linearizes the PC87108A address space. The selected register bank occupies address locations at offsets 0 to 7. The configuration and GPIO registers are accessible at offsets 08h to 0Dh. A total of 14 locations are used. The two locations at offsets 0Eh and 0Fh are reserved.

In the CS Mode, address inputs A4 to A15 are unused and should be pulled up to V_{DD} through a 1 kΩ resistor.

The configuration and GPIO registers, with index and address offset values, are shown in *Table 19*. A description of these registers is provided in the following sections.

TABLE 18. Base Address Configuration

BADDR1	BADDR0	Index Register	Data Register
0	0	EAh	EBh
0	1	398h	399h
1	0	150h	151h
1	1	CS Mode	CS Mode

TABLE 19. Configuration and GPIO Registers

Index/Offset	Register	Description
0/08h	BAIC	Base Address and Interrupt Control Register
1/09h	CSRT	Control Signals Routing Register
2/0Ah	MCTL	Mode Control Register
3/0Bh	GPDIR	GPIO Direction Register
4/0Ch	GPDAT	GPIO Data Register
5/0Dh	DID	Device Identification Register

4.2.1 BAIC – Base Address and Interrupt Control Register (index = 00h/offset = 08h)

This register determines the device base address. It also controls the IRQ output buffer and the selection of the register banks.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	res	res	IRQBC	IRQINV	EN__BNK	BAS1	BAS0
Reset State	X	X	X	0	0	0	0	0

FIGURE 35. Base Address and Interrupt Control Register

B1–0 BAS1 [1–0] – Base Address Select.

These Bits select one of four base addresses, when the Index/Data register accessing mode is selected. In the CS mode, they are ignored.

Bits 1–0	Base Address
0 0	3E8h
0 1	2E8h
1 0	3F8h
1 1	2F8h

B2 EN__BNK – Enable Register Banks.

When set to 1, any bank from 0 to 7 can be selected.

When this bit is cleared, only banks 0 and 1 can be selected, and any attempt to select banks 2 to 7 is ignored.

B3 IRQINV – IRQ Polarity Invert.

When set to 1, the IRQ output signal polarity is inverted.

Value	IRQ Signal
0	Active High
1	Active Low

B4 IRQBC – IRQ Output Buffer Configuration.

This bit determines whether the IRQ output buffer is configured as Open Drain or Totem Pole.

Value	Output Buffer Type
0	Open Drain
1	Totem Pole

B7–5 Reserved.

Read/write as 0.

4.2.2 CSRT – Control Signals Routing Register (index = 01h/offset = 09h)

This register is used to select the Interrupt output signal, and the DMA control signals for the device's receiver and transmitter communication channels.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	SLERR	TXD__SL1	TXD__SL0	RXD__SL1	RXD__SL0	IRQ__SL2	IRQ__SL1	IRQ__SL0
Reset State	0	0	0	0	0	0	0	0

FIGURE 36. Control Signals Routing Register

B2–0 IRQ__SL [2–0] – IRQ Signal Select.

Selects the IRQ output to be used for interrupt signaling.

After reset, no interrupt is selected, and all the IRQ output pins are in TRI-STATE® condition.

Encoding	IRQ Selected
000	None
001	IRQ3
010	IRQ4
011	IRQ5
100	IRQ7
101	IRQ9
110	IRQ11
111	IRQ15

B4–3 RXD__SL [1–0] – Receiver DMA Control Signals Select.

These bits determine which external DMA control signals are routed to the internal receiver DMA channel when the DMASWP bit is 0. Refer to the DMASWP bit description for more information.

Encoding	DMA Signals Selected
00	None
01	DRQ0/$\overline{\text{DACK0}}$
10	DRQ1/$\overline{\text{DACK1}}$
11	DRQ3/$\overline{\text{DACK3}}$

B6–5 TXD__SL [1–0] – Transmitter DMA Signals Select.

These bits determine which external DMA control signals are routed to the internal transmitter DMA channel when the DMASWP bit is 0. Refer to the DMASWP bit description for more information.

Encoding	DMA Signals Selected
00	None
01	DRQ0/$\overline{\text{DACK0}}$
10	DRQ1/$\overline{\text{DACK1}}$
11	DRQ3/$\overline{\text{DACK3}}$

B7 SLERR – DMA Signals Selection Error.

This is a read-only bit. It will be set to 1 if the same DMA control signals are selected for both the transmitter and receiver channels.

In which case all the DMA control input signals are ignored, and all the DMA control output signals are in TRI-STATE® condition.

4.0 Device Configuration (Continued)

4.2.3 MCTL – Mode Control Register (index = 02h/offset = 0Ah)

This register is used to enable the device and select the power mode.

It also returns the device's Busy/Idle state.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	MTEST	res	AUXIR__SL	BUSY__SL	BUSY2	NOM	DEV__EN
Reset State	X	0	0	0	0	0	0	0

FIGURE 37. Mode Control Register

B0 DEV__EN – Device Enable.

When set to 1, the device is enabled.

When this bit is 0, the device is disabled and the following occurs:

1. All internal modules are powered down.
2. Accesses to the UIR module registers are inhibited, and the bus is not driven during reads.
3. Accesses to the configuration and GPIO registers are handled normally.
4. UART interface outputs are set to their inactive state.
5. UART interface inputs are blocked.
6. ID/IRSL[2–0] pins programmed as outputs are not affected.
7. ID/IRSL[2–0] pins programmed as inputs, as well as ID3 are blocked.
8. IRTX is set to its inactive state.
9. IRRXn inputs are blocked.
10. IRQ and DMA control outputs are floated.
11. DMA control inputs are blocked
12. GPIO pins are fully functional.
13. Bus interface signals are fully functional.
14. All the register contents are maintained.

B1 NOM – Normal Operating Mode.

This bit must be set to 1 for normal operation. When this bit is 0, the device is in low power mode and the following occurs:

1. All internal modules are powered down.
2. Accesses to all the device's internal registers are handled normally.
3. UART interface outputs are set to their inactive state.
4. UART interface inputs except RI are blocked.
5. The RI (ring indicator) signal can be programmed to generate an interrupt.
6. ID/IRSL[2–0] pins programmed as outputs are not affected.
7. ID/IRSL[2–0] pins programmed as inputs, as well as ID3 are blocked.
8. IRTX is set to its inactive state.
9. IRRXn inputs are blocked.
10. The selected IRQ output is fully functional.
11. The selected DMA control outputs (if any) are set to their inactive state.
12. DMA control inputs are blocked.
13. GPIO pins are fully functional.
14. Bus interface signals are fully functional.
15. All the register contents are maintained.

B2 BUSY – Busy Status.

This bit is read-only. It is set to 1 whenever a data transfer is in progress. It can be used by the power management software to determine when the device can be shut down.

B3 BUSY__SL – BUSY Output Select.

Enables the BUSY bit to be driven on the GPIO3/BUSY pin, when the pin is programmed as an output (DIR3 bit in GPDIR set to 1).

Value	Pin Function
0	GPIO3
1	BUSY bit status

B4 AUXIR__SL – AUXSL Output Select.

Enables the AUX__IRRX bit in the IRCR2 register to be driven on the GPIO2/AUXSL pin, when the pin is programmed as an output (DIR2 bit in GPDIR set to 1).

Value	Pin Function
0	GPIO2
1	AUX__IRRX bit

B5 Reserved.

Write 0.

B6 MTEST – Manufacturing Test.

This bit is used for factory testing. It must be set to 0 for normal operation.

B7 Reserved.

Write 0.

4.2.4 GPDIR – GPIO Direction Register (index = 03h/offset = 0Bh)

This register determines the direction of the four General Purpose I/O pins.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	res	res	res	DIR3	DIR2	DIR1	DIR0
Reset State	X	X	X	X	0	0	0	0

FIGURE 38. GPIO Direction Register

B3–0 DIR [3–0] – Direction Select.

Setting any of these bits to 1 will program the corresponding GPIO pin as an output.

B7–4 Reserved.

Write 0's.

4.2.5 GPDAT – GPIO Data Register (index = 04h/offset = 0Ch)

This register is used to input data from or to output data to the GPIO pins.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	res	res	res	DAT3	DAT2	DAT1	DAT0
Reset State	X	X	X	X	X	X	X	X

FIGURE 39. GPIO Data Register

B3–0 DAT [3–0] – Data Bits.

When a GPIO pin is programmed as an output, data written into the corresponding data bit position will be latched and driven on the pin. If bit 3 or 4 in the MCTL register is set to 1, data written into bit DAT3 or DAT2 will be latched, but it will not appear on the output pin.

When a GPIO pin is programmed as an input, a read will return the value of the pin. If a pin is left unconnected, reading the corresponding data bit will return a value of 1. Data written into a data bit position will be latched, but it will not have any effect on the pin.

B7–4 Reserved.

Write 0's.

4.2.6 DID – Device Identification Register (index = 05h/offset = 0Dh)

This is a read-only register used for device identification.

When read, it returns the value 1Xh.

5.0 Device Specifications

5.1 Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +7.0V
Input Voltage (V_I)	−0.5V to V_{DD} + 0.5V
Output Voltage (V_O)	−0.5V to V_{DD} + 0.5V
Storage Temperature (T_{STG})	−65˚C to +165˚C
Power Dissipation (P_D)	1W
Lead Temperature (T_L)	
(Soldering, 10 seconds)	+260˚C
ESD Tolerance (Note 5)	1500V min.
C_{ZAP}	100 pF
R_{ZAP}	1.5 kΩ

Note 4: Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.

Note 5: Value Based on test complying with NSC SOP5-028 human body model ESD testing using the ETS-910 tester.

Note 6: Unless otherwise specified, all voltages are referenced to ground.

5.2 Capacitance

T_A = 0˚C to 70˚C, V_{DD} = 5V ±10% or 3.3V ±10%, V_{SS} = 0V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{IN}	Input Pin Capacitance			5	7	pF
C_{ICLK}	Clock Input Capacitance			8	10	pF
C_{IO}	I/O Pin Capacitance	f = 1 MHz		10	12	pF
C_O	Output Pin Capacitance	f = 1 MHz		6	8	pF

5.3 Electrical Characteristics

T_A = 0˚C to +70˚C, V_{DD} = 5V ±10% or 3.3V ±10%, V_{SS} = 0V

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
I_{CC}	V_{DD} Average Supply Current	V_{DD} = 5V, V_{IL} = 0.5V, V_{IH} = 2.4V, No Load			20	50	mA
		V_{DD} = 3.3V, V_{IL} = 0.5V, V_{IH} = 2.4V, No Load			12	35	mA
I_{CCSB}	V_{DD} Quiescent Supply Current in Low Power Mode	V_{DD} = 5V, V_{IL} = 0.5V, V_{IH} = 2.4V, No Load			20		µA
		V_{DD} = 3.3V, V_{IL} = 0.5V, V_{IH} = 2.4V, No Load			10		µA
V_{IH}	Input High Voltage			2.0		V_{DD}	V
V_{IL}	Input Low Voltage			−0.5		0.8	V
BUS INTERFACE SIGNALS							
V_{OH}	Output High Voltage	V_{DD} = 5V, I_{OH} = −15 mA	V_{DD} = 3.3V, I_{OH} = −7.5 mA	2.4			V
V_{OL}	Output Low Voltage	V_{DD} = 5V, I_{OL} = 24 mA	V_{DD} = 3.3V, I_{OL} = 12 mA			0.4	V
I_{IL}	Input Load Current	V_{IN} = V_{SS}				−10	µA
		V_{IN} = V_{DD}				10	µA
I_{OZ}	Output TRI-STATE Leakage Current	V_{IN} = V_{SS}				−10	µA
		V_{IN} = V_{DD}				10	µA
UART INTERFACE SIGNALS							
V_{OH}	Output High Voltage	V_{DD} = 5V, I_{OH} = −6 mA	V_{DD} = 3.3V, I_{OH} = −3 mA	2.4			V
V_{OL}	Output Low Voltage	V_{DD} = 5V, I_{OL} = 12 mA	V_{DD} = 3.3V, I_{OL} = 6 mA			0.4	V
I_{IL}	Input Load Current	V_{IN} = V_{SS}				−10	µA
		V_{IN} = V_{DD}				10	µA

5.3 Electrical Characteristics (Continued)

T_A = 0˚C to +70˚C, V_{DD} = 5V ±10% or 3.3V ±10%, V_{SS} = 0V

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
INFRARED INTERFACE SIGNALS							
V_{OH}	Output High Voltage	V_{DD} = 5V I_{OH} = −6 mA	V_{DD} = 3.3V I_{OH} = −3 mA	2.4			V
V_{OL}	Output Low Voltage	V_{DD} = 5V I_{OL} = 12 mA	V_{DD} = 3.3V I_{OL} = 6 mA			0.4	V
I_{IL}	Input Load Current	V_{IN} = V_{SS}				−10	µA
		V_{IN} = V_{DD}				10	µA
MISCELLANEOUS SIGNALS (Note 7)							
V_{OL}	Output Low Voltage	I_{OL} = 2 mA				0.4	V
I_{ICLK}	CLK Input Load Current	V_{IN} = V_{SS}				−400	µA
		V_{IN} = V_{DD}				400	µA
I_{IBAD}	BADDR[1–0] Input Load Current during Reset	V_{IN} = V_{SS}				−10	µA
		V_{IN} = V_{DD}				100	µA
I_{IGP}	GPIO Input Load Current	V_{IN} = V_{SS}				−500	µA
		V_{IN} = V_{DD}				15	µA

Note 7: GPIO pins have open drain outputs and internal pull-up resistors between 10 kΩ and 26 kΩ.

5.4 Switching Characteristics

All the timing specifications given in this section refer to 0.8V and 2.0V on all the signals as illustrated in *Figure 40*, unless specifically stated otherwise.

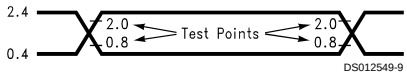


FIGURE 40. Testing Specification Standard

5.4.1 Timing Table

T_A = 0˚C to 70˚C, V_{DD} = 5V ±10% or 3.3V ±10%, V_{SS} = 0V

Symbol	*Figure*	Parameter		Min	Max	Units
CLOCK TIMING						
t_{CH}	*Figure 41*	Clock High Pulse Width		8		ns
t_{CL}	*Figure 41*	Clock Low Pulse Width		8		ns
C_{FREQ}		Clock Frequency		48 − 100 ppm	48 + 100 ppm	MHz
CPU ACCESS TIMING						
t_{AR}	*Figure 42*	Address Valid to Read Active		15		ns
t_{AW}	*Figure 43*	Address Valid to Write Active		5		ns
t_{ACS}	*Figure 42*, *Figure 43*, *Figure 44*	AEN/$\overline{CS}$ Signal Setup	Internal 16-Bit Address Decode	15		ns
			Chip Select Generated Externally	5		ns
t_{ACH}	*Figure 42*, *Figure 43*, *Figure 44*	AEN/$\overline{CS}$ Signal Hold	Internal 16-Bit Address Decode	5		ns
			Chip Select Generated Externally	1		ns
t_{DH}	*Figure 43*	Data Hold		2		ns
t_{DS}	*Figure 43*	Data Setup		18		ns
t_{HZ}	*Figure 42*	Data Bus Floating from Read Inactive			25	ns
t_{RA}	*Figure 42*	Address Hold from Read Inactive		1		ns

5.4.1 Timing Table (Continued)

T_A = 0˚C to 70˚C, V_{DD} = 5V ±10% or 3.3V ±10%, V_{SS} = 0V

Symbol	*Figure*	Parameter		Min	Max	Units
CPU ACCESS TIMING						
t_{RRV}	*Figure 42*	Read Cycle Recovery		45		ns
t_{RD}	*Figure 42*	Read Strobe Width		60	1000	ns
t_{RDH}	*Figure 42*	Read Data Hold		10		ns
t_{RDV}	*Figure 42*	Data Valid from Read Active			55	ns
t_{WA}	*Figure 43*	Address Hold from Write Inactive		1		ns
t_{WRV}	*Figure 43*	Write Cycle Recovery		45		ns
t_{WR}	*Figure 43*	Write Strobe Width		60	1000	ns
t_{RI}	*Figure 42*	IRQn Reset Delay from Read Inactive			60	ns
t_{WI}	*Figure 43*	IRQn Reset Delay from Write Inactive			60	ns
RC	*Figure 42*	Read Cycle Time (RC > t_{AR} + t_{RD} + t_{RRV})		123		ns
WR	*Figure 43*	Write Cycle Time (WR > t_{AW} + t_{WR} + t_{WRV})		123		ns
DMA ACCESS TIMING						
t_{DSW}	*Figure 44*	Read or Write Signal Width		60	1000	ns
t_{DSQ}	*Figure 44*	DRQ Inactive from Read or Write Active			60	ns
t_{DKS}	*Figure 44*	$\overline{DACK}$ Signal Setup		15		ns
t_{DKH}	*Figure 44*	$\overline{DACK}$ Signal Hold		0		ns
t_{TCS}	*Figure 44*	TC Signal Setup		60		ns
t_{TCH}	*Figure 44*	TC Signal Hold from Read or Write Inactive		2		ns
UART AND INFRARED INTERFACE TIMING						
t_{CMW}	*Figure 45*	Modulation Signal Pulse Width in Sharp-IR and Consumer-IR	Transmitter	t_{CWN} − 25 ns (Note 8)	t_{CWN} + 25 ns	
			Receiver	500		ns
t_{CMP}	*Figure 45*	Modulation Signal Period in Sharp-IR and Consumer-IR	Transmitter	t_{CPN} − 25 ns (Note 9)	t_{CPN} + 25 ns	
			Receiver	t_{MMIN} (Note 10)	t_{MMAX}	
t_{BT}	*Figure 45*	Single Bit Time in UART and Sharp-IR	Transmitter	t_{BTN} − 25 ns (Note 11)	t_{BTN} + 25 ns	
			Receiver	t_{BTN} − 2%	t_{BTN} + 2%	
S_{DRT}		SIR Data Rate Tolerance. Percent of Nominal Data Rate	Transmitter		±0.87%	
			Receiver		±2.0%	
t_{SJT}		SIR Leading Edge Jitter. Percent of Nominal Bit Duration	Transmitter		±2.5%	
			Receiver		±6.0%	
t_{SPW}	*Figure 46*	SIR Pulse Width	Transmitter, Variable	(3/16) x t_{BTN} − 15 ns (Note 11)	−(3/16) x t_{BTN} − 15 ns	
			Transmitter, Fixed	1.48	1.78	µs
			Receiver	1 µs	(1/2) x t_{BTN}	
M_{DRT}		MIR Data Rate Tolerance. Percent of Nominal Data Rate	Transmitter		±0.1%	
			Receiver		±0.15%	
t_{MJT}		MIR Leading Edge Jitter. Percent of Nominal Bit Duration	Transmitter		±2.9%	
			Receiver		±6.0%	
t_{MPW}	*Figure 46*	MIR Pulse Width	Transmitter	t_{MWN} − 15 ns (Note 12)	t_{MWN} + 15 ns	
			Receiver	60 ns	(1/2) x t_{BTN} (Note 11)	

5.4.1 Timing Table (Continued)

T_A = 0˚C to 70˚C, V_{DD} = 5V ±10% or 3.3V ±10%, V_{SS} = 0V

Symbol	*Figure*	Parameter		Min	Max	Units
UART AND INFRARED INTERFACE TIMING						
F_{DRT}		FIR Data Rate Tolerance. Percent of Nominal Data Rate	Transmitter		±0.01%	
			Receiver		±0.01%	
t_{FJT}		FIR Leading Edge Jitter. Percent of Nominal Chip Duration	Transmitter		±4.0%	
			Receiver		±25.0%	
t_{FPW}	*Figure 46*	FIR Single Pulse Width (Note 13)	Transmitter	115	135	ns
			Receiver Leading Edge Jitter = 0 ns	80	175	ns
			Receiver Leading Edge Jitter = ± 25 ns	90	150	ns
t_{DPW}	*Figure 46*	FIR Double Pulse Width (Note 13)	Transmitter	115	135	ns
			Receiver Leading Edge Jitter = 0 ns	205	300	ns
			Receiver Leading Edge Jitter = ± 25 ns	215	310	ns
MISCELLANEOUS TIMING						
t_{WOD}	*Figure 47*	IRSLn, GPIOn, $\overline{RTS}$ and $\overline{DTR}$ Delay from Write Inactive			60	ns
t_{MRW}	*Figure 48*	Master Reset Pulse Width		1000		ns
t_{MRF}	*Figure 48*	Output Signals Floating from Reset Active			700	ns

Note 8: t_{CWN} is the nominal pulse width of the modulation signal for Sharp-IR and Consumer-IR modes. It is determined by the MCPW [2–0] and TXHSC bits in the IRTXMC and RCCFG registers.

Note 9: t_{CPN} is the nominal period of the modulation signal for Sharp-IR and Consumer-IR modes. It is determined by the MCFR [4–0] and TXHSC bits in the IRTXMC and RCCFG registers.

Note 10: t_{MMIN} and t_{MMAX} define the time range within which the period of the incoming subcarrier signal has to fall in order for the signal to be accepted by the receiver. These time values are determined by the content of register IRRXDC and the setting of bit RXHSC in the RCCFG register.

Note 11: t_{BTN} is the nominal bit time in UART, Sharp-IR, SIR, MIR and CEIR modes.

Note 12: t_{MWN} is the nominal pulse width for MIR mode. It is determined by the MPW [3–0] and MDRS bits in the MIR__PW and IRCR2 registers.

Note 13: The receiver pulse width requirements for various jitter values can be obtained by assuming a linear pulse-width/jitter relationship. For example, if the jitter is ± 10 ns, the width of a single pulse must fall between 84 and 165 ns.

5.4.2 Timing Diagrams

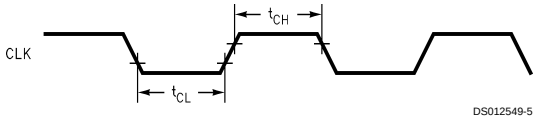


FIGURE 41. Clock Timing

5.4.2 Timing Diagrams (Continued)

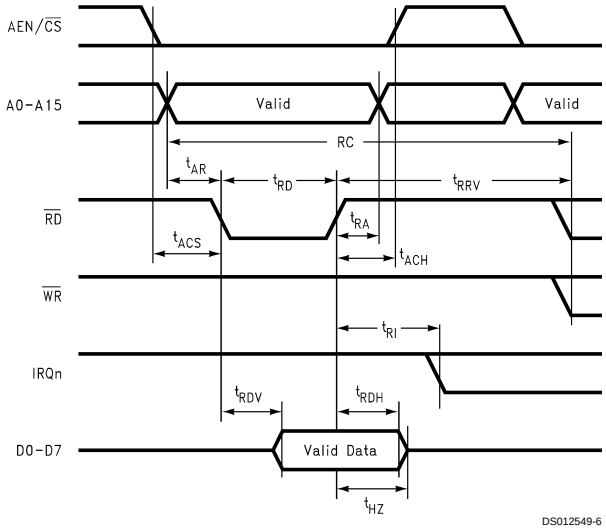


FIGURE 42. CPU Read Timing

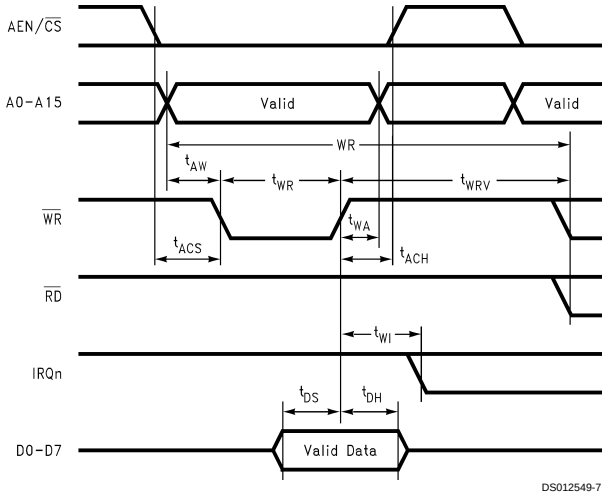


FIGURE 43. CPU Write Timing

5.4.2 Timing Diagrams (Continued)

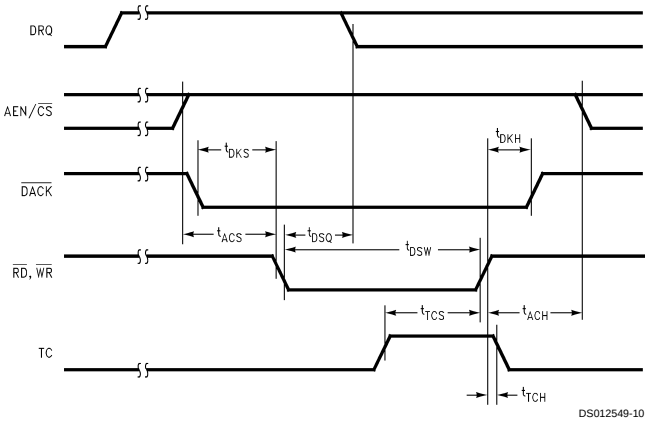
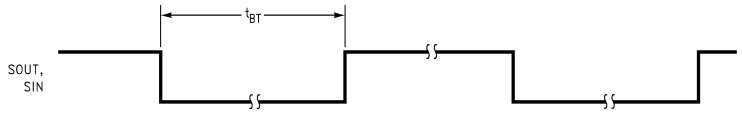


FIGURE 44. DMA Access Timing



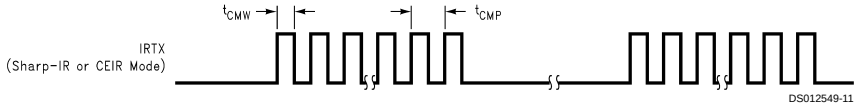
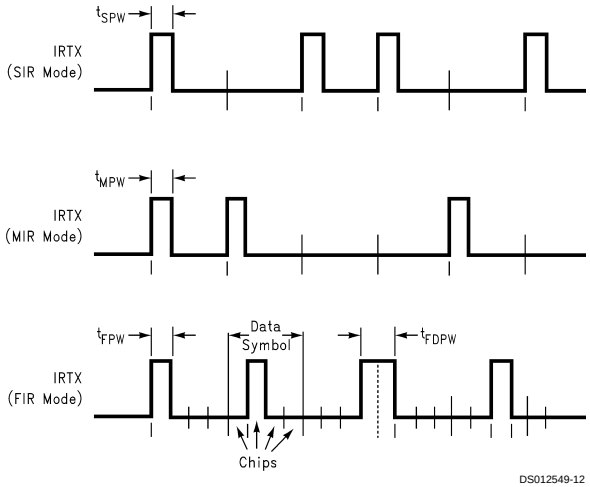


FIGURE 45. UART, Sharp-IR and Consumer-IR Timing



Note: The infrared signals at the IRRXn inputs have opposite polarity.
The signals shown here represent the infrared signals at the IRTX output.

FIGURE 46. SIR, MIR and FIR Timing

5.4.2 Timing Diagrams (Continued)

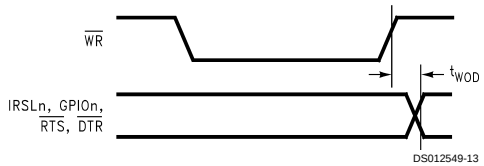


FIGURE 47. GPIOn and IRSLn Write Timing

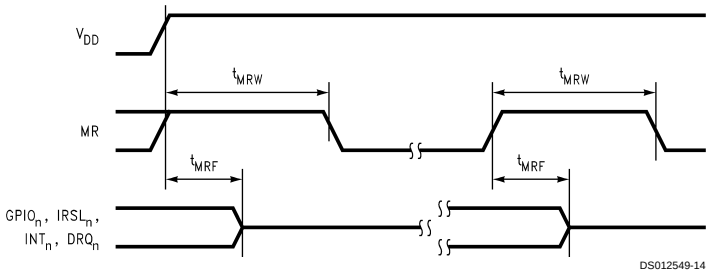
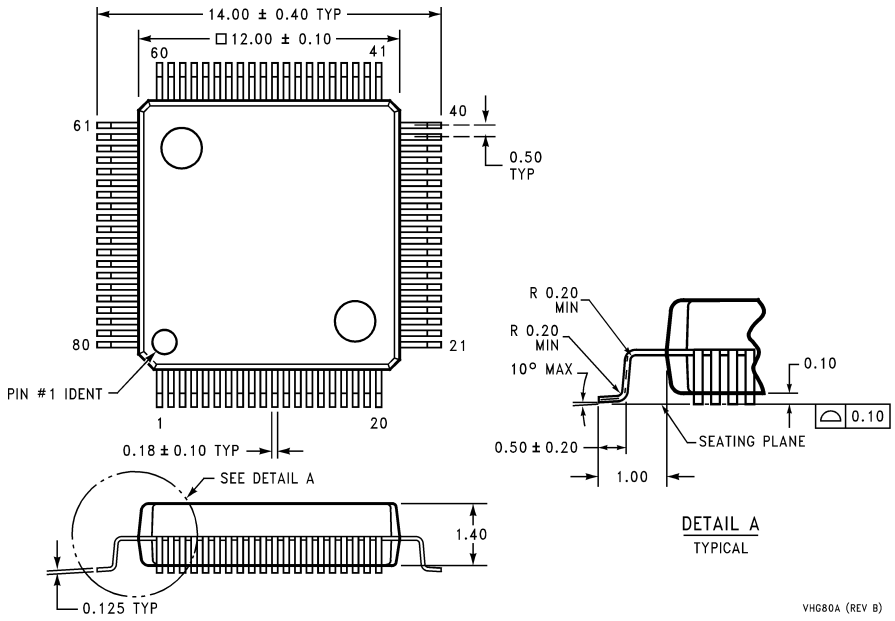


FIGURE 48. Reset Timing

Physical Dimensions inches (millimeters) unless otherwise noted



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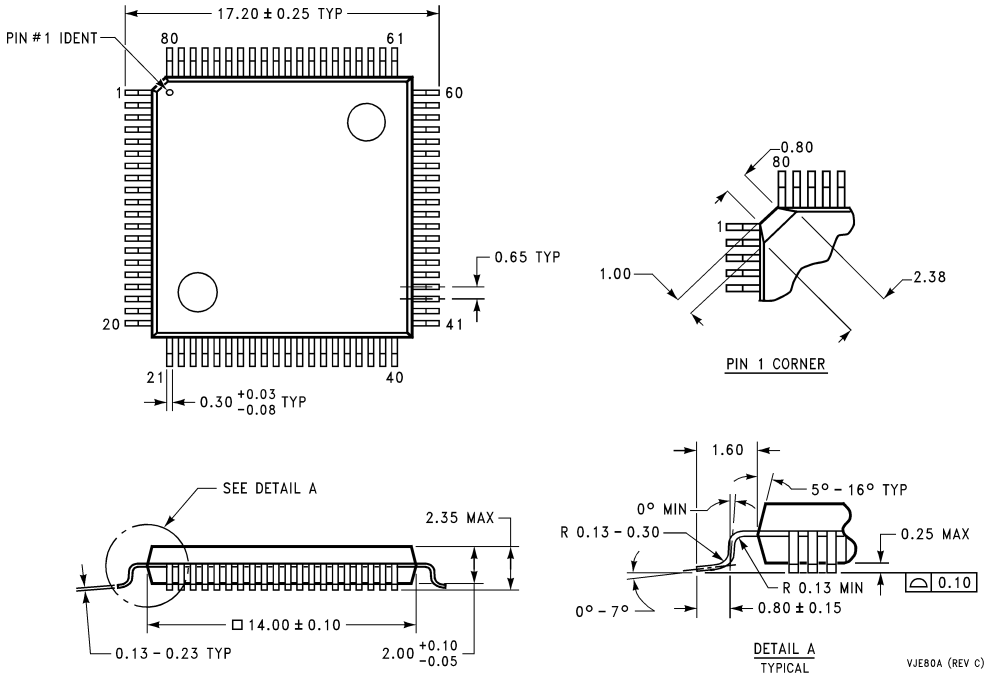
NS Package Number VHG80A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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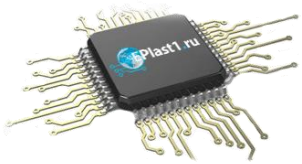

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