# CPC7582
## Line Card Access Switch

### Features
- Small 16 pin surface mount SOIC package
- Monolithic IC reliability
- Low matched $RDS_{ON}$
- Eliminates the need for zero cross switching
- Flexible switch timing to transition from ringing mode to idle/talk mode.
- Clean, bounce free switching
- Tertiary protection consisting of integrated current limiting, thermal shutdown and SLIC protection
- 5V operation with power consumption <10mW
- Intelligent battery monitor
- Latched logic level inputs, no drive circuitry
- Pin to pin compatible to the Lucent 7582 family

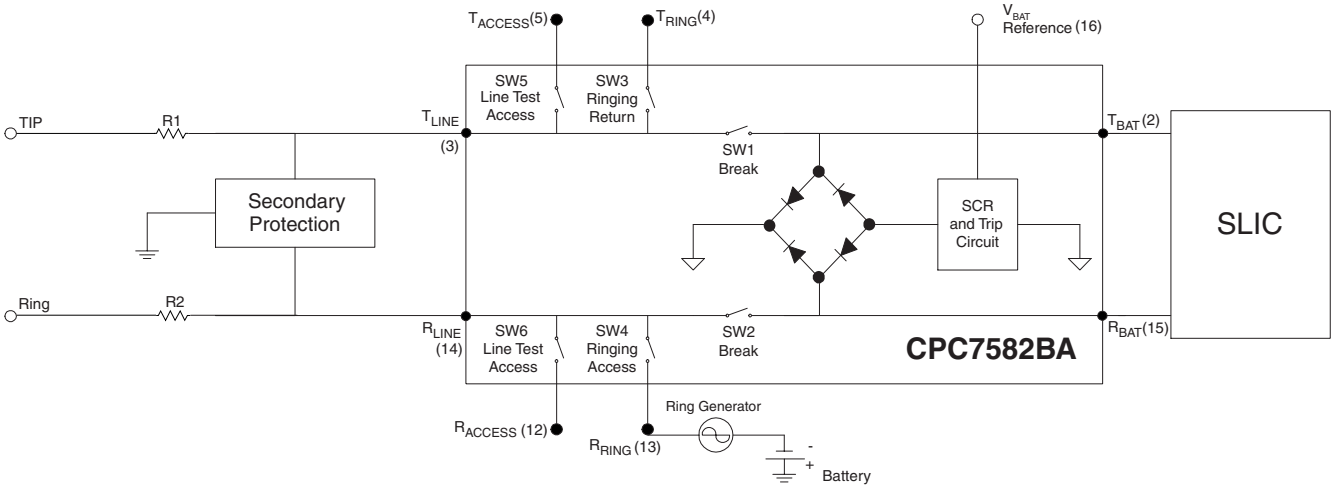
### Applications
- Central office (CO)
- Digital Loop Carrier (DLC)
- PBX Systems
- Digitally Added Main Line (DAML)
- Hybrid Fiber Coax (HFC)
- Fiber in the Loop (FITL)
- Pair Gain System
- Channel Banks

### Description
The CPC7582 is a monolithic solid state switch in a 16 pin surface mount SOIC package. It provides the necessary functions to replace two 2-Form-C electromechanical relays on analog line cards found in Central Office, Access and PBX equipment. The device contains solid state switches for tip and ring line break, ring injection/ring return and line test access. The CPC7582 requires only a +5V supply and offers “break-before-make” or “make-before-break” switch operation using simple logic level input control. There are two versions of the CPC7582, the CPC7582BA and the CPC7582BB. The “BA” version has a protection SCR which provides protection to the SLIC device and subsequent circuitry during fault conditions.

### Ordering Information

| Part # | Description |
|---|---|
| CPC7582BA | 6 Pole with protection SCR |
| CPC7582BB | 6 Pole without protection SCR |
| CPC7582BA-TR | Tape & Reel Version |
| CPC7582BB-TR | Tape & Reel Version |

### Block Diagram



## Absolute Maximum Ratings (@ 25˚ C)

| Parameter | Min | Max | Units |
|---|---|---|---|
| Operating Temperature Range | -40 | +110 | ˚C |
| Storage Temperature Range | -40 | +150 | ˚C |
| Relative Humidity Range | 5 | 95 | % |
| Pin Soldering Temperature (t=10 s max) | - | +260 | ˚C |
| +5V Power Supply | - | 7 | V |
| Battery Supply | - | -85 | V |
| Logic Input Voltage | - | 7 | V |
| Logic Input to Switch Output Isolation | - | 330 | V |
| Switch Isolation (SW1, SW2, SW3, SW5, SW6) | - | 330 | V |
| Switch Isolation (SW4) | - | 480 | V |

*Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure of the device to the absolute maximum ratings for an extended period may degrade the device and effect its reliability.*

## Electrical Characteristics TA = -40ºC to +85ºC

(unless otherwise specified)

Minimum and maximum values are production testing requirements. Typical values are characteristic of the device and are the result of engineering evaluations. Typical values are provided for information purposes only and are not part of the testing requirements.

## Power Supply Specifications

| Supply | Min | Typ | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ | +4.5 | +5.0 | +5.5 | V |
| $V_{BAT}$ [1] | -19 | - | -72 | V |

[1] $V_{BAT}$ is used only as a reference for internal protection circuitry.
If $V_{BAT}$ rises above -10V, the device will enter an all off state and will remain in the all off state until the battery voltage drops below -15V.

| ESD Rating (HBM) |
|---|
| 1000V |

## Table 1. Break Switch, SW1 and SW2

| Parameters | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Off-state Leakage Current: | | | | | | |
| +25˚C | Vsw (differential)= -320V to Gnd<br>Vsw (differential)= -60V to +260V | Isw | - | 0.1 | 1 | µA |
| +85˚C | Vsw (differential)= -330V to Gnd<br>Vsw (differential)= -60V to +270V | Isw | - | 0.3 | 1 | µA |
| -40˚C | Vsw (differential)= -310V to Gnd<br>Vsw (differential)= -60V to +250V | Isw | - | 0.1 | 1 | µA |
| $RDS_{ON}$ (SW1,SW2): | | | | | | |
| +25˚C | $T_{LINE}$= +/-10 mA, +/-40mA, $T_{BAT}$= -2V | Δ V | - | 14.5 | - | Ω |
| +85˚C | $T_{LINE}$= +/-10 mA, +/-40mA, $T_{BAT}$= -2V | Δ V | - | 20.5 | 28 | Ω |
| -40˚C | $T_{LINE}$= +/-10 mA, +/-40mA, $T_{BAT}$= -2V | Δ V | - | 10.5 | - | Ω |
| $RDS_{ON}$ Match | Per ON-resistance Test Condition of SW1, SW2$R_{ON}$ SW1-$R_{ON}$SW2 | Magnitude | - | 0.15 | 0.8 | Ω |
| dc Current Limit: | | | | | | |
| +25˚C | $V_{SW}$ (on) = +/- 10V | Isw | - | 300 | - | mA |
| +85˚C | $V_{SW}$ (on) = +/- 10V | Isw | 80 | 160 | - | mA |
| -40˚C | $V_{SW}$ (on) = +/- 10V | Isw | - | 400 | 425 | mA |
| Dynamic Current Limit: (t=<0.5µs) | Break switches in ON state, Ringing access switches OFF, Apply +/- 1000V at 10/1000ms pulse, Appropriate secondary protection in place. | Isw | - | 2.5 | - | A |

### Table 1. Break Switch, SW1 and SW2 (Continued)

| Parameters | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Logic Input to Switch Output Isolation: | | | | | | |
| +25˚C | Vsw ($T_{LINE}$, $R_{LINE}$) = +/-320V<br>Logic Inputs = Gnd | Isw | - | 0.1 | 1 | µA |
| +85˚C | Vsw ($T_{LINE}$, $R_{LINE}$) = +/-330V<br>Logic Inputs = Gnd | Isw | - | 0.3 | 1 | µA |
| -40˚C | Vsw ($T_{LINE}$, $R_{LINE}$) = +/-310V<br>Logic Inputs = Gnd | Isw | - | 0.1 | 1 | µA |
| dv/dt Sensitivity[1] | - | - | - | 200 | - | V/µs |

[1] Applied voltage is 100 Vp-p square wave at 100Hz.

### Table 2. Ring Return Switch, SW3

| Parameters | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Off-state Leakage Current | | | | | | |
| +25˚C | Vsw (differential)= -320V to Gnd<br>Vsw (differential)= -60V to +260V | Isw | - | 0.1 | 1 | µA |
| +85˚C | Vsw (differential)= -330V to Gnd<br>Vsw (differential)= -60V to +270V | Isw | - | 0.3 | 1 | µA |
| -40˚C | Vsw (differential)= -310V to Gnd<br>Vsw (differential)= -60V to +250V | Isw | - | 0.1 | 1 | µA |
| dc Current Limit: | | | | | | |
| +25˚C | Vsw (on) = +/- 10V | Isw | - | 135 | - | mA |
| +85˚C | Vsw (on) = +/- 10V | Isw | - | 85 | - | mA |
| -40˚C | Vsw (on) = +/- 10V | Isw | - | 210 | - | mA |
| Dynamic Current Limit:<br>(t=<0.5ms) | Break switches in ON state, Ringing access switches OFF, Apply +/- 1000V at 10/1000ms pulse, Appropriate secondary protection in place. | Isw | - | 2.5 | - | A |
| $RDS_{ON}$ | | | | | | |
| +25˚C | Isw (on) = +/-0mA, +/-10mA | Δ V | - | 60 | - | Ω |
| +85˚C | Isw (on) = +/-0mA, +/-10mA | Δ V | - | 85 | 100 | Ω |
| -40˚C | Isw (on) = +/-0mA, +/-10mA | Δ V | - | 45 | - | Ω |
| Logic Input to Switch Output Isolation | | | | | | |
| +25˚C | Vsw ($T_{RING}$, $T_{LINE}$) = +/-320V<br>Logic Inputs = Gnd | Isw | - | 0.1 | 1 | µA |
| +85˚C | Vsw ($T_{RING}$, $T_{LINE}$) = +/-330V<br>Logic Inputs = Gnd | Isw | - | 0.3 | 1 | µA |
| -40˚C | Vsw ($T_{RING}$, $T_{LINE}$) = +/-310V<br>Logic Inputs = Gnd | Isw | - | 0.1 | 1 | µA |

### Table 3. Ringing Access Switch, SW4

| Parameters | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Off-state Leakage Current | | | | | | |
| +25˚C | Vsw (differential)= -255V to +210V<br>Vsw (differential)= +255V to -210V | Isw | - | 0.05 | 1 | µA |
| +85˚C | Vsw (differential)= -270V to +210V<br>Vsw (differential)= +270V to -210V | Isw | - | 0.1 | 1 | µA |
| -40˚C | Vsw (differential)= -245V to +210V<br>Vsw (differential)= +245V to -210V | Isw | - | .05 | 1 | µA |
| ON Voltage | Isw (on) = +/- 1mA | - | - | 1.5 | 3 | V |
| Ring Generator Current During Ring | Vcc = 5V, INaccess = 0 | $I_R$ | - | 0.1 | 0.25 | mA |
| Surge Current | - | - | - | - | 2 | A |
| Release Current | - | - | - | 300 | - | µA |
| $RDS_{ON}$ | Isw (on) = +/-70mA, +/-80mA | Δ V | - | 8.5 | 12 | Ω |
| Logic Input to Switch Output Isolation: | | | | | | |
| +25˚C | Vsw ($R_{RING}$, $R_{LINE}$) = +/-320V<br>Logic Inputs = Gnd | Isw | - | .05 | 1 | µA |
| +85˚C | Vsw ($R_{RING}$, $R_{LINE}$) = +/-330V<br>Logic Inputs = Gnd | Isw | - | 0.1 | 1 | µA |
| -40˚C | Vsw ($R_{RING}$, $R_{LINE}$) = +/-310V<br>Logic Inputs = Gnd | Isw | - | .05 | 1 | µA |

### Table 4. Loop Access Switches, SW5 and SW6

| Parameters | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Off-state Leakage Current | | | | | | |
| +25˚C | Vsw (differential)= -320V to Gnd<br>Vsw (differential)= -60V to +260V | Isw | - | 0.1 | 1 | µA |
| +85˚C | Vsw (differential)= -330V to Gnd<br>Vsw (differential)= -60V to +270V | Isw | - | 0.3 | 1 | µA |
| -40˚C | Vsw (differential)= -310 to Gnd<br>Vsw (differential)= -60V to +250V | Isw | - | 0.1 | 1 | µA |
| DC Current Limit: | | | | | | |
| +25˚C | Vsw (on) = +/- 10V | Isw | - | 175 | - | mA |
| +85˚C | Vsw (on) = +/- 10V | Isw | 80 | 110 | - | mA |
| -40˚C | Vsw (on) = +/- 10V | Isw | - | 210 | 250 | mA |
| Dynamic Current Limit: (t=<0.5µs) | Break switches in ON state, Ringing access switches OFF, Apply +/- 1000V at 10/1000ms pulse, Appropriate secondary protection in place. | Isw | - | 2.5 | - | A |
| $RDS_{ON}$: | | | | | | |
| +25˚C | Isw (on) = +/-10 mA, +/-40mA | Δ V | - | 38 | - | Ω |
| +85˚C | Isw (on) = +/-10 mA, +/-40mA | Δ V | - | 46 | 70 | Ω |
| -40˚C | Isw (on) = +/-10 mA, +/-40mA | Δ V | - | 28 | - | Ω |
| Logic Input to Switch Output Isolation: | | | | | | |
| +25˚C | Vsw ($T_{ACCESS}$, $T_{LINE}$) = +/-320V<br>Logic Inputs = Gnd | Isw | - | 0.1 | 1 | µA |
| +85˚C | Vsw ($T_{ACCESS}$, $T_{LINE}$) = +/-330V<br>Logic Inputs = Gnd | Isw | - | 0.3 | 1 | µA |
| -40˚C | Vsw ($T_{ACCESS}$, $T_{LINE}$) = +/-310V<br>Logic Inputs = Gnd | Isw | - | 0.1 | 1 | µA |

## Table 5. Additional Electrical Characteristics

| Parameters | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Digital Input Characteristics** | | | | | | |
| Input Low Voltage | - | - | - | - | 1.5 | V |
| Input High Voltage | - | - | 3.5 | - | - | V |
| Input Leakage Current (High) | $V_{DD}$ = 5.5V, $V_{BAT}$ = -75V, $V_{log}$ = 5V | $I_{log}$ | - | 0.1 | 1 | µA |
| Input Leakage Current (Low) | $V_{DD}$ = 5.5V, $V_{BAT}$ = -75V, $V_{log}$ = 0V | $I_{log}$ | - | 0.1 | 1 | µA |
| **Power Requirements** | | | | | | |
| Power Dissipation | $V_{DD}$ = 5V, $V_{BAT}$ = -48V, | | | | | |
| | Idle/Talk State or All Off State | $I_{DD}$, $I_{BAT}$ | - | 5.5 | 7.5 | mW |
| | Ringing State or Access State | $I_{DD}$ | - | 6.5 | 10 | mW |
| $V_{DD}$ Current | $V_{DD}$ = 5V, | | | | | |
| | Idle/Talk State or All Off State | $I_{DD}$ | - | 1.1 | 1.5 | mA |
| | Ringing State or Access State | $I_{DD}$ | - | 1.3 | 1.9 | mA |
| $V_{BAT}$ Current | $V_{BAT}$ = -48V, | | | | | |
| | Idle/Talk State or All Off State | $I_{BAT}$ | - | 0.1 | 10 | µA |
| | Ringing State or Access State | $I_{BAT}$ | - | 0.1 | 10 | µA |
| **Temperature Shutdown Requirements**[1] | | | | | | |
| Shutdown Activation Temperature | - | - | 110 | 125 | 150 | ˚C |
| Shutdown Circuit Hysteresis | - | - | 10 | - | 25 | ˚C |

[1] Temperature shutdown flag (TSD) will be high during normal operation and low during temperature shutdown state.

## Table 6. Make-Before-Break Operation (Ringing to Idle/Talk Transition)

| Access | Input | TSD | State | Timing | Break Switches 1 & 2 | Ring Return Switch 3 | Ring Access Switch 4 | Line Access Switches 5 & 6 |
|---|---|---|---|---|---|---|---|---|
| 0V | 5V | Float | Ringing | - | Open | Closed | Closed | Open |
| 0V | 0V | Float | Make-before-break | SW4 waiting for next zero current crossing to turn off. Maximum time is one half of ringing. In this transition state, current that is limited to the dc break switch current limit value will be sourced from the ring node of the SLIC | Closed | Open | Closed | Open |
| 0V | 0V | Float | Idle / Talk | Zero cross current has occurred | Closed | Open | Open | Open |

### Table 7. Break-Before-Make Operation (Ringing to Idle/Talk Transition)

| Access | Input | TSD | State | Timing | Break Switches 1 & 2 | Return Switch 3 | Ring Access Switch 4 | Ring Line Access Switches 5 & 6 |
|---|---|---|---|---|---|---|---|---|
| 0V | 5V | Float | Ringing | - | Open | Closed | Closed | Open |
| 5V | 5V | Float | All Off | Hold this state for <= 25ms. SW4 waiting for zero current to turn off. | Open | Open | Closed | Open |
| 5V | 5V | Float | All Off SW4 has opened. | Zero current has occurred. | Open | Open | Open | Open |
| 0V | 0V | Float | Idle/Talk | Release Break Switches | Closed | Open | Open | Open |

### Alternate "Break-Before-Make" Operation

Note that the "break-before-make" operation can also be achieved using TSD as an input. In lines 2 & 3 of Table 7, instead of using the logic input pins to force the "all off" state, force TSD to ground. This will override the logic inputs and also force the all off state. Hold this state for 25 ms. During this 25 ms all off state, toggle the inputs from the ringing state (Input=5V, Access=0V) to the idle/talk state (Input=0V, Access=0V). After 25 ms, release TSD to return switch control to the input pins which will set the idle talk state.

When using the CPC7582 in this mode, forcing TSD to ground will override the INPUT pins and force an all off state. Setting TSD to +5V will allow switch control via the logic INPUT pins. However, setting TSD to +5V will also disable the thermal shutdown mechanism. This is not recommended. Therefore, to allow switch control via the logic INPUT pins, allow TSD to float.

Thus when using TSD as an input, the two recommended states are 0 (overrides logic input pins and forces all off state) and float (allows switch control via logic input pins and thermal shutdown mechanism is active). This may require use of an open collector buffer.

### Table 8. Electrical Specifications, Protection Circuitry

| Parameters | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Parameters Related to Diodes (in Diode Bridge)** | | | | | | |
| Voltage Drop @ Continuous Current (50/60 Hz) | Apply +/-dc current limit of break switches | Forward Voltage | - | 2.1 | 3 | V |
| Voltage Drop @ Surge Current | Apply +/-dynamic current limit of break switches | Forward Voltage | - | 5 | - | V |
| **Parameters Related to Protection SCR[1]** | | | | | | |
| Surge Current | - | - | - | - | * | A |
| Trigger Current (+25˚C) | - | $I_{TRIG}$ | - | 60 | - | mA |
| Hold Current (+25˚C) | - | $I_{HOLD}$ | - | 100 | - | mA |
| Trigger Current (+85˚C) | - | $I_{TRIG}$ | - | 35 | - | mA |
| Hold Current (+85˚C) | | $I_{HOLD}$ | 60 | 70 | - | mA |
| Gate Trigger Voltage | Trigger Current | - | $V_{BAT}$ - 4 | - | $V_{BAT}$ - 2 | V |
| Reverse Leakage Current | $V_{BAT}$ | - | - | - | 1.0 | µA |
| ON State Voltage[1] | 0.5A t = 0.5 ms | $V_{on}$ | - | -3 | - | V |
| | 2.0A t = 0.5 ms | - | - | -5 | - | V |

[1] Only for the CPC7581BA.
* Passes GR1089 & ITU-T K.20 with appropriate secondary protection in place.

## Table 9. Truth Table

| Input | Access | TSD | Tip Break Switch | Ring Break Switch | Ringing Return Switch | Ring Switch | Tip Access Switch | Ring Access Switch |
|---|---|---|---|---|---|---|---|---|
| 0V | 0V | 5V/Float[5] | On | On | Off | Off | Off | Off[1] |
| 5V | 0V | 5V/Float[5] | Off | Off | On | On | Off | Off[2] |
| 0V | 5V | 5V/Float[5] | Off | Off | Off | Off | On | On[3] |
| 5V | 5V | 5V/Float[5] | Off | Off | Off | Off | Off | Off[4] |
| Don't Care | Don't Care | 0V[6] | Off | Off | Off | Off | Off | Off[4] |

[1] Idle/Talk State

[2] Power Ringing State

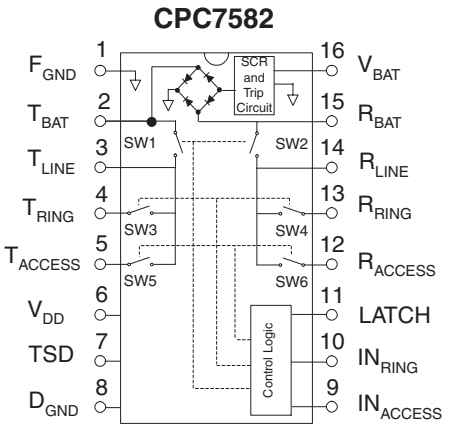
[3] Test out message waiting state.

[4] All OFF State

[5] If TSD = 5V, the thermal shutdown mechanism is disabled.
If TSD if floating, the thermal shutdown mechanism is active.

[6] Forcing TSD to ground overrides the logic input pins and forces an all off state.

## Package Pinout




* Only the CPC7582BA contains the protection SCR.

| Pin | Name | Function |
|---|---|---|
| 1 | $F_{GND}$ | Fault ground |
| 2 | $T_{BAT}$ | Connect to TIP on SLIC side |
| 3 | $T_{LINE}$ | Connect to TIP on line side |
| 4 | $T_{RING}$ | Connect to return ground for ringing generator |
| 5 | $T_{ACCESS}$ | Test access |
| 6 | $V_{DD}$ | +5V supply |
| 7 | TSD | Temperature shutdown pin. Can be used as a logic level input or output. See Tables 6, 7 and 9 for more details. As an output, will read +5V when device is in its operational mode and 0V in the thermal shutdown mode. To disable the thermal shutdown mechanism, tie this pin to +5V (NOT Recommended). |
| 8 | $D_{GND}$ | Digital ground |
| 9 | $IN_{ACCESS}$ | Logic level switch control |
| 10 | $IN_{RING}$ | Logic level input switch control |
| 11 | LATCH | Data latch control, active high, transparent low |
| 12 | $R_{ACCESS}$ | Test access |
| 13 | $R_{RING}$ | Connect to ringing generator |
| 14 | $R_{LINE}$ | Connect to RING on line side |
| 15 | $R_{BAT}$ | Connect to RING on SLIC side |
| 16 | $V_{BAT}$ | Battery voltage. Used as a reference for protection circuit |

## Functional Description

### Introduction

The CPC7582 has four states:

- Idle/talk state (line break switches SW1, and SW2 closed, ringing switches SW3, SW4 open and loop access switches SW5, SW6 open),
- Ringing state (line break switches SW1, and SW2 open, ringing switches SW3, SW4 closed and loop access switches SW5, SW6 open)
- Loop access (line break switches SW1, and SW2 open, ringing switches SW3, SW4 open and loop access switches SW5, SW6 closed)
- All Off state (line break switches SW1, and SW2 open, ringing switches SW3, SW4 open and loop access switches SW5, SW6 open)

The CPC7582 offers break-before-make and make-before-break switching with simple logic level input control. Solid state switch construction means no impulse noise is generated when switching during ring cadence or ring trip, thus eliminating the need for external “zero cross” switching circuitry. State control is via logic level input so no additional driver circuitry is required. The line break switches SW1 and SW2 are linear switches that have exceptionally low $RDS_{ON}$ and excellent matching characteristics. The ringing access switch SW4 has a breakdown voltage rating of >480V which is sufficiently high, with proper protection, to prevent breakdown in the presence of a transient fault condition (i.e., passing the transient on to the ring generator).

Integrated into the CPC7582 is a diode bridge/SCR clamping circuit, current limiting and thermal shutdown mechanism to provide protection to the SLIC device during a fault condition. Positive and negative surges are reduced by the current limiting circuitry and steered to ground via diodes and the integrated SCR. Power cross transients are also reduced by the current limiting and thermal shutdown circuits. Please note that only the CPC7582BA has the integrated protection SCR.

To protect the CPC7582 from an overvoltage fault condition, use of a secondary protector is required. The secondary protector must limit the voltage seen at the tip and ring terminals to a level below the max breakdown voltage of the switches. To minimize the stress on the solid-state contacts, use of a foldback or crowbar type secondary protector is recommended. With proper selection of the secondary protector, a line card using the CPC7582 will meet all relevant ITU, LSSGR, FCC or UL protection requirements.

The CPC7582 operates from a +5V supply only. This gives the device extremely low idle and active power dissipation and allows use with virtually any range of battery voltage. A battery voltage is also used by the CPC7582 as a reference for the integrated protection circuit. In the event of a loss of battery voltage, the CPC7582 will enter an “all off” state.

### Switch Timing

The CPC7582 provides, when switching from the ringing state to the idle/talk state, the ability to control the timing when the ringing access switches SW3 and SW4 are released relative to the state of the line break switches SW1 and SW2 using simple logic level input. This is referred to a “make before break” or “break before make” operation. When the line break switch contacts (SW1, SW2) are closed (or made) before the ringing access switch contact (SW3, SW4) is opened (or broken), this is referred to a ‘make-before-break’ operation. Break-before-make operation occurs when the ringing access contact (SW3, SW4) is opened (broken) before the line break switch contacts (SW1, SW2) are closed (made). With the CPC7582 the “make before break” and “break before make” operations can easily be selected by applying logic level inputs to pins 9 and 10 ($IN_{ring}$ and $IN_{access}$) of the device.

The logic sequences for either mode of operation are given in Tables 6 and 7. Logic states and explanations are given in Table 9.

Break-before make operation can also be achieved using pin 7 (TSD) as an input. In table 7 lines 2 and 3 it is possible to induce the switches to “all off” by grounding pin 7 (TSD) instead of apply logic input to the pins. This has the effect of overriding the logic inputs and forcing the device to the “all off” state. Hold this input state for 25ms. During this hold period, toggle the inputs from the ringing state (10) to the idle/talk state (00). After the 25ms release pin 7 (TSD) to return the switch control to the input pins 9 and 10 and reset the device to the idle/talk state.

Setting TSD to +5V will allow switch control using the logic pins 9 and 10. This setting, however, will also disable the thermal shutdown circuit and is therefore not recommended. When using logic controls via the input pins 9 and 10, pin 7 (TSD) should be allowed to float. As a result the two recommended states when using pin 7 (TSD) as a control are 0 which forces the device to the “all of state” or float which allows logic inputs to pins 9 and 10 to remain active. This may require use of an open collector buffer.

### Ring Access Switch Zero Cross Current Turn Off

After the application of a logic input to turn SW4 off, the ring access switch is designed to delay the change in state until the next zero crossing. Once on, the switch requires a zero current cross to turn off and therefore should not be used to switch a pure DC signal. The switch will remain in the on state no matter what logic input until the next zero crossing. For proper operation, pin 13 ($R_{Ring}$) should be connected using proper impedance to a ring generator or other ac source. These switching characteristics will reduce and possibly eliminate overall system impulse noise normally associated with ringing access switches. The attributes of ringing access switch SW4 may make it possible to eliminate the need for a zero cross switching scheme. A minimum impedence of 300Ω in series with the ring generator is recommended.

### Power Supplies

Both a +5V supply and battery voltage are connected to the CPC7582. CPC7582 switch state control is powered exclusively by the +5V supply. As a result, the CPC7582 exhibits extremely low power dissipation during both active and idle states.

The battery voltage is not used for switch control but rather as a reference by the integrated secondary protection circuitry. The integrated SCR is designed to trigger when pin 2 ($T_{BAT}$) or pin 15 ($R_{BAT}$) drops 2 to 4V below the battery. This trigger prevents a fault induced overvoltage event at the $T_{BAT}$ or $R_{BAT}$ nodes.

### Battery Voltage Monitor

The CPC7582 also uses the voltage reference to monitor battery voltage. If battery voltage is lost, the CPC7582 will immediately enter the “all off” state and remain in this state until the battery voltage is restored. The device will also enter the “all off” state if the battery voltage rises above –10V and will remain there until the battery voltage drops below –15V. This battery monitor feature draws a small current from the battery (<1μA typ.) and will add slightly to the device’s overall power dissipation.

### Protection

#### Diode Bridge/SCR

The CPC7582 uses a combination of current limited break switches, a diode bridge/SCR clamping circuit and a thermal shutdown mechanism to protect the SLIC device or other associated circuitry from damage during line transient events such as lightning. During a positive transient condition, the fault current is conducted through the diode bridge to ground. Voltage is clamped to the diode drop above ground. During a negative transient of 2 - 4 volts more negative than the battery, the SCR conducts and faults are shunted to ground via the SCR and diode bridge.

Also, in order for the SCR to crowbar or foldback, the on voltage (see Table 8) of the SCR must be less negative than the battery reference voltage. If the battery voltage is less negative the SCR on voltage, the SCR will not crowbar, however it will conduct fault currents to ground.

For power induction or power cross fault conditions, the positive cycle of the transient is clamped to the diode drop above ground and the fault current directed to ground. The negative cycle of the transient will cause the SCR to conduct when the voltage exceeds the battery reference voltage by two to four volts, steering the current to ground.

### Current Limiting function

If a lightning strike transient occurs when the device in the talk/idle state, the current is passed along the line to the integrated protection circuitry and limited by the dynamic current limit response of break switches SW1 and SW2. When a 1000V 10x1000 pulse (LSSGR lightning) is applied to the line though a properly clamped external protector, the current seen at pins 2 ($T_{BAT}$) and pin 15 ($R_{BAT}$) will be a pulse with a typical magnitude and duration of 2.5A and < 0.5ms.

If a power cross fault occurs with device in the talk/idle state, the current is passed though the break switches SW1 and SW2 on to the integrated protection circuit and is limited by the dynamic DC current limit response of the two break switches. The DC current limit, specified over temperature, is between 80mA and 425mA and the circuitry has a negative temperature coefficient. As a result, if the device is subjected to extended heating due to power cross fault, the measured current at pin 2 ($T_{BAT}$) and pin 15 ($R_{BAT}$) will decrease as the device temperature increases. If the device temperature rises sufficiently, the temperature shutdown mechanism will activate and the device will default to the “all off” state.

### Temperature Shutdown

The thermal shutdown mechanism will activate when the device temperature reaches a minimum of 110°C placing the device in the “all off” state regardless of logic input. During this thermal shutdown mode, pin 7 (TSD) will read 0V. Normal output of TSD is $+V_{DD}$

If presented with a short duration transient such as a lightning event, the thermal shutdown feature will not typically activate. But in an extended power cross transient, the device temperature will rise and the thermal shutdown will activate forcing the switches to an "all off" state. At this point the current measured at pin 2 ($T_{BAT}$) and pin 15 ($R_{BAT}$) will drop to zero. Once the device enters thermal shutdown it will remain in the "all off" state until the temperature of the device drops below the activation level of the thermal shutdown circuit. This will return the device to the state prior to thermal shutdown. If the transient has not passed, current will flow at the value allowed by the dynamic DC current limiting of the switches and heating will begin again, reactivating the thermal shutdown mechanism. This cycle of entering and exiting the thermal shutdown mode will continue as long as the fault condition persists. If the magnitude of the fault condition is great enough, the external secondary protector could activate and shunt all current to ground.

The thermal shutdown mechanism of the CPC7582 can be disable by applying $+V_{DD}$ to pin 7 (TSD)

## External Protection Elements

The CPC7582 requires only one overvoltage secondary protector on the loop side of the device. The integrated protection feature described above negates the need for protection on the line side. The purpose of the secondary protector is to limit voltage transients to levels that do not exceed the breakdown voltage or input-output isolation barrier of the CPC7582. A foldback or crowbar type protector is recommended to minimize stresses on the device.

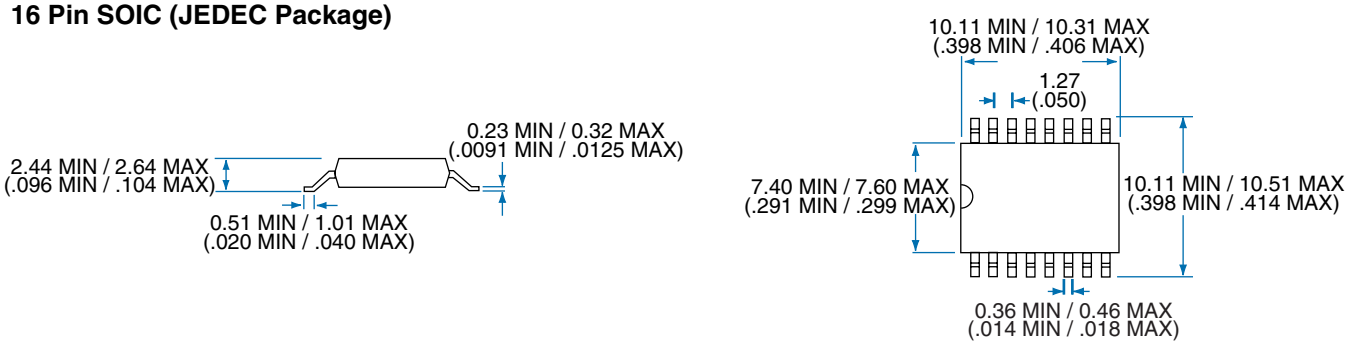
Consult Clare's application note, AN-100, "Designing Surge and Power Fault Protection Circuits for Solid State Subscriber Line Interfaces" for equations related to the specifications of external secondary protectors, fused resistors and PTCs.

## Data Latch

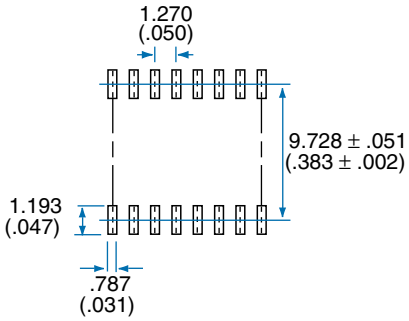
The CPC7582 has an integrated data latch. The latch operation is controlled by logic level input pin 11 (LATCH). The data input of the latch is pin 10 ($IN_{RING}$) and pin 9 ($IN_{ACCESS}$) of the device while the output of the data latch is an internal node used for state control. When LATCH control pin is at logic 0, the data latch is transparent and data control signals flow directly through to state control. A change in input will be reflected in a change is switch state. When LATCH control pin is at logic 1, the data latch is now active and a change in input control will not affect switch state. The switches will remain in the position they were in when the LATCH changed from logic 0 to logic 1 and will not respond to changes in input as long as the latch is at logic 1. In addition, TSD input is not tied to the data latch. Therefore, TSD is not affected by the LATCH input and TSD input will override state control via pin 10 ($IN_{RING}$) and pin 9 ($IN_{ACCESS}$) and the LATCH.

## MECHANICAL DIMENSIONS

### 16 Pin SOIC (JEDEC Package)




### PC Board Pattern
### (Top View)




Dimensions
mm
(Inches)

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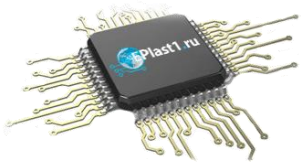
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