ESD7108

ESD Protection Diode

Low Capacitance Array for High Speed Data Lines

The ESD7108 transient voltage suppressor is designed specifically to protect four high speed differential pairs. Ultra−low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines. The flow−through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance for the high speed lines.

Features

- Integrated 4 Pairs (8 Lines) High Speed Data
- Single Connect, Flow through Routing
- Low Capacitance (0.25 pF Max, I/O to GND)
- Protection for the Following IEC Standards: IEC 61000−4−2 Level 4
- UL Flammability Rating of 94 V−0
- This is a Pb−Free Device

Typical Applications

- V−by−One HS
- LVDS

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
IEC 61000−4−2 Contact (ESD) IEC 61000−4−2 Air (ESD)	ESD ESD	±15 ±15	kV kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.

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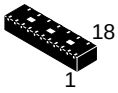
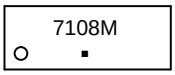


UDFN18
CASE 517BV

MARKING DIAGRAM

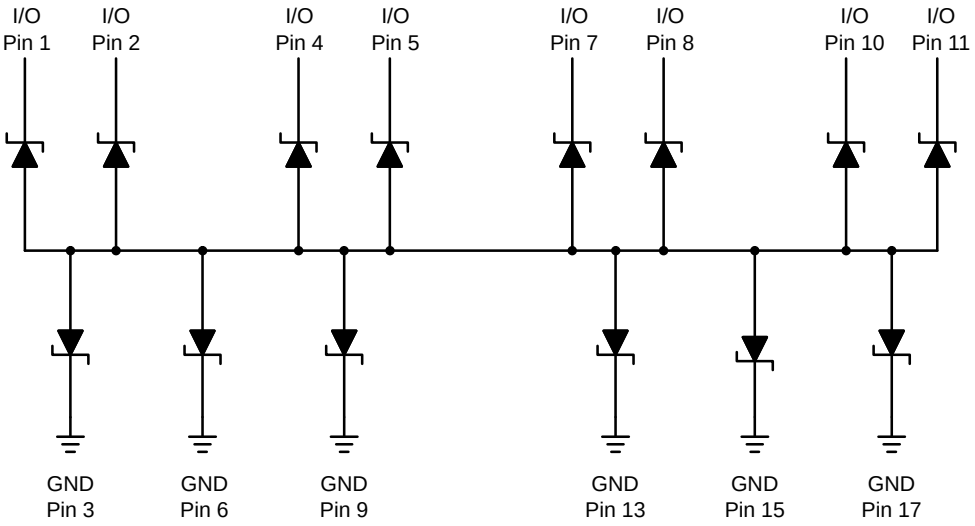


7108 = Specific Device Code
M = Date Code
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
ESD7108MUTAG	UDFN18 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



Note: Only Minimum of 1 GND connection required

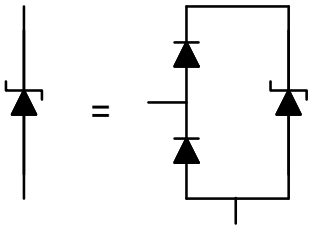


Figure 1. Pin Schematic

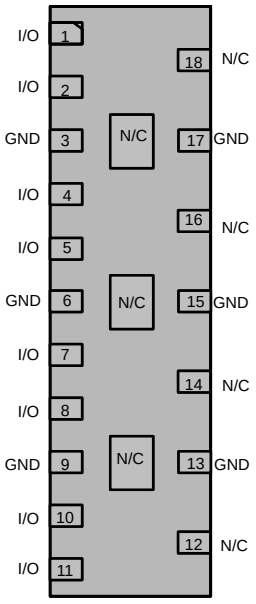


Figure 2. Pin Configuration

Note: Only minimum of one pin needs to be connected to ground for functionality of all pins. All pins labeled “N/C” should have no electrical connection.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			5.0	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	5.5		8.5	V
Reverse Leakage Current	I_R	V_{RWM} = 5 V, I/O Pin to GND			1.0	μA
Clamping Voltage TLP (Note 1)	V_C	I_{PP} = ±8 A I_{PP} = ±16 A		14.5 19.5		
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND			0.25	pF
Junction Capacitance Difference	ΔC_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND		0.02		pF

1. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 3. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 4 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

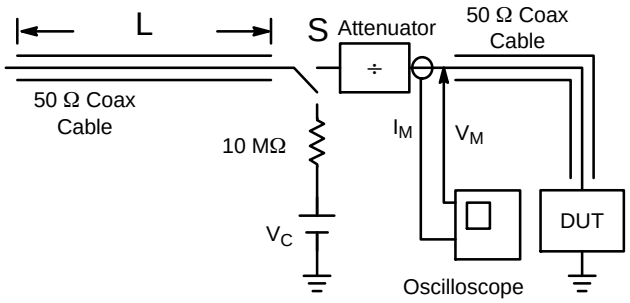


Figure 3. Simplified Schematic of a Typical TLP System

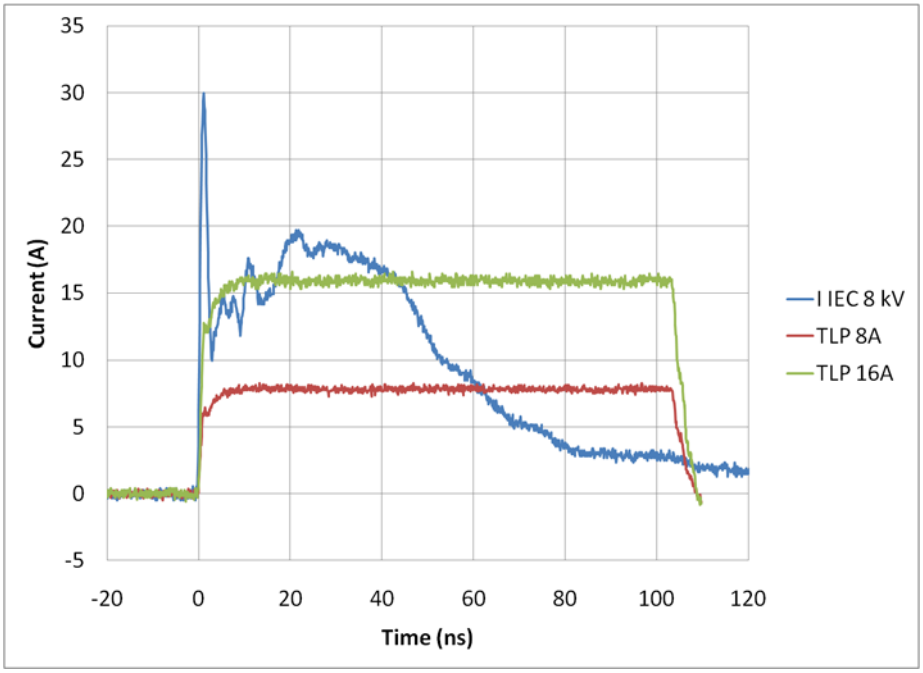


Figure 4. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

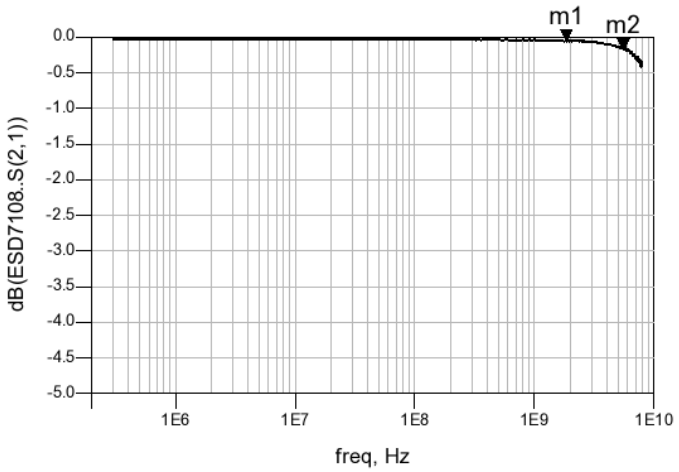


Figure 5. ESD7108 Insertion Loss

Interface	Data Rate (Gbps)	Fundamental Frequency (GHz)	3rd Harmonic Frequency (GHz)	ESD7108 Insertion Loss (−dB)
V−by−One HS Full HD (1920 x 1080p) 240 Hz, 36bit color depth	3.71	1.854 (m1)	5.562 (m2)	M1 = 0.058 M2 = 0.175

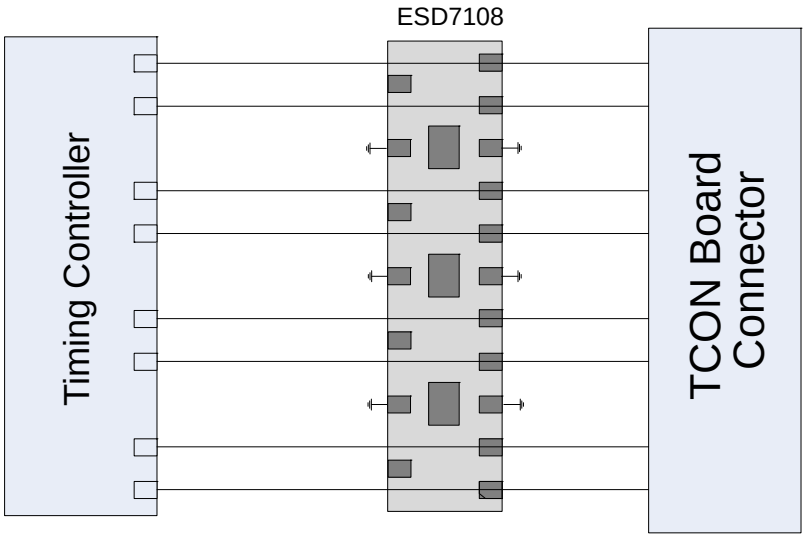
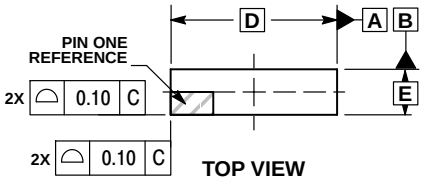


Figure 6. V−by−One HS Layout Diagram (for LCD Panel)

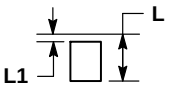
ESD7108

PACKAGE DIMENSIONS

UDFN18, 5.5x1.5, 0.5P
CASE 517BV
ISSUE O



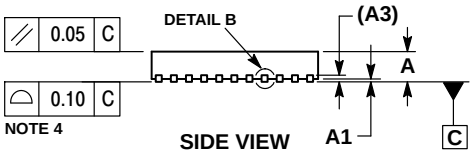
TOP VIEW



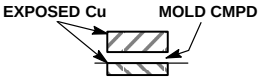
DETAIL A
OPTIONAL CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. EXPOSED ENDS OF TERMINALS ARE ELECTRICALLY ACTIVE.

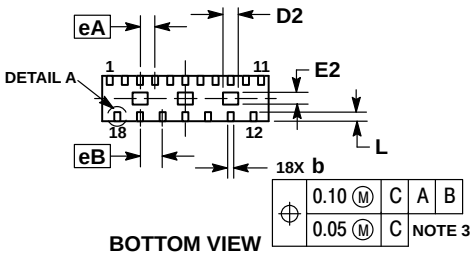
	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	5.50 BSC	
D2	0.45	0.55
E	1.50 BSC	
E2	0.35	0.45
eA	0.50 BSC	
eB	0.75 BSC	
L	0.20	0.40
L1	0.00	0.05



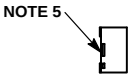
SIDE VIEW



DETAIL B
OPTIONAL CONSTRUCTION

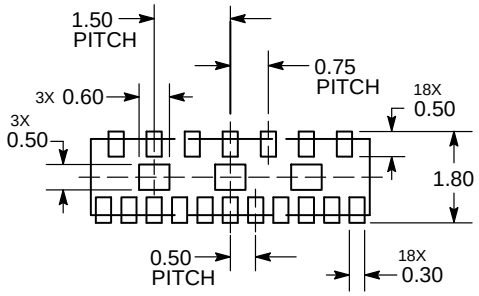


BOTTOM VIEW



END VIEW

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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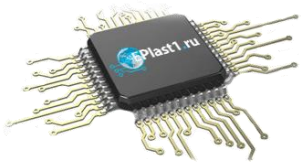
- Защита от снятия компонента с производства.



Как с нами связаться

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