

# TMD2672

## Digital Proximity Detector

### General Description

The TMD2672 family of devices provides a complete proximity detection system and digital interface logic in a single 8-pin surface mount module. The devices are register-set and pin-compatible with the TMD2671 series and includes new and improved proximity detection features. The proximity detection includes improved signal-to-noise and accuracy. A proximity offset register allows compensation for optical system crosstalk between the IR LED and the sensor. To prevent false proximity data measurement readings, a proximity saturation indicator bit signals that the internal analog circuitry has reached saturation. Interrupts have been enhanced with the addition of a sleep-on-interrupt feature that also allows for a single cycle operation. The device internal state machine provides the ability to put the device in a low-power mode in between proximity measurements, providing very low average power consumption.

The proximity detection system includes an LED driver and an IR LED, which are factory trimmed to eliminate the need for end-equipment calibration due to component variations.

*[Ordering Information](#) and [Content Guide](#) appear at end of datasheet.*

## Key Benefits & Features

The benefits and features of the TMD2672 digital proximity detector, are listed below:

**Figure 1:**  
Added Value of Using TMD2672

| Benefits  | Features   |
|---|--|
| <ul style="list-style-type: none"> <li>• Eliminates need for customer end-product calibration.</li> <li>• Reduces the proximity noise</li> <li>• Control of system crosstalk and offset</li> <li>• Prevents false proximity detection in bright light</li> <li>• Selectable IR power-level without external resistor</li> <li>• Enables wide operating range</li> </ul> | <ul style="list-style-type: none"> <li>• Digital Proximity Detector, LED Driver, and IR LED in a Single Optical Module</li> <li>• Register Set- and Pin-Compatible with the TMD2671 Series</li> <li>• Proximity Detection                             <ul style="list-style-type: none"> <li>- Reduced Proximity Count Variation <sup>(1)</sup></li> <li>- Programmable Offset Control Register <sup>(1)</sup></li> <li>- Saturation Indicator <sup>(1)</sup></li> <li>- Programmable Integration Time and Offset</li> <li>- Current Sink Driver for IR LED</li> <li>- 16,000:1 Dynamic Range</li> </ul> </li> </ul> |
| <ul style="list-style-type: none"> <li>• Reduces external processor burden</li> </ul>   | <ul style="list-style-type: none"> <li>• Maskable Proximity Interrupt                             <ul style="list-style-type: none"> <li>- Programmable Upper and Lower Thresholds with Persistence Filter</li> </ul> </li> </ul>  |
| <ul style="list-style-type: none"> <li>• Enables dynamic power dissipation control</li> </ul>   | <ul style="list-style-type: none"> <li>• Power Management                             <ul style="list-style-type: none"> <li>- Low Power 2.2µA Sleep State with User-Selectable Sleep-After-Interrupt Mode <sup>(1)</sup></li> <li>- 90µA Wait State with Programmable Wait Time from 2.7ms to &gt; 8 seconds</li> </ul> </li> </ul>   |
| <ul style="list-style-type: none"> <li>• Industry standard two-wire interface</li> </ul>  | <ul style="list-style-type: none"> <li>• I<sup>2</sup>C Fast Mode Compatible Interface                             <ul style="list-style-type: none"> <li>- Data Rates up to 400kbit/s</li> <li>- Input Voltage Levels Compatible with V<sub>DD</sub> or 1.8V Bus</li> </ul> </li> </ul>   |
| <ul style="list-style-type: none"> <li>• Small foot-print module</li> </ul>   | <ul style="list-style-type: none"> <li>• 3.94mm × 2.36mm × 1.35mm Package</li> </ul>   |

**Note(s) and/or Footnote(s):**

1. New or improved feature

## Applications

- Mobile Handset Touchscreen Control and Automatic Speakerphone Enable
- Mechanical Switch Replacement
- Paper Alignment

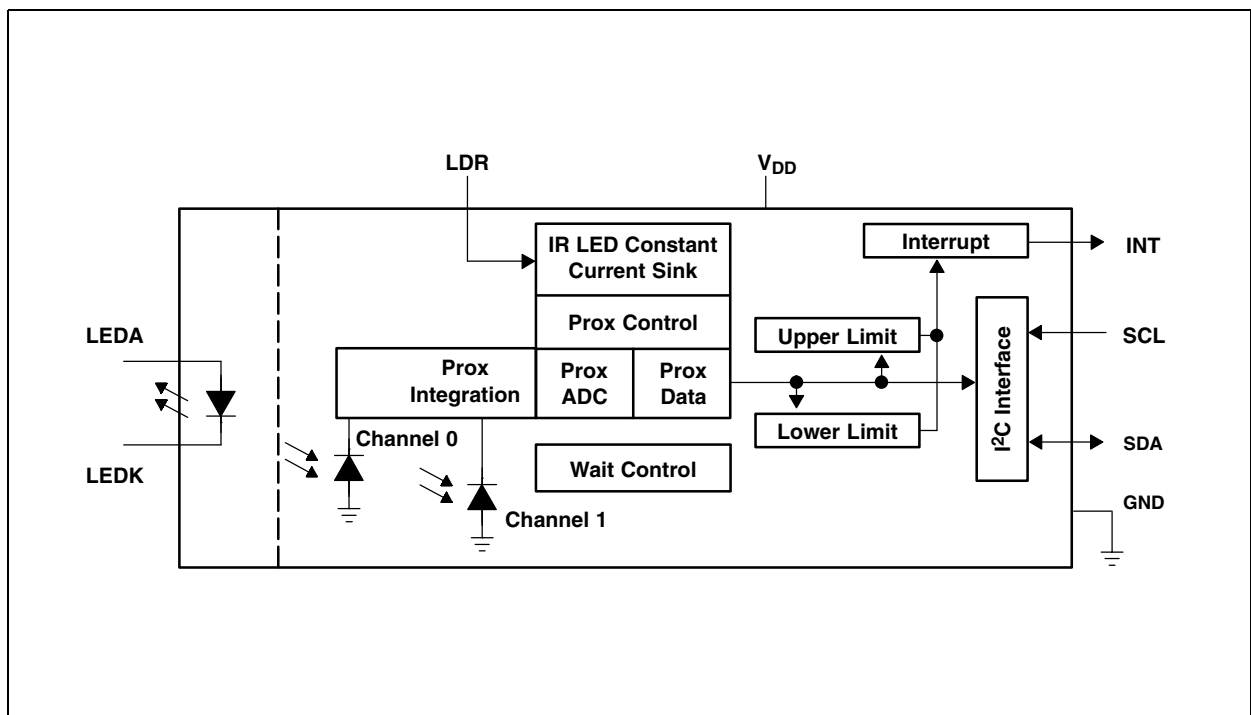
### End Products and Market Segments

- Mobile Handsets, Tablets, Laptops and HDTVs
- White Goods
- Toys
- Digital Signage
- Printing

### Block Diagram

The functional blocks of this device for reference are shown below:

Figure 2:  
TMD2672 Block Diagram



## Detailed Description

A fully integrated proximity detection solution is provided with an 850nm IR LED, LED driver circuit, and proximity detection engine. An internal LED driver (LDR) pin, is externally connected to the LED cathode (LEDK) to provide a controlled LED sink current. This is accomplished with a proprietary current calibration technique that accounts for all variances in silicon, optics, package, and most important, IR LED output power. This eliminates or greatly reduces the need for factory calibration that is required for most discrete proximity sensor solutions. The device is factory calibrated to achieve a proximity count reading at a specified distance with a specific number of pulses. In use, the number of proximity LED pulses can be programmed from 1 to 255 pulses, which allows different proximity distances to be achieved. Each pulse has a 16 $\mu$ s period, with a 7.2 $\mu$ s on time.

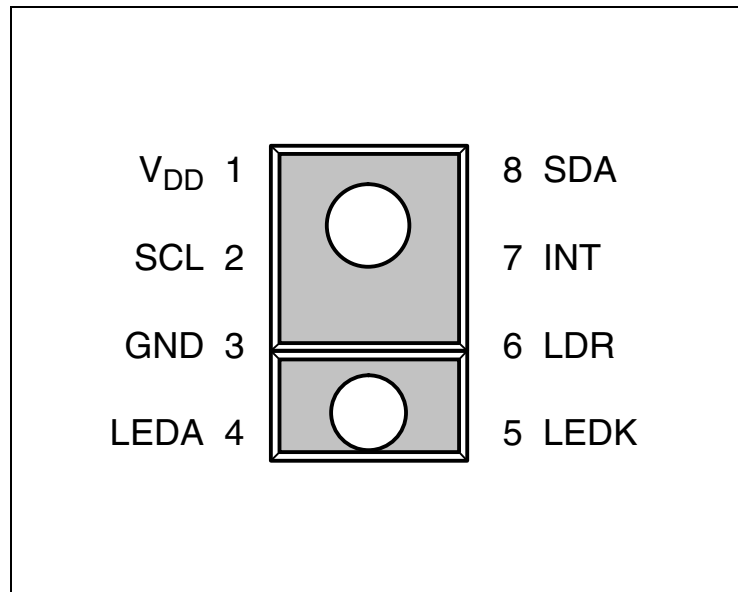
The device provides a separate pin for level-style interrupts. When interrupts are enabled and a pre-set value is exceeded, the interrupt pin is asserted and remains asserted until cleared by the controlling firmware. The interrupt feature simplifies and improves system efficiency by eliminating the need to poll a sensor for a proximity value. An interrupt is generated when the value of a proximity conversion exceeds either an upper or lower threshold. In addition, a programmable interrupt persistence feature allows the user to determine how many consecutive exceeded thresholds are necessary to trigger an interrupt.

## Pin Assignments

The TMD2672 pin assignments are described below:

**Figure 3:**  
Pin Diagram (Top View)

**Package Module-8:**  
Package drawing is not to scale



**Figure 4:**  
Terminal Functions

| Terminal        |     | Type | Description  |
|-----------------|-----|------|--|
| Name            | No. |      |  |
| V <sub>DD</sub> | 1   |      | Supply voltage   |
| SCL             | 2   | I    | I <sup>2</sup> C serial clock input terminal - clock signal for I <sup>2</sup> C serial data |
| GND             | 3   |      | Power supply ground. All voltages are referenced to GND.                                     |
| LEDA            | 4   |      | LED anode  |
| LEDK            | 5   |      | LED cathode. Connect to LDR pin when using internal LED driver circuit.                      |
| LDR             | 6   | O    | LED driver input for proximity IR LED, constant current source LED driver                    |
| INT             | 7   | O    | Interrupt - open drain (active low)  |
| SDA             | 8   | I/O  | I <sup>2</sup> C serial data I/O terminal - serial data I/O for I <sup>2</sup> C             |

## Absolute Maximum Ratings

Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 5:**  
**Absolute Maximum Ratings over Operating Free-Air Temperature Range (unless otherwise noted)**

| Symbol    | Parameter                            | Min   | Max | Unit |
|-----------|--------------------------------------|-------|-----|------|
| $V_{DD}$  | Supply voltage <sup>(1)</sup>        |       | 3.8 | V    |
|           | Input terminal voltage               | -0.5  | 3.8 | V    |
|           | Output terminal voltage (except LDR) | -0.5  | 3.8 | V    |
|           | Output terminal voltage (LDR)        |       | 3.8 | V    |
|           | Output terminal current (except LDR) | -1    | 20  | mA   |
| $T_{stg}$ | Storage temperature range            | -40   | 85  | °C   |
|           | ESD tolerance, human body model      | ±2000 |     | V    |

**Note(s) and/or Footnote(s):**

1. All voltages are with respect to GND.

## Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

**Figure 6:**  
Recommended Operating Conditions

| Symbol   | Parameter  | Min | Nom | Max | Unit |
|----------|--|-----|-----|-----|------|
| $V_{DD}$ | Supply voltage   | 2.6 | 3   | 3.6 | V    |
|          | Supply voltage accuracy, $V_{DD}$ total error including transients | -3  |     | 3   | %    |
| $T_A$    | Operating free-air temperature range <sup>(1)</sup>                | -30 |     | 85  | °C   |

**Note(s) and/or Footnote(s):**

1. While the device is operational across the temperature range, functionality will vary with temperature. Specifications are stated only at 25°C unless otherwise noted.

**Figure 7:**  
Operating Characteristics,  $V_{DD} = 3V$ ,  $T_A = 25^\circ C$  (unless otherwise noted)

| Symbol     | Parameter                           | Test Conditions                            | Min          | Typ | Max          | Unit    |
|------------|-------------------------------------|--|--------------|-----|--------------|---------|
| $I_{DD}$   | Supply current                      | Active - LDR pulse off                     |              | 195 | 250          | $\mu A$ |
|            |                                     | Wait state                                 |              | 90  |              |         |
|            |                                     | Sleep state - no I <sup>2</sup> C activity |              | 2.2 | 4            |         |
| $V_{OL}$   | INT, SDA output low voltage         | 3mA sink current                           | 0            |     | 0.4          | V       |
|            |                                     | 6mA sink current                           | 0            |     | 0.6          |         |
| $I_{LEAK}$ | Leakage current, SDA, SCL, INT pins |  | -5           |     | 5            | $\mu A$ |
| $I_{LEAK}$ | Leakage current, LDR pin            |  | -5           |     | 5            | $\mu A$ |
| $V_{IH}$   | SCL, SDA input high voltage         | TMD26721                                   | $0.7 V_{DD}$ |     |              | V       |
|            |                                     | TMD26723                                   | 1.25         |     |              |         |
| $V_{IL}$   | SCL, SDA input low voltage          | TMD26721                                   |              |     | $0.3 V_{DD}$ | V       |
|            |                                     | TMD26723                                   |              |     | 0.54         |         |

**Figure 8:**  
 Proximity Characteristics,  $V_{DD} = V_{LEDA} = 3V$ ,  $T_A = 25^\circ C$ ,  $PEN = 1$  (unless otherwise noted)

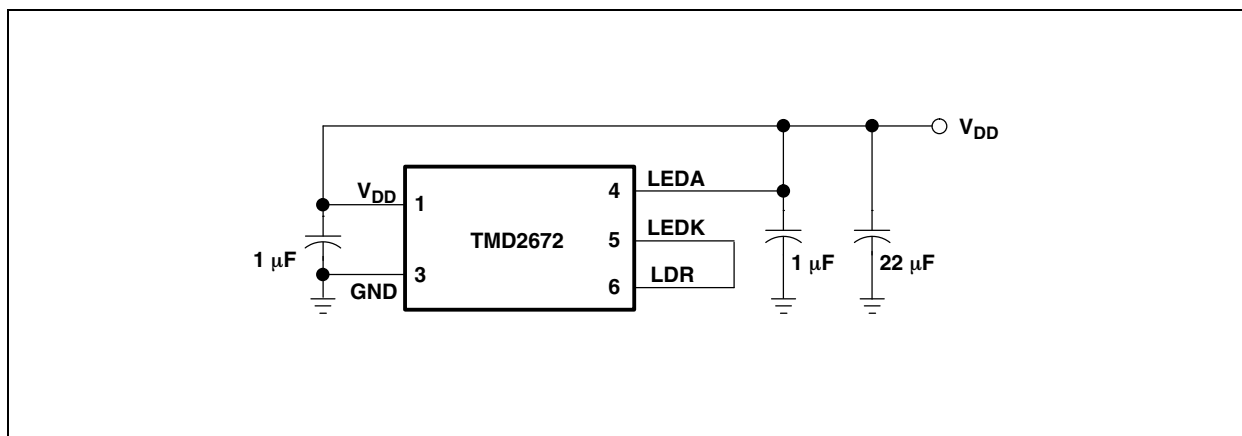
| Symbol     | Parameter                               | Test Conditions   | Min  | Typ  | Max  | Unit    |
|------------|---|---|------|------|------|---------|
| $I_{DD}$   | Supply current                          | LED On  |      | 3    |      | mA      |
| $I_{LEDA}$ | LEDA current <sup>(1)</sup>             | LED On, PDRIVE = 0  |      | 100  |      | mA      |
|            |   | LED On, PDRIVE = 1  |      | 50   |      |         |
|            |   | LED On, PDRIVE = 2  |      | 25   |      |         |
|            |   | LED On, PDRIVE = 3  |      | 12.5 |      |         |
| PTIME      | ADC conversion steps                    |   | 1    |      | 256  | steps   |
| PTIME      | ADC conversion time                     | PTIME = 0xFF<br>(= 1 conversion step)   | 2.58 | 2.73 | 2.9  | ms      |
| PTIME      | ADC counts per step                     | PTIME = 0xFF<br>(= 1 conversion step)   | 0    |      | 1023 | counts  |
| PPULSE     | LED pulses <sup>(5)</sup>               |   | 0    |      | 255  | pulses  |
| LED On     | LED pulse width                         | PPULSE = 1, PDRIVE = 0  |      | 7.3  |      | $\mu s$ |
|            | LED pulse period                        | PPULSE = 2, PDRIVE = 0  |      | 16.0 |      | $\mu s$ |
|            | Proximity response, no target (offset)  | PPULSE = 8, PDRIVE = 0,<br>PGAIN = 4x <sup>(2)</sup>  |      | 100  |      | counts  |
|            | Prox count, 100mm target <sup>(3)</sup> | 73mm x 83mm, 90%<br>reflective Kodak Gray Card,<br>PGAIN = 4x, PPULSE = 8,<br>PDRIVE = 0, PTIME = 0xFF <sup>(4)</sup> | 450  | 520  | 590  | counts  |

**Note(s) and/or Footnote(s):**

- Value is factory-adjusted to meet the Prox count specification. Considerable variation (relative to the typical value) is possible after adjustment.
- Proximity offset varies with power supply characteristics and noise.
- $I_{LEDA}$  is factory calibrated to achieve this specification. Offset and crosstalk directly sum with this value and is system dependent.
- No glass or aperture above the module. Tested value is the average of 5 consecutive readings.
- These parameters are ensured by design and characterization and are not 100% tested.
- Proximity test was done using the following circuit. See "Application Information: Hardware" on page 31. section for recommended application circuit.



**Figure 9:**  
Proximity Test Circuit



**Figure 10:**  
IR LED Characteristics,  $V_{DD} = 3V$ ,  $T_A = 25^\circ C$

| Symbol          | Parameter                    | Test Conditions                                     | Min | Typ | Max | Unit |
|-----------------|------------------------------|---|-----|-----|-----|------|
| $V_F$           | Forward Voltage              | $I_F = 20mA$  |     | 1.4 | 1.5 | V    |
| $V_R$           | Reverse Voltage              | $I_R = 10\mu A$                                     | 5   |     |     | V    |
| $P_O$           | Radiant Power                | $I_F = 20mA$  | 4.5 |     |     | mW   |
| $\lambda_p$     | Peak Wavelength              | $I_F = 20mA$  |     | 850 |     | nm   |
| $\Delta\lambda$ | Spectral Radiation Bandwidth | $I_F = 20mA$  |     | 40  |     | nm   |
| $T_R$           | Optical Rise Time            | $I_F = 100mA$ , $T_W = 125ns$ ,<br>duty cycle = 25% |     | 20  | 40  | ns   |
| $T_F$           | Optical Fall Time            | $I_F = 100mA$ , $T_W = 125ns$ ,<br>duty cycle = 25% |     | 20  | 40  | ns   |

**Figure 11:**  
Wait Characteristics,  $V_{DD} = 3V$ ,  $T_A = 25^\circ C$ , WEN = 1 (unless otherwise noted)

| Parameter  | Test Conditions              | Min | Typ  | Max | Unit  |
|------------|------------------------------|-----|------|-----|-------|
| Wait time  | WTIME = 0xFF (= 1 wait step) |     | 2.73 | 2.9 | ms    |
| Wait steps |                              | 1   |      | 256 | steps |

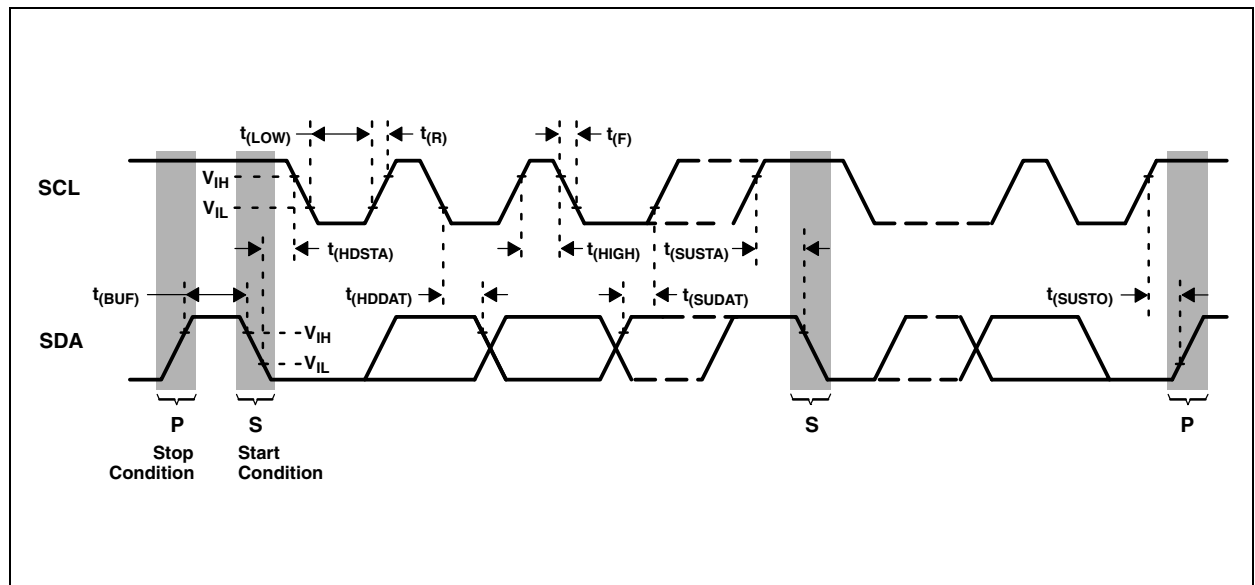
**Figure 12:**  
AC Electrical Characteristics,  $V_{DD} = 3V$ ,  $T_A = 25^\circ C$  (unless otherwise noted)

| Symbol        | Parameter (1)  | Test Conditions | Min | Typ | Max | Unit    |
|---------------|--|-----------------|-----|-----|-----|---------|
| $f_{(SCL)}$   | Clock frequency (I <sup>2</sup> C only)  |                 | 0   |     | 400 | kHz     |
| $t_{(BUF)}$   | Bus free time between start and stop condition   |                 | 1.3 |     |     | $\mu s$ |
| $t_{(HDSTA)}$ | Hold time after (repeated) start condition. After this period, the first clock is generated. |                 | 0.6 |     |     | $\mu s$ |
| $t_{(SUSTA)}$ | Repeated start condition setup time  |                 | 0.6 |     |     | $\mu s$ |
| $t_{(SUSTO)}$ | Stop condition setup time  |                 | 0.6 |     |     | $\mu s$ |
| $t_{(HDDAT)}$ | Data hold time   |                 | 0   |     |     | $\mu s$ |
| $t_{(SUDAT)}$ | Data setup time  |                 | 100 |     |     | ns      |
| $t_{(LOW)}$   | SCL clock low period   |                 | 1.3 |     |     | $\mu s$ |
| $t_{(HIGH)}$  | SCL clock high period  |                 | 0.6 |     |     | $\mu s$ |
| $t_F$         | Clock/data fall time   |                 |     |     | 300 | ns      |
| $t_R$         | Clock/data rise time   |                 |     |     | 300 | ns      |
| $C_i$         | Input pin capacitance  |                 |     |     | 10  | pF      |

**Note(s) and/or Footnote(s):**

1. Specified by design and characterization; not production tested.

**Figure 13:**  
Parameter Measurement Information: Timing Diagrams



## Typical Operating Characteristics

Figure 14:  
Spectral Responsivity

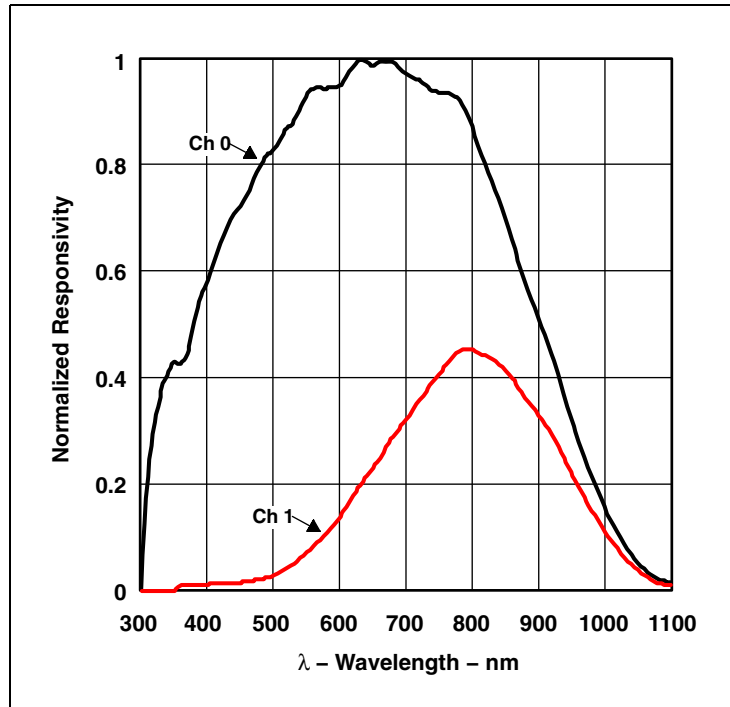


Figure 15:  
Normalized Responsivity vs. Angular Displacement

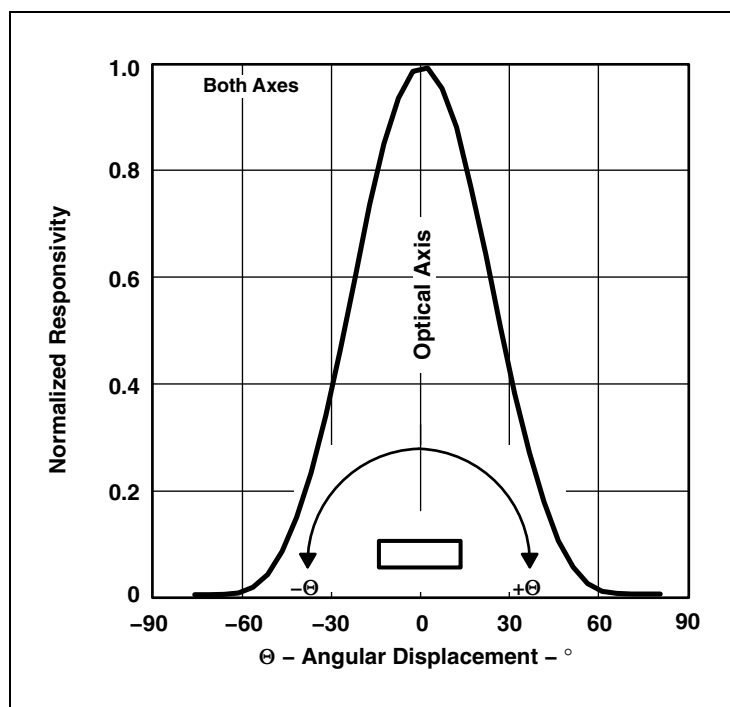


Figure 16:  
Typical LDR Current vs. Voltage

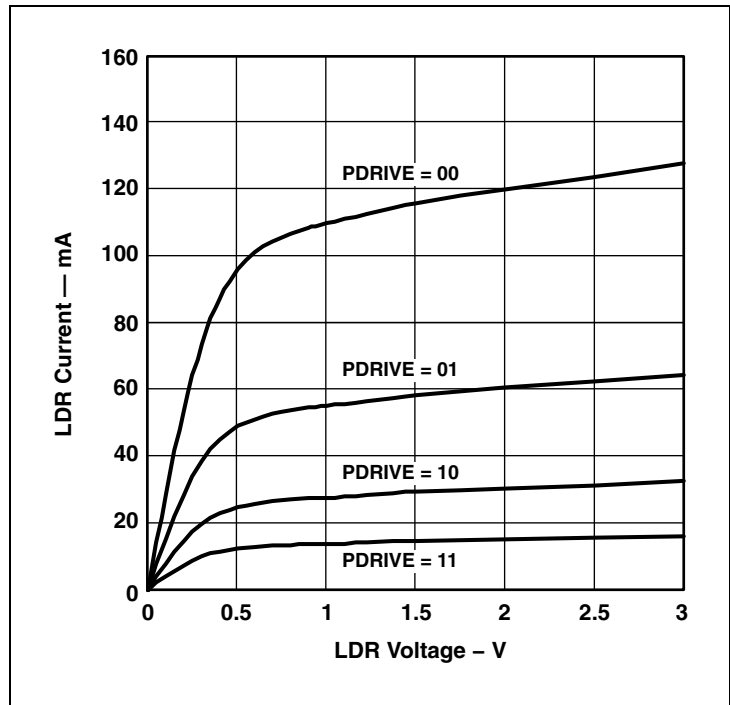
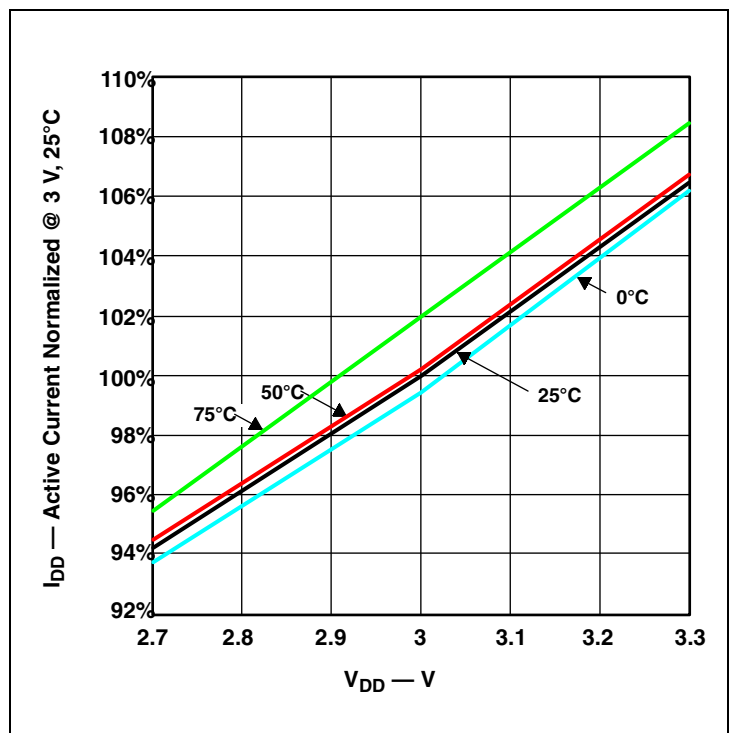


Figure 17:  
Normalized  $I_{DD}$  vs.  $V_{DD}$  and Temperature



## Principles of Operation

### System State Machine

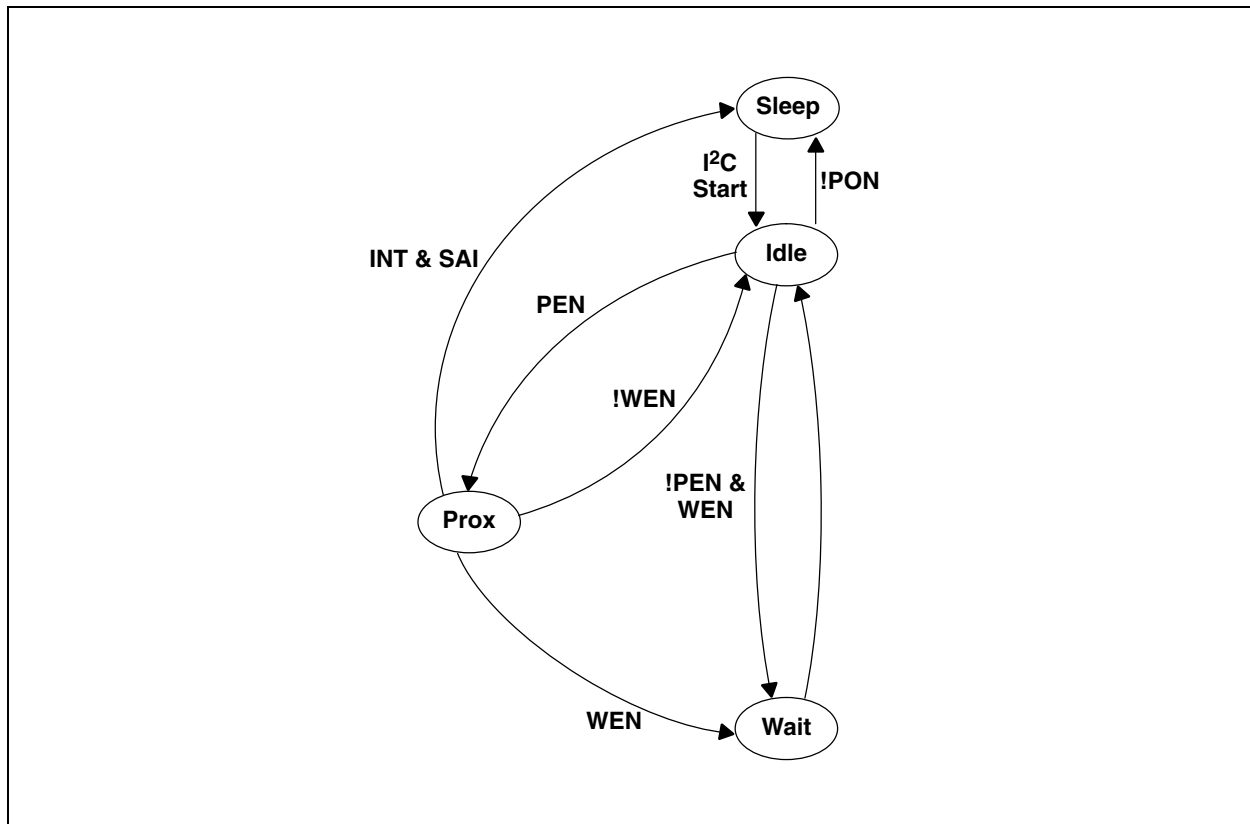
An internal state machine provides system control of the proximity detection and power management features of the device. At power up, an internal power-on-reset initializes the device and puts it in a low-power Sleep state.

When a start condition is detected on the I<sup>2</sup>C bus, the device transitions to the Idle state where it checks the Enable register (0x00) PON bit. If PON is disabled, the device will return to the Sleep state to save power. Otherwise, the device will remain in the Idle state until a proximity function is enabled. Once enabled, the device will execute the Prox and Wait states in sequence as indicated in Figure 18. Upon completion and return to Idle, the device will automatically begin a new prox-wait cycle as long as PON and PEN are enabled.

If the Prox function generates an interrupt and the Sleep-After-Interrupt (SAI) feature is enabled the device will transition to the Sleep state and remain in a low-power mode until an I<sup>2</sup>C command is received.

See [Interrupts](#) for additional information.

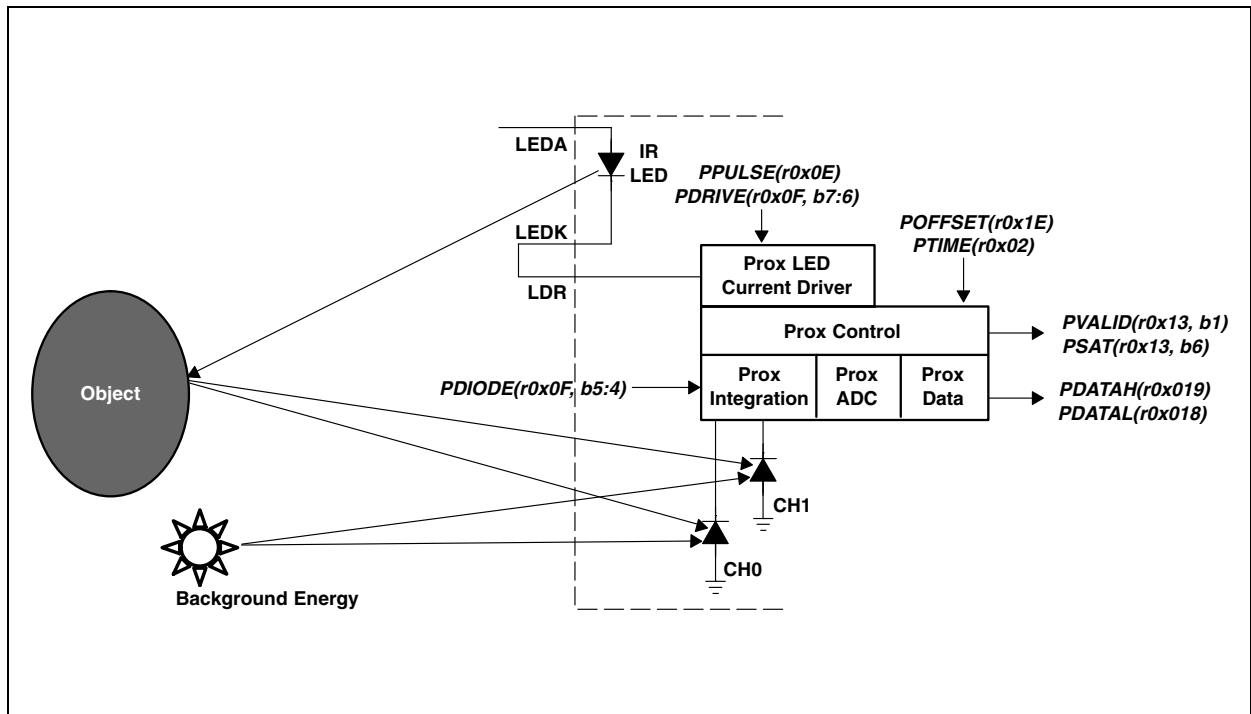
**Figure 18:**  
Simplified State Diagram



### Proximity Detection

Proximity detection is accomplished by measuring the amount of IR energy, from the internal IR LED, reflected off an object to determine its distance. The internal proximity IR LED is driven by the integrated proximity LED current driver as shown in Figure 19.

Figure 19: Proximity Detection



The LED current driver, output on the LDR terminal, provides a regulated current sink that eliminates the need for an external current limiting resistor. PDRIVE sets the drive current to one of four selectable levels.

Referring to the Detailed State Machine figure, the LED current driver pulses the IR LED as shown in Figure 20 during the Prox Accum state. Figure 20 also illustrates that the LED On pulse has a fixed width of 7.3µs and period of 16.0µs. So, in addition to setting the proximity drive current, 1 to 255 proximity pulses (PPULSE) can be programmed. When deciding on the number of proximity pulses, keep in mind that the signal increases proportionally to PPULSE, while noise increases by the square root of PPULSE.

**Figure 20:**  
Proximity LED Current Driver Waveform

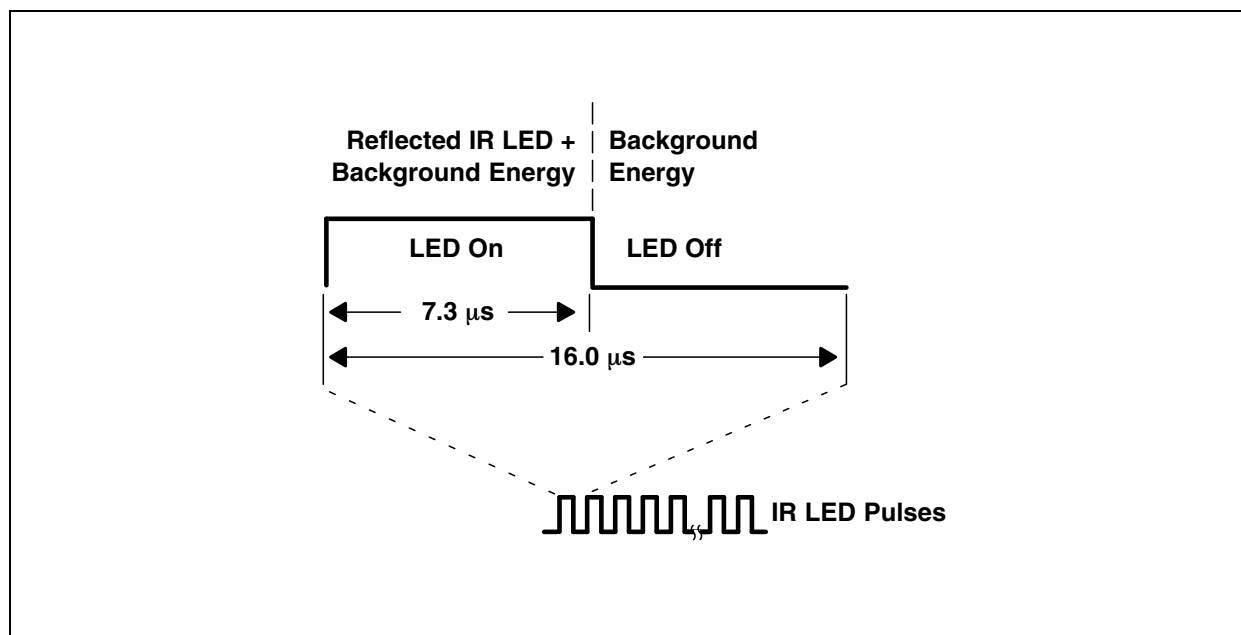


Figure 19 illustrates light rays emitting from the internal IR LED, reflecting off an object, and being absorbed by the CH0 and CH1 photodiodes. The proximity diode selector (PDIODE) determines which of the two photodiodes is used for a given proximity measurement. Note that neither photodiode is selected when the device first powers up, so PDIODE must be set for proximity detection to work.

Referring again to Figure 20, the reflected IR LED and the background energy is integrated during the LED On time, then during the LED Off time, the integrated background energy is subtracted from the LED On time energy, leaving the IR LED energy to accumulate from pulse to pulse. During LED On time integration, the proximity saturation bit in the Status register (0x13) will be set if the integrator saturates. This condition can occur if the proximity gain is set too high for the lighting conditions, such as in the presence of bright sunlight. Once asserted, PSAT will remain set until a special function proximity interrupt clear command is received from the host (see [Command Register](#))

After the programmed number of proximity pulses have been generated, the proximity ADC converts and scales the proximity measurement to a 16-bit value, then stores the result in two 8-bit proximity data (PDATAx) registers. ADC scaling is controlled by the proximity ADC conversion time (PTIME) which is programmable from 1 to 256 2.73ms time units. However, depending on the application, scaling the proximity data will equally scale any accumulated noise. Therefore, in general, it is recommended to leave PTIME at the default value of one 2.73ms ADC conversion time (0xFF).

In many practical proximity applications, a number of optical system and environmental conditions can produce an offset in the proximity measurement result. To counter these effects, a proximity offset (POFFSET) is provided which allows the proximity data to be shifted positive or negative. Additional information on the use of the proximity offset feature is provided in available **ams** application notes.

Once the first proximity cycle has completed, the proximity valid (PVALID) bit in the Status register will be set and remain set until the proximity detection function is disabled (PEN).

For additional information on using the proximity detection function behind glass and for optical system design guidance, please see available **ams** application notes.



### Interrupts

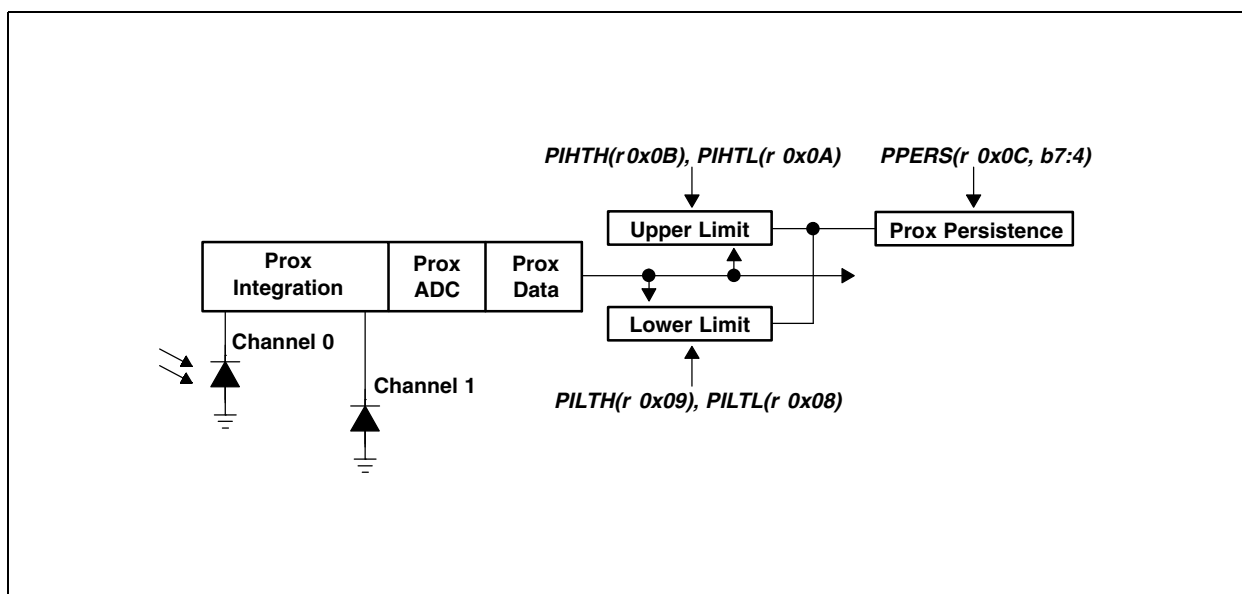
The interrupt feature simplifies and improves system efficiency by eliminating the need to poll the sensor for proximity values outside a user-defined range. While the interrupt function is always enabled and its status is available in the Status register (0x13), the output of the interrupt state can be enabled using the proximity interrupt enable (PIEN) field in the Enable register (0x00).

Two 16-bit interrupt threshold registers allow the user to set limits below and above a desired proximity range. An interrupt can be generated when the proximity data (PDATA) falls below the proximity interrupt low threshold (PILTx) or exceeds the proximity interrupt high threshold (PIHTx).

It is important to note that the thresholds are evaluated in sequence, first the low threshold, then the high threshold. As a result, if the low threshold is set above the high threshold, the high threshold is ignored and only the low threshold is evaluated.

To further control when an interrupt occurs, the device provides an interrupt persistence feature. The persistence filter allows the user to specify the number of consecutive out-of-range proximity occurrences before an interrupt is generated. The persistence filter register (0x0C) allows the user to set the proximity persistence filter (PPERS) values. See the persistence filter register for details on the persistence filter values. Once the persistence filter generates an interrupt, it will continue until a special function interrupt clear command is received (see [Command Register](#)).

**Figure 21:**  
Programmable Interrupt



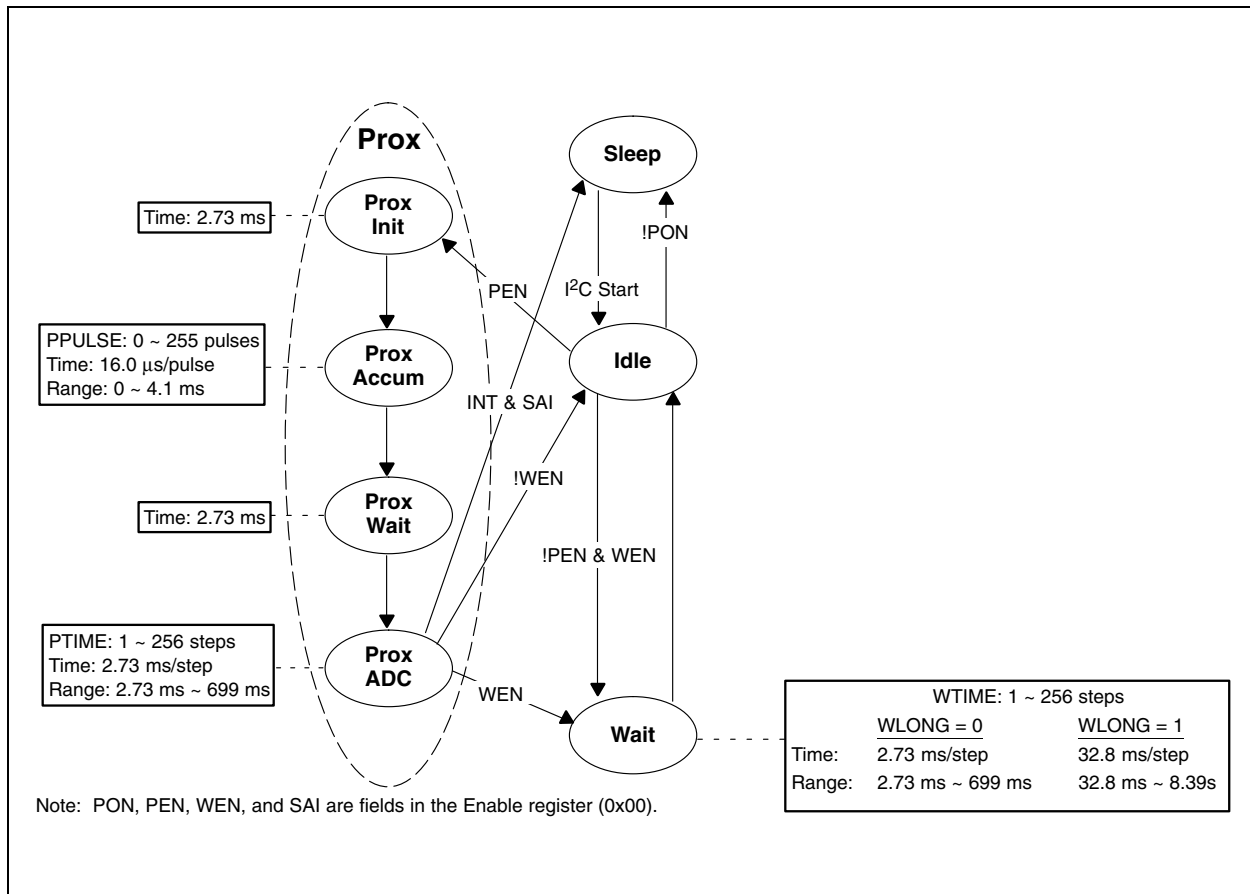
### State Diagram

The system state machine shown in Figure 18 provides an overview of the states and state transitions that provide system control of the device. This section highlights the programmable features that affect the state machine cycle time, and provides details to determine system level timing.

When the proximity detection feature is enabled (PEN), the state machine transitions through the Prox Init, Prox Accum, Prox Wait, and Prox ADC states. The Prox Init and Prox Wait times are a fixed 2.73ms, whereas the Prox Accum time is determined by the number of proximity LED pulses (PPULSE) and the Prox ADC time is determined by the integration time (PTIME). The formulas to determine the Prox Accum and Prox ADC times are given in the associated boxes in Figure 22. If an interrupt is generated as a result of the proximity cycle, it will be asserted at the end of the Prox ADC state and transition to the Sleep state if SAI is enabled.

When the power management feature is enabled (WEN), the state machine will transition in turn to the Wait state. The wait time is determined by WLONG, which extends normal operation by 12x when asserted, and WTIME. The formula to determine the wait time is given in the box associated with the Wait state in Figure 22.

Figure 22: Expanded State Diagram



## Power Management

Power consumption can be managed with the Wait state because the wait state consumes only 90µA of I<sub>DD</sub> current. An example of the power management feature is shown in [Figure 23](#). With the assumptions provided in the example, the average I<sub>DD</sub> is estimated to be 157µA.

**Figure 23:**  
Power Management

| System State<br>Machine State | Programmable<br>Parameter | Programmed<br>Value | Duration               | Typical<br>Current |
|-------------------------------|---------------------------|---------------------|------------------------|--------------------|
| Prox Init                     |                           |                     | 2.73ms                 | 0.195mA            |
| Prox Accum                    | PPULSE                    | 0x04                | 0.064ms                |                    |
| Prox Accum – LED On           |                           |                     | 0.029ms <sup>(1)</sup> | 103mA              |
| Prox Accum – LED Off          |                           |                     | 0.035ms <sup>(2)</sup> | 0.195mA            |
| Prox Wait                     |                           |                     | 2.73ms                 | 0.195mA            |
| Prox ADC                      | PTIME                     | 0xFF                | 2.73ms                 | 0.195mA            |
| Wait                          | WTIME                     | 0xEE                | 49.2ms                 | 0.090mA            |
|                               | WLONG                     | 0                   |                        |                    |

**Note(s) and/or Footnote(s):**

1. Prox Accum - LED On time = 7.3µs per pulse × 4 pulses = 29.3µs = 0.029ms

2. Prox Accum - LED Off time = 8.7µs per pulse × 4 pulses = 34.7µs = 0.035ms

Average IDD Current = ((2.73 × 0.195) + (0.029 × 103) + (0.035 × 0.195) + (2 × 2.73 × 0.195) + (49.2 × 0.090)) / 57.45 ≈ 157 µA

Keeping with the same programmed values as the example, [Figure 24](#) shows how the average IDD current is affected by the Wait state time, which is determined by WEN, WTIME, and WLONG. Note that the worst-case current occurs when the Wait state is not enabled.

**Figure 24:**  
Average I<sub>DD</sub> Current

| WEN | WTIME | WLONG | Wait State | Average I <sub>DD</sub> Current |
|-----|-------|-------|------------|---------------------------------|
| 0   | n/a   | n/a   | 0ms        | 556µA                           |
| 1   | 0xFF  | 0     | 2.73ms     | 440µA                           |
| 1   | 0xEE  | 0     | 49.2ms     | 157µA                           |
| 1   | 0x00  | 0     | 699ms      | 99µA                            |
| 1   | 0x00  | 1     | 8389ms     | 90µA                            |

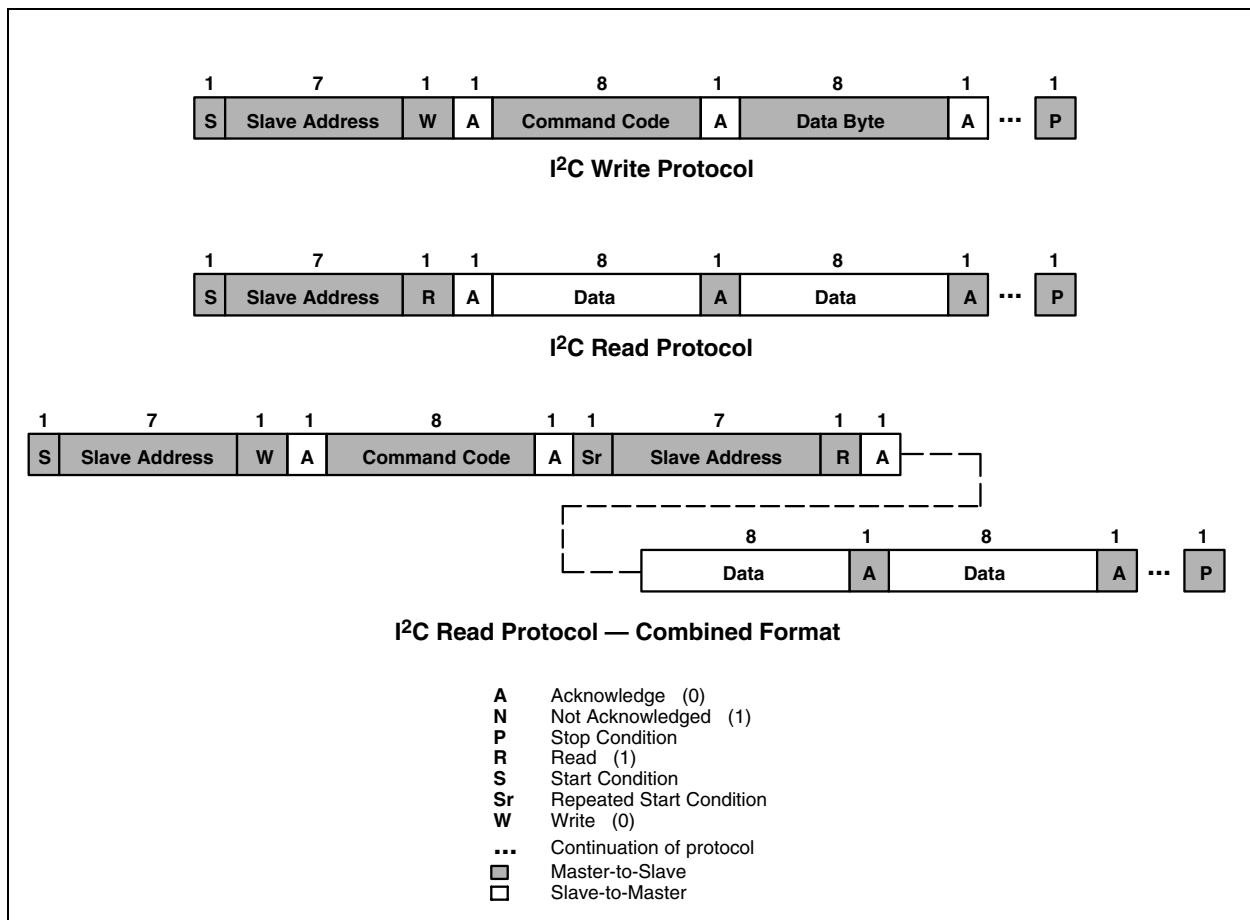
### I<sup>2</sup>C Protocol

Interface and control are accomplished through an I<sup>2</sup>C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The devices support the 7-bit I<sup>2</sup>C addressing protocol.

The I<sup>2</sup>C standard provides for three types of bus transaction: read, write, and a combined protocol (Figure 25). During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

The I<sup>2</sup>C bus protocol was developed by Philips (now NXP). For a complete description of the I<sup>2</sup>C protocol, please review the NXP I<sup>2</sup>C design specification at <http://www.i2c-bus.org/references>.

Figure 25:  
I<sup>2</sup>C Protocols



## Register Set

The device is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The Register Set is summarized in [Figure 26](#).

**Figure 26:**  
Register Address

| Address | Register Name | R/W | Register Function                            | Reset Value |
|---------|---------------|-----|--|-------------|
| ---     | COMMAND       | W   | Specifies register address                   | 0x00        |
| 0x00    | ENABLE        | R/W | Enables states and interrupts                | 0x00        |
| 0x02    | PTIME         | R/W | Proximity ADC time                           | 0xFF        |
| 0x03    | WTIME         | R/W | Wait time                                    | 0xFF        |
| 0x08    | PILTL         | R/W | Proximity interrupt low threshold low byte   | 0x00        |
| 0x09    | PILTH         | R/W | Proximity interrupt low threshold high byte  | 0x00        |
| 0x0A    | PIHTL         | R/W | Proximity interrupt high threshold low byte  | 0x00        |
| 0x0B    | PIHTH         | R/W | Proximity interrupt high threshold high byte | 0x00        |
| 0x0C    | PERS          | R/W | Interrupt persistence filter                 | 0x00        |
| 0x0D    | CONFIG        | R/W | Configuration                                | 0x00        |
| 0x0E    | PPULSE        | R/W | Proximity pulse count                        | 0x00        |
| 0x0F    | CONTROL       | R/W | Control register                             | 0x00        |
| 0x11    | REVISION      | R   | Die revision number                          | Rev Num.    |
| 0x12    | ID            | R   | Device ID                                    | ID          |
| 0x13    | STATUS        | R   | Device status                                | 0x00        |
| 0x18    | PDATAH        | R   | Proximity ADC high data register             | 0x00        |
| 0x19    | PDATAH        | R   | Proximity ADC high data register             | 0x00        |
| 0x1E    | POFFSET       | R/W | Proximity Offset register                    | 0x00        |

The mechanics of accessing a specific register depends on the specific protocol used. See the section on I<sup>2</sup>C protocols on the previous pages. In general, the Command register is written first to specify the specific control/status register for following read/write operations.

### Command Register

The Command Register specifies the address of the target register for future write and read operations.

**Figure 27:**  
Command Register

|                |             |   |   |            |   |   |   |   |
|----------------|-------------|---|---|------------|---|---|---|---|
|                | 7           | 6 | 5 | 4          | 3 | 2 | 1 | 0 |
| <b>COMMAND</b> | <b>TYPE</b> |   |   | <b>ADD</b> |   |   |   |   |

| Field   | Bits | Description   |  |
|---------|------|---|--|
| COMMAND | 7    | Select Command Register. Must write as 1 when addressing Command Register.  |  |
| TYPE    | 6:5  | Selects type of transaction to follow in subsequent data transfers:   |  |
|         |      | <b>Field Value</b>  | <b>Description</b>                       |
|         |      | 00  | Repeated byte protocol transaction       |
|         |      | 01  | Auto-increment protocol transaction      |
|         |      | 10  | Reserved - Do not use                    |
|         |      | 11  | Special function - See description below |
|         |      | Transaction type 00 will repeatedly read the same register with each data access. Transaction type 01 will provide an auto-increment function to read successive register bytes.  |  |
| ADD     | 4:0  | Address Register/Special Function Register. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control-status-register for following write and read transactions: |  |
|         |      | <b>Field Value</b>  | <b>Description</b>                       |
|         |      | 00000   | Normal - no action                       |
|         |      | 00101   | Proximity interrupt clear                |
|         |      | Proximity Interrupt Clear clears any pending proximity interrupt. This special function is self clearing.   |  |

### Enable Register (0x00)

The Enable Register is used to power the device on/off, enable functions, and interrupts.

**Figure 28:**  
Enable Register

|                 |            |             |                 |            |            |                 |            |   |
|-----------------|------------|-------------|-----------------|------------|------------|-----------------|------------|---|
|                 | 7          | 6           | 5               | 4          | 3          | 2               | 1          | 0 |
| <b>Reserved</b> | <b>SAI</b> | <b>PIEN</b> | <b>Reserved</b> | <b>WEN</b> | <b>PEN</b> | <b>Reserved</b> | <b>PON</b> |   |

| Field    | Bits | Description  |
|----------|------|--|
| Reserved | 7    | Reserved. Write as 0.  |
| SAI      | 6    | Sleep After Interrupt. 0 = not enabled, 1 = enabled  |
| PIEN     | 5    | Proximity Interrupt Mask. When asserted, permits proximity interrupts to be generated.   |
| Reserved | 4    | Reserved. Write as 0.  |
| WEN      | 3    | Wait Enable. This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.   |
| PEN      | 2    | Proximity Enable. This bit activates the proximity function. Writing a 1 enables proximity. Writing a 0 disables proximity.  |
| Reserved | 1    | Reserved. Write as 0.  |
| PON      | 0    | Power ON. This bit activates the internal oscillator to permit the timers and ADC channel to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator. |

### Proximity Time Control Register (0x02)

The Proximity Timing Register controls the integration time of the proximity ADC in 2.73ms increments. Upon power up, the Proximity Time Register is set to 0xFF. It is recommended that this register be programmed to a value of 0xFF (1 integration cycle).

**Figure 29:**  
Proximity Time Control Register

| Field | Bits | Description  |                     |             |                  |
|-------|------|--------------|---------------------|-------------|------------------|
| PTIME | 7:0  | <b>Value</b> | <b>INTEG_CYCLES</b> | <b>Time</b> | <b>Max Count</b> |
|       |      | 0xFF         | 1                   | 2.73ms      | 1023             |

### Wait Time Register (0x03)

Wait time is set 2.73ms increments unless the WLONG bit is asserted, in which case the wait times are 12x longer. WTIME is programmed as a 2's complement number. Upon power up, the Wait Time Register is set to 0xFF.

**Figure 30:**  
Proximity Time Control Register

| Field | Bits | Description           |                  |                         |                         |
|-------|------|-----------------------|------------------|-------------------------|-------------------------|
| WTIME | 7:0  | <b>Register Value</b> | <b>Wait Time</b> | <b>Time (WLONG = 0)</b> | <b>Time (WLONG = 1)</b> |
|       |      | 0xFF                  | 1                | 2.72ms                  | 0.032 sec               |
|       |      | 0xB6                  | 74               | 200ms                   | 2.4 sec                 |
|       |      | 0x00                  | 256              | 700ms                   | 8.3 sec                 |

**Note(s) and/or Footnote(s):**

1. The Proximity Wait Time Register should be configured before PEN is asserted.

### Proximity Interrupt Threshold Register (0x08 - 0x0B)

The Proximity Interrupt Threshold Registers provide the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by proximity channel crosses below the lower threshold specified, or above the higher threshold, an interrupt is signaled to the host processor.

**Figure 31:**  
Proximity Interrupt Threshold Register

| Register | Address | Bits | Description                         |
|----------|---------|------|-------------------------------------|
| PILTL    | 0x08    | 7:0  | Proximity low threshold lower byte  |
| PILTH    | 0x09    | 7:0  | Proximity low threshold upper byte  |
| PIHTL    | 0x0A    | 7:0  | Proximity high threshold lower byte |
| PIHTL    | 0x0B    | 7:0  | Proximity high threshold upper byte |



### Persistence Register (0x0C)

The Persistence Register controls the filtering interrupt capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after each ADC integration cycle or if the ADC integration has produced a result that is outside of the values specified by threshold register for some specified amount of time.

**Figure 32:**  
Persistence Register

|  |              |   |   |   |                 |   |   |   |
|--|--------------|---|---|---|-----------------|---|---|---|
|  | 7            | 6 | 5 | 4 | 3               | 2 | 1 | 0 |
|  | <b>PPERS</b> |   |   |   | <b>Reserved</b> |   |   |   |

| Field    | Bits | Description  |                |  |
|----------|------|--|----------------|--|
| PPERS    | 7:4  | Proximity Interrupt Persistence. Controls rate of proximity interrupt to the host processor. |                |  |
|          |      | <b>Field Value</b>   | <b>Meaning</b> | <b>Interrupt Persistence Function</b>        |
|          |      | 0000   | ----           | Every proximity cycle generates an interrupt |
|          |      | 0001   | 1              | 1 proximity value out of range               |
|          |      | 0010   | 2              | 2 consecutive proximity values out of range  |
|          |      | ....   | ....           | ....   |
|          |      | 1111   | 15             | 15 consecutive proximity values out of range |
| Reserved | 3:0  | Default setting is 0x00.   |                |  |

### Configuration Register (0x0D)

The Configuration Register sets the wait long time.

**Figure 33:**  
Enable Register

|  |                 |   |   |   |   |              |                 |   |
|--|-----------------|---|---|---|---|--------------|-----------------|---|
|  | 7               | 6 | 5 | 4 | 3 | 2            | 1               | 0 |
|  | <b>Reserved</b> |   |   |   |   | <b>WLONG</b> | <b>Reserved</b> |   |

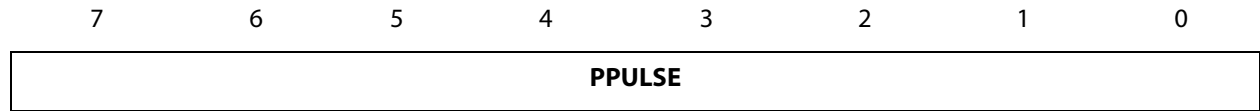
  

| Field    | Bits | Description   |
|----------|------|---|
| Reserved | 7:2  | Reserved. Write as 0.   |
| WLONG    | 1    | Wait Long. When asserted, the wait cycles are increased by a factor 12x from that programmed in the WTIME register. |
| Reserved | 0    | Reserved. Write as 0.   |

**Proximity Pulse Count Register (0x0E)**

The Proximity Pulse Count Register sets the number of proximity pulses that will be transmitted. PPULSE defines the number of pulses to be transmitted at a 62.5kHz rate.

**Figure 34:**  
Proximity Pulse Count Register



| Field  | Bits | Description  |
|--------|------|--|
| PPULSE | 7:0  | Proximity Pulse Count. Specifies the number of proximity pulses to be generated. |

## Control Register (0x0F)

The Control Register provides four bits of control to the analog block. These bits control the diode drive current and diode selection functions.

**Figure 35:**  
Control Register

| 7             | 6 | 5             | 4 | 3            | 2 | 1               | 0 |
|---------------|---|---------------|---|--------------|---|-----------------|---|
| <b>PDRIVE</b> |   | <b>PDIODE</b> |   | <b>PGAIN</b> |   | <b>Reserved</b> |   |

| Field                 | Bits | Description                  |                               |                               |
|-----------------------|------|------------------------------|-------------------------------|-------------------------------|
| PDRIVE <sup>(1)</sup> | 7:6  | Proximity LED Drive Strength |                               |                               |
|                       |      | <b>Field Value</b>           | <b>LED STRENGTH - PDL = 0</b> | <b>LED STRENGTH - PDL = 1</b> |
|                       |      | 00                           | <i>100mA</i>                  | <i>11.1mA</i>                 |
|                       |      | 01                           | <i>50mA</i>                   | <i>5.6mA</i>                  |
|                       |      | 10                           | <i>25mA</i>                   | <i>2.8mA</i>                  |
|                       |      | 11                           | <i>12.5mA</i>                 | <i>1.4mA</i>                  |
| PDIODE                | 5:4  | Proximity Diode Selector     |                               |                               |
|                       |      | <b>Field Value</b>           | <b>Diode Selection</b>        |                               |
|                       |      | 00                           | Proximity uses neither diode  |                               |
|                       |      | 01                           | Proximity uses the CH0 diode  |                               |
|                       |      | 10                           | Proximity uses the CH1 diode  |                               |
|                       |      | 11                           | Reserved - Do not write       |                               |
| PGAIN                 | 3:2  | Proximity Gain               |                               |                               |
|                       |      | <b>Field Value</b>           | <b>Proximity Gain Value</b>   |                               |
|                       |      | 00                           | 1× gain                       |                               |
|                       |      | 01                           | 2× gain                       |                               |
|                       |      | 10                           | 4× gain                       |                               |
|                       |      | 11                           | 8× gain                       |                               |
| Reserved              | 1:0  | Reserved                     |                               |                               |

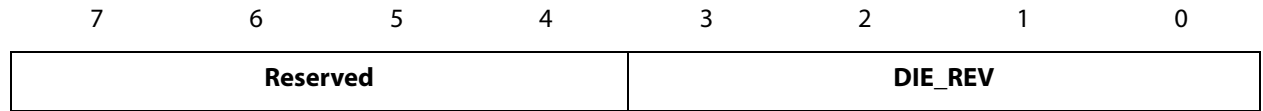
**Note(s) and/or Footnote(s):**

1. LED STRENGTH values (italic) are nominal operating values. Specifications can be found in the Proximity Characteristics table.

### Revision Register (0x11)

The Revision Register shows the silicon revision number. It is a read-only register and shows the revision level of the silicon used internally.

Figure 36:  
Revision Register

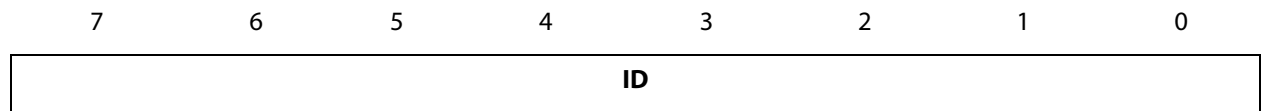


| Field    | Bits | Description         |                     |
|----------|------|---------------------|---------------------|
| Reserved | 7:4  | Reserved            | Bits read as 0      |
| DIE_REV  | 3:0  | Die revision number | Die revision number |

### ID Register (0x12)

The ID Register provides the value for the part number. The ID Register is a read-only register.

Figure 37:  
ID Register



| Field | Bits | Description                |                 |
|-------|------|----------------------------|-----------------|
| ID    | 7:0  | Part number identification | 0x32 = TMD26721 |
|       |      |                            | 0x3B = TMD26723 |

### Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

**Figure 38:**  
Status Register

|                 |             |             |                 |   |   |               |                 |
|-----------------|-------------|-------------|-----------------|---|---|---------------|-----------------|
| 7               | 6           | 5           | 4               | 3 | 2 | 1             | 0               |
| <b>Reserved</b> | <b>PSAT</b> | <b>PINT</b> | <b>Reserved</b> |   |   | <b>PVALID</b> | <b>Reserved</b> |

| Field    | Bits | Description   |
|----------|------|---|
| Reserved | 7    | Reserved  |
| PSAT     | 6    | Proximity Saturation. Indicates that the proximity measurement saturated.   |
| PINT     | 5    | Proximity Interrupt. Indicates that the device is asserting a proximity interrupt.                                    |
| Reserved | 4:2  | Reserved. Bits read as 0.   |
| PVALID   | 1    | Proximity Valid. Indicates that the proximity channel has completed an integration cycle after PEN has been asserted. |
| Reserved | 0    | Reserved  |

### Proximity Data Register (0x18 - 0x19h)

Proximity data is stored as a 16-bit value. To ensure the data is read correctly, a two-byte I<sup>2</sup>C read transaction should be utilized with auto increment protocol bits set in the Command Register. With this operation, when the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if the next ADC cycle ends between the reading of the lower and upper registers.

**Figure 39:**  
PDATA Registers

| Register           | Address | Bits | Description              |
|--------------------|---------|------|--------------------------|
| PDATA <sub>L</sub> | 0x18    | 7:0  | Proximity data low byte  |
| PDATA <sub>H</sub> | 0x19    | 7:0  | Proximity data high byte |

### Proximity Offset Register (0x1E)

The 8-bit Proximity Offset Register provides compensation for proximity offsets caused by device variations, optical crosstalk, and other environmental factors. Proximity offset is a sign-magnitude value where the sign bit, bit 7, determines if the offset is negative (bit 7 = 0) or positive (bit 7 = 1). At power up, the register is set to 0x00. The magnitude of the offset compensation depends on the proximity gain (PGAIN), proximity LED drive strength (PDRIVE), and the number of proximity pulses (PPULSE). Because a number of environmental factors contribute to proximity offset, this register is best suited for use in an adaptive closed-loop control system. See available **ams** application notes for proximity offset register application information.

**Figure 40:**  
Proximity Offset Register

|  |             |                  |   |   |   |   |   |   |
|--|-------------|------------------|---|---|---|---|---|---|
|  | 7           | 6                | 5 | 4 | 3 | 2 | 1 | 0 |
|  | <b>SIGN</b> | <b>MAGNITUDE</b> |   |   |   |   |   |   |

| Field     | Bits | Description  |
|-----------|------|--|
| SIGN      | 7    | Proximity Offset Sign. The offset sign shifts the proximity data negative when equal to 0 and positive when equal to 1.  |
| MAGNITUDE | 6:0  | Proximity Offset Magnitude. The offset magnitude shifts the proximity data positive or negative, depending on the proximity offset sign. The actual amount of the shift depends on the proximity gain (PGAIN), proximity LED drive strength (PDRIVE), and the number of proximity pulses (PPULSE). |

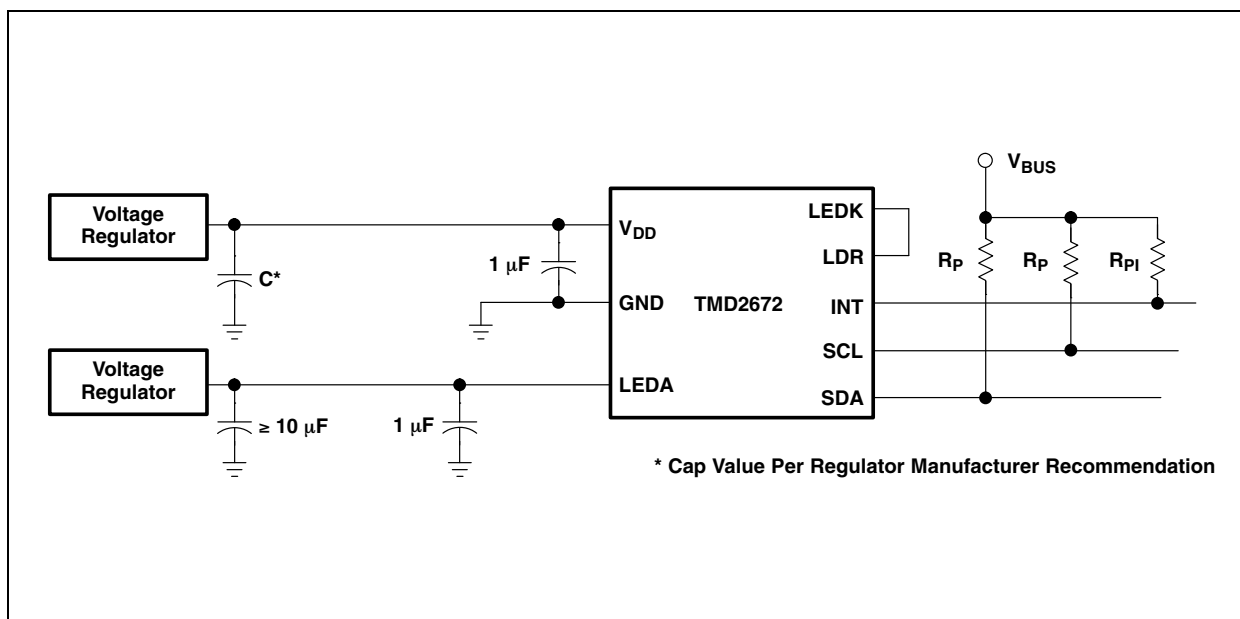
## Application Information: Hardware

### LED Driver Pin with Proximity Detection

In a proximity sensing system, the included IR LED can be pulsed with more than 100mA of rapidly switching current, therefore, a few design considerations must be kept in mind to get the best performance. The key goal is to reduce the power supply noise coupled back into the device during the LED pulses. Averaging of multiple proximity samples is recommended to reduce the proximity noise.

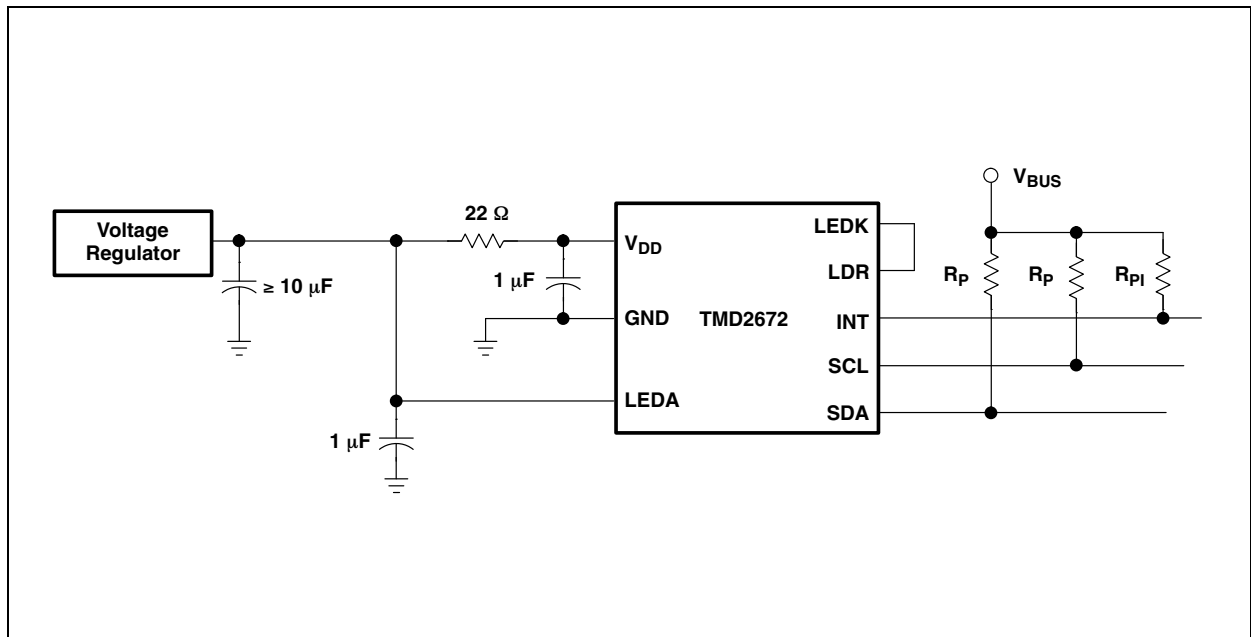
The first recommendation is to use two power supplies; one for the device  $V_{DD}$  and the other for the IR LED. In many systems, there is a quiet analog supply and a noisy digital supply. By connecting the quiet supply to the  $V_{DD}$  pin and the noisy supply to the LEDA pin, the key goal can be met. Place a  $1\mu\text{F}$  low-ESR decoupling capacitor as close as possible to the  $V_{DD}$  pin and another at the LEDA pin, and at least  $10\mu\text{F}$  of bulk capacitance to supply the 100mA current surge. This may be distributed as two  $4.7\mu\text{F}$  capacitors.

**Figure 41:**  
Proximity Sensing Using Separate Power Supplies



If it is not possible to provide two separate power supplies, the device can be operated from a single supply. A  $22\Omega$  resistor in series with the  $V_{DD}$  supply line and a  $1\mu\text{F}$  low ESR capacitor effectively filter any power supply noise. The previous capacitor placement considerations apply.

Figure 42:  
Proximity Sensing Using Single Power Supply



$V_{BUS}$  in the above figures refers to the I<sup>2</sup>C bus voltage which is either  $V_{DD}$  or 1.8V. Be sure to apply the specified I<sup>2</sup>C bus voltage shown in the [Ordering Information](#) table for the specific device being used.

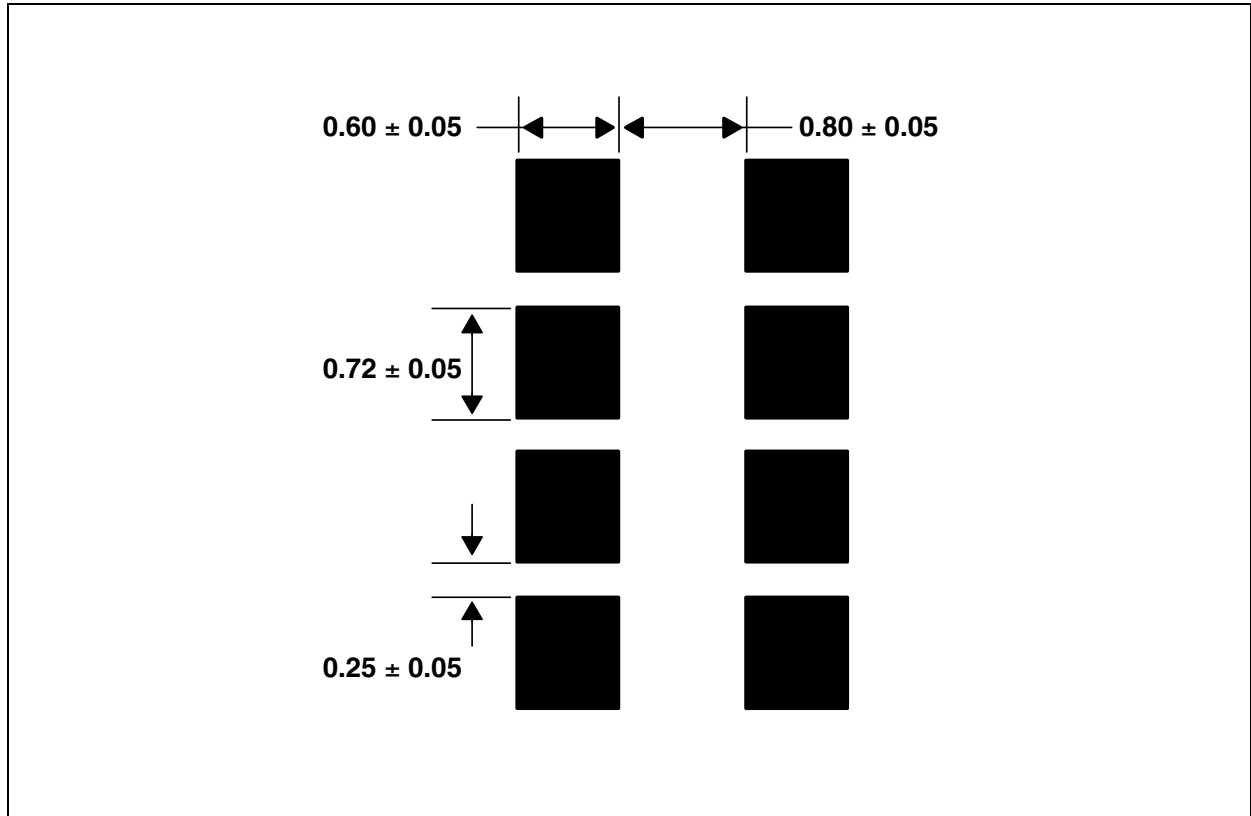
The I<sup>2</sup>C signals and the Interrupt are open-drain outputs and require pull-up resistors. The pull-up resistor ( $R_P$ ) value is a function of the I<sup>2</sup>C bus speed, the I<sup>2</sup>C bus voltage, and the capacitive load. The **ams** EVM running at 400kbps, uses 1.5k $\Omega$  resistors. A 10k $\Omega$  pull-up resistor ( $R_{PI}$ ) can be used for the interrupt line.



### PCB Pad Layout

Suggested PCB pad layout guidelines for the surface mount module are shown in [Figure 43](#). Flash Gold is recommended surface finish for the landing pads.

**Figure 43:**  
Suggested Module PCB Layout

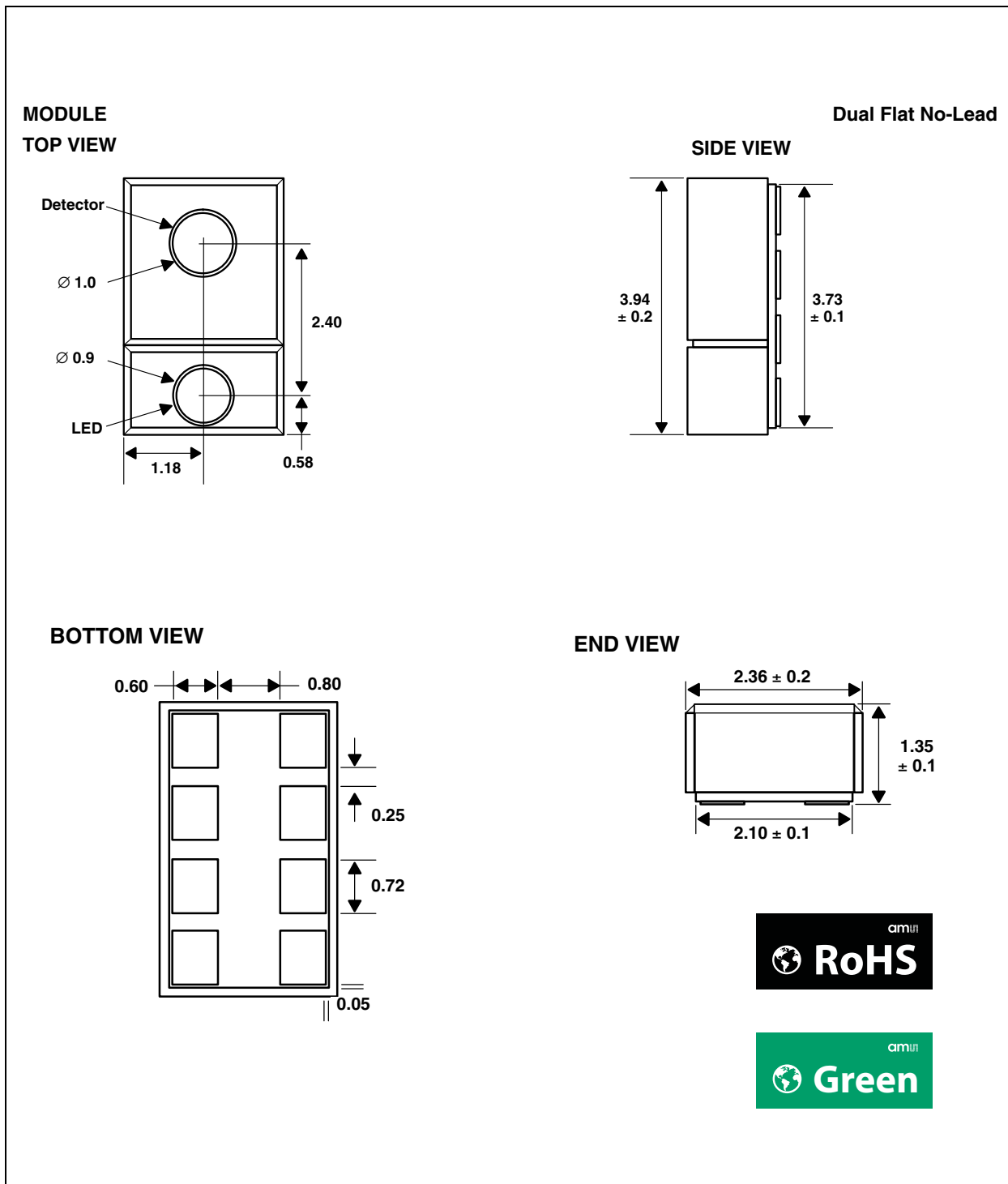


**Note(s) and/or Footnote(s):**

1. All linear dimensions are in mm.
2. This drawing is subject to change without notice.

### Package Information

Figure 44:  
Module Packaging Configuration

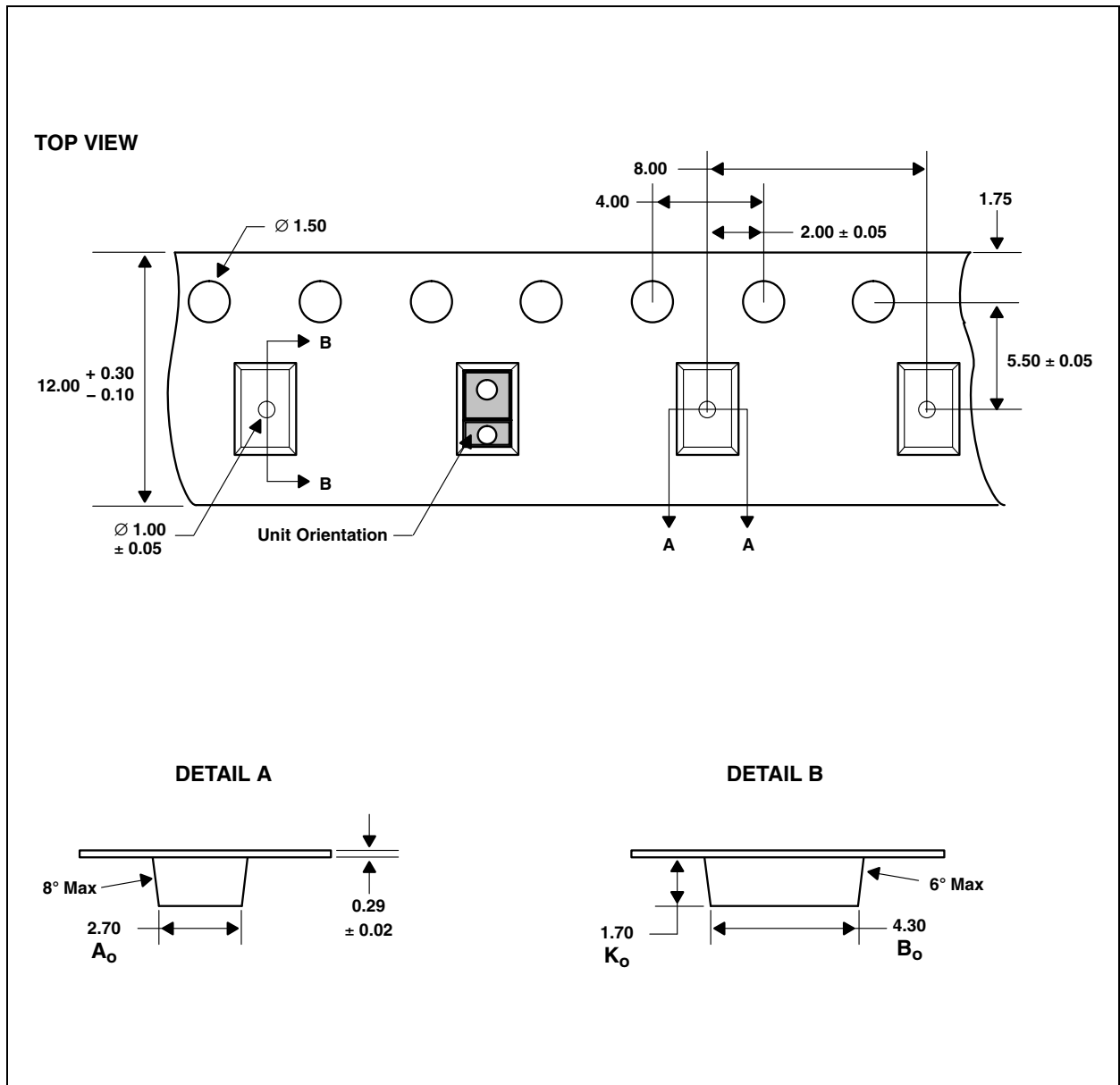


**Note(s) and/or Footnote(s):**

1. All linear dimensions are in millimeters. Dimension tolerance is ± 0.05mm unless otherwise noted.
2. Contacts are copper with NiPdAu plating.
3. This package contains no lead (Pb).
4. This drawing is subject to change without notice.

## Carrier Tape & Reel Information

**Figure 45:**  
Module Carrier Tape



**Note(s) and/or Footnote(s):**

1. All linear dimensions are in millimeters. Dimension tolerance is  $\pm 0.10$  mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing  $A_o$ ,  $B_o$ , and  $K_o$  are defined in ANSI EIA Standard 481-B 2001.
4. Each reel is 330 millimeters in diameter and contains 2500 parts.
5. **ams** packaging tape and reel conform to the requirements of EIA Standard 481-B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

## Soldering & Storage Information

### Soldering Information

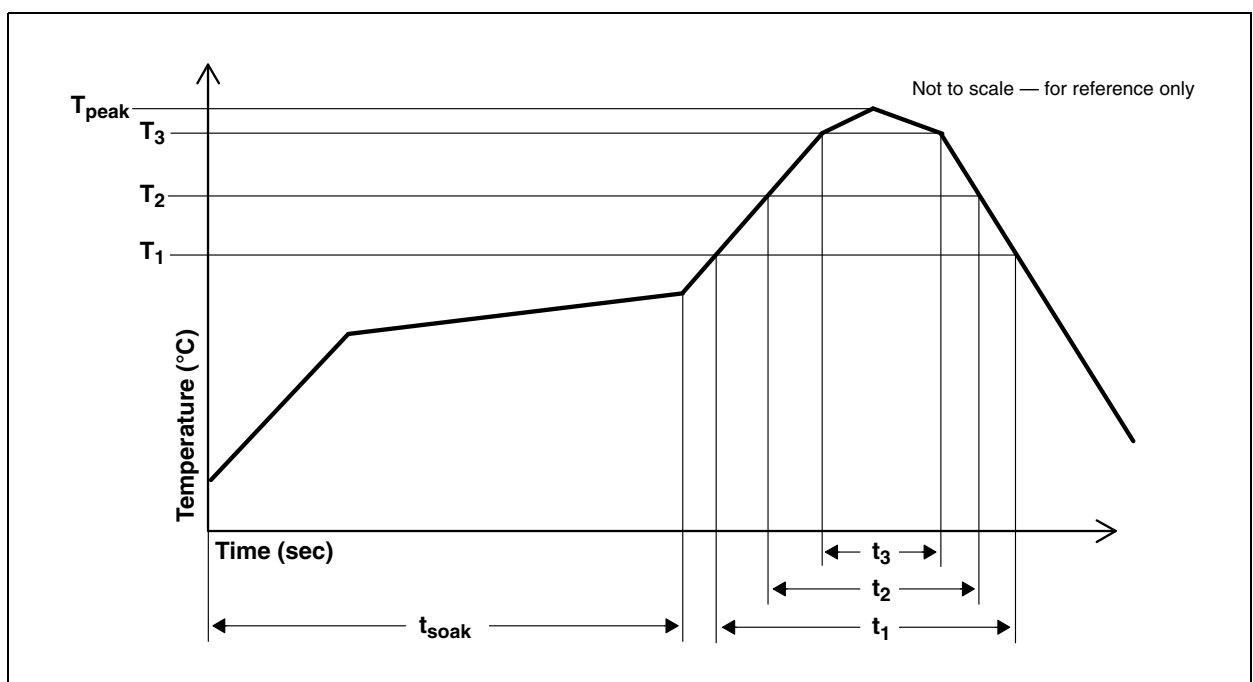
The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The process, equipment, and materials used in these test are detailed below.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

**Figure 46:**  
Solder Reflow Profile

| Parameter  | Reference  | Device         |
|--|------------|----------------|
| Average temperature gradient in preheating         |            | 2.5°C/sec      |
| Soak time  | $t_{soak}$ | 2 to 3 minutes |
| Time above 217°C ( $T_1$ )                         | $t_1$      | Max 60 sec     |
| Time above 230°C ( $T_2$ )                         | $t_2$      | Max 50 sec     |
| Time above $T_{peak} - 10^\circ\text{C}$ ( $T_3$ ) | $t_3$      | Max 10 sec     |
| Peak temperature in reflow                         | $T_{peak}$ | 260°C          |
| Temperature gradient in cooling                    |            | Max -5°C/sec   |

**Figure 47:**  
Solder Reflow Profile Graph



## Storage Information

### ***Moisture Sensitivity***

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is dry-baked prior to being packed for shipping. Devices are packed in a sealed aluminized envelope called a moisture barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

The Moisture Barrier Bags should be stored under the following conditions:

- Temperature Range: < 40°C
- Relative Humidity: < 90%
- Total Time: No longer than 12 months from the date code on the aluminized envelope if unopened.

Rebaking of the reel will be required if the devices have been stored unopened for more than 12 months and the Humidity Indicator Card shows the parts to be out of the allowable moisture region.

Opened reels should be used within 168 hours if exposed to the following conditions:

- Temperature Range: < 30°C
- Relative Humidity: < 60%

If rebaking is required, it should be done at 50°C for 12 hours.

The Module has been assigned a moisture sensitivity level of MSL 3.

## Ordering & Contact Information

Figure 48:  
Ordering Information

| Device                  | Address | Leads    | Interface Description                             | Ordering Number |
|-------------------------|---------|----------|---|-----------------|
| TMD26721                | 0x39    | Module-8 | I <sup>2</sup> C Vbus = V <sub>DD</sub> Interface | TMD26721        |
| TMD26723                | 0x39    | Module-8 | I <sup>2</sup> C Vbus = 1.8V Interface            | TMD26723        |
| TMD26725 <sup>(1)</sup> | 0x29    | Module-8 | I <sup>2</sup> C Vbus = V <sub>DD</sub> Interface | TMD26725        |
| TMD26727 <sup>(1)</sup> | 0x29    | Module-8 | I <sup>2</sup> C Vbus = 1.8V Interface            | TMD26727        |

**Note(s) and/or Footnote(s):**

1. Contact **ams** for availability.

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## Revision Information

| Changes from 149C (2012-Aug) to current revision 1-00 (2015-Mar-23)     | Page |
|---|------|
| Content of TAOS datasheet was converted to the latest <b>ams</b> design |      |

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision
2. Correction of typographical errors is not explicitly mentioned.

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