



PSMN5R6-100PS

N-channel 100 V 5.6 mΩ standard level MOSFET in TO220

30 November 2012

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in a TO-220 package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Improved dynamic avalanche performance
- Suitable for standard level gate drive sources

1.3 Applications

- DC-to-DC converters
- Load switching
- Motor control
- Server power supplies

1.4 Quick reference data

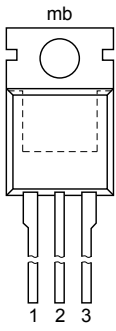
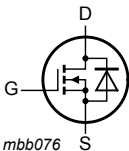
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$		-	-	100	V
I_D	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ Fig. 1	[1]	-	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Fig. 2		-	-	306	W
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ Fig. 11 ; Fig. 12		-	4.3	5.6	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 80\text{ A}; V_{DS} = 50\text{ V};$ Fig. 13 ; Fig. 14		-	43	-	nC
$Q_{G(tot)}$	total gate charge			-	141	-	nC
Avalanche Ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C}; I_D = 100\text{ A};$ $V_{sup} \leq 100\text{ V}; R_{GS} = 50\text{ Ω};$ unclamped		-	-	469	mJ

[1] Continuous current limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>TO-220AB (SOT78)</p>	 <p>mbb076</p>
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN5R6-100PS	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN5R6-100PS	PSMN5R6-100PS

5. Limiting values

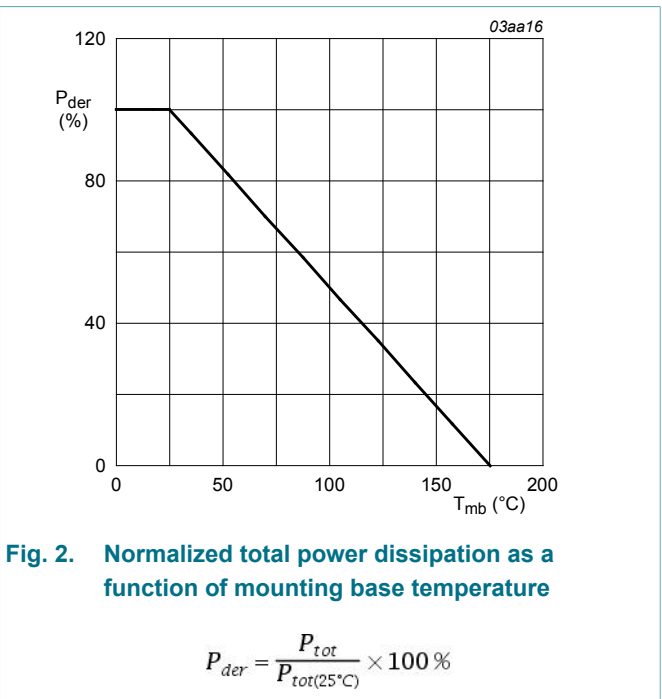
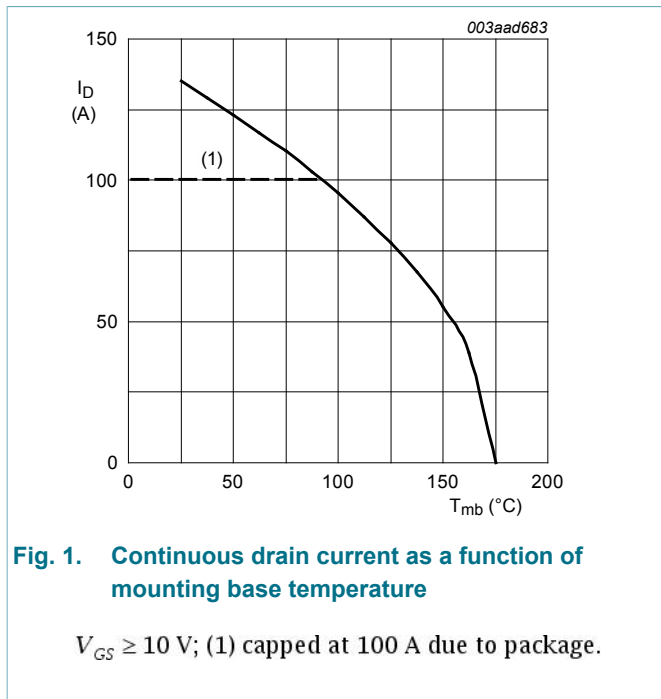
Table 5. Limiting values

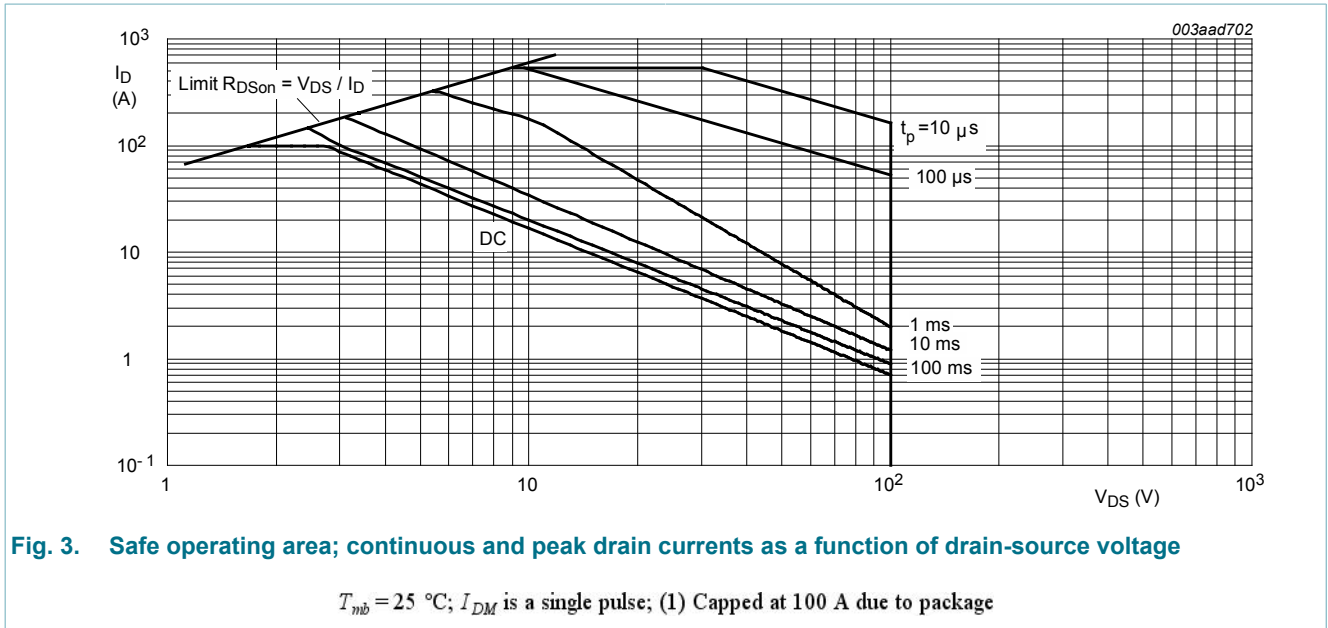
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_j = 100\text{ °C}$; Fig. 1	-	95	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 1	[1]	100	A

Symbol	Parameter	Conditions	Min	Max	Unit
I_{DM}	peak drain current	pulsed; $t_p \leq 10 \mu s$; $T_{mb} = 25 \text{ }^\circ\text{C}$; Fig. 3	-	539	A
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$; Fig. 2	-	306	W
T_{stg}	storage temperature		-55	175	$^\circ\text{C}$
T_j	junction temperature		-55	175	$^\circ\text{C}$
Source-drain diode					
I_S	source current	$T_{mb} = 25 \text{ }^\circ\text{C}$	[1]	100	A
I_{SM}	peak source current	pulsed; $t_p \leq 10 \mu s$; $T_{mb} = 25 \text{ }^\circ\text{C}$	-	539	A
Avalanche Ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; $I_D = 100 \text{ A}$; $V_{sup} \leq 100 \text{ V}$; $R_{GS} = 50 \text{ } \Omega$; unclamped	-	469	mJ

[1] Continuous current limited by package.

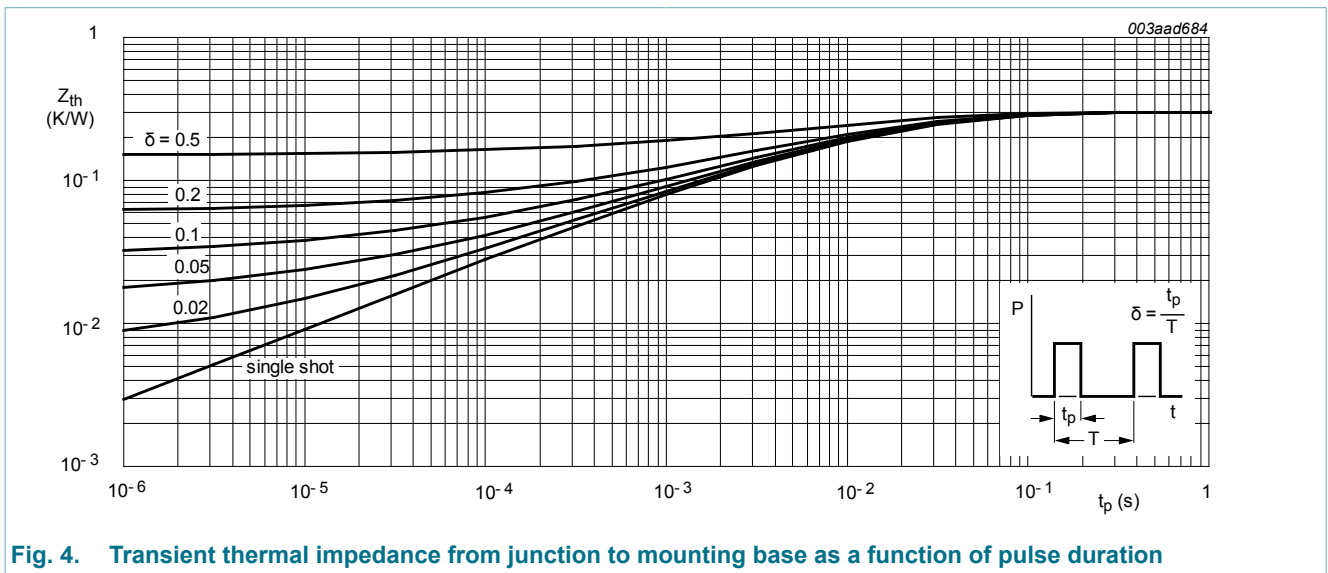




6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.3	0.49	K/W



7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	100	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 8 ; Fig. 9	2	3	4	V
V_{GSth}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 9	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ Fig. 9	-	-	4.6	V
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	10	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 10	-	-	15.7	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 11 ; Fig. 12	-	4.3	5.6	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	-	0.97	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 80 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 13 ; Fig. 14	-	141	-	nC
Q_{GS}	gate-source charge		-	36	-	nC
Q_{GD}	gate-drain charge		-	43	-	nC
C_{iss}	input capacitance	$V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ Fig. 15 ; Fig. 16	-	8061	-	pF
C_{oss}	output capacitance	$V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ Fig. 15	-	561	-	pF
C_{rSS}	reverse transfer capacitance	$V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ Fig. 15 ; Fig. 16	-	330	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50 \text{ V}; R_L = 0.6 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 1.5 \text{ } \Omega$	-	31	-	ns
t_r	rise time		-	46	-	ns
$t_{d(off)}$	turn-off delay time		-	83	-	ns
t_f	fall time		-	34	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 17	-	0.79	1.2	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rr}	reverse recovery time	$I_S = 25 \text{ A}$; $di_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$;	-	67	-	ns
Q_r	recovered charge	$V_{DS} = 50 \text{ V}$	-	182	-	nC

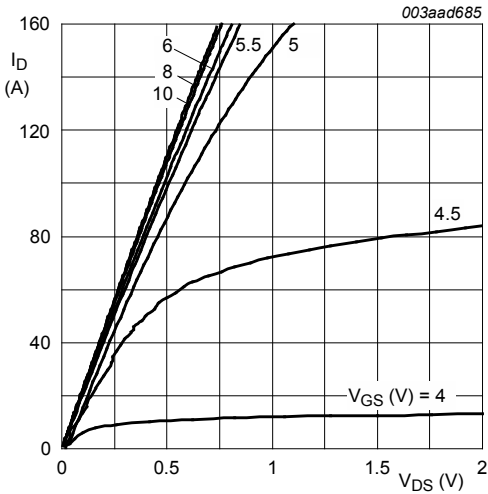


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25 \text{ }^\circ\text{C}$

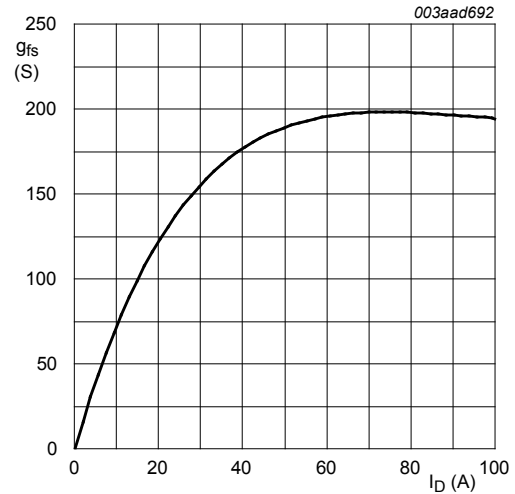


Fig. 6. Forward transconductance as a function of drain current; typical values

$T_j = 25 \text{ }^\circ\text{C}$; $V_{DS} = 25 \text{ V}$

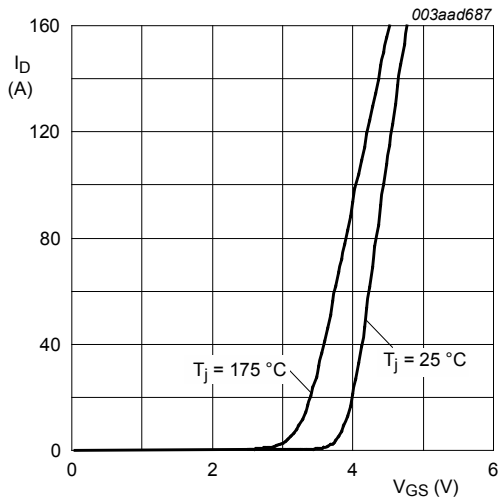


Fig. 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} > I_D \times R_{DS(on)}$

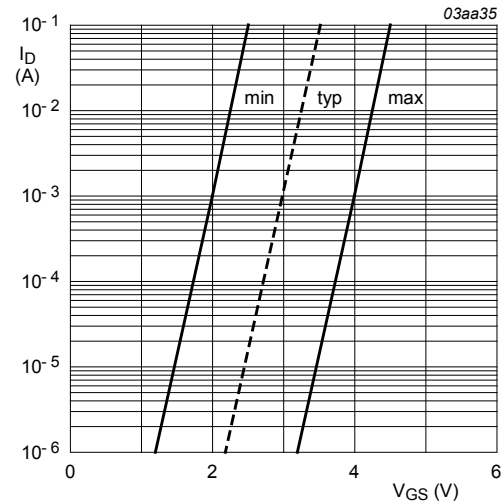


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25 \text{ }^\circ\text{C}$; $V_{DS} = 5 \text{ V}$

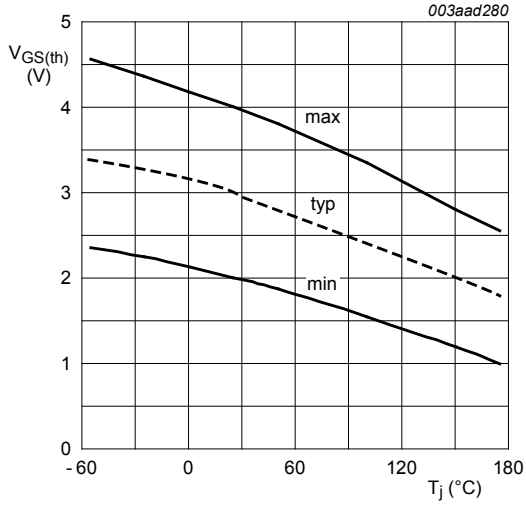


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

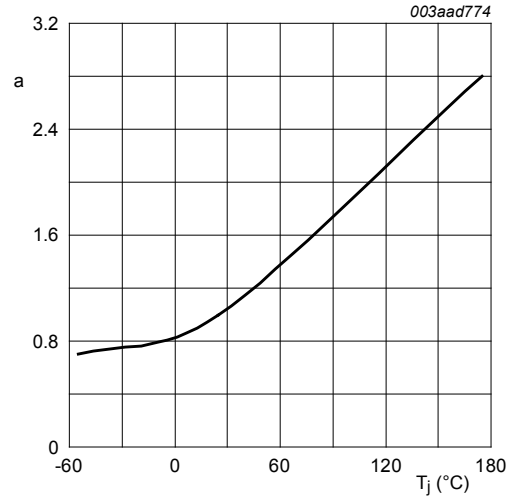


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

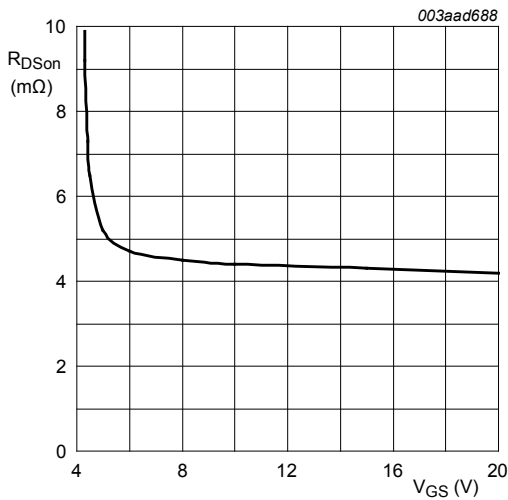


Fig. 11. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25^\circ\text{C}; I_D = 25 \text{ A}$$

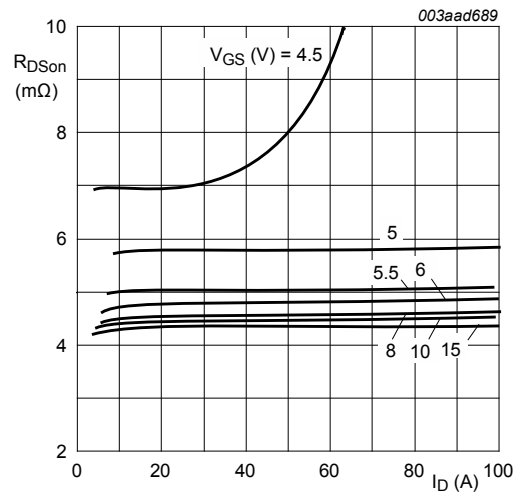


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

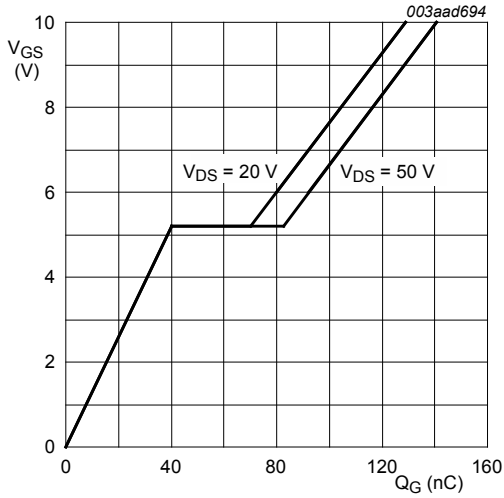


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$T_j = 25\text{ °C}; I_D = 25\text{ A}$



Fig. 14. Gate charge waveform definitions

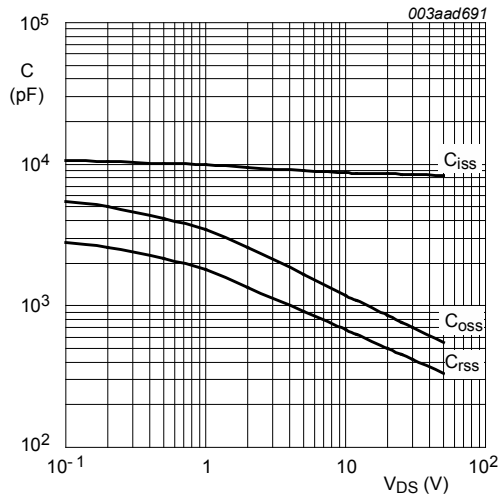


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

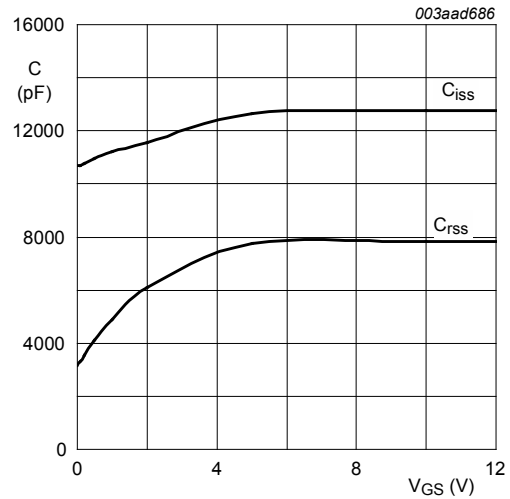


Fig. 16. Input and reverse transfer capacitances as a function of gate-source voltage, typical values

$f = 1\text{ MHz}; V_{DS} = 0\text{ V};$

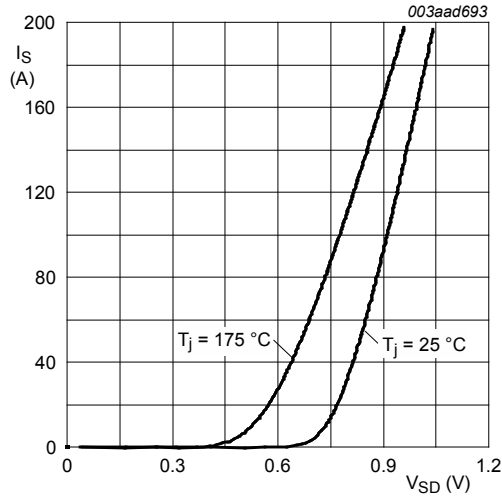


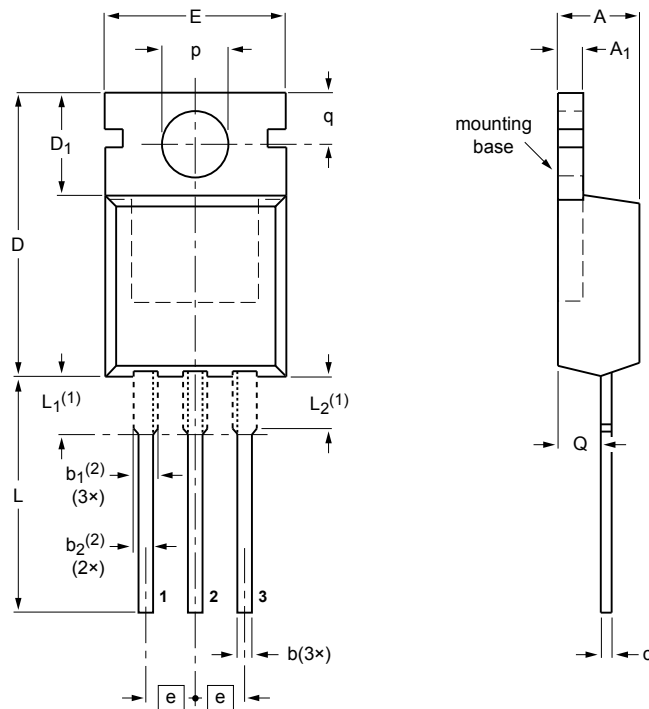
Fig. 17. Source current as a function of source-drain voltage; typical values

$$V_{GS} = 0 \text{ V}$$

8. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁ (2)	b ₂ (2)	c	D	D ₁	E	e	L	L ₁ (1)	L ₂ (1) max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

Notes

- 1. Lead shoulder designs may vary.
- 2. Dimension includes excess dambar.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT78		3-lead TO-220AB	SC-46		08-04-23 08-06-13

Fig. 18. Package outline TO-220AB (SOT78)

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 30 November 2012



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