



PIC12F510/16F506

Data Sheet

8/14-Pin, 8-Bit Flash Microcontrollers

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PIC12F510/16F506

8/14-Pin, 8-Bit Flash Microcontroller

Devices Included In This Data Sheet:

- PIC16F506
- PIC12F510

High-Performance RISC CPU:

- Only 33 Single-Word Instructions to Learn
- All Single-Cycle Instructions except for Program Branches, which are Two-Cycle
- 12-Bit Wide Instructions
- Two-Level Deep Hardware Stack
- Direct, Indirect and Relative Addressing modes for Data and Instructions
- 8-Bit Wide Data Path
- 10 Special Function Hardware Registers (PIC12F510)
- 13 Special Function Hardware Registers (PIC16F506)
- Operating Speed:
 - DC – 8 MHz Crystal Oscillator (PIC12F510)
 - DC – 500 ns instruction cycle (PIC12F510)
 - DC – 20 MHz Crystal Oscillator (PIC16F506)
 - DC – 200 ns instruction cycle (PIC16F506)

Special Microcontroller Features:

- 4 or 8 MHz Selectable Precision Internal Oscillator:
 - Factory calibrated to $\pm 1\%$
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Debugging (ICD) Support
- Power-on Reset (POR)
- Device Reset Timer (DRT):
 - Short DRT (1.125 ms, typical) for INTOSC, EXTRC and EC
 - DRT (18 ms, typical) for HS, XT and LP
- Watchdog Timer (WDT) with Dedicated On-Chip RC Oscillator for Reliable Operation
- Programmable Code Protection
- Multiplexed $\overline{\text{MCLR}}$ Input Pin
- Selectable Internal Weak Pull-Ups on I/O Pins
- Power-Saving Sleep mode
- Wake-up from Sleep on Pin Change
- Wake-up from Sleep on Comparator Change

Selectable Oscillator Options:

- INTOSC: 4/8 MHz precision Internal oscillator
- EXTRC: External low-cost RC oscillator
- XT: Standard crystal/resonator
- LP: Power-saving, low-frequency crystal
- HS: High-speed crystal/resonator (PIC16F506 only)
- EC: High-speed external clock input (PIC16F506 only)

Analog-to-Digital (A/D) Converter:

- 8-bit resolution
- 4-input channels (1 channel is dedicated to conversion of the internal 0.6V absolute voltage reference)
- High Current Sink/Source for Direct LED Drive
- 8-Bit Real-Time Clock/Counter (TMR0) with 8-Bit Programmable Prescaler

Low-Power Features/CMOS Technology:

- Operating Current:
 - < 175 μA @ 2V, 4 MHz, typical
- Standby Current:
 - 100 nA @ 2V, typical
- Low-Power, High-Speed Flash Technology:
 - 100,000 cycle Flash endurance
 - > 40-year retention
- Fully Static Design
- Wide Operating Voltage Range: 2.0V to 5.5V
- Wide Temperature Range:
 - Industrial: -40°C to +85°C
 - Extended: -40°C to +125°C

Peripheral Features (PIC12F510):

- 6 I/O Pins:
 - 5 I/O pins with individual direction control
 - 1 input only pin
- 1 Analog Comparator with Absolute Reference

Peripheral Features (PIC16F506):

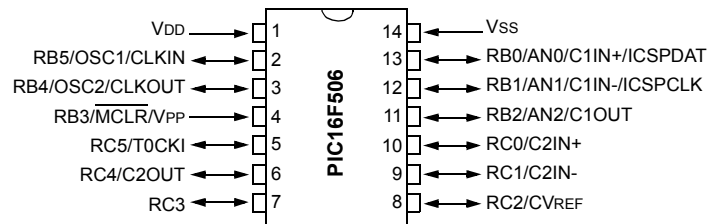
- 12 I/O Pins:
 - 11 I/O pins with individual direction control
 - 1 input only pin
- 2 Analog Comparators with Absolute Reference and Programmable Reference

PIC12F510/16F506

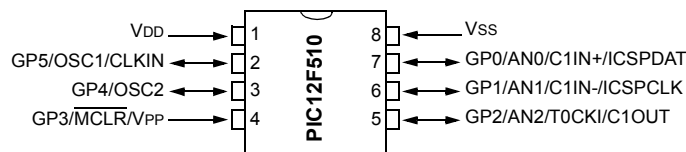
| Device | Program Memory | Data Memory | I/O | Timers 8-bit |
|-----------|----------------|--------------|-----|-----------------|
| | Flash (words) | SRAM (bytes) | | |
| PIC16F506 | 1024 | 67 | 12 | 1 |
| PIC12F510 | 1024 | 38 | 6 | 1 |

Pin Diagrams

PDIP, SOIC and TSSOP



PDIP, SOIC, MSOP



DFN

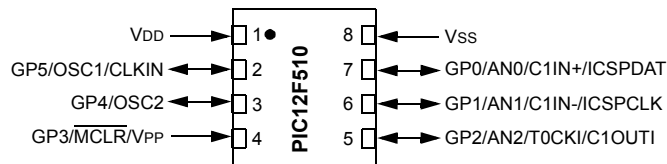


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PIC12F510/16F506

NOTES:

1.0 GENERAL DESCRIPTION

The PIC12F510/16F506 devices from Microchip Technology are low-cost, high-performance, 8-bit, fully-static, Flash-based CMOS microcontrollers. They employ a RISC architecture with only 33 single-word/single-cycle instructions. All instructions are single-cycle except for program branches, which take two cycles. The PIC12F510/16F506 devices deliver performance in an order of magnitude higher than their competitors in the same price category. The 12-bit wide instructions are highly symmetrical, resulting in a typical 2:1 code compression over other 8-bit microcontrollers in its class. The easy-to-use and easy-to-remember instruction set reduces development time significantly.

The PIC12F510/16F506 products are equipped with special features that reduce system cost and power requirements. The Power-on Reset (POR) and Device Reset Timer (DRT) eliminate the need for external Reset circuitry. There are four oscillator configurations to choose from (six on the PIC16F506), including INTOSC Internal Oscillator mode and the Power-Saving LP (Low-power) Oscillator mode. Power-Saving Sleep mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The PIC12F510/16F506 devices allow the customer to take full advantage of Microchip's price leadership in Flash programmable microcontrollers, while benefiting from the Flash programmable flexibility.

The PIC12F510/16F506 products are supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a 'C' compiler, a low-cost development programmer and a full featured programmer. All the tools are supported on IBM[®] PC and compatible machines.

1.1 Applications

The PIC12F510/16F506 devices fit in applications ranging from personal care appliances and security systems to low-power remote transmitters/receivers. The Flash technology makes customizing application programs (transmitter codes, appliance settings, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make these microcontrollers perfect for applications with space limitations. Low-cost, low-power, high-performance, ease-of-use and I/O flexibility make the PIC12F510/16F506 devices very versatile, even in areas where no microcontroller use has been considered before (e.g., timer functions, logic and PLDs in larger systems and coprocessor applications).

TABLE 1-1: PIC12F510/16F506 DEVICES

| | | PIC16F506 | PIC12F510 |
|-------------|--------------------------------------|--------------------------|-----------------------------|
| Clock | Maximum Frequency of Operation (MHz) | 20 | 8 |
| Memory | Flash Program Memory (words) | 1024 | 1024 |
| | Data Memory (bytes) | 67 | 38 |
| Peripherals | Timer Module(s) | TMR0 | TMR0 |
| | Wake-up from Sleep on Pin Change | Yes | Yes |
| Features | I/O Pins | 11 | 5 |
| | Input Only Pin | 1 | 1 |
| | Internal Pull-ups | Yes | Yes |
| | In-Circuit Serial Programming | Yes | Yes |
| | Number of Instructions | 33 | 33 |
| | Packages | 14-pin PDIP, SOIC, TSSOP | 8-pin PDIP, SOIC, MSOP, DFN |

The PIC12F510/16F506 devices have Power-on Reset, selectable Watchdog Timer, selectable code-protect, high I/O current capability and precision internal oscillator.

The PIC12F510/16F506 devices use serial programming with data pin RB0/GP0 and clock pin RB1/GP1.

PIC12F510/16F506

NOTES:

2.0 PIC12F510/16F506 DEVICE VARIETIES

A variety of packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC12F510/16F506 Product Identification System at the back of this data sheet to specify the correct part number.

2.1 Quick Turn Programming (QTP) Devices

Microchip offers a QTP programming service for factory production orders. This service is made available for users who choose not to program medium-to-high quantity units and whose code patterns have stabilized. The devices are identical to the Flash devices, but with all Flash locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

2.2 Serialized Quick Turn ProgrammingSM (SQTPSM) Devices

Microchip offers a unique programming service, where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number, which can serve as an entry code, password or ID number.

PIC12F510/16F506

NOTES:

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC12F510/16F506 devices can be attributed to a number of architectural features commonly found in RISC microprocessors. The PIC12F510/16F506 devices use a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architectures where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide, making it possible to have all single-word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (200 ns @ 20 MHz, 1 μ s @ 4 MHz) except for program branches.

Table 3-1 lists program memory (Flash) and data memory (RAM) for the PIC12F510/16F506 devices.

TABLE 3-1: PIC12F510/16F506 MEMORY

| Device | Memory | |
|-----------|-----------|--------|
| | Program | Data |
| PIC12F510 | 1024 x 12 | 38 x 8 |
| PIC16F506 | 1024 x 12 | 67 x 8 |

The PIC12F510/16F506 devices can directly or indirectly address its register files and data memory. All Special Function Registers (SFRs), including the PC, are mapped in the data memory. The PIC12F510/16F506 devices have a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation, on any register, using any addressing mode. This symmetrical nature and lack of “special optimal situations” make programming with the PIC12F510/16F506 devices simple, yet efficient. In addition, the learning curve is reduced significantly.

The PIC12F510/16F506 devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, one operand is typically the W (working) register. The other operand is either a file register or an immediate constant. In single-operand instructions, the operand is either the W register or a file register.

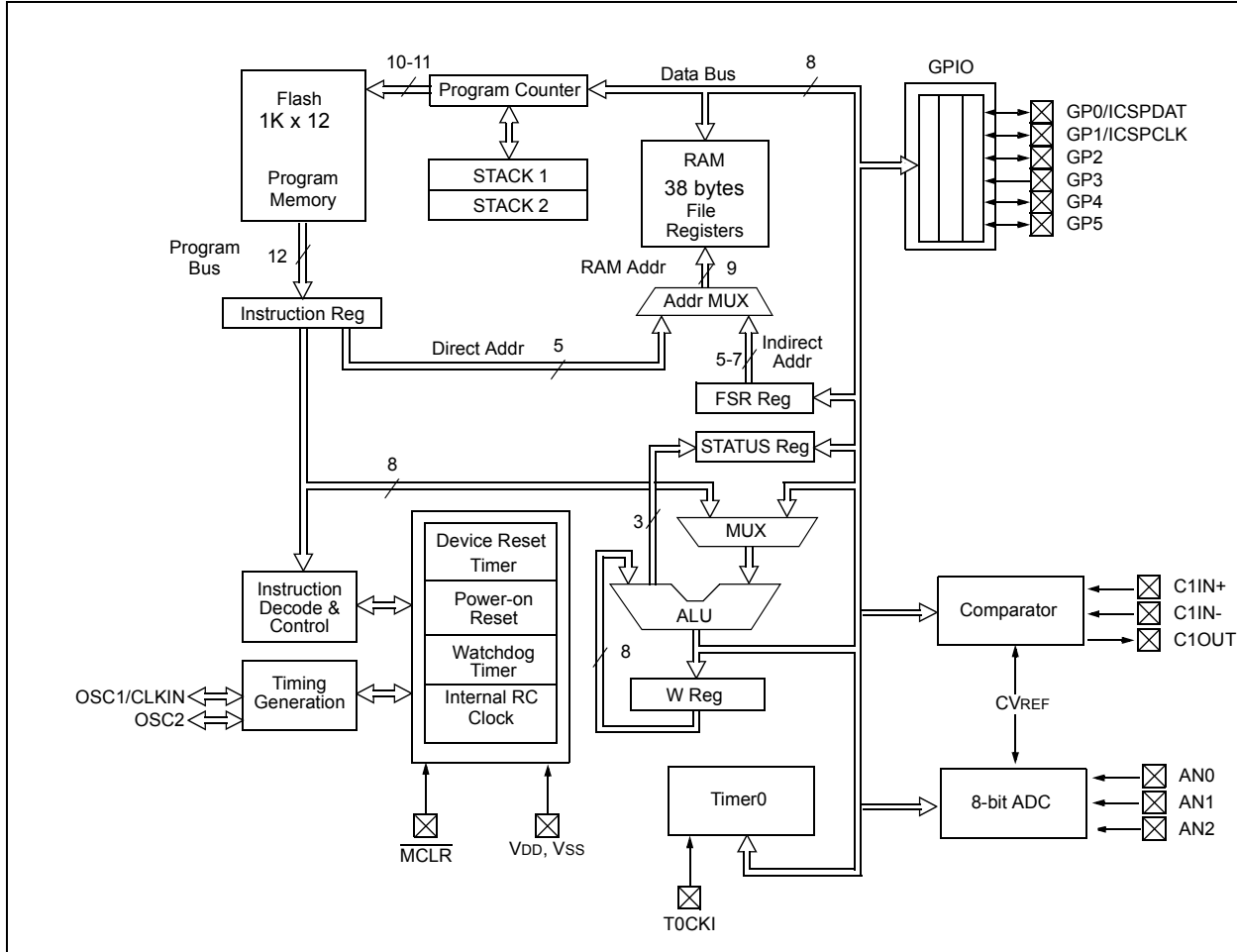
The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC) and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1 for PIC12F510 with the corresponding device pins described in Table 3-2. A simplified block diagram for PIC16F506 is shown in Figure 3-2 with the corresponding device pins described in Table 3-3.

PIC12F510/16F506

FIGURE 3-1: PIC12F510 SERIES BLOCK DIAGRAM



PIC12F510/16F506

TABLE 3-2: PIN DESCRIPTIONS – PIC12F510

| Name | I/O/P Type | Input Type | Output Type | Description |
|-----------------------|------------|------------|-------------|--|
| GP0/AN0/C1IN+/ICSPDAT | GP0 | TTL | CMOS | Bidirectional I/O port. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change. |
| | AN0 | AN | — | ADC channel input. |
| | C1IN+ | AN | — | Comparator input. |
| | ICSPDAT | ST | CMOS | In-Circuit Serial Programming data pin. |
| GP1/AN1/C1IN-/ICSPCLK | GP1 | TTL | CMOS | Bidirectional I/O port. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change. |
| | AN1 | AN | — | ADC channel input. |
| | C1IN- | AN | — | Comparator input. |
| | ICSPCLK | ST | — | In-Circuit Serial Programming clock pin. |
| GP2/AN2/T0CKI/C1OUT | GP2 | TTL | CMOS | Bidirectional I/O port. |
| | AN2 | AN | — | ADC channel input. |
| | T0CKI | ST | — | Timer0 clock input. |
| | C1OUT | — | CMOS | Comparator output. |
| GP3/MCLR/VPP | GP3 | TTL | — | Standard TTL input. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change. |
| | MCLR | ST | — | MCLR input – weak pull-up always enabled in this mode. |
| | VPP | HV | — | Programming Voltage input. |
| GP4/OSC2 | GP4 | TTL | CMOS | Bidirectional I/O port. |
| | OSC2 | — | XTAL | XTAL oscillator output pin. |
| GP5/OSC1/CLKIN | GP5 | TTL | CMOS | Bidirectional I/O port. |
| | OSC1 | XTAL | — | XTAL oscillator input pin. |
| | CLKIN | ST | — | EXTRC Schmitt Trigger input. |
| VDD | VDD | P | — | Positive supply for logic and I/O pins. |
| VSS | VSS | P | — | Ground reference for logic and I/O pins. |

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input, AN = Analog Voltage, HV = High Voltage

PIC12F510/16F506

FIGURE 3-2: PIC16F506 SERIES BLOCK DIAGRAM

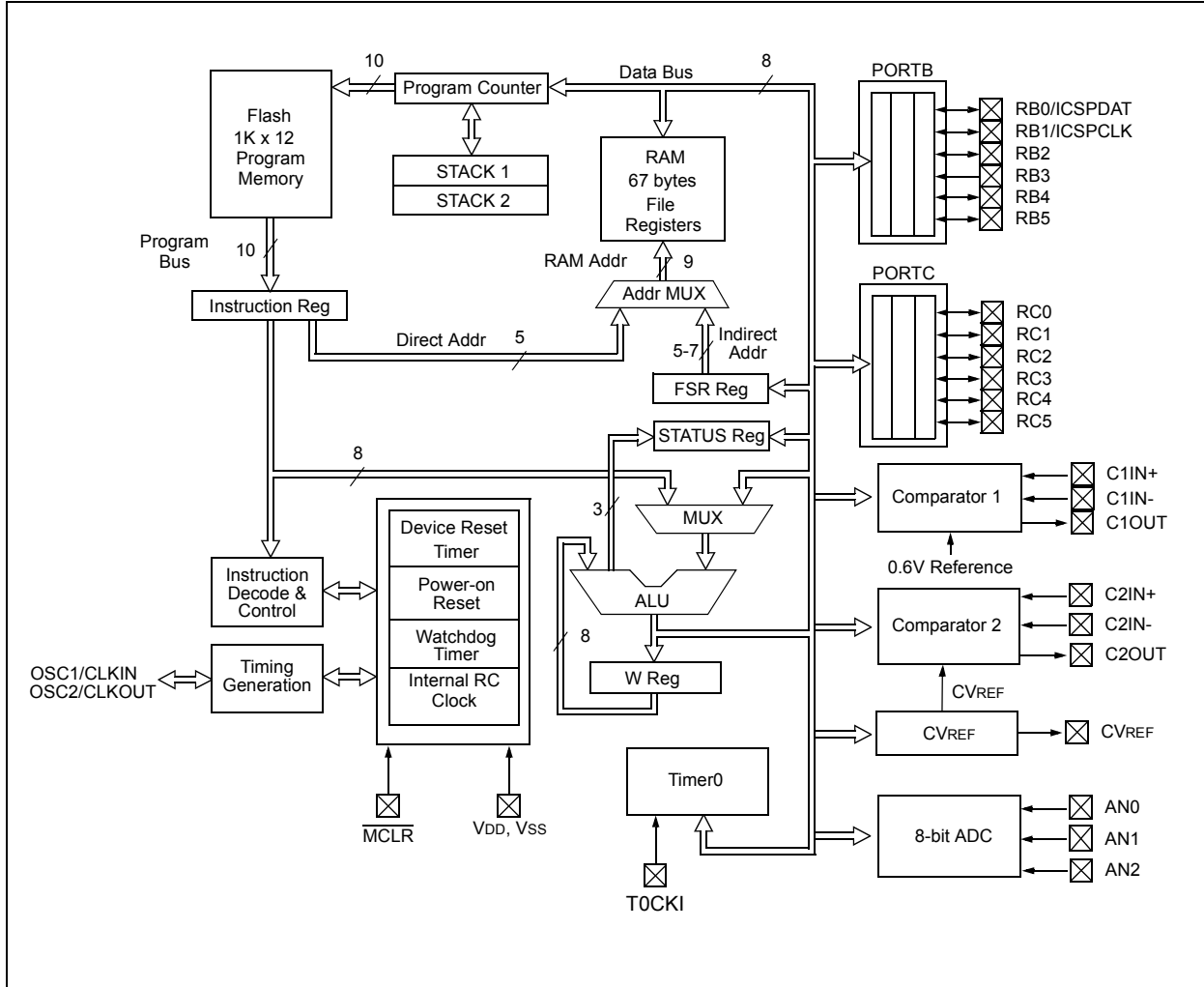


TABLE 3-3: PIN DESCRIPTIONS – PIC16F506

| Name | Function | Input Type | Output Type | Description |
|------------------------------------|--------------------------|------------|-------------|--|
| RB0/AN0/C1IN+/ICSPDAT | RB0 | TTL | CMOS | Bidirectional I/O port. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change. |
| | AN0 | AN | — | ADC channel input. |
| | C1IN+ | AN | — | Comparator 1 input. |
| | ICSPDAT | ST | CMOS | In-Circuit Serial Programming data pin. |
| RB1/AN1/C1IN-/ICSPCLK | RB1 | TTL | CMOS | Bidirectional I/O port. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change. |
| | AN1 | AN | — | ADC channel input. |
| | C1IN- | AN | — | Comparator 1 input. |
| | ICSPCLK | ST | — | In-Circuit Serial Programming clock pin. |
| RB2/AN2/C1OUT | RB2 | TTL | CMOS | Bidirectional I/O port. |
| | AN2 | AN | — | ADC channel input. |
| | C1OUT | — | CMOS | Comparator 1 output. |
| RB3/ $\overline{\text{MCLR}}$ /VPP | RB3 | TTL | — | Standard TTL input. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change. |
| | $\overline{\text{MCLR}}$ | ST | — | $\overline{\text{MCLR}}$ input – weak pull-up always enabled in this mode. |
| | VPP | HV | — | Programming voltage input. |
| RB4/OSC2/CLKOUT | RB4 | TTL | CMOS | Bidirectional I/O port. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change. |
| | OSC2 | — | XTAL | XTAL oscillator output pin. |
| | CLKOUT | — | CMOS | EXTRC/INTOSC CLKOUT pin ($F_{osc}/4$). |
| RB5/OSC1/CLKIN | RB5 | TTL | CMOS | Bidirectional I/O port. |
| | OSC1 | XTAL | — | XTAL oscillator input pin. |
| | CLKIN | ST | — | EXTRC/EC Schmitt Trigger input. |
| RC0/C2IN+ | RC0 | TTL | CMOS | Bidirectional I/O port. |
| | C2IN+ | AN | — | Comparator 2 input. |
| RC1/C2IN- | RC1 | TTL | CMOS | Bidirectional I/O port. |
| | C2IN- | AN | — | Comparator 2 input. |
| RC2/CVREF | RC2 | TTL | CMOS | Bidirectional I/O port. |
| | CVREF | — | AN | Programmable Voltage Reference output. |
| RC3 | RC3 | TTL | CMOS | Bidirectional I/O port. |
| RC4/C2OUT | RC4 | TTL | CMOS | Bidirectional I/O port. |
| | C2OUT | — | CMOS | Comparator 2 output. |
| RC5/T0CKI | RC5 | TTL | CMOS | Bidirectional I/O port. |
| | T0CKI | ST | — | Timer0 clock input. |
| VDD | VDD | P | — | Positive supply for logic and I/O pins. |
| VSS | VSS | P | — | Ground reference for logic and I/O pins. |

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input, AN = Analog Voltage, HV = High Voltage

PIC12F510/16F506

3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the PC is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-3 and Example 3-1.

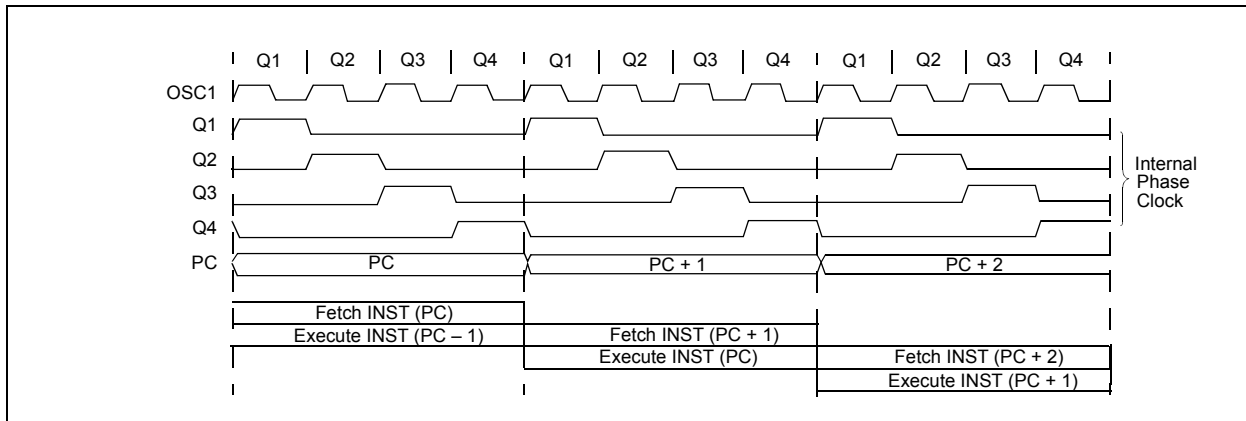
3.2 Instruction Flow/Pipelining

An instruction cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute take another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the PC to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 3-1).

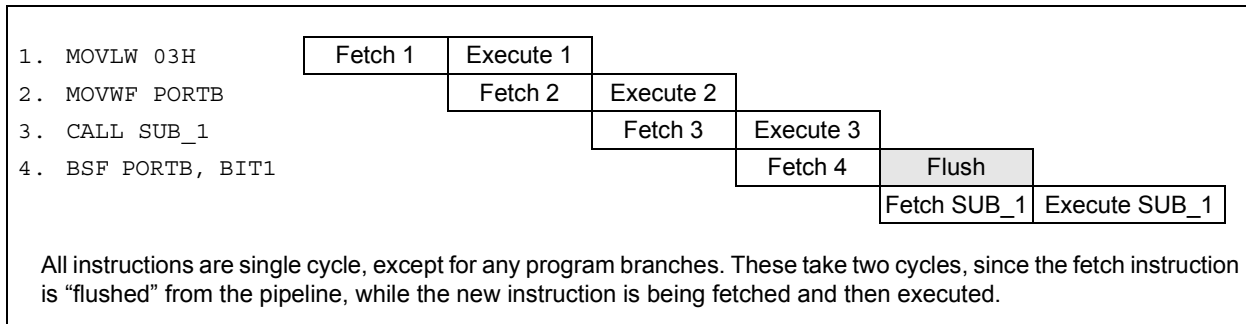
A fetch cycle begins with the PC incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-3: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



4.0 MEMORY ORGANIZATION

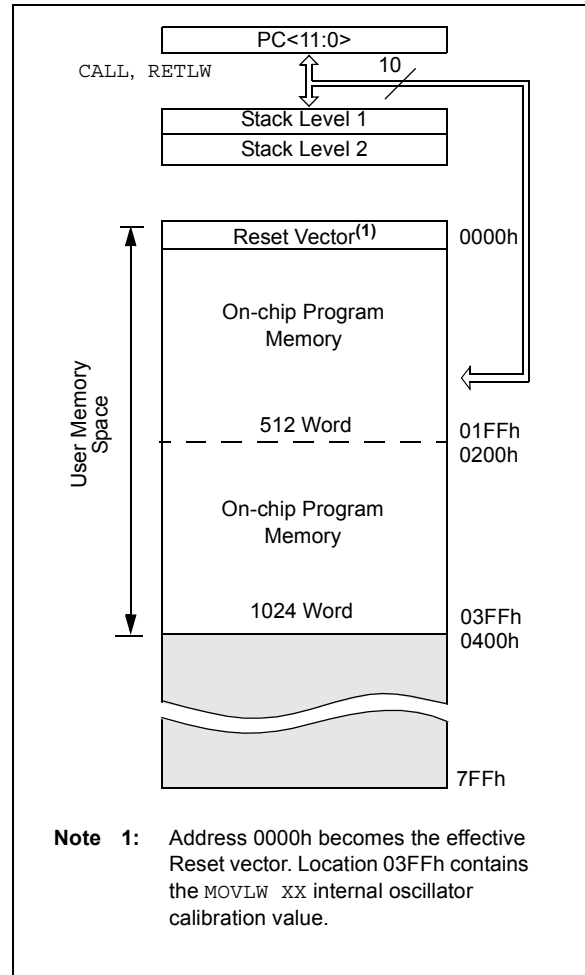
The PIC12F510/16F506 memories are organized into program memory and data memory. For devices with more than 512 bytes of program memory, a paging scheme is used. Program memory pages are accessed using STATUS register bit PA0. For the PIC12F510 and PIC16F506, with data memory register files of more than 32 registers, a banking scheme is used. Data memory banks are accessed using the File Select Register (FSR).

4.1 Program Memory Organization for the PIC12F510/16F506

The PIC12F510/16F506 devices have a 10-bit Program Counter (PC) capable of addressing a 2K x 12 program memory space.

Only the first 1K x 12 (0000h-03FFh) are physically implemented (see Figure 4-1). Accessing a location above these boundaries will cause a wraparound within the 1K x 12 space. The effective Reset vector is a 0000h (see Figure 4-1). Location 03FFh contains the internal clock oscillator calibration value. This value should never be overwritten.

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC12F510/16F506



PIC12F510/16F506

4.2 Data Memory Organization

Data memory is composed of registers or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: Special Function Registers (SFRs) and General Purpose Registers (GPRs).

The Special Function Registers include the TMR0 register, the Program Counter (PCL), the STATUS register, the I/O registers (ports) and the File Select Register (FSR). In addition, Special Function Registers are used to control the I/O port configuration and prescaler options.

The General Purpose Registers are used for data and control information under command of the instructions.

For the PIC12F510, the register file is composed of 10 Special Function Registers, 6 General Purpose Registers and 32 General Purpose Registers accessed by banking (see Figure 4-2).

For the PIC16F506, the register file is composed of 13 Special Function Registers, 3 General Purpose Registers and 64 General Purpose Registers, accessed by banking (see Figure 4-3).

4.2.1 GENERAL PURPOSE REGISTER FILE

The General Purpose Register file is accessed either directly or indirectly through the File Select Register (FSR). See Section 4.8 "Indirect Data Addressing: INDF and FSR Registers".

FIGURE 4-2: PIC12F510 REGISTER FILE MAP

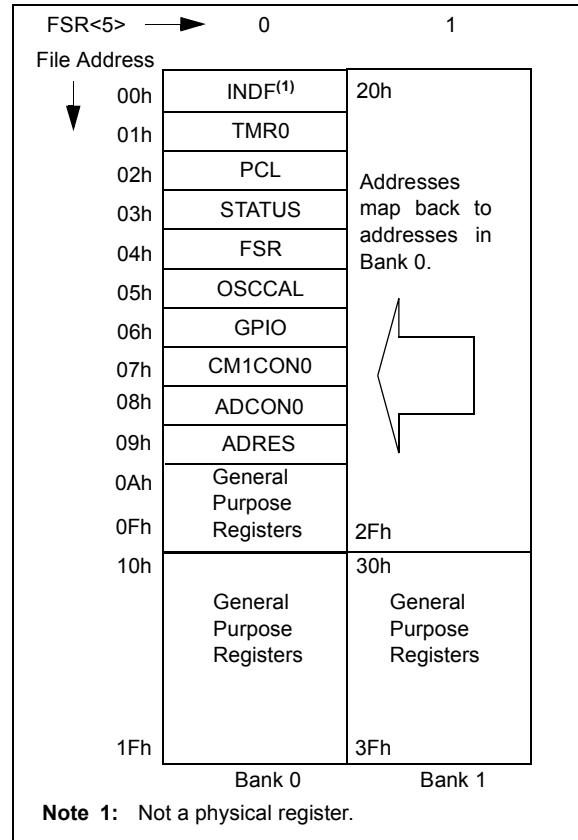
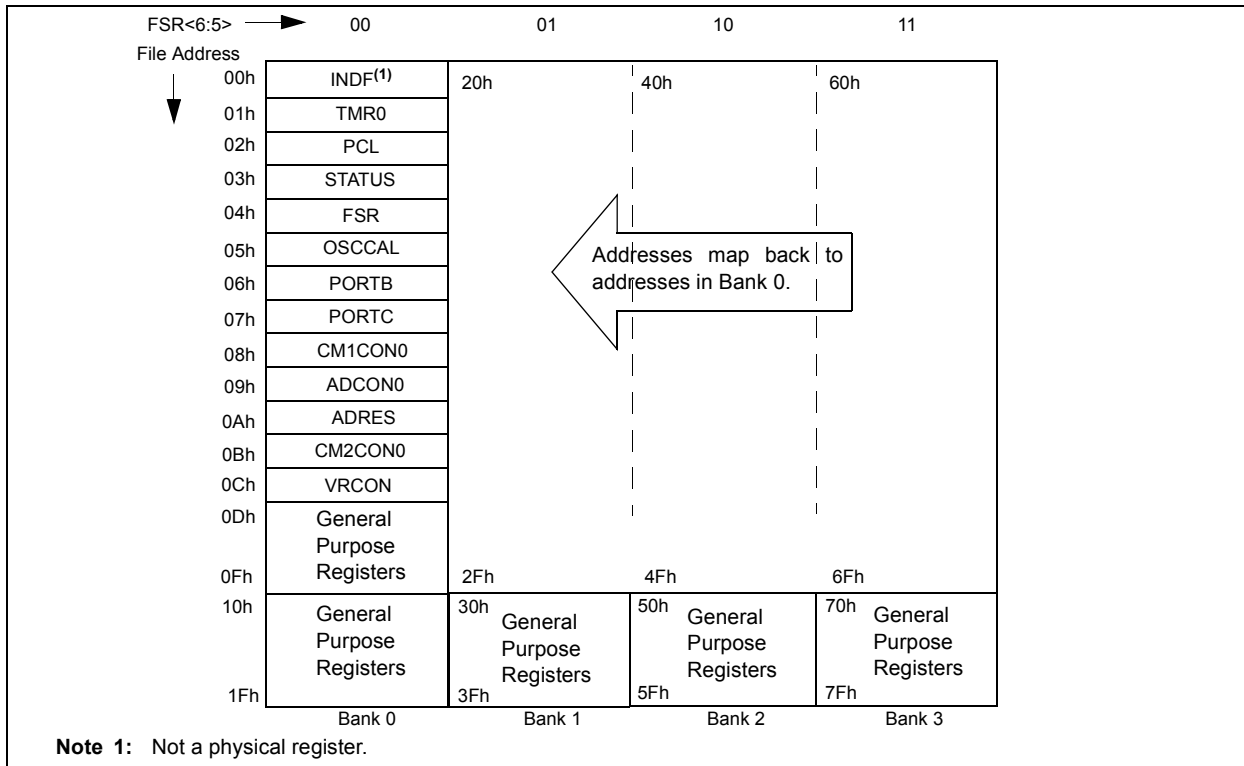


FIGURE 4-3: PIC16F506 REGISTER FILE MAP



4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions to control the operation of the device (see Table 4-1).

The Special Function Registers can be classified into two sets. The Special Function Registers associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTER SUMMARY – PIC12F510

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-on Reset |
|--------------------|---------|---|----------------------|-------|---------------------|-----------------|--------|----------------------|-------------------|-------------------------|
| N/A | TRIS | I/O Control Registers (TRISGPIO) | | | | | | | | --11 1111 |
| N/A | OPTION | Contains control bits to configure Timer0 and Timer0/WDT Prescaler | | | | | | | | 1111 1111 |
| 00h | INDF | Uses contents of FSR to address data memory (not a physical register) | | | | | | | | xxxx xxxx |
| 01h | TMR0 | Timer0 Module Register | | | | | | | | xxxx xxxx |
| 02h ⁽¹⁾ | PCL | Low Order 8 bits of PC | | | | | | | | 1111 1111 |
| 03h | STATUS | GPWUF | CWUF | PA0 | \overline{TO} | \overline{PD} | Z | DC | C | 0001 1xxx |
| 04h | FSR | Indirect Data Memory Address Pointer | | | | | | | | 110x xxxx |
| 05h | OSCCAL | CAL6 | CAL5 | CAL4 | CAL3 | CAL2 | CAL1 | CAL0 | — | 1111 111- |
| 06h | GPIO | — | — | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | --xx xxxx |
| 07h | CM1CON0 | C1OUT | $\overline{C1OUTEN}$ | C1POL | $\overline{C1T0CS}$ | C1ON | C1NREF | C1PREF | $\overline{C1WU}$ | 1111 1111 |
| 08h | ADCON0 | ANS1 | ANS0 | ADCS1 | ADCS0 | CHS1 | CHS0 | $\overline{GO/DONE}$ | ADON | 1111 1100 |
| 09h | ADRES | ADC Conversion Result | | | | | | | | xxxx xxxx |

Legend: x = unknown, u = unchanged, – = unimplemented, read as ‘0’ (if applicable). Shaded cells = unimplemented or unused.

Note 1: The upper byte of the Program Counter is not directly accessible. See **Section 4.6 “Program Counter”** for an explanation of how to access these bits.

PIC12F510/16F506

TABLE 4-2: SPECIAL FUNCTION REGISTER SUMMARY – PIC16F506

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-on Reset |
|--------------------|---------|---|----------------------|-------|---------------------|-----------------|--------|---------|-------------------|-------------------------|
| N/A | TRIS | I/O Control Registers (TRISB, TRISC) | | | | | | | | --11 1111 |
| N/A | OPTION | Contains control bits to configure Timer0 and Timer0/WDT Prescaler | | | | | | | | 1111 1111 |
| 00h | INDF | Uses contents of FSR to address data memory (not a physical register) | | | | | | | | xxxx xxxx |
| 01h | TMR0 | Timer0 Module Register | | | | | | | | xxxx xxxx |
| 02h ⁽¹⁾ | PCL | Low Order 8 bits of PC | | | | | | | | 1111 1111 |
| 03h | STATUS | RBWUF | CWUF | PA0 | \overline{TO} | \overline{PD} | Z | DC | C | 0001 1xxx |
| 04h | FSR | Indirect Data Memory Address Pointer | | | | | | | | 100x xxxx |
| 05h | OSCCAL | CAL6 | CAL5 | CAL4 | CAL3 | CAL2 | CAL1 | CAL0 | — | 1111 111- |
| 06h | PORTB | — | — | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | --xx xxxx |
| 07h | PORTC | — | — | RC5 | RC4 | RC3 | RC2 | RC1 | RC0 | --xx xxxx |
| 08h | CM1CON0 | C1OUT | $\overline{C1OUTEN}$ | C1POL | $\overline{C1T0CS}$ | C1ON | C1NREF | C1PREF | $\overline{C1WU}$ | 1111 1111 |
| 09h | ADCON0 | ANS1 | ANS0 | ADCS1 | ADCS0 | CHS1 | CHS0 | GO/DONE | ADON | 1111 1100 |
| 0Ah | ADRES | ADC Conversion Result | | | | | | | | xxxx xxxx |
| 0Bh | CM2CON0 | C2OUT | $\overline{C2OUTEN}$ | C2POL | C2PREF2 | C2ON | C2NREF | C2PREF1 | $\overline{C2WU}$ | 1111 1111 |
| 0Ch | VRCON | VREN | VROE | VRR | — ⁽²⁾ | VR3 | VR2 | VR1 | VR0 | 0011 1111 |

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0' (if applicable). Shaded cells = unimplemented or unused.

Note 1: The upper byte of the Program Counter is not directly accessible. See **Section 4.6 “Program Counter”** for an explanation of how to access these bits.

2: Unimplemented bit VRCON<4> read as '1'.

4.3 STATUS Register

This register contains the arithmetic status of the ALU, the Reset status and the page preselect bit.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the \overline{TO} and \overline{PD} bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS`, will clear the upper three bits and set the Z bit. This leaves the STATUS register as 000u u1uu (where u = unchanged).

Therefore, it is recommended that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS register. These instructions do not affect the Z, DC or C bits from the STATUS register. For other instructions which do affect Status bits, see **Section 11.0 “Instruction Set Summary”**.

REGISTER 4-1: STATUS: STATUS REGISTER (PIC12F510)

| | | | | | | | |
|-------|-------|-------|-----------------|-----------------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R-1 | R-1 | R/W-x | R/W-x | R/W-x |
| GPWUF | CWUF | PA0 | \overline{TO} | \overline{PD} | Z | DC | C |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

| | | | | | | | | | | |
|---------------------------|---|--|---------------|--------------------|----------------------|----------------------------|--|---------------------------|-----------------------|--|
| bit 7 | <p>GPWUF: GPIO Reset bit</p> <p>1 = Reset due to wake-up from Sleep on pin change</p> <p>0 = After power-up or other Reset</p> | | | | | | | | | |
| bit 6 | <p>CWUF: Comparator Reset bit</p> <p>1 = Reset due to wake-up from Sleep on comparator change</p> <p>0 = After power-up or other Reset</p> | | | | | | | | | |
| bit 5 | <p>PA0: Program Page Preselect bit</p> <p>1 = Page 1 (200h-3FFh)</p> <p>0 = Page 0 (000h-1FFh)</p> <p>Each page is 512 bytes.</p> <p>Using the PA0 bit as a general purpose read/write bit in devices which do not use it for program page preselect is not recommended, since this may affect upward compatibility with future products.</p> | | | | | | | | | |
| bit 4 | <p>\overline{TO}: Time-Out bit</p> <p>1 = After power-up, CLRWDT instruction, or SLEEP instruction</p> <p>0 = A WDT time-out occurred</p> | | | | | | | | | |
| bit 3 | <p>\overline{PD}: Power-Down bit</p> <p>1 = After power-up or by the CLRWDT instruction</p> <p>0 = By execution of the SLEEP instruction</p> | | | | | | | | | |
| bit 2 | <p>Z: Zero bit</p> <p>1 = The result of an arithmetic or logic operation is zero</p> <p>0 = The result of an arithmetic or logic operation is not zero</p> | | | | | | | | | |
| bit 1 | <p>DC: Digit Carry/Borrow bit (for ADDWF and SUBWF instructions)</p> <p><u>ADDWF:</u></p> <p>1 = A carry from the 4th low-order bit of the result occurred</p> <p>0 = A carry from the 4th low-order bit of the result did not occur</p> <p><u>SUBWF:</u></p> <p>1 = A borrow from the 4th low-order bit of the result did not occur</p> <p>0 = A borrow from the 4th low-order bit of the result occurred</p> | | | | | | | | | |
| bit 0 | <p>C: Carry/Borrow bit (for ADDWF, SUBWF and RRF, RLF instructions)</p> <table> <tr> <td><u>ADDWF:</u></td> <td><u>SUBWF:</u></td> <td><u>RRF or RLF:</u></td> </tr> <tr> <td>1 = A carry occurred</td> <td>1 = A borrow did not occur</td> <td>Load bit with LSB or MSb, respectively</td> </tr> <tr> <td>0 = A carry did not occur</td> <td>0 = A borrow occurred</td> <td></td> </tr> </table> | <u>ADDWF:</u> | <u>SUBWF:</u> | <u>RRF or RLF:</u> | 1 = A carry occurred | 1 = A borrow did not occur | Load bit with LSB or MSb, respectively | 0 = A carry did not occur | 0 = A borrow occurred | |
| <u>ADDWF:</u> | <u>SUBWF:</u> | <u>RRF or RLF:</u> | | | | | | | | |
| 1 = A carry occurred | 1 = A borrow did not occur | Load bit with LSB or MSb, respectively | | | | | | | | |
| 0 = A carry did not occur | 0 = A borrow occurred | | | | | | | | | |

PIC12F510/16F506

REGISTER 4-2: STATUS: STATUS REGISTER (PIC16F506)

| | | | | | | | |
|-------|-------|-------|-----------------|-----------------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R-1 | R-1 | R/W-x | R/W-x | R/W-x |
| RBWUF | CWUF | PA0 | \overline{TO} | \overline{PD} | Z | DC | C |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

- bit 7 **RBWUF**: PORTB Reset bit
 1 = Reset due to wake-up from Sleep on pin change
 0 = After power-up or other Reset
- bit 6 **CWUF**: Comparator Reset bit
 1 = Reset due to wake-up from Sleep on comparator change
 0 = After power-up or other Reset
- bit 5 **PA0**: Program Page Preselect bit
 1 = Page 1 (200h-3FFh)
 0 = Page 0 (000h-1FFh)
 Each page is 512 bytes.
 Using the PA0 bit as a general purpose read/write bit in devices which do not use it for program page preselect is not recommended, since this may affect upward compatibility with future products.
- bit 4 **\overline{TO}** : Time-Out bit
 1 = After power-up, *CLRWDT* instruction, or *SLEEP* instruction
 0 = A WDT time-out occurred
- bit 3 **\overline{PD}** : Power-Down bit
 1 = After power-up or by the *CLRWDT* instruction
 0 = By execution of the *SLEEP* instruction
- bit 2 **Z**: Zero bit
 1 = The result of an arithmetic or logic operation is zero
 0 = The result of an arithmetic or logic operation is not zero
- bit 1 **DC**: Digit Carry/Borrow bit (for *ADDWF* and *SUBWF* instructions)
ADDWF :
 1 = A carry from the 4th low-order bit of the result occurred
 0 = A carry from the 4th low-order bit of the result did not occur
SUBWF :
 1 = A borrow from the 4th low-order bit of the result did not occur
 0 = A borrow from the 4th low-order bit of the result occurred
- bit 0 **C**: Carry/Borrow bit (for *ADDWF*, *SUBWF* and *RRF*, *RLF* instructions)
ADDWF : SUBWF : RRF or RLF :
 1 = A carry occurred 1 = A borrow did not occur Load bit with LSb or MSb, respectively
 0 = A carry did not occur 0 = A borrow occurred

4.4 OPTION Register

The OPTION register is a 8-bit wide, write-only register, that contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the OPTION instruction, the contents of the W register will be transferred to the OPTION register. A Reset sets the OPTION<7:0> bits.

Note 1: If TRIS bit is set to '0', the wake-up on change and pull-up functions are disabled for that pin (i.e., note that TRIS overrides Option control of GPPU/RBPU and GPWU/RBWU).

2: If the T0CS bit is set to '1', it will override the TRIS function on the T0CKI pin.

REGISTER 4-3: OPTION_REG: OPTION REGISTER (PIC12F510)

| | | | | | | | |
|-------|------|------|------|-----|-----|-----|-------|
| W-1 | W-1 | W-1 | W-1 | W-1 | W-1 | W-1 | W-1 |
| GPWU | GPPU | T0CS | T0SE | PSA | PS2 | PS1 | PS0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared

x = Bit is unknown

bit 7 **GPWU:** Enable Wake-up On Pin Change bit (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 6 **GPPU:** Enable Weak Pull-Ups bit (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 5 **T0CS:** Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

| Bit Value | Timer0 Rate | WDT Rate |
|-----------|-------------|----------|
| 000 | 1 : 2 | 1 : 1 |
| 001 | 1 : 4 | 1 : 2 |
| 010 | 1 : 8 | 1 : 4 |
| 011 | 1 : 16 | 1 : 8 |
| 100 | 1 : 32 | 1 : 16 |
| 101 | 1 : 64 | 1 : 32 |
| 110 | 1 : 128 | 1 : 64 |
| 111 | 1 : 256 | 1 : 128 |

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REGISTER 4-4: OPTION_REG: OPTION REGISTER (PIC16F506)

| | | | | | | | |
|--------------------------|--------------------------|------|------|-----|-----|-----|-------|
| W-1 | W-1 | W-1 | W-1 | W-1 | W-1 | W-1 | W-1 |
| $\overline{\text{RBWU}}$ | $\overline{\text{RBPU}}$ | T0CS | T0SE | PSA | PS2 | PS1 | PS0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 **$\overline{\text{RBWU}}$** : Enable Wake-up On Pin Change bit (RB0, RB1, RB3, RB4)

1 = Disabled
 0 = Enabled

bit 6 **$\overline{\text{RBPU}}$** : Enable Weak Pull-Ups bit (RB0, RB1, RB3, RB4)

1 = Disabled
 0 = Enabled

bit 5 **T0CS**: Timer0 Clock Source Select bit

1 = Transition on T0CKI pin
 0 = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE**: Timer0 Source Edge Select bit

1 = Increment on high-to-low transition on T0CKI pin
 0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA**: Prescaler Assignment bit

1 = Prescaler assigned to the WDT
 0 = Prescaler assigned to Timer0

bit 2-0 **PS<2:0>**: Prescaler Rate Select bits

| Bit Value | Timer0 Rate | WDT Rate |
|-----------|-------------|----------|
| 000 | 1 : 2 | 1 : 1 |
| 001 | 1 : 4 | 1 : 2 |
| 010 | 1 : 8 | 1 : 4 |
| 011 | 1 : 16 | 1 : 8 |
| 100 | 1 : 32 | 1 : 16 |
| 101 | 1 : 64 | 1 : 32 |
| 110 | 1 : 128 | 1 : 64 |
| 111 | 1 : 256 | 1 : 128 |

4.5 OSCCAL Register

The Oscillator Calibration (OSCCAL) register is used to calibrate the internal precision 4/8 MHz oscillator. It contains seven bits for calibration.

Note: Erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be read prior to erasing the part so it can be reprogrammed correctly later.

After you move in the calibration constant, do not change the value. See **Section 10.2.5 “Internal 4/8 MHz RC Oscillator”**.

REGISTER 4-5: OSCCAL: OSCILLATOR CALIBRATION REGISTER

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | U-0 |
| CAL6 | CAL5 | CAL4 | CAL3 | CAL2 | CAL1 | CAL0 | — |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 7-1 **CAL<6:0>**: Oscillator Calibration bits

01111111 = Maximum frequency

•

•

•

0000001

0000000 = Center frequency

11111111

•

•

•

1000000 = Minimum frequency

bit 0 **Unimplemented:** Read as '0'

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4.6 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

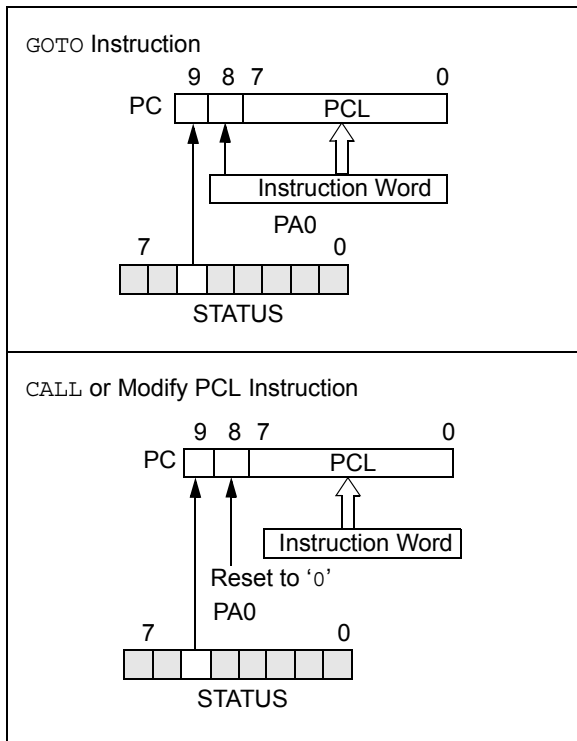
For a `GOTO` instruction, bits 8:0 of the PC are provided by the `GOTO` instruction word. The Program Counter (PCL) is mapped to PC<7:0>. Bit 5 of the STATUS register provides page information to bit 9 of the PC (Figure 4-4).

For a `CALL` instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-4).

Instructions where the PCL is the destination or modify PCL instructions include `MOVWF PC`, `ADDWF PC` and `BSF PC, 5`.

Note: Because PC<8> is cleared in the `CALL` instruction or any modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-4: LOADING OF PC BRANCH INSTRUCTIONS



4.6.1 EFFECTS OF RESET

The PC is set upon a Reset, which means that the PC addresses the last location in the last page (i.e., the oscillator calibration instruction). After executing `MOVLW XX`, the PC will roll over to location 00h and begin executing user code.

The STATUS register page preselect bits are cleared upon a Reset, which means that page 0 is preselected.

Therefore, upon a Reset, a `GOTO` instruction will automatically cause the program to jump to page 0 until the value of the page bits is altered.

4.7 Stack

The PIC12F510/16F506 devices have a two-deep, 12-bit wide hardware PUSH/POP stack.

A `CALL` instruction will PUSH the current value of Stack 1 into Stack 2 and then PUSH the current PC value, incremented by one, into Stack Level 1. If more than two sequential `CALL`s are executed, only the most recent two return addresses are stored.

A `RETLW` instruction will POP the contents of Stack Level 1 into the PC and then copy Stack Level 2 contents into Stack Level 1. If more than two sequential `RETLW`s are executed, the stack will be filled with the address previously stored in Stack Level 2.

Note 1: The W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

2: There are no Status bits to indicate stack overflows or stack underflow conditions.

3: There are no instruction mnemonics called `PUSH` or `POP`. These are actions that occur from the execution of the `CALL` and `RETLW` instructions.

4.8 Indirect Data Addressing: INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

4.8.1 INDIRECT ADDRESSING EXAMPLE

- Register file 07 contains the value 10h
- Register file 08 contains the value 0Ah
- Load the value 07 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 08)
- A read of the INDR register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 4-1.

EXAMPLE 4-1: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```

MOV LW 0x10 ;initialize pointer
MOV WF FSR ;to RAM
NEXT CLR F INDF ;clear INDF register
INCF FSR,F ;inc pointer
BTFSC FSR,4 ;all done?
GOTO NEXT ;NO, clear next
CONTINUE
: ;YES, continue
:
    
```

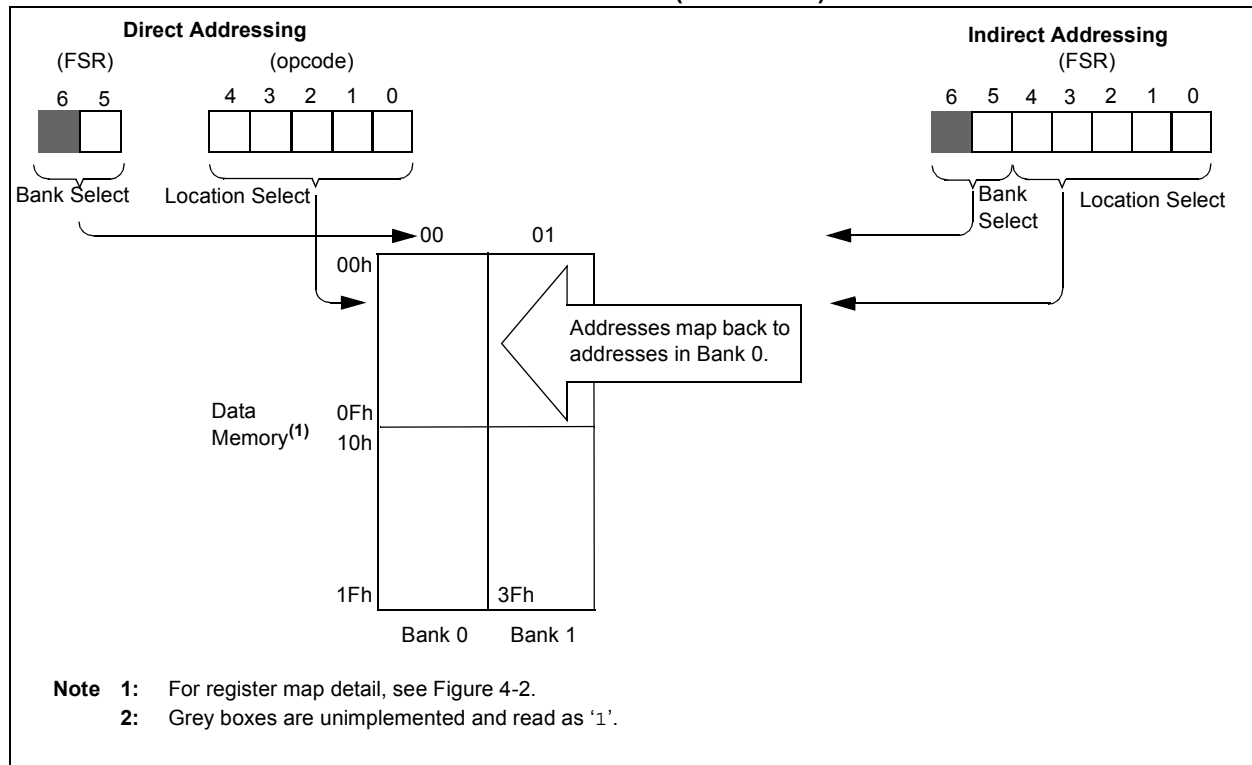
The FSR is a 5-bit wide register. It is used in conjunction with the INDF register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

PIC16F506 – Uses FSR<6:5>. Selects from Bank 0 to Bank 3. FSR<7> is unimplemented, read as '1'.

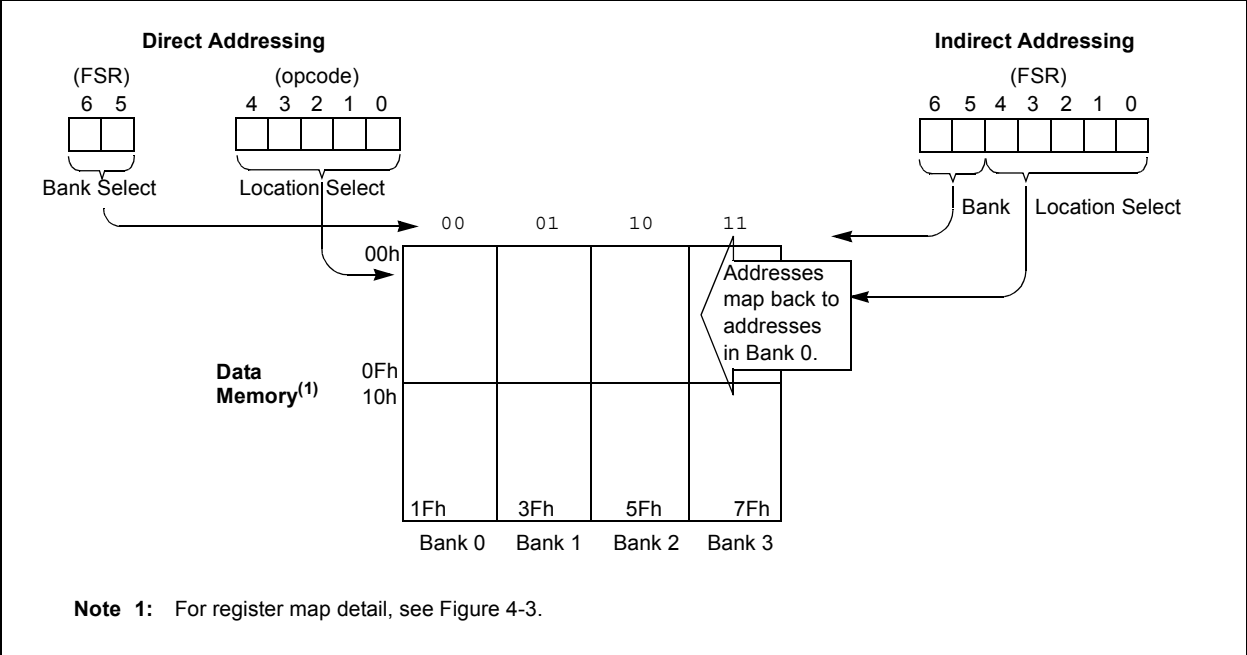
PIC12F510 – Uses FSR<5>. Selects from Bank 0 to Bank 1. FSR<7:6> are unimplemented, read as '11'.

FIGURE 4-5: DIRECT/INDIRECT ADDRESSING (PIC12F510)



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FIGURE 4-6: DIRECT/INDIRECT ADDRESSING (PIC16F506)



5.0 I/O PORT

As with any other register, the I/O register(s) can be written and read under program control. However, read instructions (e.g., `MOVF PORTB, W`) always read the I/O pins independent of the pin's Input/Output modes. On Reset, all I/O ports are defined as input (inputs are at high-impedance) since the I/O control registers are all set.

Note: On the PIC12F510, I/O PORTB is referenced as GPIO. On the PIC16F506, I/O PORTB is referenced as PORTB.

5.1 PORTB/GPIO

PORTB/GPIO is an 8-bit I/O register. Only the low-order 6 bits are used (RB/GP<5:0>). Bits 7 and 6 are unimplemented and read as '0's. Please note that RB3/GP3 is an input only pin. The Configuration Word can set several I/O's to alternate functions. When acting as alternate functions, the pins will read as '0' during a port read. Pins RB0/GP0, RB1/GP1, RB3/GP3 and RB4 (PIC16F506 only) can be configured with weak pull-up and also for wake-up on change. The wake-up on change and weak pull-up functions are not pin selectable. If RB3/GP3/MCLR is configured as MCLR, weak pull-up is always on and wake-up on change for this pin is not enabled.

5.2 PORTC (PIC16F506 Only)

PORTC is an 8-bit I/O register. Only the low-order 6 bits are used (RC<5:0>). Bits 7 and 6 are unimplemented and read as '0's.

5.3 TRIS Registers

The Output Driver Control register is loaded with the contents of the W register by executing the `TRIS f` instruction. A '1' from a TRIS register bit puts the corresponding output driver in a High-Impedance mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer. The exception is RB3/GP3, which are input only, and the T0CKI pin, which may be controlled by the OPTION register. See Register 4-3.

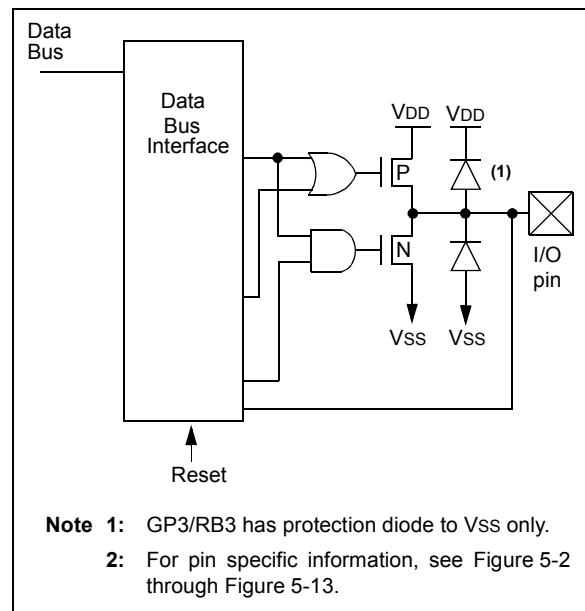
Note: A read of the port reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high but the external system is holding it low, a read of the port will indicate that the pin is low.

Note: The TRIS registers are write-only and are set (output drivers disabled) upon Reset.

5.4 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 5-1. All port pins, except RB3/GP3 which is input only, may be used for both input and output operations. For input operations, these ports are non-latching. Any input must be present until read by an input instruction (e.g., `MOVF PORTB, W`). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit in TRIS must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin (except RB3/GP3) can be programmed individually as input or output.

FIGURE 5-1: PIC12F510/16F506 EQUIVALENT CIRCUIT FOR PIN DRIVE⁽²⁾



PIC12F510/16F506

FIGURE 5-2: BLOCK DIAGRAM OF GP0/RB0 AND GP1/RB1

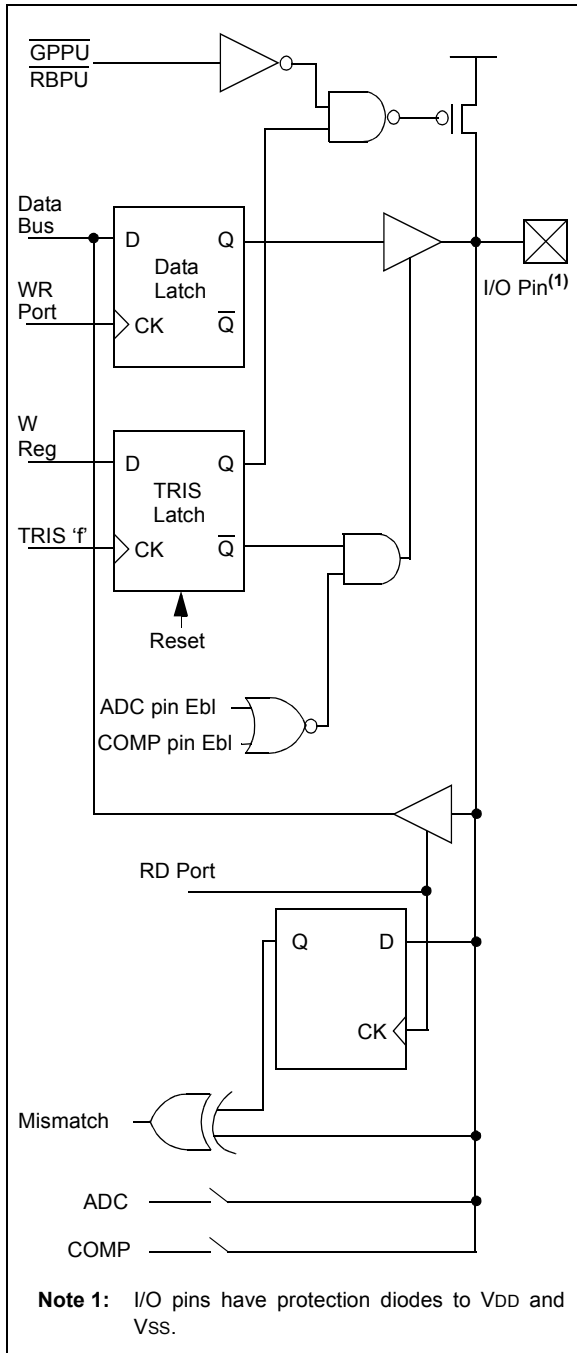


FIGURE 5-3: BLOCK DIAGRAM OF GP3/RB3 (With Weak Pull-up And Wake-up On Change)

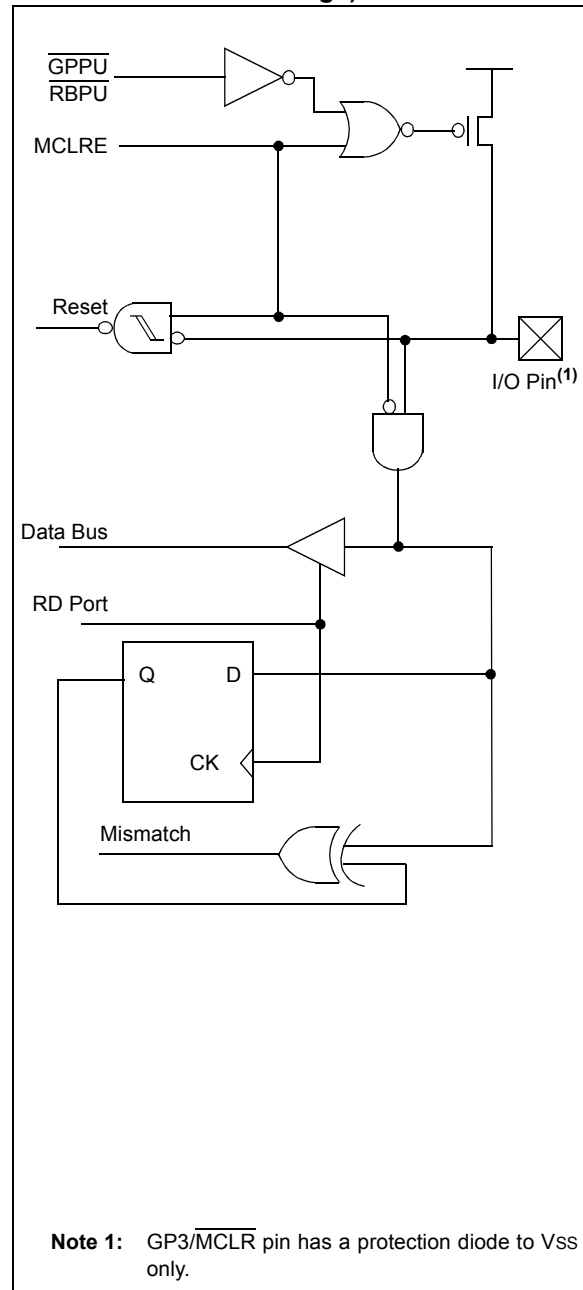


FIGURE 5-4: BLOCK DIAGRAM OF GP2

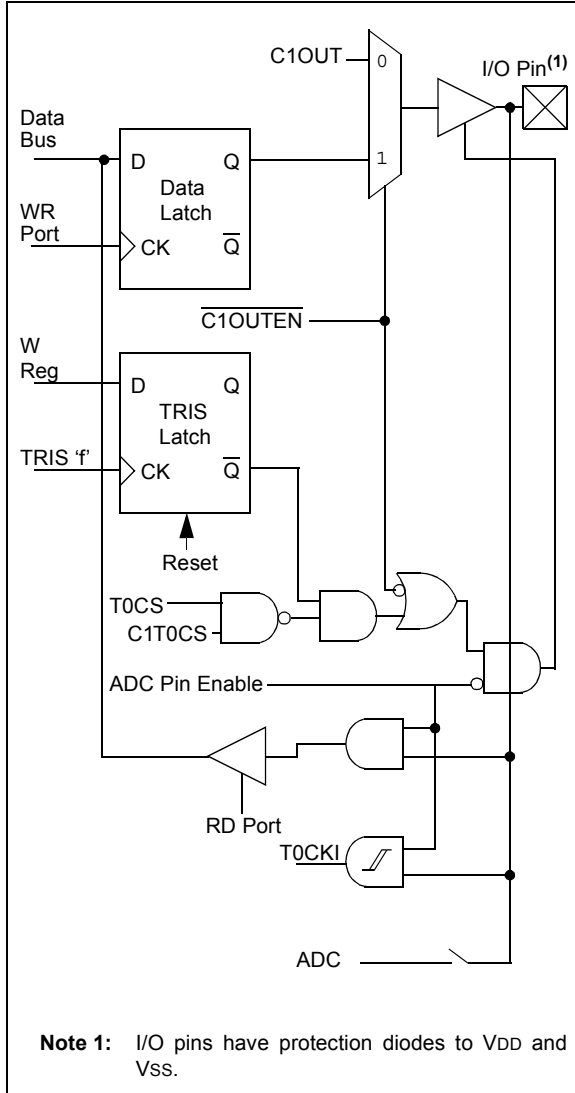
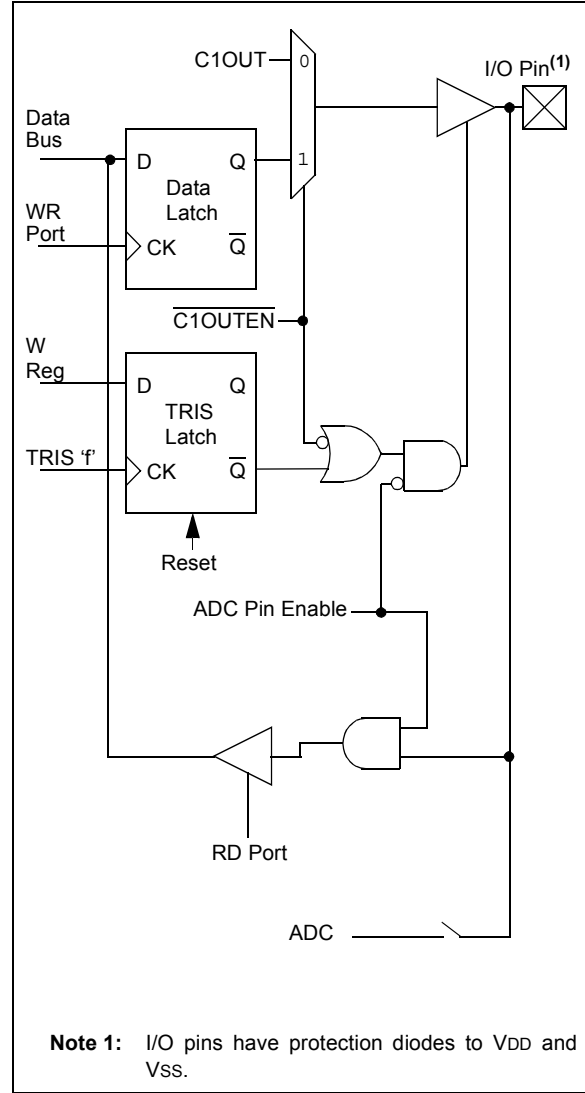


FIGURE 5-5: BLOCK DIAGRAM OF RB2



PIC12F510/16F506

FIGURE 5-6: BLOCK DIAGRAM OF RB4

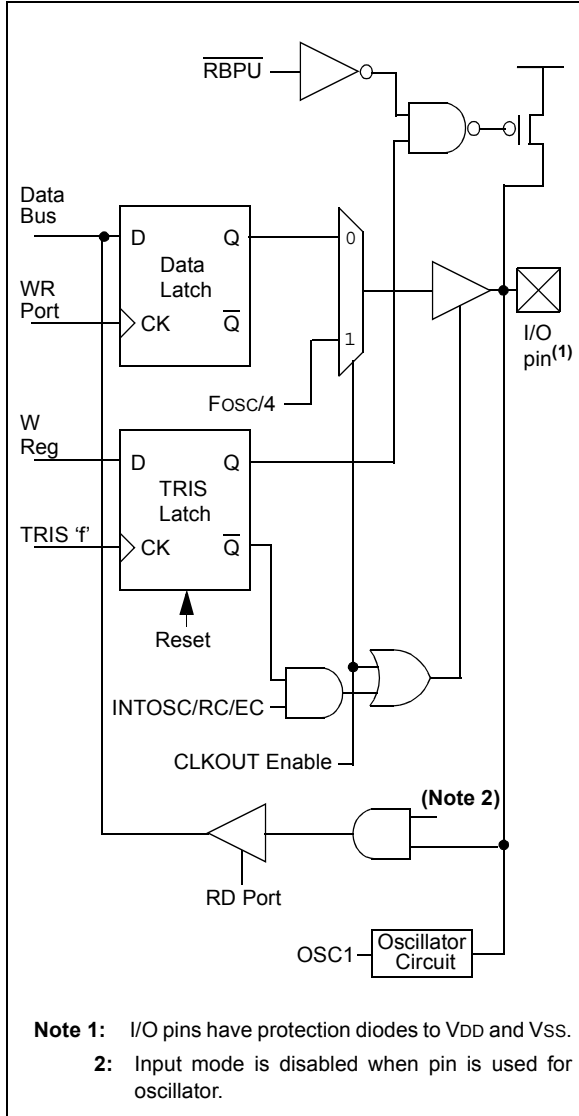


FIGURE 5-7: BLOCK DIAGRAM OF GP4

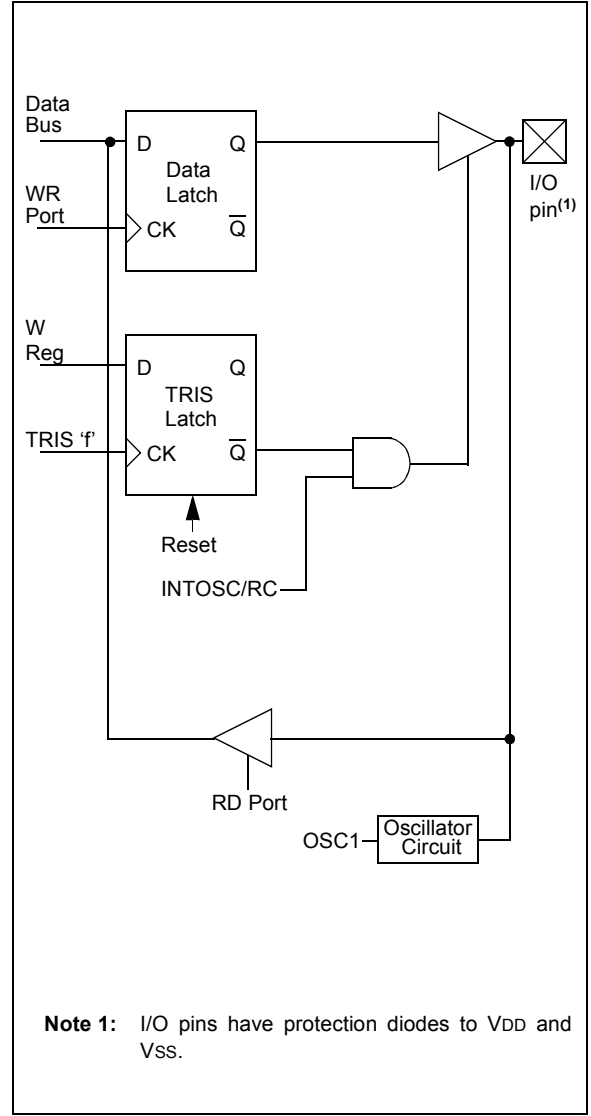


FIGURE 5-8: BLOCK DIAGRAM OF RB5/GP5

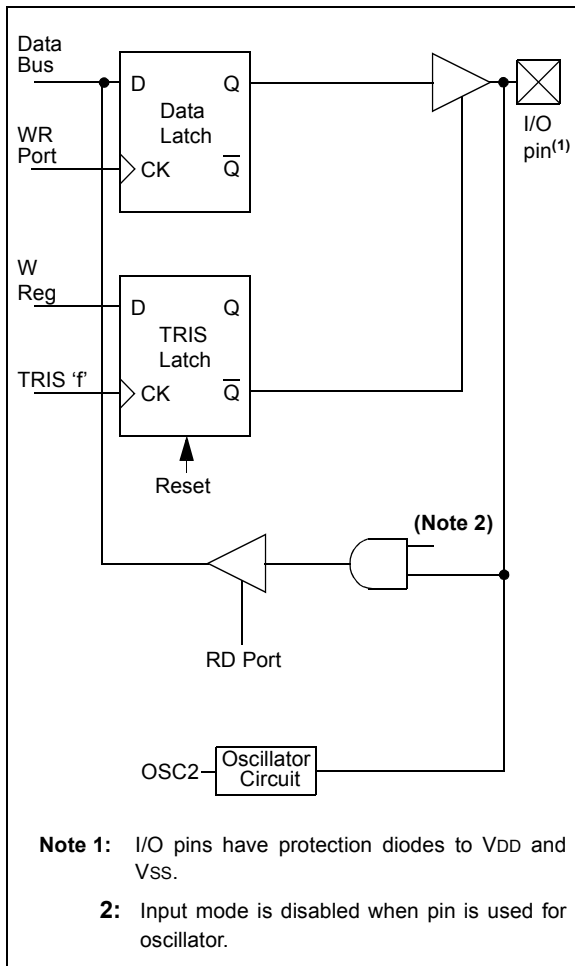
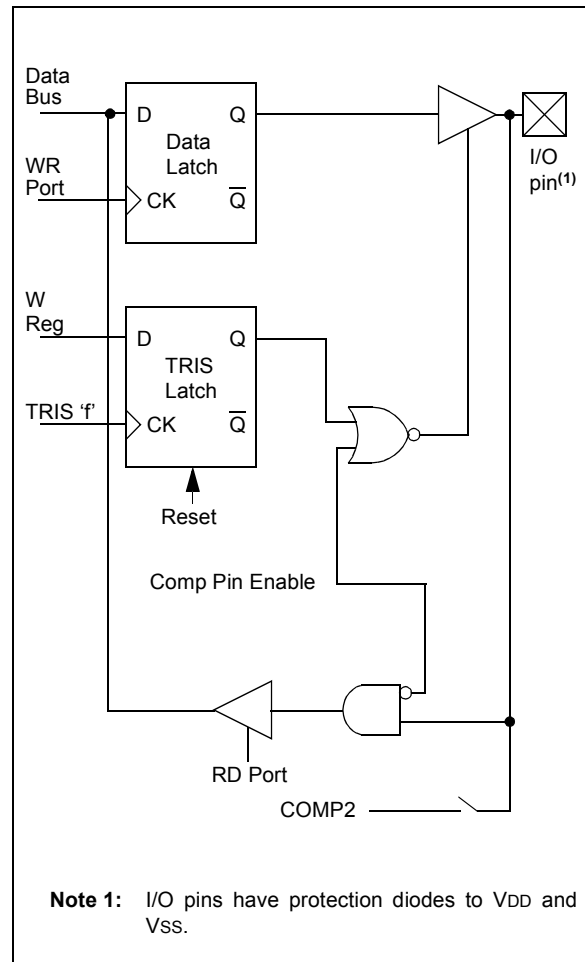


FIGURE 5-9: BLOCK DIAGRAM OF RC0/RC1



PIC12F510/16F506

FIGURE 5-10: BLOCK DIAGRAM OF RC2

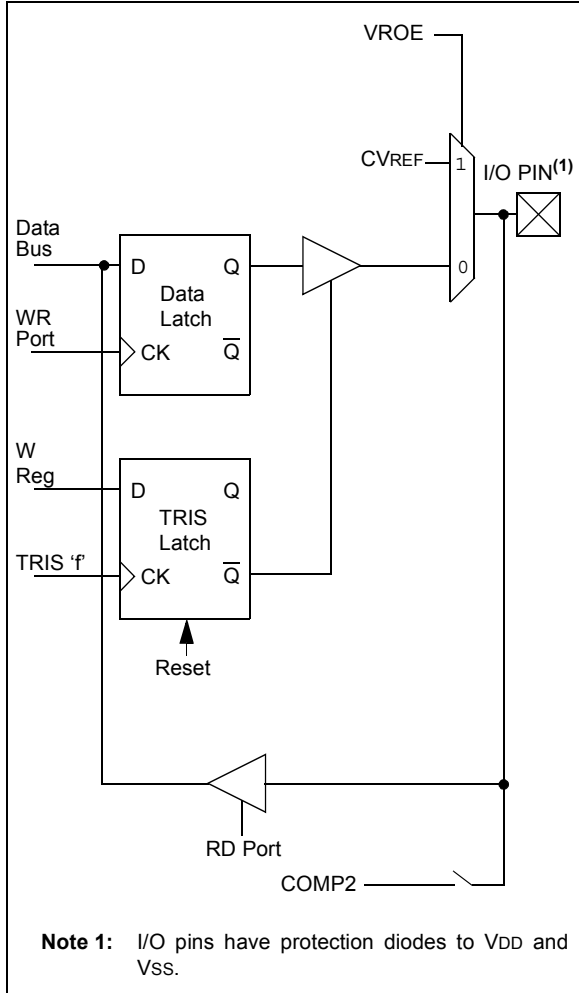


FIGURE 5-11: BLOCK DIAGRAM OF RC3

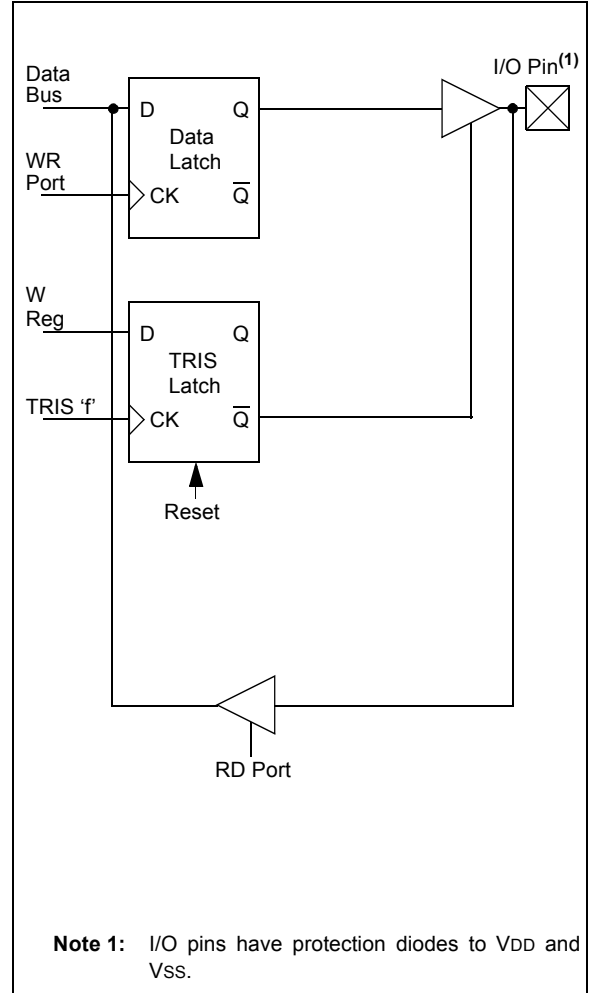


FIGURE 5-12: BLOCK DIAGRAM OF RC4

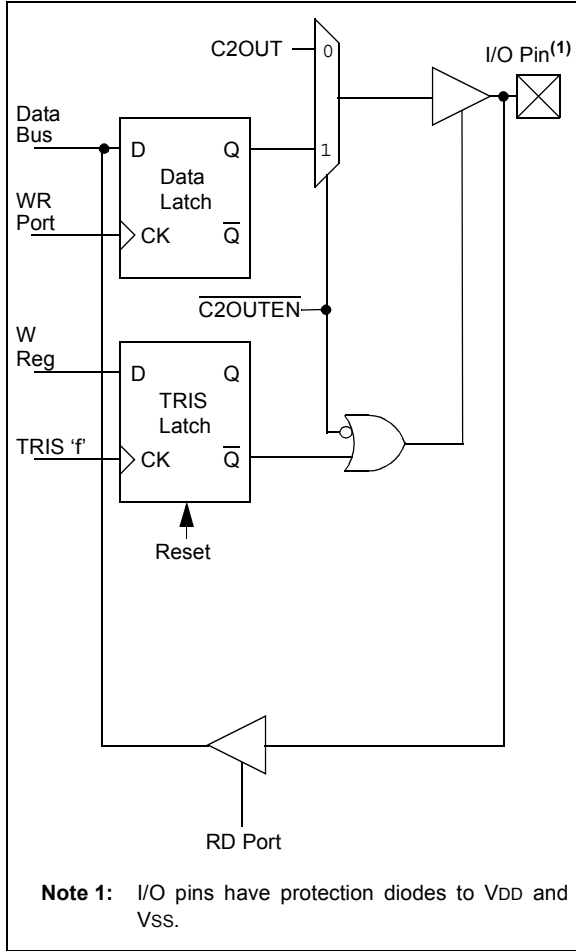
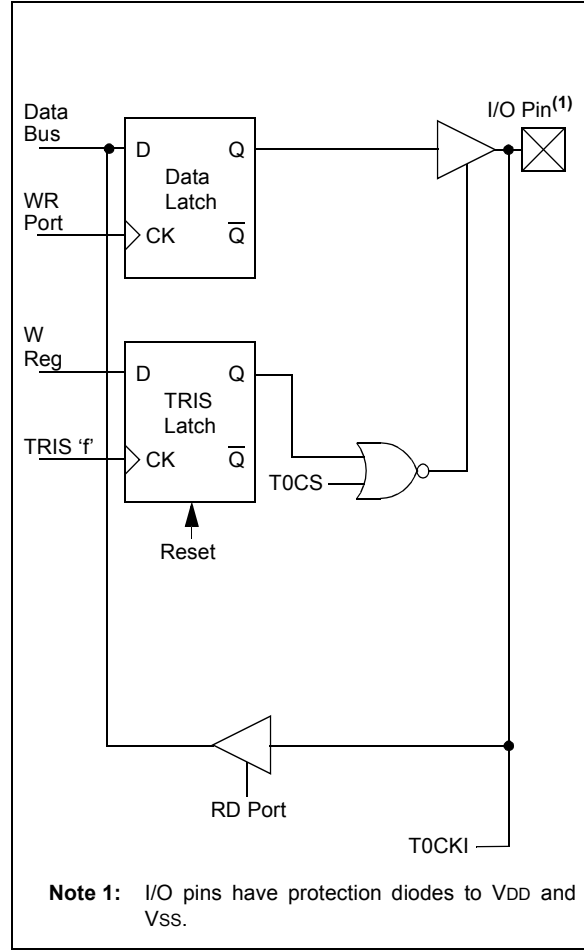


FIGURE 5-13: BLOCK DIAGRAM OF RC5



PIC12F510/16F506

TABLE 5-1: SUMMARY OF PORT REGISTERS

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-On Reset | Value on All Other Resets |
|---------|-------------------------|--------------------------|--------------------------|----------------------|------------------------|------------------------|-------|-------|-------|-------------------------|---------------------------|
| N/A | TRISGPIO ⁽¹⁾ | — | — | I/O Control Register | | | | | | --11 1111 | --11 1111 |
| N/A | TRISB ⁽²⁾ | — | — | I/O Control Register | | | | | | --11 1111 | --11 1111 |
| N/A | TRISC ⁽²⁾ | — | — | I/O Control Register | | | | | | --11 1111 | --11 1111 |
| N/A | OPTION ⁽¹⁾ | $\overline{\text{GPWU}}$ | $\overline{\text{GPPU}}$ | T0CS | TOSE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| N/A | OPTION ⁽²⁾ | $\overline{\text{RBWU}}$ | $\overline{\text{RBPu}}$ | T0CS | TOSE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| 03h | STATUS ⁽¹⁾ | GPWUF | CWUF | PA0 | $\overline{\text{TO}}$ | $\overline{\text{PD}}$ | Z | DC | C | 0001 1xxx | qq0q quuu ⁽³⁾ |
| 03h | STATUS ⁽²⁾ | RBWUF | CWUF | PA0 | $\overline{\text{TO}}$ | $\overline{\text{PD}}$ | Z | DC | C | 0001 1xxx | qq0q quuu ⁽³⁾ |
| 06h | GPIO ⁽¹⁾ | — | — | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | --xx xxxx | --uu uuuu |
| 06h | PORTB ⁽²⁾ | — | — | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | --xx xxxx | --uu uuuu |
| 07h | PORTC ⁽²⁾ | — | — | RC5 | RC4 | RC3 | RC2 | RC1 | RC0 | --xx xxxx | --uu uuuu |

Legend: — = unimplemented read as '0', x = unknown, u = unchanged, q = depends on condition.

Note 1: PIC12F510 only.

Note 2: PIC16F506 only.

Note 3: If Reset was due to wake-up on pin change, then bit 7 = 1. All other Resets will cause bit 7 = 0.

TABLE 5-2: I/O PIN FUNCTION ORDER OF PRECEDENCE (PIC16F506)

| Priority | RB0 | RB1 | RB2 | RB3 | RB4 | RB5 |
|----------|-----------|-----------|-------|---------------------------------|-------------|------------|
| 1 | AN0/C1IN+ | AN1/C1IN- | AN2 | Input/ $\overline{\text{MCLR}}$ | OSC2/CLKOUT | OSC1/CLKIN |
| 2 | TRISB | TRISB | C1OUT | — | TRISB | TRISB |
| 3 | — | — | TRISB | — | — | — |

TABLE 5-3: I/O PIN FUNCTION ORDER OF PRECEDENCE (PIC16F506)

| Priority | RC0 | RC1 | RC2 | RC3 | RC4 | RC5 |
|----------|-------|-------|-------|-------|-------|-------|
| 1 | C2IN+ | C2IN- | CVREF | TRISC | C2OUT | T0CKI |
| 2 | TRISC | TRISC | TRISC | — | TRISC | TRISC |

TABLE 5-4: I/O PIN FUNCTION ORDER OF PRECEDENCE (PIC12F510)

| Priority | GP0 | GP1 | GP2 | GP3 | GP4 | GP5 |
|----------|-----------|-----------|--------|---------------------------------|--------|------------|
| 1 | AN0/C1IN+ | AN1/C1IN- | AN2 | Input/ $\overline{\text{MCLR}}$ | OSC2 | OSC1/CLKIN |
| 2 | TRISIO | TRISIO | C1OUT | — | TRISIO | TRISIO |
| 3 | — | — | T0CKI | — | — | — |
| 4 | — | — | TRISIO | — | — | — |

PIC12F510/16F506

TABLE 5-5: REQUIREMENTS FOR DIGITAL PIN OPERATION (PIC12F510)

| | GP0 | GP0 | GP1 | GP1 | GP2 | GP2 | GP3 | GP4 | GP5 |
|----------------|--------|--------|------------|------------|-----|-----|-----|----------|----------|
| CM1CON0 | | | | | | | | | |
| C1ON | 0 | 1 | 0 | 1 | 0 | 1 | — | — | — |
| C1PREF | — | 0 | — | 1 | — | — | — | — | — |
| C1NREF | — | — | — | 0 | — | — | — | — | — |
| C1T0CS | — | — | — | — | — | 1 | — | — | — |
| C1OUTEN | — | — | — | — | — | 1 | — | — | — |
| CM2CON0 | | | | | | | | | |
| C2ON | — | — | — | — | — | — | — | — | — |
| C2PREF1 | — | — | — | — | — | — | — | — | — |
| C2PREF2 | — | — | — | — | — | — | — | — | — |
| C2NREF | — | — | — | — | — | — | — | — | — |
| C2OUTEN | — | — | — | — | — | — | — | — | — |
| VRCON0 | | | | | | | | | |
| VROE | — | — | — | — | — | — | — | — | — |
| VREN | — | — | — | — | — | — | — | — | — |
| OPTION | | | | | | | | | |
| T0CS | — | — | — | — | — | 0 | — | — | — |
| ADCON0 | | | | | | | | | |
| ANS<1:0> | 00, 01 | 00, 01 | 00, 01, 10 | 00, 01, 10 | 00 | 00 | — | — | — |
| CONFIG | | | | | | | | | |
| MCLRE | — | — | — | — | — | — | — | — | — |
| INTOSC | — | — | — | — | — | — | — | — | — |
| LP | — | — | — | — | — | — | — | Disabled | Disabled |
| EXTRC | — | — | — | — | — | — | — | — | Disabled |
| XT | — | — | — | — | — | — | — | Disabled | Disabled |

Note 1: Multiple column entries for a pin demonstrate the different permutations to arrive at digital functionality for the pin.

2: Shaded cells indicate the bit status does not affect the pins digital functionality.

PIC12F510/16F506

TABLE 5-6: REQUIREMENTS FOR DIGITAL PIN OPERATION (PIC16F506 PORTB)^{(1), (2)}

| | RB0 | RB0 | RB0 | RB1 | RB1 | RB2 | RB2 | RB3 | RB4 | RB5 |
|----------------|--------|--------|--------|------------|------------|-----|-----|-----|----------|----------|
| CM1CON0 | | | | | | | | | | |
| C1ON | — | 0 | 1 | 0 | 1 | 0 | 1 | — | — | — |
| C1PREF | — | — | 0 | — | — | — | — | — | — | — |
| C1NREF | — | — | — | — | 0 | — | — | — | — | — |
| C1T0CS | — | — | — | — | — | — | — | — | — | — |
| C1OUTEN | — | — | — | — | — | — | 1 | — | — | — |
| CM2CON0 | | | | | | | | | | |
| C2ON | 1 | — | — | — | — | — | — | — | — | — |
| C2PREF1 | 0 | — | — | — | — | — | — | — | — | — |
| C2PREF2 | 1 | — | — | — | — | — | — | — | — | — |
| C2NREF | — | — | — | — | — | — | — | — | — | — |
| C2OUTEN | — | — | — | — | — | — | — | — | — | — |
| OPTION | | | | | | | | | | |
| T0CS | — | — | — | — | — | — | — | — | — | — |
| ADCON0 | | | | | | | | | | |
| ANS<1:0> | 00, 01 | 00, 01 | 00, 01 | 00, 01, 10 | 00, 01, 10 | 00 | 00 | — | — | — |
| CONFIG | | | | | | | | | | |
| MCLRE | — | — | — | — | — | — | — | 0 | — | — |
| INTOSC | — | — | — | — | — | — | — | — | — | — |
| LP | — | — | — | — | — | — | — | — | Disabled | Disabled |
| EXTRC | — | — | — | — | — | — | — | — | — | Disabled |
| XT | — | — | — | — | — | — | — | — | Disabled | Disabled |
| EC | — | — | — | — | — | — | — | — | — | Disabled |
| HS | — | — | — | — | — | — | — | — | Disabled | Disabled |
| INTOSC CLKOUT | — | — | — | — | — | — | — | — | Disabled | Disabled |
| EXTRC CLOCKOUT | — | — | — | — | — | — | — | — | Disabled | Disabled |

Note 1: Multiple column entries for a pin demonstrate the different permutations to arrive at digital functionality for the pin.

2: Shaded cells indicate the bit status does not affect the pins digital functionality.

TABLE 5-7: REQUIREMENTS FOR DIGITAL PIN OPERATION (PIC16F506 PORTC)^{(1), (2)}

| | RC0 | RC0 | RC1 | RC1 | RC2 | RC3 | RC4 | RC4 | RC5 | RC5 |
|----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| CM2CON0 | | | | | | | | | | |
| C2ON | 0 | 1 | 0 | 1 | — | — | 0 | 1 | — | — |
| C2PREF1 | — | 0 | — | — | — | — | — | — | — | — |
| C2PREF2 | — | 0 | — | — | — | — | — | — | — | — |
| C2NREF | — | — | — | 0 | — | — | — | — | — | — |
| C2OUTEN | — | — | — | — | — | — | — | 1 | — | — |
| VRCON0 | | | | | | | | | | |
| VROE | — | — | — | — | 0 | — | — | — | — | — |
| OPTION | | | | | | | | | | |
| T0CS | — | — | — | — | — | — | — | — | 0 | — |

Note 1: Multiple column entries for a pin demonstrate the different permutations to arrive at digital functionality for the pin.

2: Shaded cells indicate the bit status does not affect the pins digital functionality.

5.5 I/O Programming Considerations

5.5.1 BIDIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. For example, the BCF and BSF instructions read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit 5 of PORTB/GPIO will cause all eight bits of PORTB/GPIO to be read into the CPU, bit 5 to be set and the PORTB/GPIO value to be written to the output latches. If another bit of PORTB/GPIO is used as a bidirectional I/O pin (say bit '0') and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit '0' is switched into Output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential Read-Modify-Write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired OR", "wired AND"). The resulting high output currents may damage the chip.

EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT (e.g., PIC16F506)

```

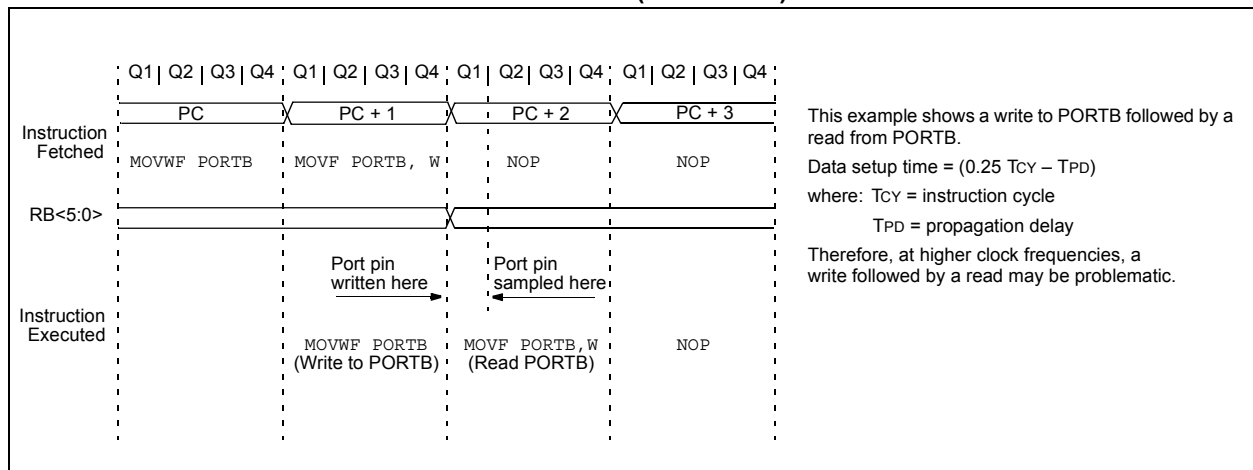
;Initial PORTB Settings
;PORTB<5:3> Inputs
;PORTB<2:0> Outputs
;
;
;           PORTB latch  PORTB pins
;           -----  -----
BCF   PORTB, 5 ;--01 -ppp  --11 pppp
BCF   PORTB, 4 ;--10 -ppp  --11 pppp
MOVLW 007h;
TRIS  PORTB   ;--10 -ppp  --11 pppp
;
    
```

Note: The user may have expected the pin values to be '--00 pppp'. The 2nd BCF caused RB5 to be latched as the pin value (High).

5.5.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle. Whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-14). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction causes the file to be read into the CPU. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 5-14: SUCCESSIVE I/O OPERATION (PIC16F506)



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NOTES:

6.0 TMR0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select:
 - Edge select for external clock
 - External clock from either the T0CKI pin or from the output of the comparator

Figure 6-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to the TMR0 register.

There are two types of Counter mode. The first Counter mode uses the T0CKI pin to increment Timer0. It is selected by setting the T0CKI bit (OPTION<5>), setting the $\overline{C1T0CS}$ bit (CM1CON0<4>) and setting the $\overline{C1OUTEN}$ bit (CM1CON0<6>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.1 “Using Timer0 With An External Clock”.

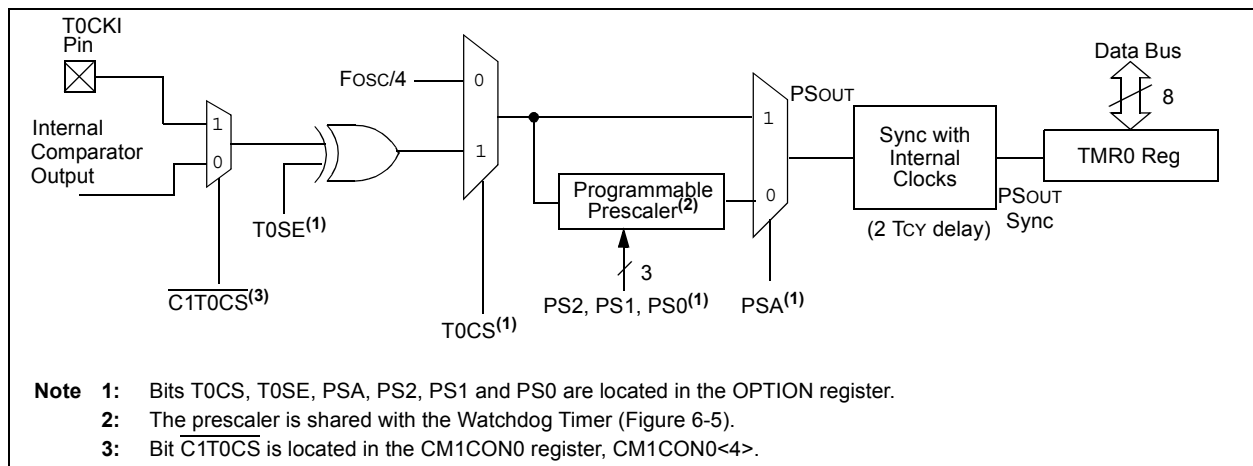
The second Counter mode uses the output of the comparator to increment Timer0. It can be entered in two different ways. The first way is selected by setting the T0CS bit (OPTION<5>), and clearing the $\overline{C1T0CS}$ bit (CM1CON0<4>) ($\overline{C1OUTEN}$ [CM1CON0<6>] does not affect this mode of operation). This enables an internal connection between the comparator and the Timer0.

The second way is selected by setting the T0CS bit (OPTION<5>), setting the $\overline{C1T0CS}$ bit (CM1CON0) and clearing the $\overline{C1OUTEN}$ bit (CM1CON0<6>). This allows the output of the comparator onto the T0CKI pin, while keeping the T0CKI input active. Therefore, any comparator change on the COUT pin is fed back into the T0CKI input. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input as discussed in Section 6.1 “Using Timer0 With An External Clock”.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable. Section 6.2 “Prescaler” details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 6-1.

FIGURE 6-1: TIMER0 BLOCK DIAGRAM



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FIGURE 6-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE

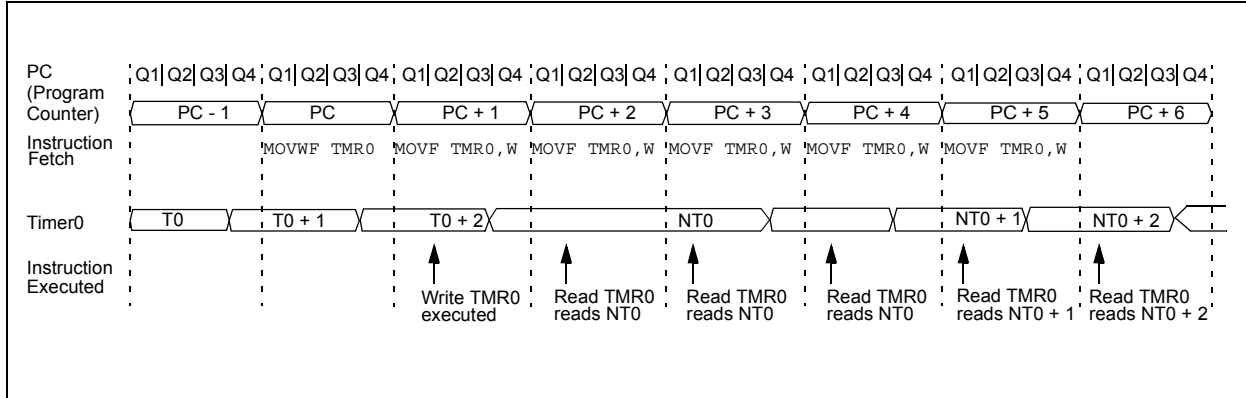


FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

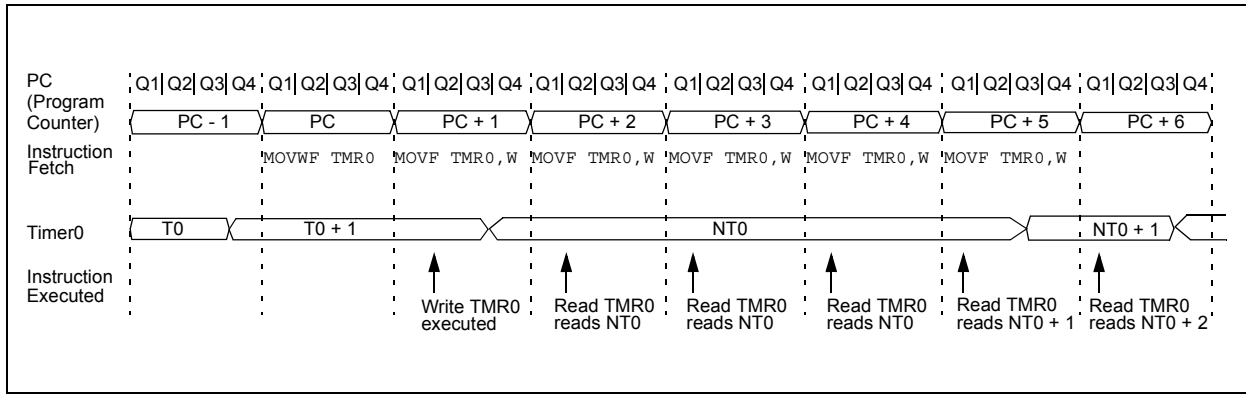


TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

| Addr | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-On Reset | Value on All Other Resets |
|------|-------------------------|--|----------------------|----------------------|---------------------|-------|--------|--------|-------------------|-------------------------|---------------------------|
| 01h | TMR0 | Timer0 – 8-bit Real-Time Clock/Counter | | | | | | | | xxxx xxxx | uuuu uuuu |
| 07h | CM1CON0 ⁽²⁾ | C1OUT | $\overline{C1OUTEN}$ | C1POL | $\overline{C1T0CS}$ | C1ON | C1NREF | C1PREF | $\overline{C1WU}$ | 1111 1111 | uuuu uuuu |
| 08h | CM1CON0 ⁽³⁾ | C1OUT | $\overline{C1OUTEN}$ | C1POL | $\overline{C1T0CS}$ | C1ON | C1NREF | C1PREF | $\overline{C1WU}$ | 1111 1111 | uuuu uuuu |
| N/A | OPTION | \overline{GPWU} | \overline{GPPU} | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| N/A | TRISGPIO ⁽¹⁾ | — | — | I/O Control Register | | | | | | ---- 1111 | --11 1111 |

Legend: Shaded cells not used by Timer0, – = unimplemented, x = unknown, u = unchanged.

- Note**
- 1: The TRIS of the T0CKI pin is overridden when T0CS = 1.
 - 2: For PIC12F510.
 - 3: For PIC16F506.

6.1 Using Timer0 With An External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

6.1.1 EXTERNAL CLOCK SYNCHRONIZATION

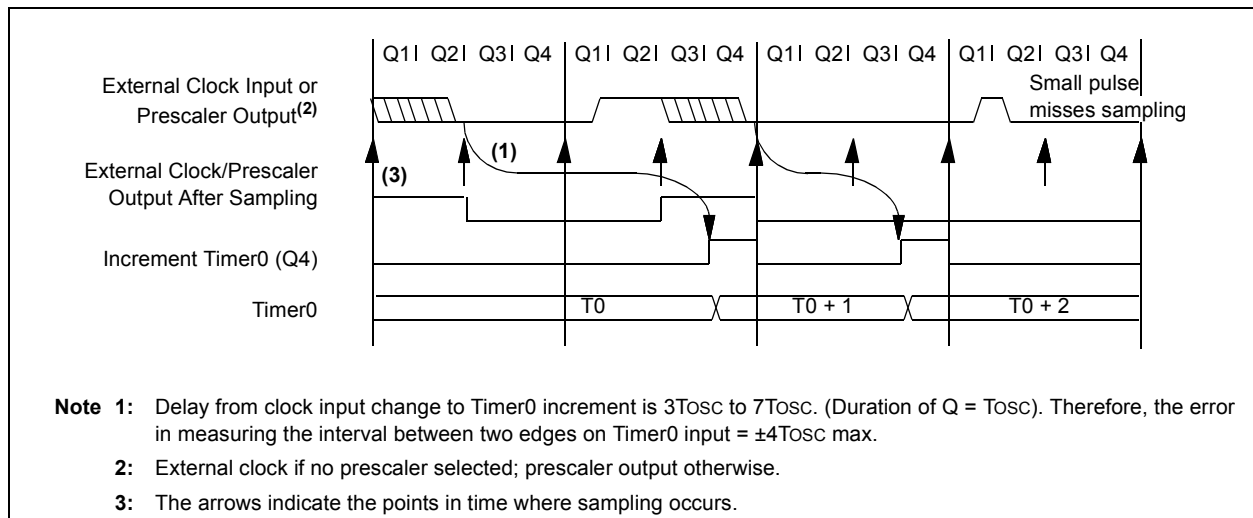
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of an external clock with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-4). Therefore, it is necessary for T0CKI or the comparator output to be high for at least 2Tosc (and a small RC delay of 2Tt0H) and low for at least 2Tosc (and a small RC delay of 2Tt0H). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler, so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI or the comparator output to have a period of at least 4Tosc (and a small RC delay of 4Tt0H) divided by the prescaler value. The only requirement on T0CKI or the comparator output high and low time is that they do not violate the minimum pulse width requirement of Tt0H. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

6.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-4 shows the delay from the external clock edge to the timer incrementing.

FIGURE 6-4: TIMER0 TIMING WITH EXTERNAL CLOCK



6.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module or as a postscaler for the Watchdog Timer (WDT), respectively (see Figure 10-12). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet.

Note: The prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x, etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a Reset, the prescaler contains all '0's.

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6.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on-the-fly” during program execution). To avoid an unintended device Reset, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0 → WDT)

```

CLRWDWDT          ;Clear WDT
CLRWF   TMR0      ;Clear TMR0 & Prescaler
MOVLW  '00xx1111'b ;These 3 lines (5, 6, 7)
OPTION          ;are required only if
                ;desired
CLRWDWDT          ;PS<2:0> are 000 or 001
MOVLW  '00xx1xxx'b ;Set Postscaler to
OPTION          ;desired WDT rate
    
```

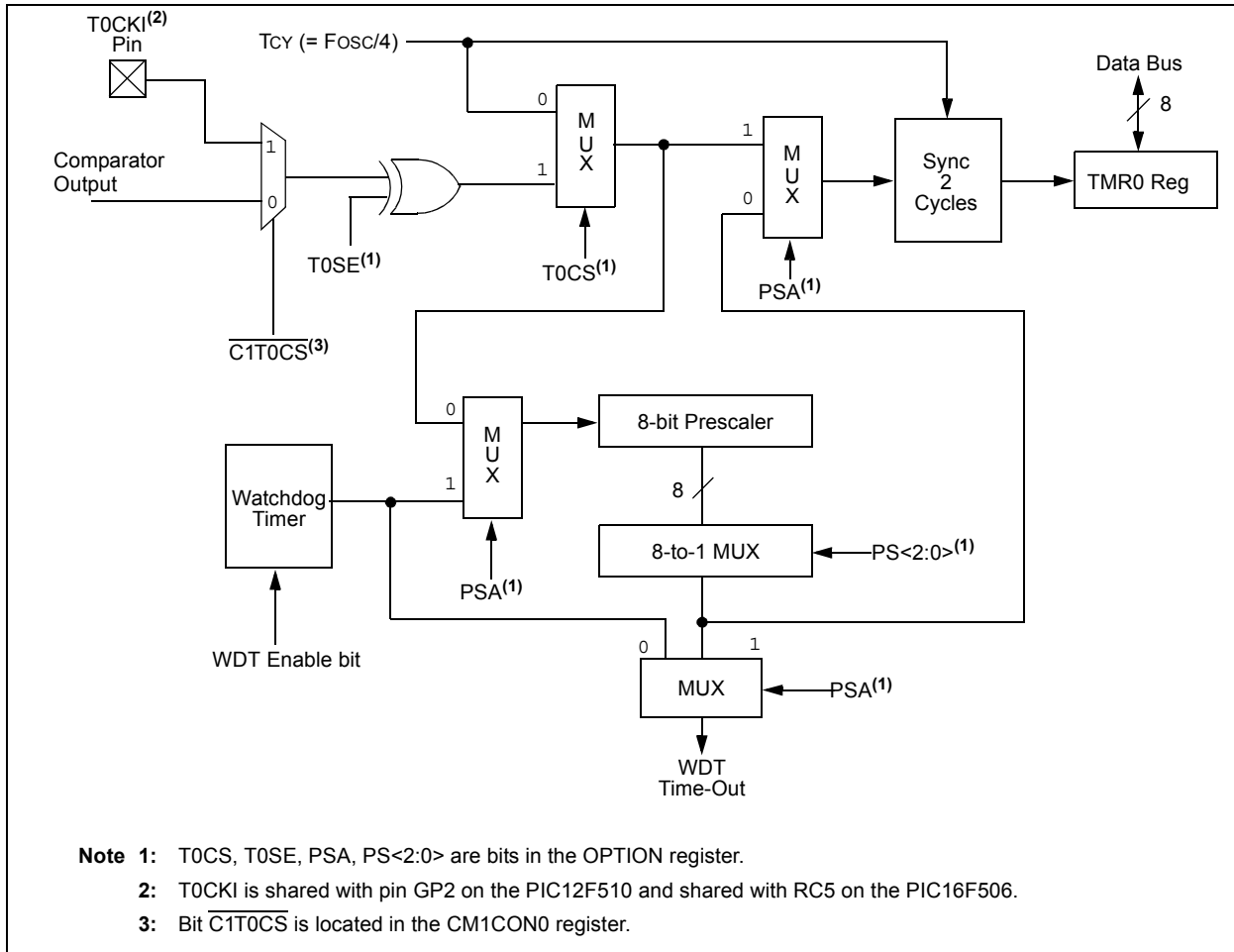
To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2. This sequence must be used even if the WDT is disabled. A CLRWDWDT instruction should be executed before switching the prescaler.

EXAMPLE 6-2: CHANGING PRESCALER (WDT → TIMER0)

```

CLRWDWDT          ;Clear WDT and
                ;prescaler
MOVLW  'xxxx0xxx' ;Select TMR0, new
                ;prescale value and
                ;clock source
OPTION
    
```

FIGURE 6-5: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



7.0 COMPARATOR(S)

The PIC12F510 contains one analog comparator module. The PIC16F506 contains two comparators and a comparator voltage reference.

REGISTER 7-1: CM1CON0: COMPARATOR C1 CONTROL REGISTER (PIC12F510)

| | | | | | | | |
|-------|----------------------|-------|---------------------|-------|--------|--------|-------------------|
| R-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| C1OUT | $\overline{C1OUTEN}$ | C1POL | $\overline{C1T0CS}$ | C1ON | C1NREF | C1PREF | $\overline{C1WU}$ |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

| | |
|-------|--|
| bit 7 | C1OUT: Comparator Output bit 1 = $V_{IN+} > V_{IN-}$ 0 = $V_{IN+} < V_{IN-}$ |
| bit 6 | $\overline{C1OUTEN}$: Comparator Output Enable bit ^{(1), (2)} 1 = Output of comparator is NOT placed on the C1OUT pin 0 = Output of comparator is placed in the C1OUT pin |
| bit 5 | C1POL: Comparator Output Polarity bit ⁽²⁾ 1 = Output of comparator is not inverted 0 = Output of comparator is inverted |
| bit 4 | $\overline{C1T0CS}$: Comparator TMR0 Clock Source bit ⁽²⁾ 1 = TMR0 clock source selected by T0CS control bit 0 = Comparator output used as TMR0 clock source |
| bit 3 | C1ON: Comparator Enable bit 1 = Comparator is on 0 = Comparator is off |
| bit 2 | C1NREF: Comparator Negative Reference Select bit ⁽²⁾ 1 = C1IN- pin 0 = 0.6V internal reference |
| bit 1 | C1PREF: Comparator Positive Reference Select bit ⁽²⁾ 1 = C1IN+ pin 0 = C1IN- pin |
| bit 0 | $\overline{C1WU}$: Comparator Wake-up On Change Enable bit ⁽²⁾ 1 = Wake-up On Comparator Change is disabled 0 = Wake-up On Comparator Change is enabled |

Note 1: Overrides T0CS bit for TRIS control of RB2.

Note 2: When comparator is turned on, these control bits assert themselves.

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REGISTER 7-2: CM1CON0: COMPARATOR C1 CONTROL REGISTER (PIC16F506)

| R-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|-------|-----------------------------|-------|----------------------------|-------|--------|--------|--------------------------|
| C1OUT | $\overline{\text{C1OUTEN}}$ | C1POL | $\overline{\text{C1T0CS}}$ | C1ON | C1NREF | C1PREF | $\overline{\text{C1WU}}$ |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 7 **C1OUT:** Comparator Output bit
 1 = $V_{IN+} > V_{IN-}$
 0 = $V_{IN+} < V_{IN-}$
- bit 6 **C1OUTEN:** Comparator Output Enable bit^{(1), (2)}
 1 = Output of comparator is NOT placed on the C1OUT pin
 0 = Output of comparator is placed in the C1OUT pin
- bit 5 **C1POL:** Comparator Output Polarity bit⁽²⁾
 1 = Output of comparator is not inverted
 0 = Output of comparator is inverted
- bit 4 **C1T0CS:** Comparator TMR0 Clock Source bit⁽²⁾
 1 = TMR0 clock source selected by T0CS control bit
 0 = Comparator output used as TMR0 clock source
- bit 3 **C1ON:** Comparator Enable bit
 1 = Comparator is on
 0 = Comparator is off
- bit 2 **C1NREF:** Comparator Negative Reference Select bit⁽²⁾
 1 = C1IN- pin
 0 = 0.6V internal reference
- bit 1 **C1PREF:** Comparator Positive Reference Select bit⁽²⁾
 1 = C1IN+ pin
 0 = C1IN- pin
- bit 0 **C1WU:** Comparator Wake-up On Change Enable bit⁽²⁾
 1 = Wake-up On Comparator Change is disabled
 0 = Wake-up On Comparator Change is enabled

Note 1: Overrides T0CS bit for TRIS control of RB2.

2: When comparator is turned on, these control bits assert themselves. Otherwise, the other registers have precedence.

PIC12F510/16F506

REGISTER 7-3: CM2CON0: COMPARATOR C2 CONTROL REGISTER (PIC16F506)

| R-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|-------|-----------------------------|-------|---------|-------|--------|---------|--------------------------|
| C2OUT | $\overline{\text{C2OUTEN}}$ | C2POL | C2PREF2 | C2ON | C2NREF | C2PREF1 | $\overline{\text{C2WU}}$ |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **C2OUT:** Comparator Output bit
 1 = $V_{IN+} > V_{IN-}$
 0 = $V_{IN+} < V_{IN-}$
- bit 6 **$\overline{\text{C2OUTEN}}$:** Comparator Output Enable bit^{(1), (2)}
 1 = Output of comparator is NOT placed on the C2OUT pin
 0 = Output of comparator is placed in the C2OUT pin
- bit 5 **C2POL:** Comparator Output Polarity bit⁽²⁾
 1 = Output of comparator not inverted
 0 = Output of comparator inverted
- bit 4 **C2PREF2:** Comparator Positive Reference Select bit⁽²⁾
 1 = C1IN+ pin
 0 = C2IN- pin
- bit 3 **C2ON:** Comparator Enable bit
 1 = Comparator is on
 0 = Comparator is off
- bit 2 **C2NREF:** Comparator Negative Reference Select bit⁽²⁾
 1 = C2IN- pin
 0 = CVREF
- bit 1 **C2PREF1:** Comparator Positive Reference Select bit⁽²⁾
 1 = C2IN+ pin
 0 = C2PREF2 controls analog input selection
- bit 0 **$\overline{\text{C2WU}}$:** Comparator Wake-up on Change Enable bit⁽²⁾
 1 = Wake-up on Comparator change is disabled
 0 = Wake-up on Comparator change is enabled.

Note 1: Overrides TOCS bit for TRIS control of RC4.

2: When comparator is turned on, these control bits assert themselves. Otherwise, the other registers have precedence.

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FIGURE 7-1: COMPARATOR 1 BLOCK DIAGRAM FOR PIC12F510/16F506

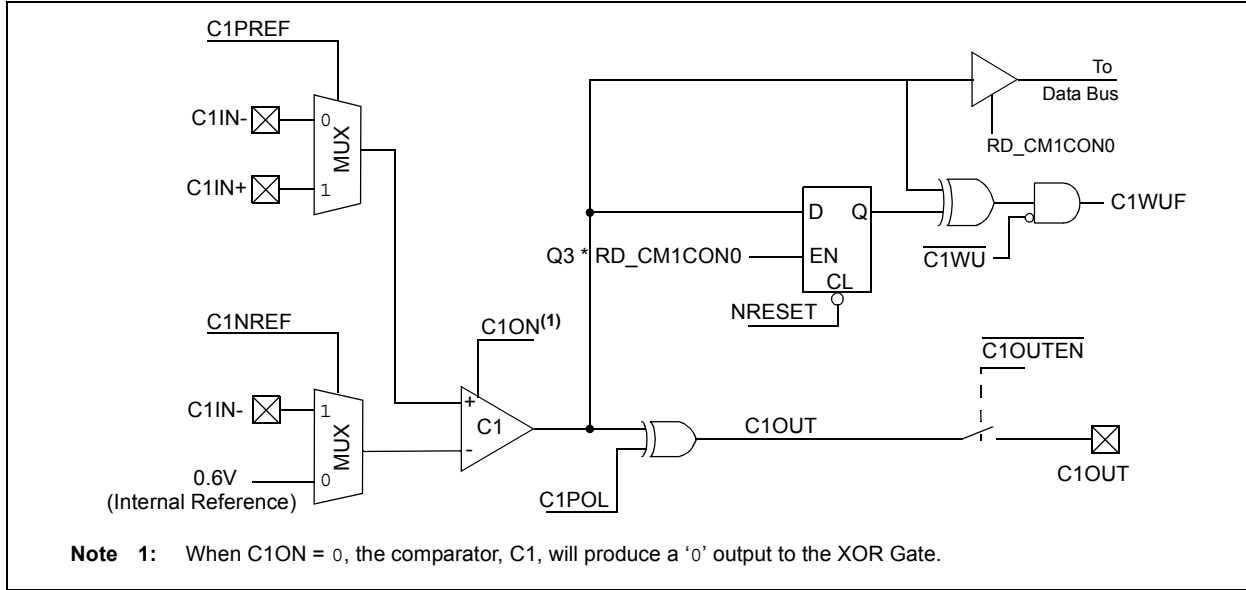
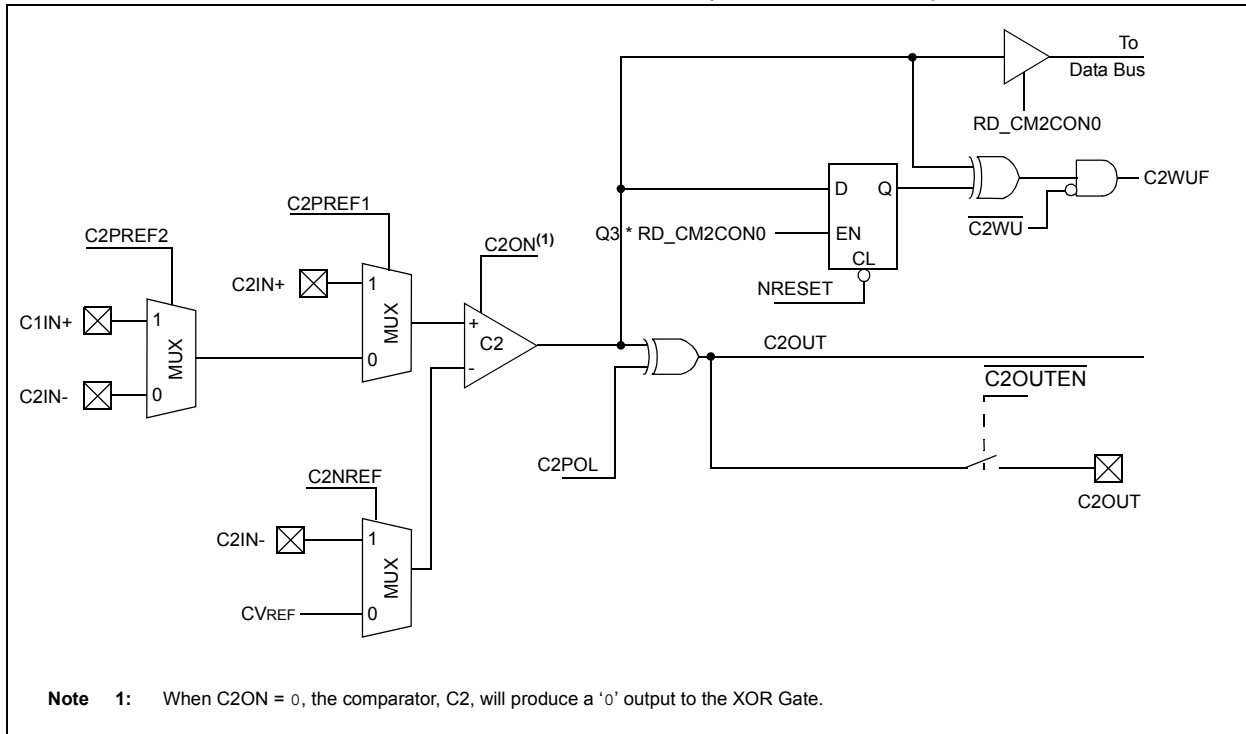


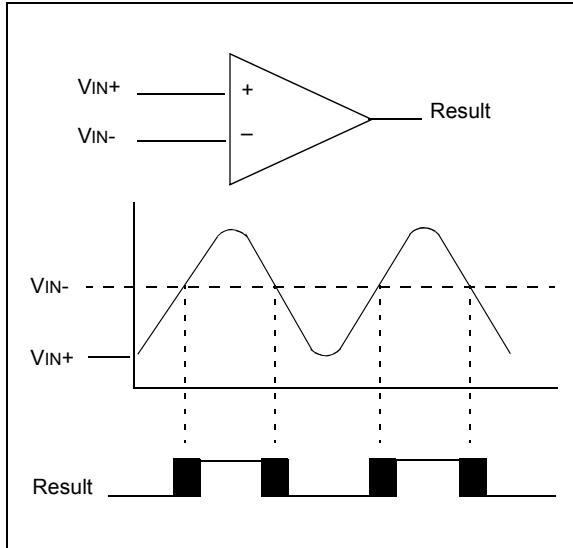
FIGURE 7-2: COMPARATOR 2 BLOCK DIAGRAM (PIC16F506 ONLY)



7.1 Comparator Operation

A single comparator is shown in Figure 7-3 along with the relationship between the analog input levels and the digital output. When the analog input at V_{IN+} is less than the analog input V_{IN-} , the output of the comparator is a digital low level. The shaded area of the output of the comparator in Figure 7-3 represent the uncertainty due to input offsets and response time. See Table 13-1 for Common Mode Voltage.

FIGURE 7-3: SINGLE COMPARATOR



7.2 Comparator Reference

An internal reference signal may be used depending on the comparator operating mode. The analog signal that is present at V_{IN-} is compared to the signal at V_{IN+} , and the digital output of the comparator is adjusted accordingly (Figure 7-3). Please see **Section 8.0 “Comparator Voltage Reference Module (PIC16F506 only)”** for internal reference specifications.

7.3 Comparator Response Time

Response time is the minimum time after selecting a new reference voltage or input source before the comparator output is to have a valid level. If the comparator inputs are changed, a delay must be used to allow the comparator to settle to its new state. Please see Table 13-1 for comparator response time specifications.

7.4 Comparator Output

The comparator output is read through the $CM1CON0$ or $CM2CON0$ register. This bit is read-only. The comparator output may also be used externally, see Figure 7-3.

Note: Analog levels on any pin that is defined as a digital input may cause the input buffer to consume more current than is specified.

7.5 Comparator Wake-up Flag

The Comparator Wake-up Flag is set whenever all of the following conditions are met:

- $\overline{C1WU} = 0$ ($CM1CON0<0>$) or $\overline{C2WU} = 0$ ($CM2CON0<0>$)
- $CM1CON0$ or $CM2CON0$ has been read to latch the last known state of the $C1OUT$ and $C2OUT$ bit ($MOVF CM1CON0, W$)
- Device is in Sleep
- The output of a comparator has changed state

The wake-up flag may be cleared in software or by another device Reset.

7.6 Comparator Operation During Sleep

When the comparator is enabled it is active. To minimize power consumption while in Sleep mode, turn off the comparator before entering Sleep.

7.7 Effects of Reset

A Power-on Reset (POR) forces the $CM2CON0$ register to its Reset state. This forces the Comparator input pins to analog Reset mode. Device current is minimized when analog inputs are present at Reset time.

7.8 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 7-4. Since the analog pins are connected to a digital output, they have reverse biased diodes to V_{DD} and V_{SS} . The analog input, therefore, must be between V_{SS} and V_{DD} . If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur. A maximum source impedance of 10 k Ω is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

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FIGURE 7-4: ANALOG INPUT MODE

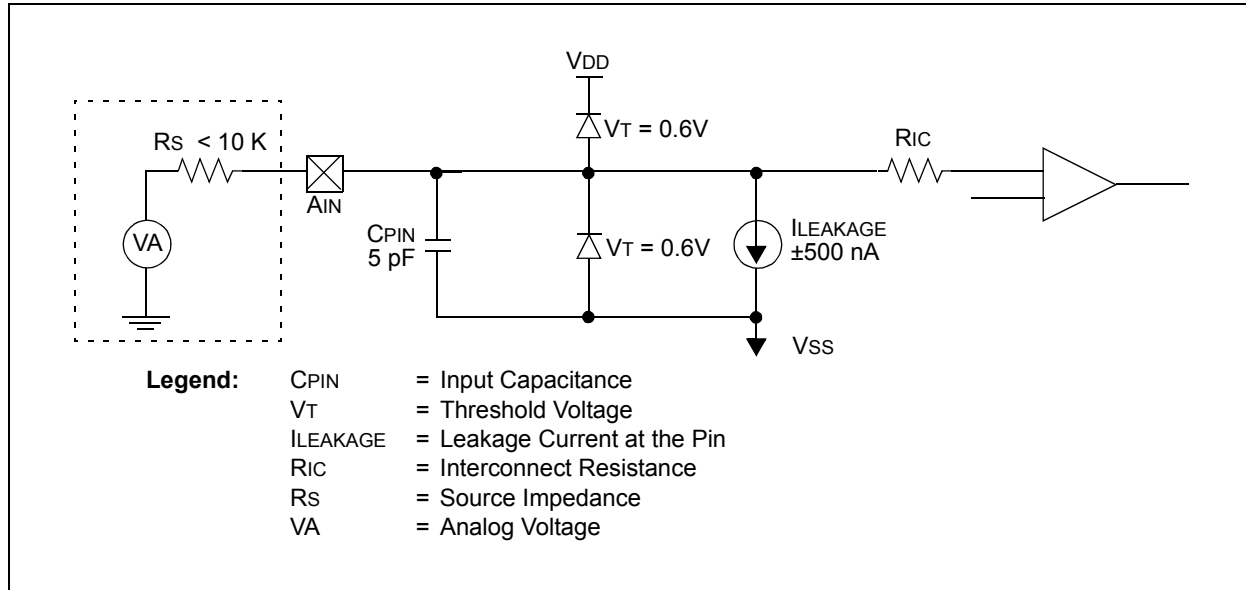


TABLE 7-1: REGISTERS ASSOCIATED WITH COMPARATOR MODULE

| Add | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR | Value on All Other Resets |
|-----|-------------------------|-------|----------------------|----------------------|---------------------|-----------------|--------|---------|-------------------|--------------|---------------------------|
| 03h | STATUS | GPWUF | CWUF | PA0 | \overline{TO} | \overline{PD} | Z | DC | C | 0001 1xxx | qq0q quuu |
| 07h | CM1CON0 ⁽¹⁾ | C1OUT | $\overline{C1OUTEN}$ | C1POL | $\overline{C1T0CS}$ | C1ON | C1NREF | C1PREF | $\overline{C1WU}$ | 1111 1111 | uuuu uuuu |
| 08h | CM1CON0 ⁽²⁾ | C1OUT | $\overline{C1OUTEN}$ | C1POL | $\overline{C1T0CS}$ | C1ON | C1NREF | C1PREF | $\overline{C1WU}$ | 1111 1111 | uuuu uuuu |
| 0Bh | CM2CON0 ⁽²⁾ | C2OUT | $\overline{C2OUTEN}$ | C2POL | C2PREF2 | C2ON | C2NREF | C2PREF1 | $\overline{C2WU}$ | 1111 1111 | uuuu uuuu |
| N/A | TRISB ⁽²⁾ | — | — | I/O Control Register | | | | | | --11 1111 | --11 1111 |
| N/A | TRISC ⁽²⁾ | — | — | I/O Control Register | | | | | | --11 1111 | --11 1111 |
| N/A | TRISGPIO ⁽¹⁾ | — | — | I/O Control Register | | | | | | --11 1111 | --11 1111 |

Legend: x = Unknown, u = Unchanged, — = Unimplemented, read as '0', q = Depends on condition.

Note 1: PIC12F510 only.

Note 2: PIC16F506 only.

8.0 COMPARATOR VOLTAGE REFERENCE MODULE (PIC16F506 ONLY)

The comparator voltage reference module also allows the selection of an internally generated voltage reference for one of the C2 comparator inputs. The VRCON register (Register 8-1) controls the voltage reference module shown in Figure 8-1.

8.1 Configuring The Voltage Reference

The voltage reference can output 32 voltage levels; 16 in a high range and 16 in a low range.

Equation 8-1 determines the output voltages:

EQUATION 8-1:

$$VRR = 1 \text{ (low range): } CVREF = (VR<3:0>/24) \times VDD$$

$$VRR = 0 \text{ (high range):}$$

$$CVREF = (VDD/4) + (VR<3:0> \times VDD/32)$$

8.2 Voltage Reference Accuracy/Error

The full range of VSS to VDD cannot be realized due to construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 8-1) keep CVREF from approaching VSS or VDD. The exception is when the module is disabled by clearing the VREN bit (VRCON<7>). When disabled, the reference voltage is VSS when VR<3:0> is '0000' and the VRR (VRCON<5>) bit is set. This allows the comparator to detect a zero-crossing and not consume the CVREF module current.

The voltage reference is VDD derived and, therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the comparator voltage reference can be found in **Section 13.2 "DC Characteristics: PIC12F510/16F506 (Extended)"**.

REGISTER 8-1: VRCON: VOLTAGE REFERENCE CONTROL REGISTER (PIC16F506 ONLY)

| | | | | | | | |
|-------|-------|-------|-----|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-1 | U-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| VREN | VROE | VRR | — | VR3 | VR2 | VR1 | VR0 |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0', except if denoted otherwise |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

- bit 7 **VREN:** CVREF Enable bit
1 = CVREF is powered on
0 = CVREF is powered down, no current is drawn
- bit 6 **VROE:** CVREF Output Enable bit⁽¹⁾
1 = CVREF output is enabled
0 = CVREF output is disabled
- bit 5 **VRR:** CVREF Range Selection bit
1 = Low range
0 = High range
- bit 4 **Unimplemented:** Read as '1'
- bit 3-0 **VR<3:0>** CVREF Value Selection bit
When VRR = 1: CVREF = (VR<3:0>/24)*VDD
When VRR = 0: CVREF = VDD/4+(VR<3:0>/32)*VDD

Note 1: When this bit is set, the TRIS for the CVREF pin is overridden and the analog voltage is placed on the CVREF pin.

2: CVREF controls for ratio metric reference applies to Comparator 2 on the PIC16F506 only.

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FIGURE 8-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

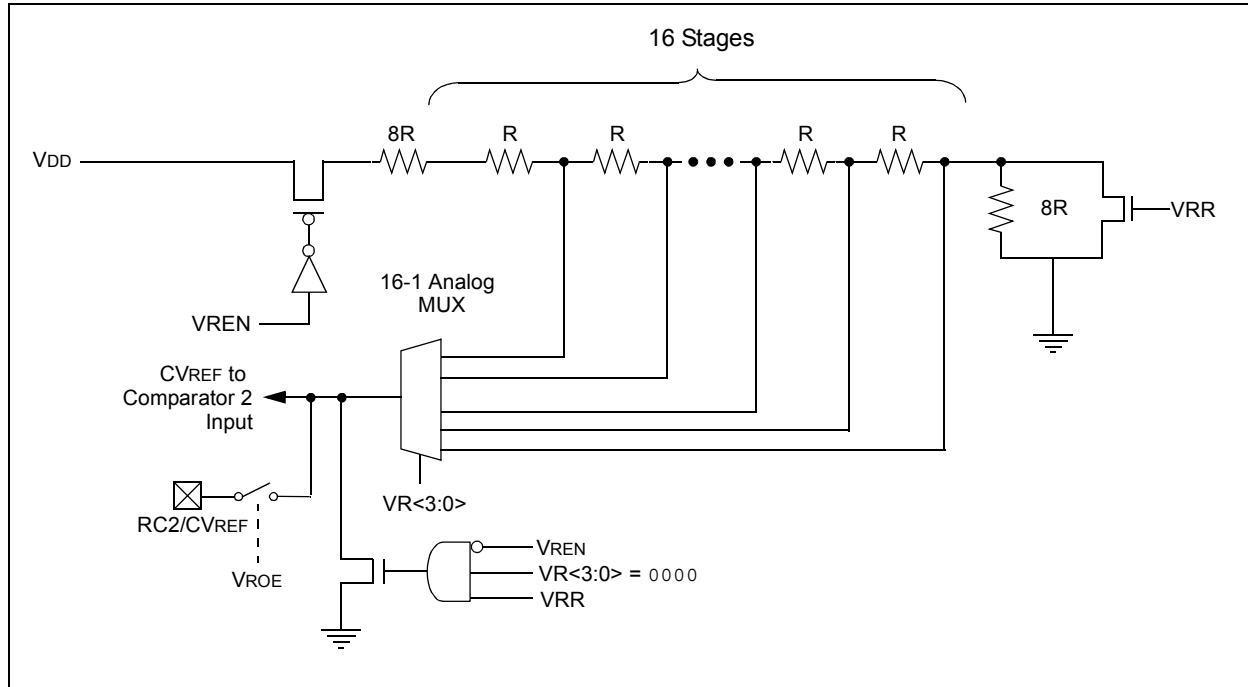


TABLE 8-1: REGISTERS ASSOCIATED WITH COMPARATOR VOLTAGE REFERENCE

| Add | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR | Value on all other Resets |
|-----|------------------------|-------|----------------------|-------|---------------------|-------|--------|---------|-------------------|--------------|---------------------------|
| 0Ch | VRCON | VREN | VROE | VRR | — | VR3 | VR2 | VR1 | VR0 | 001- 1111 | 001- 1111 |
| 08h | CM1CON0 ⁽¹⁾ | C1OUT | $\overline{C1OUTEN}$ | C1POL | $\overline{C1T0CS}$ | C1ON | C1NREF | C1PREF | $\overline{C1WU}$ | 1111 1111 | uuuu uuuu |
| 0Bh | CM2CON0 ⁽¹⁾ | C2OUT | $\overline{C2OUTEN}$ | C2POL | C2PREF2 | C2ON | C2NREF | C2PREF1 | $\overline{C2WU}$ | 1111 1111 | uuuu uuuu |

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'.

Note 1: PIC16F506 only.

9.0 ANALOG-TO-DIGITAL (A/D) CONVERTER

The A/D Converter allows conversion of an analog signal into an 8-bit digital signal.

9.1 Clock Divisors

The ADC has 4 clock source settings ADCS<1:0>. There are 3 divisor values 16, 8 and 4. The fourth setting is INTOSC with a divisor of 4. These settings will allow a proper conversion when using an external oscillator at speeds from 20 MHz to 350 kHz. Using an external oscillator at a frequency below 350 kHz (TAD > 50 μ s) requires the ADC oscillator setting to be INTOSC/4 for valid ADC results.

The ADC requires 13 TAD periods to complete a conversion. The divisor values do not affect the number of TAD periods required to perform a conversion. The divisor values determine the length of the TAD period.

When the ADCS<1:0> bits are changed while an ADC conversion is in process, the new ADC clock source will not be selected until the next conversion is started. This clock source selection will be lost when the device enters Sleep.

9.1.1 VOLTAGE REFERENCE

There is no external voltage reference for the ADC. The ADC reference voltage will always be VDD.

9.1.2 ANALOG MODE SELECTION

The ANS<1:0> bits are used to configure pins for analog input. Upon any Reset, ANS<1:0> defaults to 11. This configures pins AN0, AN1 and AN2 as analog inputs. Pins configured as analog inputs are not available for digital output. Users should not change the ANS bits while a conversion is in process. ANS bits are active regardless of the condition of ADON.

9.1.3 ADC CHANNEL SELECTION

The CHS bits are used to select the analog channel to be sampled by the ADC. The CHS<1:0> bits can be changed at any time without adversely effecting a conversion. To acquire an analog signal the CHS<1:0> selection must match one of the pin(s) selected by the ANS<1:0> bits. When the ADC is on (ADON = 1) and a channel is selected that is also being used by the comparator, then both the comparator and the ADC will see the analog voltage on the pin.

Note: It is the users responsibility to ensure that use of the ADC and comparator simultaneously on the same pin, does not adversely affect the signal being monitored or adversely effect device operation.

When the CHS<1:0> bits are changed during an ADC conversion, the new channel will not be selected until the current conversion is completed. This allows the current conversion to complete with valid results. All channel selection information will be lost when the device enters Sleep.

TABLE 9-1: CHANNEL SELECT (ADCS) BITS AFTER AN EVENT

| Event | ADCS<1:0> |
|-----------------------|-----------|
| MCLR | 11 |
| Conversion completed | CS<1:0> |
| Conversion terminated | CS<1:0> |
| Power-on | 11 |
| Wake from Sleep | 11 |

9.1.4 THE GO/DONE BIT

The GO/DONE bit is used to determine the status of a conversion, to start a conversion and to manually halt a conversion in process. Setting the GO/DONE bit starts a conversion. When the conversion is complete, the ADC module clears the GO/DONE bit. A conversion can be terminated by manually clearing the GO/DONE bit while a conversion is in process. Manual termination of a conversion may result in a partially converted result in ADRES.

The GO/DONE bit is cleared when the device enters Sleep, stopping the current conversion. The ADC does not have a dedicated oscillator, it runs off of the instruction clock. Therefore, no conversion can occur in sleep.

The GO/DONE bit cannot be set when ADON is clear.

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9.1.5 SLEEP

This ADC does not have a dedicated ADC clock, and therefore, no conversion in Sleep is possible. If a conversion is underway and a Sleep command is executed, the GO/DONE and ADON bit will be cleared. This will stop any conversion in process and power-down the ADC module to conserve power. Due to the nature of the conversion process, the ADRES may contain a partial conversion. At least 1 bit must have been converted prior to Sleep to have partial conversion data in ADRES. The ADCS and CHS bits are reset to their default condition; ANS<1:0> = 11 and CHS<1:0> = 11.

- For accurate conversions, TAD must meet the following:
 - 500 ns < TAD < 50 μs
 - TAD = 1/(FOSC/divisor)

Shaded areas indicate TAD out of range for accurate conversions. If analog input is desired at these frequencies, use INTOSC/4 for the ADC clock source.

TABLE 9-2: TAD FOR ADCS SETTINGS WITH VARIOUS OSCILLATORS

| Source | ADCS <1:0> | Divisor | 20 ⁽¹⁾ MHz | 16 ⁽¹⁾ MHz | 8 MHz | 4 MHz | 1 MHz | 500 kHz | 350 kHz | 200 kHz | 100 kHz | 32 kHz |
|--------|------------|---------|-----------------------|-----------------------|-------|-------|-------|---------|---------|---------|---------|--------|
| INTOSC | 11 | 4 | — | — | .5 μs | 1 μs | — | — | — | — | — | — |
| FOSC | 10 | 4 | .2 μs | .25 μs | .5 μs | 1 μs | 4 μs | 8 μs | 11 μs | 20 μs | 40 μs | 125 μs |
| FOSC | 01 | 8 | .4 μs | .5 μs | 1 μs | 2 μs | 8 μs | 16 μs | 23 μs | 40 μs | 80 μs | 250 μs |
| FOSC | 00 | 16 | .8 μs | 1 μs | 2 μs | 4 μs | 16 μs | 32 μs | 46 μs | 80 μs | 160 μs | 500 μs |

Note 1: When operating with external oscillator frequencies of 16 MHz or higher, better ADC performance will result from selection of a suitable FOSC divisor value from Table 9-2 than from use of the INTOSC/4 option for the ADC clock.

TABLE 9-3: EFFECTS OF SLEEP ON ADCON0

| | ANS1 | ANS0 | ADCS1 | ADCS0 | CHS1 | CHS0 | GO/DONE | ADON |
|----------------|-----------|-----------|-------|-------|------|------|---------|------|
| Entering Sleep | Unchanged | Unchanged | 1 | 1 | 1 | 1 | 0 | 0 |
| Wake or Reset | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

9.1.6 ANALOG CONVERSION RESULT REGISTER

The ADRES register contains the results of the last conversion. These results are present during the sampling period of the next analog conversion process. After the sampling period is over, ADRES is cleared (= 0). A 'leading one' is then right shifted into the ADRES to serve as an internal conversion complete bit. As each bit weight, starting with the MSB, is converted, the leading one is shifted right and the converted bit is stuffed into ADRES. After a total of 9 right

shifts of the 'leading one' have taken place, the conversion is complete; the 'leading one' has been shifted out and the $\overline{\text{GO/DONE}}$ bit is cleared.

If the $\overline{\text{GO/DONE}}$ bit is cleared in software during a conversion, the conversion stops. The data in ADRES is the partial conversion result. This data is valid for the bit weights that have been converted. The position of the 'leading one' determines the number of bits that have been converted. The bits that were not converted before the $\overline{\text{GO/DONE}}$ was cleared are unrecoverable.

REGISTER 9-1: ADCON0: A/D CONTROL REGISTER (PIC12F510)

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-----------------------------|-------|
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |
| ANS1 | ANS0 | ADCS1 | ADCS0 | CHS1 | CHS0 | $\overline{\text{GO/DONE}}$ | ADON |
| bit 7 | | | | | | bit 0 | |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 7-6 **ANS<1:0>**: ADC Analog Input Pin Select bits^{(1), (2)}

- 00 = No pins configured for analog input
- 01 = AN2 configured as an analog input
- 10 = AN2 and AN0 configured as analog inputs
- 11 = AN2, AN1 and AN0 configured as analog inputs

bit 5-4 **ADCS<1:0>**: ADC Conversion Clock Select bits

- 00 = Fosc/16
- 01 = Fosc/8
- 10 = Fosc/4
- 11 = INTOSC/4

bit 3-2 **CHS<1:0>**: ADC Channel Select bits

- 00 = Channel AN0
- 01 = Channel AN1
- 10 = Channel AN2
- 11 = 0.6V absolute voltage reference

bit 1 **$\overline{\text{GO/DONE}}$** : ADC Conversion Status bit⁽⁴⁾

- 1 = ADC conversion in progress. Setting this bit starts an ADC conversion cycle. This bit is automatically cleared by hardware when the ADC is done converting.
- 0 = ADC conversion completed/not in progress. Manually clearing this bit while a conversion is in process terminates the current conversion.

bit 0 **ADON**: ADC Enable bit

- 1 = ADC module is operating
- 0 = ADC module is shut-off and consumes no power

Note 1: When the ANS bits are set, the channels selected will automatically be forced into Analog mode, regardless of the pin function previously defined. The only exception to this is the comparator, where the analog input to the comparator and the ADC will be active at the same time. It is the users responsibility to ensure that the ADC loading on the comparator input does not affect their application.

2: The ANS<1:0> bits are active regardless of the condition of ADON.

3: CHS<1:0> bits default to 11 after any Reset.

4: If the ADON bit is clear, the $\overline{\text{GO/DONE}}$ bit cannot be set.

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REGISTER 9-2: ADRES REGISTER

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| R-X | R-X | R-X | R-X | R-X | R-X | R-X | R-X |
| ADRES7 | ADRES6 | ADRES5 | ADRES4 | ADRES3 | ADRES2 | ADRES1 | ADRES0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

EXAMPLE 9-1: PERFORMING AN ANALOG-TO-DIGITAL CONVERSION

```

;Sample code operates out of BANK0
    MOVLW 0xF1      ;configure A/D
    MOVWF ADCON0
    BSF ADCON0, 1  ;start conversion
loop0  BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop0
       MOVF ADRES, W ;read result
       MOVWF result0 ;save result

       BSF ADCON0, 2 ;setup for read of
                       ;channel 1
loop1  BSF ADCON0, 1 ;start conversion
       BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop1
       MOVF ADRES, W ;read result
       MOVWF result1 ;save result

       BSF ADCON0, 3 ;setup for read of
       BCF ADCON0, 2 ;channel 2
loop2  BSF ADCON0, 1 ;start conversion
       BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop2
       MOVF ADRES, W ;read result
       MOVWF result2 ;save result
    
```

EXAMPLE 9-2: CHANNEL SELECTION CHANGE DURING CONVERSION

```

    MOVLW 0xF1      ;configure A/D
    MOVWF ADCON0
    BSF ADCON0, 1  ;start conversion
    BSF ADCON0, 2  ;setup for read of
                       ;channel 1
loop0  BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop0
       MOVF ADRES, W ;read result
       MOVWF result0 ;save result

       BSF ADCON0, 1 ;start conversion
       BSF ADCON0, 3 ;setup for read of
       BCF ADCON0, 2 ;channel 2
loop1  BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop1
       MOVF ADRES, W ;read result
       MOVWF result1 ;save result

       BSF ADCON0, 1 ;start conversion
loop2  BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop2
       MOVF ADRES, W ;read result
       MOVWF result2 ;save result
       CLRF ADCON0 ;optional: returns
                       ;pins to Digital mode and turns off
                       ;the ADC module
    
```


10.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of real-time applications. The PIC12F510/16F506 microcontrollers have a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power-saving operating modes and offer code protection. These features are:

- Oscillator Selection
- Reset:
 - Power-on Reset (POR)
 - Device Reset Timer (DRT)
 - Wake-up from Sleep on Pin Change
- Watchdog Timer (WDT)
- Sleep
- Code Protection
- ID Locations
- In-Circuit Serial Programming™ (ICSP™)
- Clock Out

The PIC12F510/16F506 devices have a Watchdog Timer, which can be shut off only through Configuration bit WDTE. It runs off of its own RC oscillator for added reliability. If using HS (PIC16F506), XT or LP selectable oscillator options, there is always a delay, provided by the Device Reset Timer (DRT), intended to keep the chip in Reset until the crystal oscillator is stable. If using INTOSC, EXTRC or EC there is an 1.125 ms (nominal) delay only on VDD power-up. With this timer on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-Down mode. The user can wake-up from Sleep through a change-on-input pin or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application, including an internal 4/8 MHz oscillator. The EXTRC oscillator option saves system cost while the LP crystal option saves power. A set of Configuration bits are used to select various options.

10.1 Configuration Bits

The PIC12F510/16F506 Configuration Words consist of 12 bits. Configuration bits can be programmed to select various device configurations. Three bits are for the selection of the oscillator type; (two bits on the PIC12F510), one bit is the Watchdog Timer enable bit, one bit is the MCLR enable bit and one bit is for code protection (Register 10-1, Register 10-2).

PIC12F510/16F506

REGISTER 10-1: CONFIG: CONFIGURATION WORD REGISTER (PIC12F510)⁽¹⁾

| | | | | | | | |
|--------|---|---|---|---|---|---|-------|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|---|--------|-------|------------------------|------|-------|-------|
| — | — | IOSCF5 | MCLRE | $\overline{\text{CP}}$ | WDTE | FOSC1 | FOSC0 |
| bit 7 | | | | | | | bit 0 |

- bit 15-6 **Unimplemented:** Read as '1'
- bit 5 **IOSCF5:** Internal Oscillator Frequency Select bit
 1 = 8 MHz INTOSC speed
 0 = 4 MHz INTOSC speed
- bit 4 **MCLRE:** Master Clear Enable bit
 1 = GP3/ $\overline{\text{MCLR}}$ pin functions as $\overline{\text{MCLR}}$
 0 = GP3/ $\overline{\text{MCLR}}$ pin functions as GP3, $\overline{\text{MCLR}}$ internally tied to VDD
- bit 3 **$\overline{\text{CP}}$:** Code Protection bit
 1 = Code protection off
 0 = Code protection on
- bit 2 **WDTE:** Watchdog Timer Enable bit
 1 = WDT enabled
 0 = WDT disabled
- bit 1-0 **FOSC<1:0>:** Oscillator Selection bits
 00 = LP oscillator with 18 ms DRT
 01 = XT oscillator with 18 ms DRT
 10 = INTOSC with 1.125 ms DRT ⁽²⁾
 11 = EXTRC with 1.125 ms DRT ⁽²⁾

- Note 1:** Refer to the "PIC12F510 Memory Programming Specification" (DS41257) to determine how to access the Configuration Word.
- 2:** It is the responsibility of the application designer to ensure the use of the 1.125 ms (nominal) DRT will result in acceptable operation. Refer to Electrical Specifications for VDD rise time and stability requirements for this mode of operation.

REGISTER 10-2: CONFIG: CONFIGURATION WORD REGISTER (PIC16F506)⁽¹⁾

| | | | | | | | |
|--------|--------|-------|-----------------|------|-------|-------|-------|
| | | | | | | | |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |
| | | | | | | | |
| — | IOSCFS | MCLRE | \overline{CP} | WDTE | FOSC2 | FOSC1 | FOSC0 |
| bit 7 | | | | | | | bit 0 |

bit 11-7 **Unimplemented:** Read as '1'

bit 6 **IOSCFS:** Internal Oscillator Frequency Select bit
 1 = 8 MHz INTOSC speed
 0 = 4 MHz INTOSC speed

bit 5 **MCLRE:** Master Clear Enable bit
 1 = RB3/ \overline{MCLR} pin functions as \overline{MCLR}
 0 = RB3/ \overline{MCLR} pin functions as RB3, \overline{MCLR} tied internally to VDD

bit 4 **\overline{CP} :** Code Protection bit
 1 = Code protection off
 0 = Code protection on

bit 3 **WDTE:** Watchdog Timer Enable bit
 1 = WDT enabled
 0 = WDT disabled

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
 000 = LP oscillator and 18 ms DRT
 001 = XT oscillator and 18 ms DRT
 010 = HS oscillator and 18 ms DRT
 011 = EC oscillator with RB4 function on RB4/OSC2/CLKOUT and 1.125 ms DRT⁽²⁾
 100 = INTOSC with RB4 function on RB4/OSC2/CLKOUT and 1.125 ms DRT⁽²⁾
 101 = INTOSC with CLKOUT function on RB4/OSC2/CLKOUT and 1.125 ms DRT⁽²⁾
 110 = EXTRC with RB4 function on RB4/OSC2/CLKOUT and 1.125 ms DRT⁽²⁾
 111 = EXTRC with CLKOUT function on RB4/OSC2/CLKOUT and 1.125 ms DRT⁽²⁾

Note 1: Refer to the "PIC16F506 Memory Programming Specification" (DS41258) to determine how to access the Configuration Word.

2: It is the responsibility of the application designer to ensure the use of the 1.125 ms (nominal) DRT will result in acceptable operation. Refer to Electrical Specifications for VDD rise time and stability requirements for this mode of operation.

PIC12F510/16F506

10.2 Oscillator Configurations

10.2.1 OSCILLATOR TYPES

The PIC12F510/16F506 devices can be operated in up to six different oscillator modes. The user can program up to three Configuration bits (FOSC<1:0> [PIC12F510], FOSC<2:0> [PIC16F506]). To select one of these modes:

- LP: Low-Power Crystal
- XT: Crystal/Resonator
- HS: High-Speed Crystal/Resonator (PIC16F506 only)
- INTOSC: Internal 4/8 MHz Oscillator
- EXTRC: External Resistor/Capacitor
- EC: External High-Speed Clock Input (PIC16F506 only)

10.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In HS (PIC16F506), XT or LP modes, a crystal or ceramic resonator is connected to the (GP5/RB5)/OSC1/(CLKIN) and (GP4/RB4)/OSC2/(CLKOUT) pins to establish oscillation (Figure 10-1). The PIC12F510/16F506 oscillator designs require the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in HS (PIC16F506), XT or LP modes, the device can have an external clock source drive the (GP5/RB5)/OSC1/CLKIN pin (Figure 10-2). When the part is used in this fashion, the output drive levels on the OSC2 pin are very weak. This pin should be left open and unloaded. Also, when using this mode, the external clock should observe the frequency limits for the clock mode chosen (HS, XT or LP).

Note 1: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

2: The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the Oscillator mode may be required.

FIGURE 10-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)

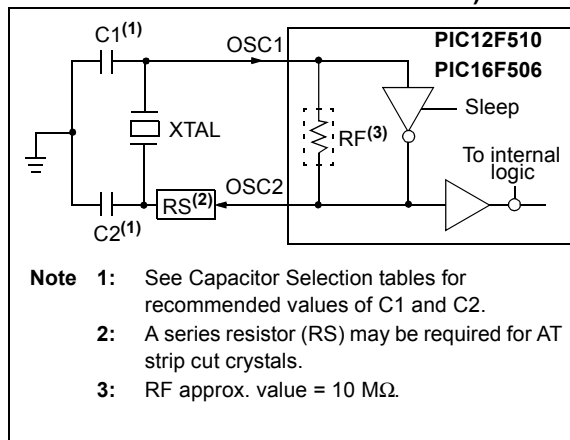


FIGURE 10-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

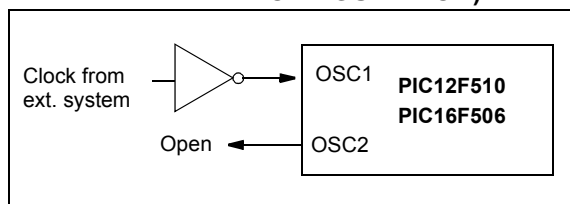


TABLE 10-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS – PIC12F510/16F506⁽¹⁾

| Osc. Type | Resonator Freq. | Cap. Range C1 | Cap. Range C2 |
|-------------------|-----------------|---------------|---------------|
| XT | 4.0 MHz | 30 pF | 30 pF |
| HS ⁽²⁾ | 16 MHz | 10-47 pF | 10-47 pF |

Note 1: These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

2: PIC16F506 only.

TABLE 10-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR – PIC12F510/16F506⁽²⁾

| Osc. Type | Resonator Freq. | Cap. Range C1 | Cap. Range C2 |
|-------------------|-----------------------|---------------|---------------|
| LP | 32 kHz ⁽¹⁾ | 15 pF | 15 pF |
| XT | 200 kHz | 47-68 pF | 47-68 pF |
| | 1 MHz | 15 pF | 15 pF |
| | 4 MHz | 15 pF | 15 pF |
| HS ⁽³⁾ | 20 MHz | 15-47 pF | 15-47 pF |

- Note 1:** For $V_{DD} > 4.5V$, $C1 = C2 \approx 30$ pF is recommended.
- 2:** These values are for design guidance only. Rs may be required to avoid overdriving crystals beyond the drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.
- 3:** PIC16F506 only.

10.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance or one with series resonance.

Figure 10-3 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 k Ω resistor provides the negative feedback for stability. The 10 k Ω potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

FIGURE 10-3: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

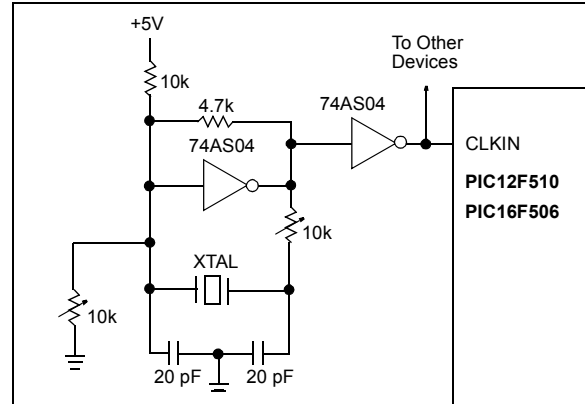
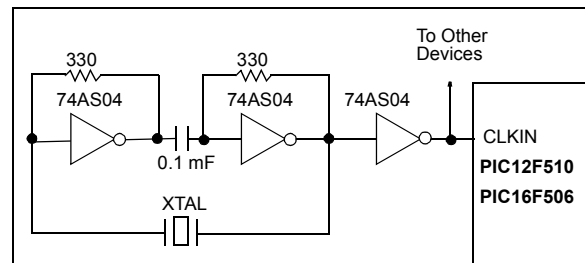


Figure 10-4 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 10-4: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



10.2.4 EXTERNAL RC OSCILLATOR

For timing insensitive applications, the EXTRC device option offers additional cost savings. The EXTRC oscillator frequency is a function of the supply voltage, the resistor (R_{EXT}) and capacitor (C_{EXT}) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit-to-unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low C_{EXT} values. The user also needs to take into account variation due to tolerance of external R and C components used.

Figure 10-5 shows how the R/C combination is connected to the PIC12F510/16F506 devices. For R_{EXT} values below 5.0 k Ω , the oscillator operation may become unstable or stop completely. For very high R_{EXT} values (e.g., 1 M Ω), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping R_{EXT} between 5.0 k Ω and 100 k Ω .

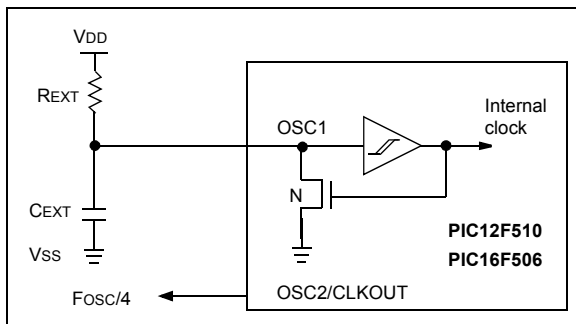
PIC12F510/16F506

Although the oscillator will operate with no external capacitor ($C_{EXT} = 0$ pF), we recommend using values above 20 pF for noise and stability reasons. With no capacitance or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

Section 13.0 “Electrical Characteristics”, shows RC frequency variation from part-to-part due to normal process variation. The variation is larger for larger values of R (since leakage current variation will affect RC frequency more for large R) and for smaller values of C (since variation of input capacitance will affect RC frequency more).

Also, see the Electrical Specifications section for variation of oscillator frequency due to V_{DD} for given R_{EXT}/C_{EXT} values, as well as frequency variation due to operating temperature for given R, C and V_{DD} values.

FIGURE 10-5: EXTERNAL RC OSCILLATOR MODE



10.2.5 INTERNAL 4/8 MHz RC OSCILLATOR

The internal RC oscillator provides a fixed 4/8 MHz (nominal) system clock (see **Section 13.0 “Electrical Characteristics”** for information on variation over voltage and temperature).

In addition, a calibration instruction is programmed into the last address of memory, which contains the calibration value for the internal RC oscillator. This location is always uncode protected, regardless of the code-protect settings. This value is programmed as a `MOVLW XX` instruction where `XX` is the calibration value, and is placed at the Reset vector. This will load the W register with the calibration value upon Reset and the PC will then roll over to the users program at address 0x000. The user then has the option of writing the value to the OSCCAL Register (05h) or ignoring it.

OSCCAL, when written to with the calibration value, will “trim” the internal oscillator to remove process variation from the oscillator frequency.

Note: Erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be read prior to erasing the part so it can be reprogrammed correctly later.

For the PIC12F510/16F506 devices, only bits <7:1> of OSCCAL are used for calibration. See Register 4-5 for more information.

Note: The 0 bit of OSCCAL is unimplemented and should be written as ‘0’ when modifying OSCCAL for compatibility with future devices.

10.3 Reset

The device differentiates between various kinds of Reset:

- Power-on Reset (POR)
- $\overline{\text{MCLR}}$ Reset during normal operation
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Time-out Reset during normal operation
- WDT Time-out Reset during Sleep
- Wake-up from Sleep Reset on pin change
- Wake-up from Sleep Reset on comparator change

Some registers are not reset in any way, they are unknown on POR and unchanged in any other Reset. Most other registers are reset to “Reset state” on Power-on Reset (POR), $\overline{\text{MCLR}}$, WDT or Wake-up from Sleep Reset on pin change or wake-up from Sleep Reset on comparator change. The exceptions are $\overline{\text{TO}}$, $\overline{\text{PD}}$, $\overline{\text{CWUF}}$ and $\overline{\text{RBWUF/GPWUF}}$ bits. They are set or cleared differently in different Reset situations. These bits are used in software to determine the nature of Reset. See Table 10-4 for a full description of Reset states of all registers.

TABLE 10-3: RESET CONDITIONS FOR REGISTERS – PIC12F510

| Register | Address | Power-on Reset | $\overline{\text{MCLR}}$ Reset, WDT Time-out, Wake-up On Pin Change, Wake-up on Comparator Change |
|----------|---------|--------------------------|---|
| W | — | qqqq qqqu ⁽¹⁾ | qqqq qqqu ⁽¹⁾ |
| INDF | 00h | xxxx xxxx | uuuu uuuu |
| TMR0 | 01h | xxxx xxxx | uuuu uuuu |
| PCL | 02h | 1111 1111 | 1111 1111 |
| STATUS | 03h | 0001 1xxx | qq0q quuu ⁽²⁾ |
| FSR | 04h | 110x xxxx | 11uu uuuu |
| OSCCAL | 05h | 1111 111- | uuuu uu- |
| GPIO | 06h | --xx xxxx | --uu uuuu |
| CM1CON0 | 07h | 1111 1111 | uuuu uuuu |
| ADCON0 | 08h | 1111 1100 | uu11 1100 |
| ADRES | 09h | xxxx xxxx | uuuu uuuu |
| OPTION | — | 1111 1111 | 1111 1111 |
| TRISIO | — | --11 1111 | --11 1111 |

Legend: u = unchanged, x = unknown, – = unimplemented bit, read as ‘0’, q = value depends on condition.

Note 1: Bits <7:2> of W register contain oscillator calibration values due to `MOVLW XX` instruction at top of memory.

2: See Table 10-5 for Reset value for specific conditions.

PIC12F510/16F506

TABLE 10-4: RESET CONDITIONS FOR REGISTERS – PIC16F506

| Register | Address | Power-on Reset | MCLR Reset, WDT Time-out, Wake-up On Pin Change, Wake-up on Comparator Change |
|----------|---------|--------------------------|---|
| W | — | qqqq qqqu ⁽¹⁾ | qqqq qqqu ⁽¹⁾ |
| INDF | 00h | xxxx xxxx | uuuu uuuu |
| TMR0 | 01h | xxxx xxxx | uuuu uuuu |
| PCL | 02h | 1111 1111 | 1111 1111 |
| STATUS | 03h | 0001 1xxx | 10uq quuu ⁽²⁾ |
| FSR | 04h | 100x xxxx | 10uu uuuu |
| OSCCAL | 05h | 1111 111- | uuuu uu- |
| PORTB | 06h | --xx xxxx | --uu uuuu |
| PORTC | 07h | --xx xxxx | --uu uuuu |
| CM1CON0 | 08h | 1111 1111 | uuuu uuuu |
| ADCON0 | 09h | 1111 1100 | uu11 1100 |
| ADRES | 0Ah | xxxx xxxx | uuuu uuuu |
| CM2CON0 | 0Bh | 1111 1111 | uuuu uuuu |
| VRCON | 0Ch | 0011 1111 | uuuu uuuu |
| OPTION | — | 1111 1111 | 1111 1111 |
| TRISB | — | --11 1111 | --11 1111 |
| TRISC | — | --11 1111 | --11 1111 |

Legend: u = unchanged, x = unknown, – = unimplemented bit, read as ‘0’, q = value depends on condition.

Note 1: Bits <7:2> of W register contain oscillator calibration values due to MOVLW XX instruction at top of memory.

2: See Table 10-5 for Reset value for specific conditions.

TABLE 10-5: RESET CONDITION FOR SPECIAL REGISTERS

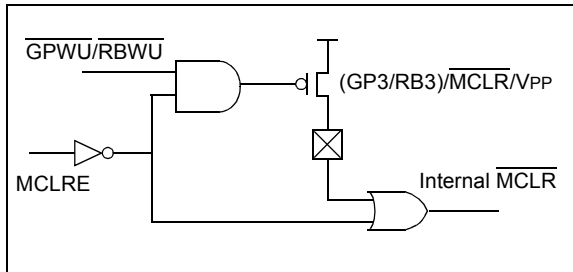
| | STATUS Addr: 03h | PCL Addr: 02h |
|--|------------------|---------------|
| Power-on Reset | 0001 1xxx | 1111 1111 |
| MCLR Reset during normal operation | 000u uuuu | 1111 1111 |
| MCLR Reset during Sleep | 0001 0uuu | 1111 1111 |
| WDT Reset during Sleep | 0000 0uuu | 1111 1111 |
| WDT Reset normal operation | 0000 uuuu | 1111 1111 |
| Wake-up from Sleep Reset on pin change | 1001 0uuu | 1111 1111 |
| Wake from Sleep Reset on Comparator Change | 0101 0uuu | 1111 1111 |

Legend: u = unchanged, x = unknown, – = unimplemented bit, read as ‘0’.

10.3.1 $\overline{\text{MCLR}}$ ENABLE

This Configuration bit, when unprogrammed (left in the '1' state), enables the external MCLR function. When programmed, the $\overline{\text{MCLR}}$ function is tied to the internal VDD and the pin is assigned to be a I/O. See Figure 10-6.

FIGURE 10-6: $\overline{\text{MCLR}}$ SELECT



10.4 Power-on Reset (POR)

The PIC12F510/16F506 devices incorporate an on-chip Power-on Reset (POR) circuitry, which provides an internal chip Reset for most power-up situations.

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. The POR is active regardless of the state of the $\overline{\text{MCLR}}$ enable bit. An internal weak pull-up resistor is implemented using a transistor (refer to Table 13-3 for the pull-up resistor ranges). This will eliminate external RC components usually needed to create an external Power-on Reset. A maximum rise time for VDD is specified. See Section 13.0 "Electrical Characteristics" for details.

When the devices start normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the devices must be held in Reset until the operating parameters are met.

A simplified block diagram of the on-chip Power-on Reset circuit is shown in Figure 10-7.

The Power-on Reset circuit and the Device Reset Timer (see Section 10.5 "Device Reset Timer (DRT)") circuit are closely related. On power-up, the Reset latch is set and the DRT is reset. The DRT timer begins counting once it detects $\overline{\text{MCLR}}$, internal or external, to be high. After the time-out period, it will reset the Reset latch and thus end the on-chip Reset signal.

A power-up example where $\overline{\text{MCLR}}$ is held low is shown in Figure 10-8. VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of Reset TDRT msec after $\overline{\text{MCLR}}$ goes high.

In Figure 10-9, the on-chip Power-on Reset feature is being used ($\overline{\text{MCLR}}$ and VDD are tied together or the pin is programmed to be GP3/RB3). The VDD is stable before the Start-up timer times out and there is no problem in getting a proper Reset. However, Figure 10-10 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses that $\overline{\text{MCLR}}$ is high and when MCLR and VDD actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip may not function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 10-9).

Note: When the devices start normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to Application Notes AN522, "Power-Up Considerations" (DS00522) and AN607, "Power-up Trouble Shooting" (DS00607).

PIC12F510/16F506

FIGURE 10-7: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

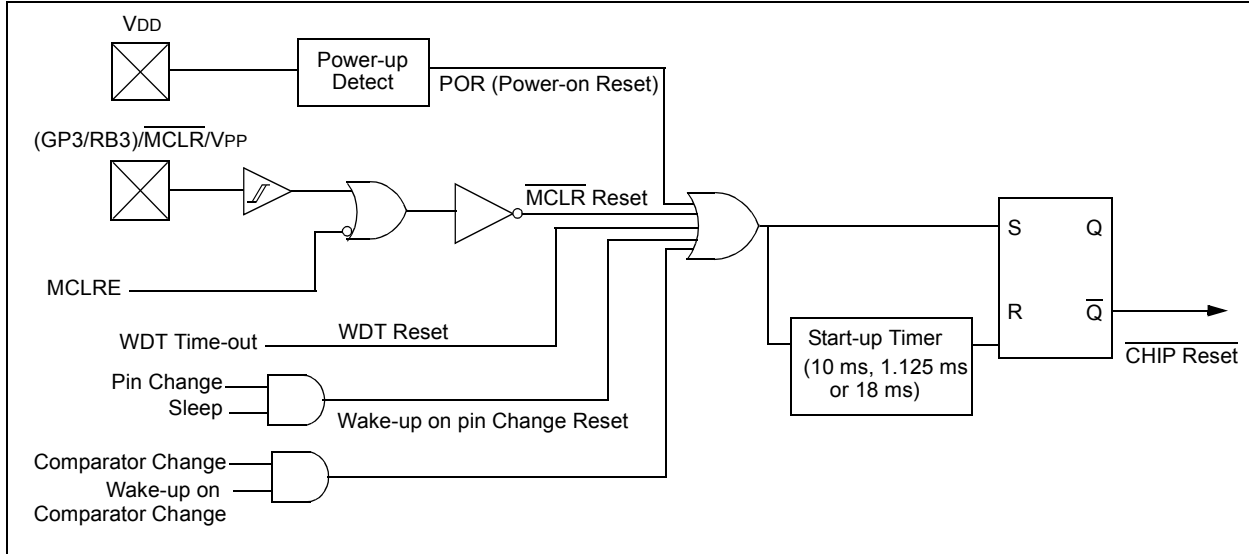


FIGURE 10-8: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ PULLED LOW)

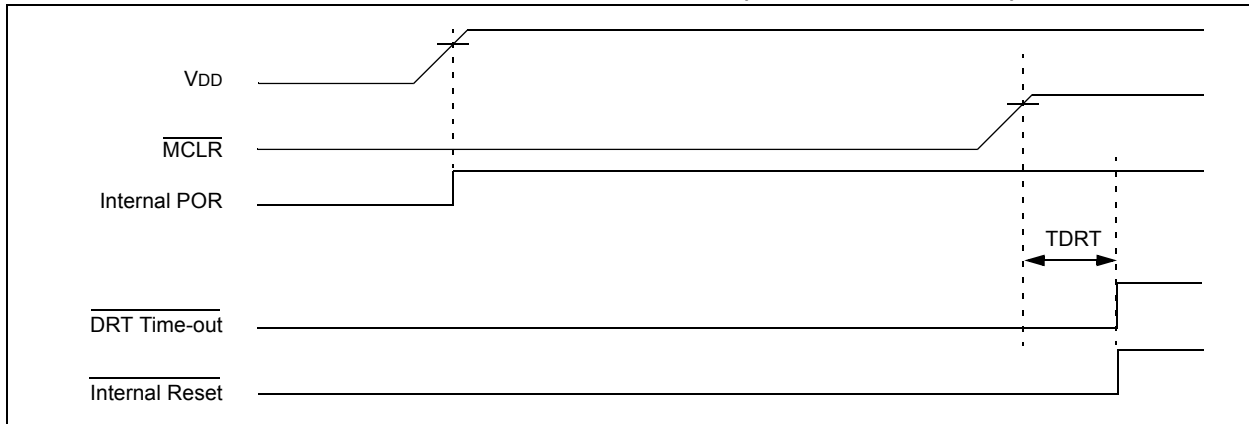


FIGURE 10-9: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD}): FAST V_{DD} RISE TIME

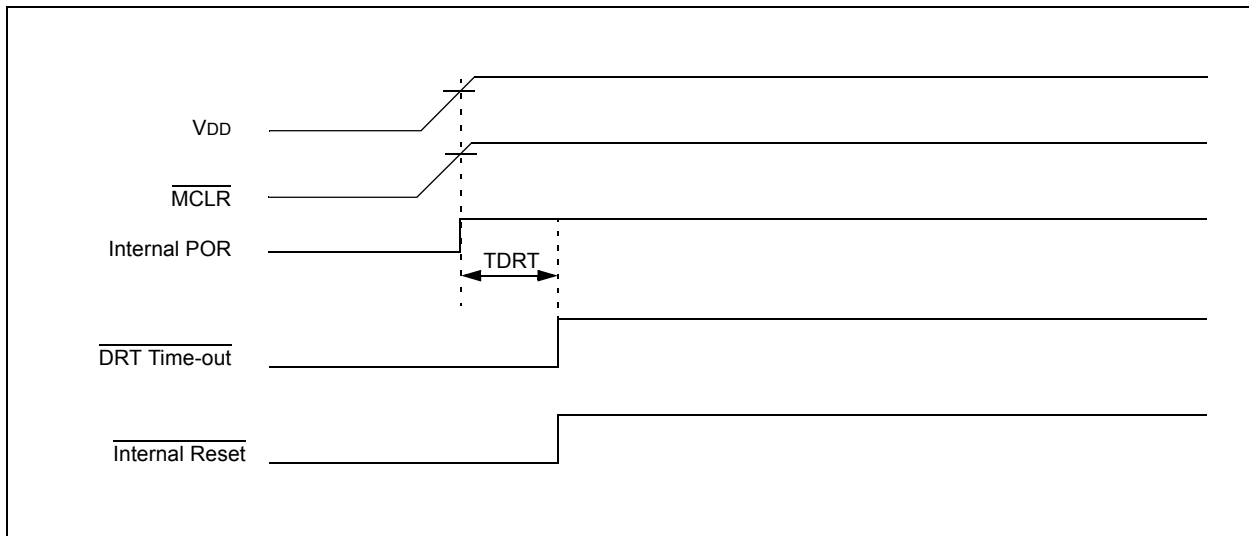


FIGURE 10-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD}): SLOW V_{DD} RISE TIME



PIC12F510/16F506

10.5 Device Reset Timer (DRT)

On the PIC12F510/16F506 devices, the DRT runs any time the device is powered up. DRT runs from Reset and varies based on oscillator selection and Reset type (see Table 10-6).

The DRT operates from a free running on-chip oscillator that is separate from INTOSC. The processor is kept in Reset as long as the DRT is active. The DRT delay allows V_{DD} to rise above V_{DD} minimum and for the oscillator to stabilize.

Oscillator circuits, based on crystals or ceramic resonators, require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the devices in a Reset for a set period, as stated in Table 10-6, after MCLR has reached a logic high (V_{IH} MCLR) level. Programming (GP3/RB3)/MCLR/V_{PP} as MCLR and using an external RC network connected to the MCLR input is not required in most cases. This allows savings in cost-sensitive and/or space restricted applications, as well as allowing the use of the (GP3/RB3)/MCLR/V_{PP} pin as a general purpose input.

The DRT delays will vary from chip-to-chip due to V_{DD}, temperature and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out from Sleep. This is particularly important for applications using the WDT to wake from Sleep mode automatically.

Reset sources are POR, MCLR, WDT time-out, Wake-up on Pin Change and Wake-up on Comparator Change. See Section 10.9.2 “Wake-up from Sleep Reset”, Notes 1, 2 and 3.

10.6 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator that does not require any external components. This RC oscillator is separate from the external RC oscillator of the (GP5/RB5)/OSC1/CLKIN pin and the internal 4/8 MHz oscillator. This means that the WDT will run even if the main processor clock has been stopped, for example, by execution of a SLEEP instruction. During normal operation or Sleep, a WDT Reset or wake-up Reset generates a device Reset.

The \overline{TO} bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset.

The WDT can be permanently disabled by programming the configuration WDTE as a ‘0’ (see Section 10.1 “Configuration Bits”). Refer to the PIC12F510/16F506 Programming Specifications to determine how to access the Configuration Word.

TABLE 10-6: TYPICAL DRT PERIODS

| Oscillator Configuration | POR Reset | Subsequent Resets |
|--------------------------|-----------|-------------------|
| LP | 18 ms | 18 ms |
| XT | 18 ms | 18 ms |
| HS ⁽¹⁾ | 18 ms | 18 ms |
| EC ⁽¹⁾ | 1.125 ms | 10 μs |
| INTOSC | 1.125 ms | 10 μs |
| EXTRC | 1.125 ms | 10 μs |

Note 1: PIC16F506 only

Note: It is the responsibility of the application designer to ensure the use of the 1.125 ms nominal DRT will result in acceptable operation. Refer to Electrical Specifications for V_{DD} rise time and stability requirements for this mode of operation.

10.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms (with no prescaler). If a longer time-out period is desired, a prescaler with a divisor ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, a time-out period of a nominal 2.3 seconds can be realized. These periods vary with temperature, V_{DD} and part-to-part process variations (see DC specs).

Under worst-case conditions (V_{DD} = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

10.6.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device Reset.

The SLEEP instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum Sleep time before a WDT wake-up Reset.

FIGURE 10-11: WATCHDOG TIMER BLOCK DIAGRAM

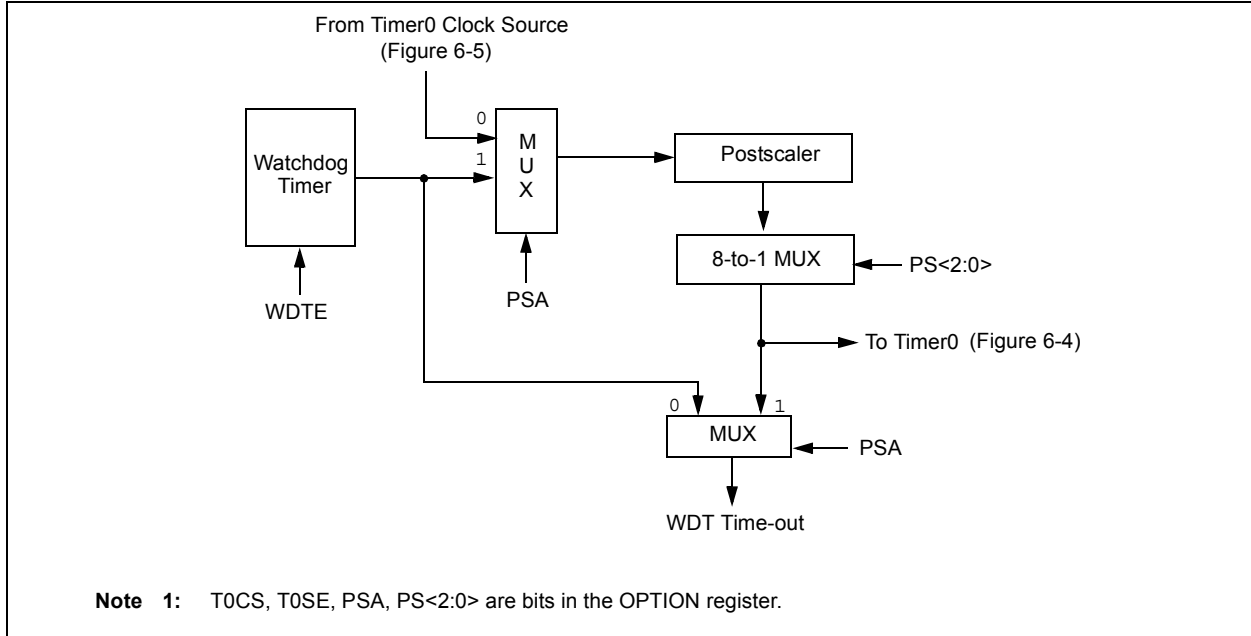


TABLE 10-7: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-On Reset | Value on All Other Resets |
|---------|-----------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------------------------|---------------------------|
| N/A | OPTION ⁽¹⁾ | GPWU | GPPU | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| N/A | OPTION ⁽²⁾ | RBWU | RBPU | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |

Legend: Shaded boxes = Not used by Watchdog Timer. – = unimplemented, read as '0', u = unchanged.

Note 1: PIC12F510 only.

2: PIC16F506 only.

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10.7 Time-out Sequence, Power-down and Wake-up from Sleep Status Bits (TO, PD, GPWUF/RBWUF)

The \overline{TO} , \overline{PD} and (GPWUF/RBWUF) bits in the STATUS register can be tested to determine if a Reset condition has been caused by a power-up condition, a MCLR or Watchdog Timer (WDT) Reset.

TABLE 10-8: $\overline{TO}/\overline{PD}/(GPWUF/RBWUF)$ STATUS AFTER RESET

| CWUF | GPWUF/RBWUF | \overline{TO} | \overline{PD} | Reset Caused By |
|------|-------------|-----------------|-----------------|---|
| 0 | 0 | 0 | 0 | WDT wake-up from Sleep |
| 0 | 0 | 0 | u | WDT time-out (not from Sleep) |
| 0 | 0 | 1 | 0 | MCLR wake-up from Sleep |
| 0 | 0 | 1 | 1 | Power-up |
| 0 | 0 | u | u | \overline{MCLR} not during Sleep |
| 0 | 1 | 1 | 0 | Wake-up from Sleep on pin change |
| 1 | 0 | 1 | 0 | Wake-up from Sleep on comparator change |

Legend: u = unchanged

10.8 Reset on Brown-out

A brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

To reset PIC12F510/16F506 devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 10-12 and Figure 10-13.

FIGURE 10-12: BROWN-OUT PROTECTION CIRCUIT 1

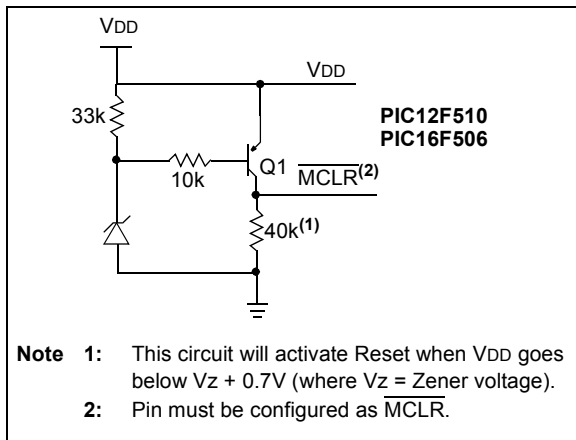


FIGURE 10-13: BROWN-OUT PROTECTION CIRCUIT 2

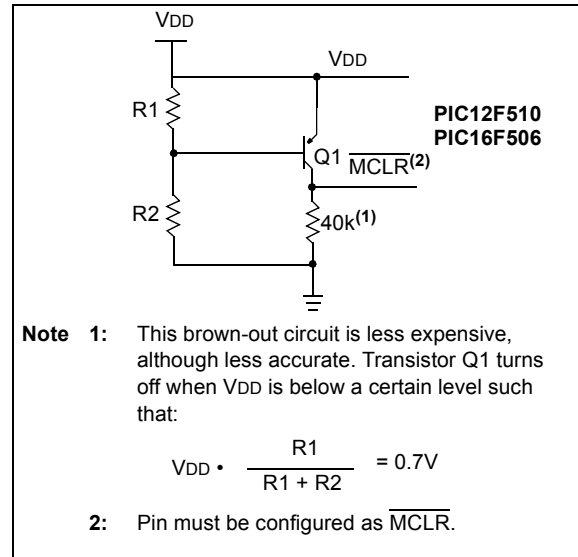
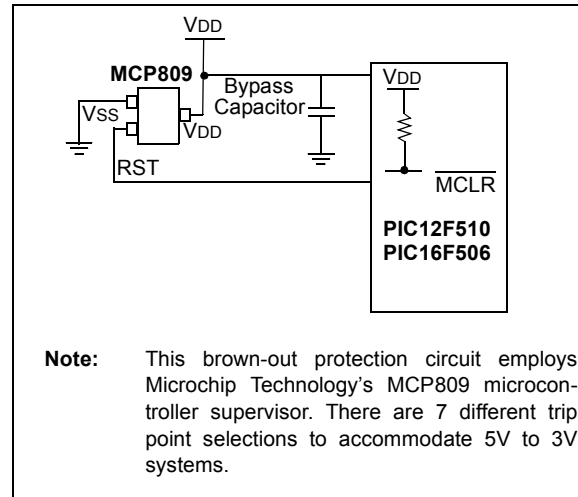


FIGURE 10-14: BROWN-OUT PROTECTION CIRCUIT 3



10.9 Power-Down Mode (Sleep)

A device may be powered down (Sleep) and later powered up (wake-up from Sleep Reset).

10.9.1 SLEEP

The Power-Down mode is entered by executing a `SLEEP` instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the \overline{TO} bit (STATUS<4>) is set, the \overline{PD} bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the `SLEEP` instruction was executed (driving high, driving low or high-impedance).

Note: A device Reset generated by a WDT time-will not drive the MCLR pin low.

For lowest current consumption while powered down, all input pins should be at V_{DD} or V_{SS} and (GP3/RB3)/MCLR/VPP pin must be at a logic high level if MCLR is enabled.

10.9.2 WAKE-UP FROM SLEEP RESET

The device can wake-up from Sleep through one of the following events:

1. An external Reset input on (GP3/RB3)/ \overline{MCLR} /VPP pin when configured as \overline{MCLR} .
2. A Watchdog Timer Time-out Reset (if WDT was enabled).
3. A change-on-input pin GP0/RB0, GP1/RB1, GP3/RB3 or RB4 when wake-up on change is enabled.
4. A change in the comparator output bits, C1OUT and C2OUT (if comparator wake-up is enabled).

These events cause a device Reset. The \overline{TO} , \overline{PD} , CWUF and GPWUF/RBWUF bits can be used to determine the cause of device Reset. The \overline{TO} bit is cleared if a WDT time-out occurred (and caused wake-up). The \overline{PD} bit, which is set on power-up, is cleared when `SLEEP` is invoked. The CWUF bit indicates a change in comparator output state while the device was in Sleep. The GPWUF/RBWUF bit indicates a change in state while in Sleep at pins GP0/RB0, GP1/RB1, GP3/RB3 or RB4 (since the last file or bit operation on GP/RB port).

Note: **Caution:** Right before entering Sleep, read the input pins. When in Sleep, wake-up occurs when the values at the pins change from the state they were in at the last reading. If a wake-up on change occurs and the pins are not read before reentering Sleep, a wake-up will occur immediately even if no pins change while in Sleep mode.

Note 1: Caution: Right before entering Sleep, read the comparator Configuration register(s) CM1CON0 and CM2CON0. When in Sleep, wake-up occurs when the comparator output bit C1OUT and C2OUT change from the state they were in at the last reading. If a wake-up on comparator change occurs and the pins are not read before re-entering Sleep, a wake-up will occur immediately, even if no pins change while in Sleep mode.

2: For 16F506 only.

The WDT is cleared when the device wakes from Sleep, regardless of the wake-up source.

10.10 Program Verification/Code Protection

If the code protection bit has not been programmed, the on-chip program memory can be read out for verification purposes.

The first 64 locations and the last location (OSCCAL) can be read, regardless of the code protection bit setting.

The last memory location can be read regardless of the code protection bit setting on the PIC12F510/16F506 devices.

10.11 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify.

Use only the lower 4 bits of the ID locations and always set the upper 4 bits as '1's. The upper 4 bits are unimplemented.

These locations can be read regardless of the code protect setting.

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10.12 In-Circuit Serial Programming™ (ICSP™)

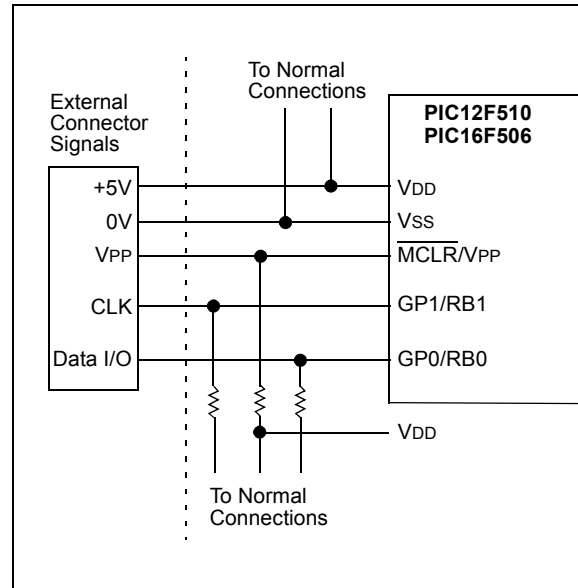
The PIC12F510/16F506 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware, or a custom firmware, to be programmed.

The devices are placed into a Program/Verify mode by holding the GP1/RB1 and GP0/RB0 pins low while raising the MCLR (VPP) pin from V_{IL} to V_{IH} (see programming specification). GP1/RB1 becomes the programming clock and GP0/RB0 becomes the programming data. Both GP1/RB1 and GP0/RB0 are Schmitt Trigger inputs in this mode.

After Reset, a 6-bit command is supplied to the device. Depending on the command and if the command was a Load or a Read, 14 bits of program data are then supplied to or from the device. For complete details of serial programming, please refer to the PIC12F510/16F506 Programming Specifications.

A typical In-Circuit Serial Programming connection is shown in Figure 10-15.

FIGURE 10-15: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



11.0 INSTRUCTION SET SUMMARY

The PIC16 instruction set is highly orthogonal and is comprised of three basic categories.

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 12-bit word divided into an **opcode**, which specifies the instruction type, and one or more **operands** which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 11-1, while the various opcode fields are summarized in Table 11-1.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bits affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

All instructions are executed within a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μ s. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μ s.

Figure 11-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 11-1: GENERAL FORMAT FOR INSTRUCTIONS

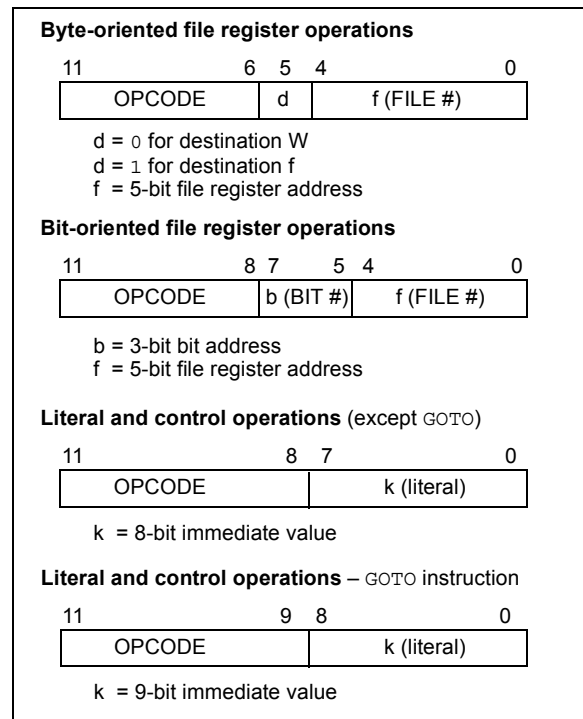


TABLE 11-1: OPCODE FIELD DESCRIPTIONS

| Field | Description |
|-----------------|---|
| f | Register file address (0x00 to 0x7F) |
| W | Working register (accumulator) |
| b | Bit address within an 8-bit file register |
| k | Literal field, constant data or label |
| x | Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools. |
| d | Destination select; d = 0 (store result in W) d = 1 (store result in file register 'f') Default is d = 1 |
| label | Label name |
| TOS | Top-of-Stack |
| PC | Program Counter |
| WDT | Watchdog Timer counter |
| \overline{TO} | Time-out bit |
| \overline{PD} | Power-down bit |
| dest | Destination, either the W register or the specified register file location |
| [] | Options |
| () | Contents |
| → | Assigned to |
| < > | Register bit field |
| ∈ | In the set of |
| <i>italics</i> | User defined term (font is courier) |

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TABLE 11-2: INSTRUCTION SET SUMMARY

| Mnemonic, Operands | Description | Cycles | 12-Bit Opcode | | Status Affected | Notes |
|--|------------------------------|--------|---------------|-----------|--------------------|---------|
| | | | MSb | LSb | | |
| ADDWF f, d | Add W and f | 1 | 0001 | 11df ffff | C, DC, Z | 1, 2, 4 |
| ANDWF f, d | AND W with f | 1 | 0001 | 01df ffff | Z | 2, 4 |
| CLRF f | Clear f | 1 | 0000 | 011f ffff | Z | 4 |
| CLRW – | Clear W | 1 | 0000 | 0100 0000 | Z | |
| COMF f, d | Complement f | 1 | 0010 | 01df ffff | Z | |
| DECF f, d | Decrement f | 1 | 0000 | 11df ffff | Z | 2, 4 |
| DECFSZ f, d | Decrement f, Skip if 0 | 1(2) | 0010 | 11df ffff | None | 2, 4 |
| INCF f, d | Increment f | 1 | 0010 | 10df ffff | Z | 2, 4 |
| INCFSZ f, d | Increment f, Skip if 0 | 1(2) | 0011 | 11df ffff | None | 2, 4 |
| IORWF f, d | Inclusive OR W with f | 1 | 0001 | 00df ffff | Z | 2, 4 |
| MOVF f, d | Move f | 1 | 0010 | 00df ffff | Z | 2, 4 |
| MOVWF f | Move W to f | 1 | 0000 | 001f ffff | None | 1, 4 |
| NOP – | No Operation | 1 | 0000 | 0000 0000 | None | |
| RLF f, d | Rotate left f through Carry | 1 | 0011 | 01df ffff | C | 2, 4 |
| RRF f, d | Rotate right f through Carry | 1 | 0011 | 00df ffff | C | 2, 4 |
| SUBWF f, d | Subtract W from f | 1 | 0000 | 10df ffff | C, DC, Z | 1, 2, 4 |
| SWAPF f, d | Swap f | 1 | 0011 | 10df ffff | None | 2, 4 |
| XORWF f, d | Exclusive OR W with f | 1 | 0001 | 10df ffff | Z | 2, 4 |
| BIT-ORIENTED FILE REGISTER OPERATIONS | | | | | | |
| BCF f, b | Bit Clear f | 1 | 0100 | bbbf ffff | None | 2, 4 |
| BSF f, b | Bit Set f | 1 | 0101 | bbbf ffff | None | 2, 4 |
| BTFSC f, b | Bit Test f, Skip if Clear | 1(2) | 0110 | bbbf ffff | None | |
| BTFSS f, b | Bit Test f, Skip if Set | 1(2) | 0111 | bbbf ffff | None | |
| LITERAL AND CONTROL OPERATIONS | | | | | | |
| ANDLW k | AND literal with W | 1 | 1110 | kkkk kkkk | Z | |
| CALL k | Call Subroutine | 2 | 1001 | kkkk kkkk | None | 1 |
| CLRWDT – | Clear Watchdog Timer | 1 | 0000 | 0000 0100 | TO, PD | |
| GOTO k | Unconditional branch | 2 | 101k | kkkk kkkk | None | |
| IORLW k | Inclusive OR literal with W | 1 | 1101 | kkkk kkkk | Z | |
| MOVLW k | Move literal to W | 1 | 1100 | kkkk kkkk | None | |
| OPTION – | Load OPTION register | 1 | 0000 | 0000 0010 | None | |
| RETLW k | Return, place literal in W | 2 | 1000 | kkkk kkkk | None | |
| SLEEP – | Go into Standby mode | 1 | 0000 | 0000 0011 | TO, PD | |
| TRIS f | Load TRIS register | 1 | 0000 | 0000 0fff | None | 3 |
| XORLW k | Exclusive OR literal to W | 1 | 1111 | kkkk kkkk | Z | |

Note 1: The 9th bit of the Program Counter will be forced to a '0' by any instruction that writes to the PC except for GOTO. See Section 4.6 "Program Counter".

- When an I/O register is modified as a function of itself (e.g. MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- The instruction TRIS f, where f = 6, causes the contents of the W register to be written to the tri-state latches of PORTB. A '1' forces the pin to a high-impedance state and disables the output buffers.
- If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared (if assigned to TMR0).

ADDWF Add W and f

Syntax: [*label*] ADDWF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: (W) + (f) → (dest)

Status Affected: C, DC, Z

Description: Add the contents of the W register and register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

BCF Bit Clear f

Syntax: [*label*] BCF f,b

Operands: $0 \leq f \leq 31$
 $0 \leq b \leq 7$

Operation: $0 \rightarrow (f)$

Status Affected: None

Description: Bit 'b' in register 'f' is cleared.

ANDLW AND literal with W

Syntax: [*label*] ANDLW k

Operands: $0 \leq k \leq 255$

Operation: (W).AND. (k) → (W)

Status Affected: Z

Description: The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

BSF Bit Set f

Syntax: [*label*] BSF f,b

Operands: $0 \leq f \leq 31$
 $0 \leq b \leq 7$

Operation: $1 \rightarrow (f)$

Status Affected: None

Description: Bit 'b' in register 'f' is set.

ANDWF AND W with f

Syntax: [*label*] ANDWF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: (W) .AND. (f) → (dest)

Status Affected: Z

Description: The contents of the W register are AND'ed with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

BTFSC Bit Test f, Skip if Clear

Syntax: [*label*] BTFSC f,b

Operands: $0 \leq f \leq 31$
 $0 \leq b \leq 7$

Operation: skip if (f) = 0

Status Affected: None

Description: If bit 'b' in register 'f' is '0', then the next instruction is skipped. If bit 'b' is '0', then the next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead, making this a two-cycle instruction.

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BTFSS **Bit Test f, Skip if Set**

Syntax: [*label*] BTFSS f,b

Operands: $0 \leq f \leq 31$
 $0 \leq b < 7$

Operation: skip if (f) = 1

Status Affected: None

Description: If bit 'b' in register 'f' is '1', then the next instruction is skipped.
 If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a two-cycle instruction.

CLRW **Clear W**

Syntax: [*label*] CLRW

Operands: None

Operation: 00h → (W);
 1 → Z

Status Affected: Z

Description: The W register is cleared. Zero bit (Z) is set.

CALL **Subroutine Call**

Syntax: [*label*] CALL k

Operands: $0 \leq k \leq 255$

Operation: (PC) + 1 → Top-of-Stack;
 k → PC<7:0>;
 (STATUS <6:5>) → PC<10:9>;
 0 → PC<8>

Status Affected: None

Description: Subroutine call. First, return address (PC + 1) is PUSHed onto the stack. The eight-bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS <6:5>, PC<8> is cleared. CALL is a two-cycle instruction.

CLRWDT **Clear Watchdog Timer**

Syntax: [*label*] CLRWDT

Operands: None

Operation: 00h → WDT;
 0 → WDT prescaler (if assigned);
 1 → \overline{TO} ;
 1 → \overline{PD}

Status Affected: \overline{TO} , \overline{PD}

Description: The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits \overline{TO} and \overline{PD} are set.

CLRF **Clear f**

Syntax: [*label*] CLRF f

Operands: $0 \leq f \leq 31$

Operation: 00h → (f);
 1 → Z

Status Affected: Z

Description: The contents of register 'f' are cleared and the Z bit is set.

COMF **Complement f**

Syntax: [*label*] COMF f,d

Operands: $0 \leq f \leq 31$
 d ∈ [0,1]

Operation: (\bar{f}) → (dest)

Status Affected: Z

Description: The contents of register 'f' are complemented. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

| DECF | Decrement f |
|------------------|--|
| Syntax: | [<i>label</i>] DECF f,d |
| Operands: | $0 \leq f \leq 31$ $d \in [0,1]$ |
| Operation: | $(f) - 1 \rightarrow (\text{dest})$ |
| Status Affected: | Z |
| Description: | Decrement register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'. |

| INCF | Increment f |
|------------------|--|
| Syntax: | [<i>label</i>] INCF f,d |
| Operands: | $0 \leq f \leq 31$ $d \in [0,1]$ |
| Operation: | $(f) + 1 \rightarrow (\text{dest})$ |
| Status Affected: | Z |
| Description: | The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. |

| DECFSZ | Decrement f, Skip if 0 |
|------------------|---|
| Syntax: | [<i>label</i>] DECFSZ f,d |
| Operands: | $0 \leq f \leq 31$ $d \in [0,1]$ |
| Operation: | $(f) - 1 \rightarrow d$; skip if result = 0 |
| Status Affected: | None |
| Description: | The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '0', the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction. |

| INCFSZ | Increment f, Skip if 0 |
|------------------|--|
| Syntax: | [<i>label</i>] INCFSZ f,d |
| Operands: | $0 \leq f \leq 31$ $d \in [0,1]$ |
| Operation: | $(f) + 1 \rightarrow (\text{dest})$, skip if result = 0 |
| Status Affected: | None |
| Description: | The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '0', then the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction. |

| GOTO | Unconditional Branch |
|------------------|--|
| Syntax: | [<i>label</i>] GOTO k |
| Operands: | $0 \leq k \leq 511$ |
| Operation: | $k \rightarrow \text{PC}<8:0>$; $\text{STATUS}<6:5> \rightarrow \text{PC}<10:9>$ |
| Status Affected: | None |
| Description: | GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS <6:5>. GOTO is a two-cycle instruction. |

| IORLW | Inclusive OR literal with W |
|------------------|--|
| Syntax: | [<i>label</i>] IORLW k |
| Operands: | $0 \leq k \leq 255$ |
| Operation: | $(W) .OR. (k) \rightarrow (W)$ |
| Status Affected: | Z |
| Description: | The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register. |

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IORWF **Inclusive OR W with f**

Syntax: [*label*] IORWF f,d
Operands: $0 \leq f \leq 31$
 $d \in [0,1]$
Operation: (W).OR. (f) → (dest)
Status Affected: Z
Description: Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

MOVWF **Move W to f**

Syntax: [*label*] MOVWF f
Operands: $0 \leq f \leq 31$
Operation: (W) → (f)
Status Affected: None
Description: Move data from the W register to register 'f'.

MOVF **Move f**

Syntax: [*label*] MOVF f,d
Operands: $0 \leq f \leq 31$
 $d \in [0,1]$
Operation: (f) → (dest)
Status Affected: Z
Description: The contents of register 'f' are moved to destination 'd'. If 'd' is '0', destination is the W register. If 'd' is '1', the destination is file register 'f'. 'd' = 1 is useful as a test of a file register, since Status flag Z is affected.

NOP **No Operation**

Syntax: [*label*] NOP
Operands: None
Operation: No operation
Status Affected: None
Description: No operation.

MOVLW **Move Literal to W**

Syntax: [*label*] MOVLW k
Operands: $0 \leq k \leq 255$
Operation: $k \rightarrow (W)$
Status Affected: None
Description: The eight-bit literal 'k' is loaded into the W register. The "don't cares" will be assembled as '0's.

OPTION **Load OPTION Register**

Syntax: [*label*] OPTION
Operands: None
Operation: (W) → Option
Status Affected: None
Description: The content of the W register is loaded into the OPTION register.

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RETLW **Return with Literal in W**

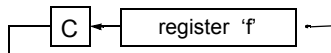
Syntax: [*label*] RETLW *k*
Operands: $0 \leq k \leq 255$
Operation: $k \rightarrow (W)$;
 TOS \rightarrow PC
Status Affected: None
Description: The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

SLEEP **Enter SLEEP Mode**

Syntax: [*label*] SLEEP
Operands: None
Operation: 00h \rightarrow WDT;
 0 \rightarrow WDT prescaler;
 1 \rightarrow \overline{TO} ;
 0 \rightarrow \overline{PD}
Status Affected: \overline{TO} , \overline{PD} , RBWUF
Description: Time-out Status bit (\overline{TO}) is set. The Power-down Status bit (\overline{PD}) is cleared.
 RBWUF is unaffected.
 The WDT and its prescaler are cleared.
 The processor is put into Sleep mode with the oscillator stopped.
 See **Section 10.9 "Power-Down Mode (Sleep)"** on Sleep for more details.

RLF **Rotate Left f through Carry**

Syntax: [*label*] RLF *f,d*
Operands: $0 \leq f \leq 31$
 $d \in [0,1]$
Operation: See description below
Status Affected: C
Description: The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.

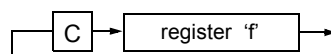


SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF *f,d*
Operands: $0 \leq f \leq 31$
 $d \in [0,1]$
Operation: $(f) - (W) \rightarrow (\text{dest})$
Status Affected: C, DC, Z
Description: Subtract (2's complement method) the W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

RRF **Rotate Right f through Carry**

Syntax: [*label*] RRF *f,d*
Operands: $0 \leq f \leq 31$
 $d \in [0,1]$
Operation: See description below
Status Affected: C
Description: The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF *f,d*
Operands: $0 \leq f \leq 31$
 $d \in [0,1]$
Operation: $(f<3:0>) \rightarrow (\text{dest}<7:4>)$;
 $(f<7:4>) \rightarrow (\text{dest}<3:0>)$
Status Affected: None
Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in W register. If 'd' is '1', the result is placed in register 'f'.

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TRIS **Load TRIS Register**

Syntax: [*label*] TRIS *f*
Operands: *f* = 6
Operation: (*W*) → TRIS register *f*
Status Affected: None
Description: TRIS register '*f*' (*f* = 6 or 7) is loaded with the contents of the *W* register

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF *f,d*
Operands: $0 \leq f \leq 31$
 $d \in [0,1]$
Operation: (*W*) .XOR. (*f*) → (*dest*)
Status Affected: Z
Description: Exclusive OR the contents of the *W* register with register '*f*'. If '*d*' is '0', the result is stored in the *W* register. If '*d*' is '1', the result is stored back in register '*f*'.

XORLW **Exclusive OR literal with W**

Syntax: [*label*] XORLW *k*
Operands: $0 \leq k \leq 255$
Operation: (*W*) .XOR. *k* → (*W*)
Status Affected: Z
Description: The contents of the *W* register are XOR'ed with the eight-bit literal '*k*'. The result is placed in the *W* register.

12.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
 - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
 - MPASM™ Assembler
 - MPLAB C18 and MPLAB C30 C Compilers
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB ASM30 Assembler/Linker/Library
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debugger
 - MPLAB ICD 2
- Device Programmers
 - PICSTART® Plus Development Programmer
 - MPLAB PM3 Device Programmer
 - PICKit™ 2 Development Programmer
- Low-Cost Demonstration and Development Boards and Evaluation Kits

12.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
 - Simulator
 - Programmer (sold separately)
 - Emulator (sold separately)
 - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Visual device initializer for easy register initialization
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as HI-TECH Software C Compilers and IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
 - Source files (assembly or C)
 - Mixed assembly and C
 - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

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12.2 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for all PIC MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

12.3 MPLAB C18 and MPLAB C30 C Compilers

The MPLAB C18 and MPLAB C30 Code Development Systems are complete ANSI C compilers for Microchip's PIC18 and PIC24 families of microcontrollers and the dsPIC30 and dsPIC33 family of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

12.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

12.5 MPLAB ASM30 Assembler, Linker and Librarian

MPLAB ASM30 Assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

12.6 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C18 and MPLAB C30 C Compilers, and the MPASM and MPLAB ASM30 Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

12.7 MPLAB ICE 2000 High-Performance In-Circuit Emulator

The MPLAB ICE 2000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers. Software control of the MPLAB ICE 2000 In-Circuit Emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The architecture of the MPLAB ICE 2000 In-Circuit Emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE 2000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows® 32-bit operating system were chosen to best make these features available in a simple, unified application.

12.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC® and MCU devices. It debugs and programs PIC® and dsPIC® Flash microcontrollers with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The MPLAB REAL ICE probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with the popular MPLAB ICD 2 system (RJ11) or with the new high speed, noise tolerant, low-voltage differential signal (LVDS) interconnection (CAT5).

MPLAB REAL ICE is field upgradeable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added, such as software breakpoints and assembly code trace. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, real-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

12.9 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PIC MCUs and can be used to develop for these and other PIC MCUs and dsPIC DSCs. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip's In-Circuit Serial Programming™ (ICSP™) protocol, offers cost-effective, in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single stepping and watching variables, and CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real time. MPLAB ICD 2 also serves as a development programmer for selected PIC devices.

12.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.

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12.11 PICSTART Plus Development Programmer

The PICSTART Plus Development Programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus Development Programmer supports most PIC devices in DIP packages up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus Development Programmer is CE compliant.

12.12 PICkit 2 Development Programmer

The PICkit™ 2 Development Programmer is a low-cost programmer and selected Flash device debugger with an easy-to-use interface for programming many of Microchip's baseline, mid-range and PIC18F families of Flash memory microcontrollers. The PICkit 2 Starter Kit includes a prototyping development board, twelve sequential lessons, software and HI-TECH's PICC™ Lite C compiler, and is designed to help get up to speed quickly using PIC® microcontrollers. The kit provides everything needed to program, evaluate and develop applications using Microchip's powerful, mid-range Flash memory family of microcontrollers.

12.13 Demonstration, Development and Evaluation Boards

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart® battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Check the Microchip web page (www.microchip.com) and the latest "Product Selector Guide" (DS00148) for the complete list of demonstration, development and evaluation kits.

13.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

| | |
|---|-----------------------|
| Ambient temperature under bias | -40°C to +125°C |
| Storage temperature | -65°C to +150°C |
| Voltage on VDD with respect to VSS | 0 to +7.0V |
| Voltage on $\overline{\text{MCLR}}$ with respect to VSS..... | 0 to +14V |
| Voltage on all other pins with respect to VSS | -0.3V to (VDD + 0.3V) |
| Total power dissipation ⁽¹⁾ | 700 mW |
| Max. current out of VSS pin | 200 mA |
| Max. current into VDD pin | 150 mA |
| Input clamp current, I _{IK} (V _I < 0 or V _I > VDD)..... | ±20 mA |
| Output clamp current, I _{OK} (V _O < 0 or V _O > VDD)..... | ±20 mA |
| Max. output current sunk by any I/O pin | 25 mA |
| Max. output current sourced by any I/O pin | 25 mA |
| Max. output current sourced by I/O port | 100 mA |
| Max. output current sunk by I/O port | 100 mA |

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

†NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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FIGURE 13-1: VOLTAGE-FREQUENCY GRAPH, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (PIC12F510)

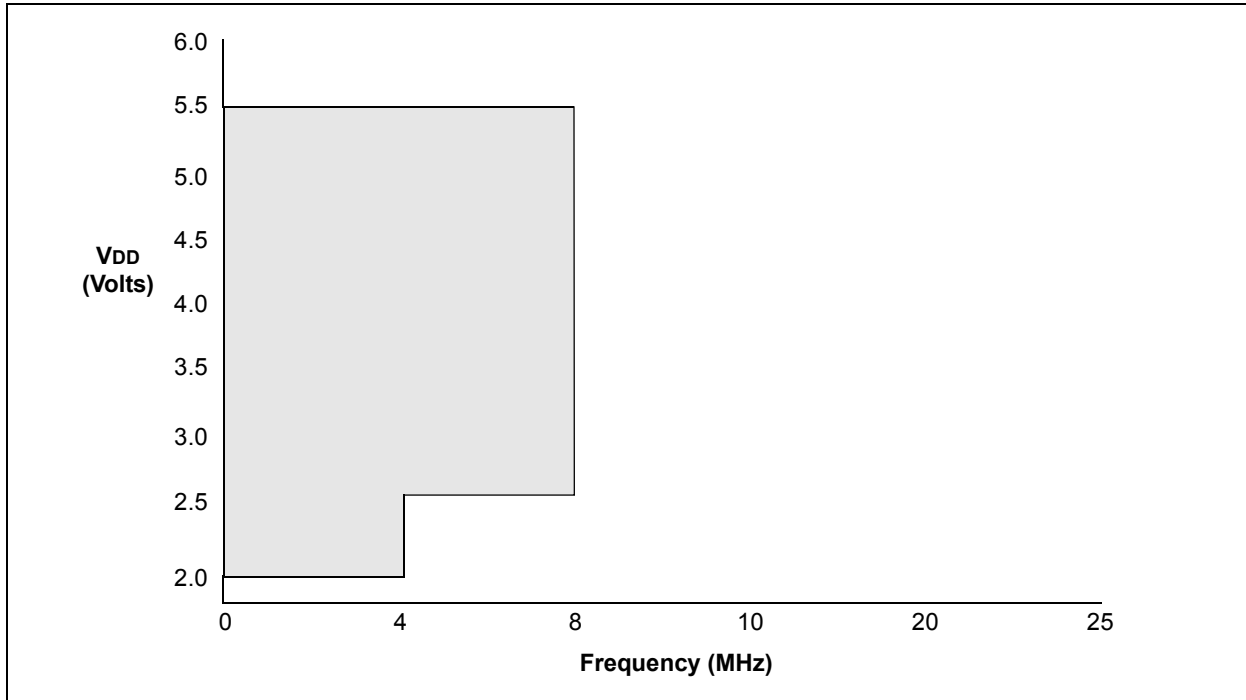


FIGURE 13-2: MAXIMUM OSCILLATOR FREQUENCY TABLE (PIC12F510)

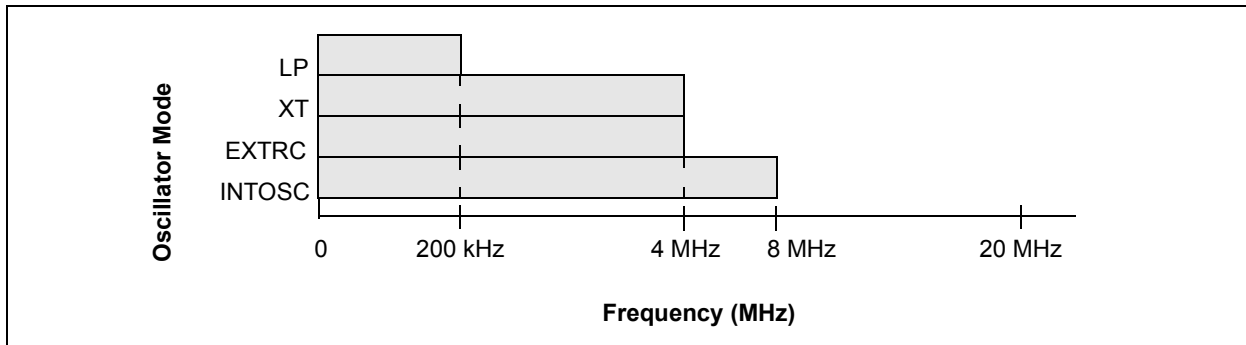


FIGURE 13-3: VOLTAGE FREQUENCY GRAPH, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (PIC16F506)

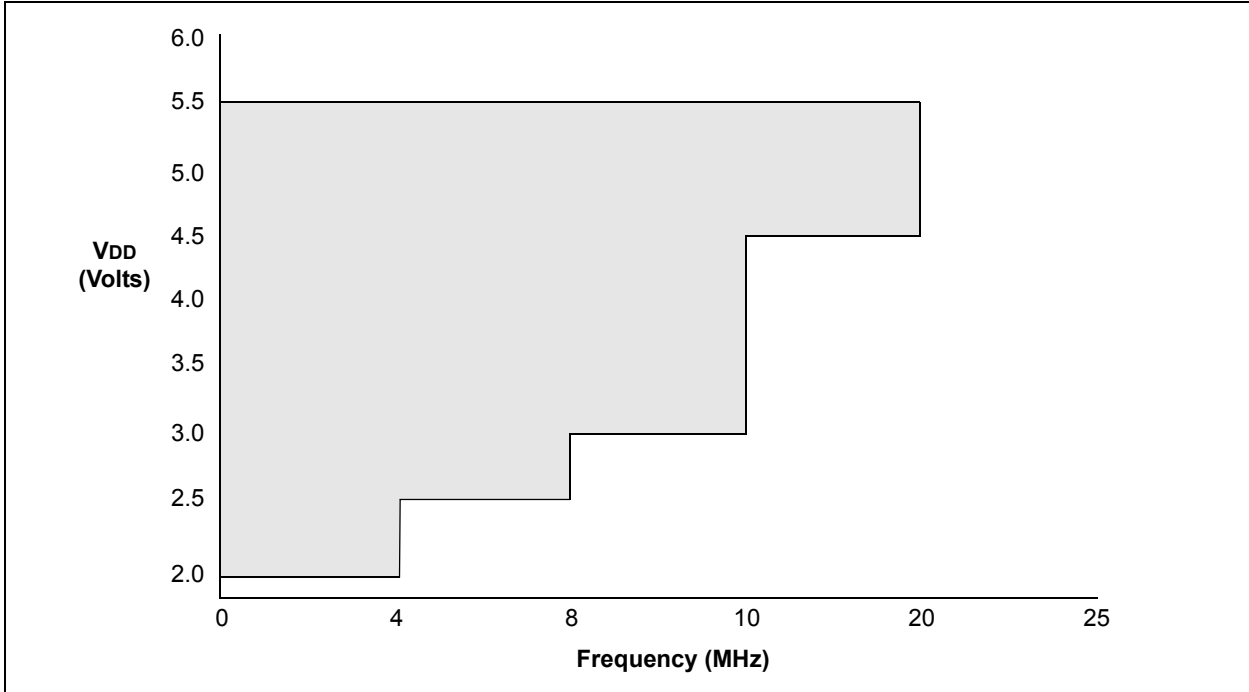
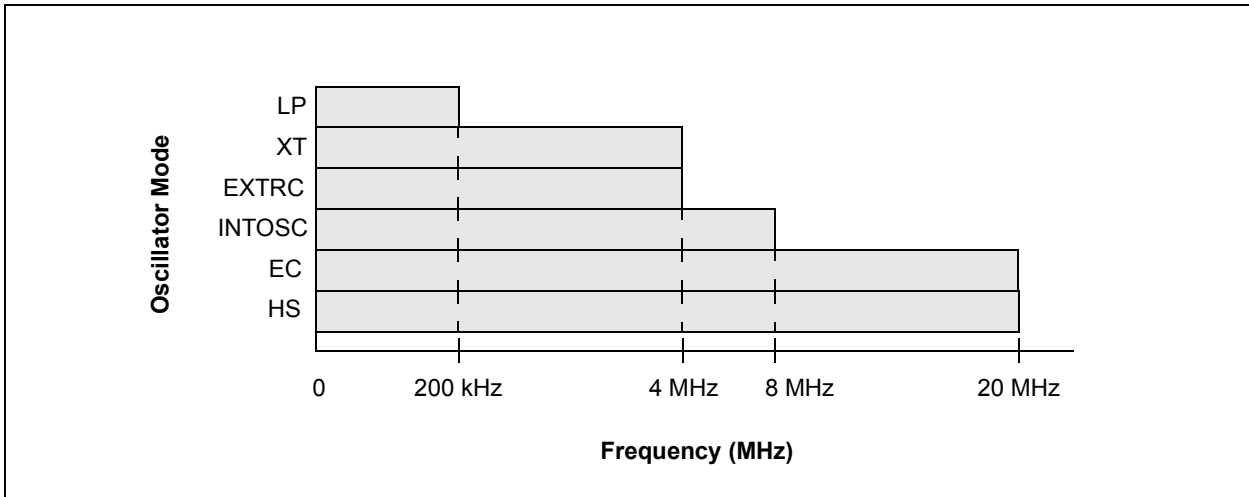


FIGURE 13-4: MAXIMUM OSCILLATOR FREQUENCY TABLE (PIC16F506)



PIC12F510/16F506

13.1 DC Characteristics: PIC12F510/16F506 (Industrial)

| DC Characteristics | | | Standard Operating Conditions (unless otherwise specified) Operating Temperature 40°C ≤ TA ≤ +85°C (industrial) | | | | |
|--------------------|--------|---|--|---------------------------|------|-------|--|
| Param No. | Sym | Characteristic | Min | Typ ⁽¹⁾ | Max | Units | Conditions |
| D001 | VDD | Supply Voltage | 2.0 | | 5.5 | V | See Figure 14-1 |
| D002 | VDR | RAM Data Retention Voltage ⁽²⁾ | — | 1.5* | — | V | Device in Sleep mode |
| D003 | VPOR | VDD Start Voltage to ensure Power-on Reset | — | VSS | — | V | See Section 10.4 “Power-on Reset (POR)” for details |
| D004 | SVDD | VDD Rise Rate to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 10.4 “Power-on Reset (POR)” for details |
| D010 | IDD | Supply Current ^(3,4) | — | 175 | 275 | μA | FOSC = 4 MHz, VDD = 2.0V |
| | | | — | 0.625 | 1.1 | mA | FOSC = 4 MHz, VDD = 5.0V |
| | | | — | 250 | 450 | μA | FOSC = 8 MHz, VDD = 2.0V |
| | | | — | 1.0 | 1.5 | mA | FOSC = 8 MHz, VDD = 5.0V |
| — | 1.4 | 2.0 | mA | FOSC = 20 MHz, VDD = 5.0V | | | |
| — | 11 | 15 | μA | FOSC = 32 kHz, VDD = 2.0V | | | |
| — | 38 | 52 | μA | FOSC = 32 kHz, VDD = 5.0V | | | |
| D020 | IPD | Power-down Current ⁽⁵⁾ | — | 0.1 | 1.2 | μA | VDD = 2.0V |
| | | | — | 0.35 | 2.4 | μA | VDD = 5.0V |
| D022 | IWDT | WDT Current ⁽⁵⁾ | — | 1.0 | 3.0 | μA | VDD = 2.0V |
| | | | — | 7.0 | 16.0 | μA | VDD = 5.0V |
| D023 | ICMP | Comparator Current ⁽⁵⁾ | — | 15 | 22 | μA | VDD = 2.0V (per comparator) |
| | | | — | 55 | 67 | μA | VDD = 5.0V (per comparator) |
| D022 | ICVREF | CVREF Current ⁽⁵⁾ | — | 30 | 60 | μA | VDD = 2.0V (high range) |
| | | | — | 75 | 125 | μA | VDD = 5.0V (high range) |
| D023 | IFVR | Internal 0.6V Fixed Voltage Reference Current ⁽⁵⁾ | — | 85 | 120 | μA | VDD = 2.0V (0.6V reference and 1 comparator enabled) |
| | | | — | 175 | 205 | μA | VDD = 5.0V (0.6V reference and 1 comparator enabled) |
| D024 | ΔIAD | A/D Conversion Current ⁽⁵⁾ | — | 120 | 150 | μA | 2.0V |
| | | | — | 200 | 250 | μA | 5.0V |

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- 2: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.
- 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
- 4: The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VSS, TOCKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
- 5: For standby current measurements, the conditions are the same as IDD, except that the device is in Sleep mode. If a module current is listed, the current is for that specific module enabled and the device in Sleep.
- 6: Does not include current through REXT. The current through the resistor can be estimated by the formula:
 $I = VDD/2REXT$ (mA) with REXT in kΩ.

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13.2 DC Characteristics: PIC12F510/16F506 (Extended)

| DC Characteristics | | | Standard Operating Conditions (unless otherwise specified) Operating Temperature 40°C ≤ TA ≤ +125°C (extended) | | | | |
|--------------------|--------|--|---|--|------|-------|--|
| Param No. | Sym | Characteristic | Min | Typ ⁽¹⁾ | Max | Units | Conditions |
| D001 | VDD | Supply Voltage | 2.0 | | 5.5 | V | See Figure 14-1 |
| D002 | VDR | RAM Data Retention Voltage⁽²⁾ | — | 1.5* | — | V | Device in Sleep mode |
| D003 | VPOR | VDD Start Voltage to ensure Power-on Reset | — | VSS | — | V | See Section 10.4 “Power-on Reset (POR)” for details |
| D004 | SVDD | VDD Rise Rate to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 10.4 “Power-on Reset (POR)” for details |
| D010 | IDD | Supply Current^(3,4) | — | 175 | 275 | μA | FOSC = 4 MHz, VDD = 2.0V FOSC = 4 MHz, VDD = 5.0V |
| | | | — | 0.625 | 1.1 | mA | |
| | | | — | 250 | 450 | μA | FOSC = 8 MHz, VDD = 2.0V FOSC = 8 MHz, VDD = 5.0V |
| | | | — | 1.0 | 1.5 | mA | |
| | | | — | 1.4 | 2.0 | mA | FOSC = 20 MHz, VDD = 5.0V |
| — | 11 | 16 | μA | FOSC = 32 kHz, VDD = 2.0V FOSC = 32 kHz, VDD = 5.0V | | | |
| — | 38 | 54 | μA | | | | |
| D020 | IPD | Power-down Current⁽⁵⁾ | — | 0.1 | 9.0 | μA | VDD = 2.0V |
| | | | — | 0.35 | 15.0 | μA | VDD = 5.0V |
| D022 | IWDT | WDT Current⁽⁵⁾ | — | 1.0 | 18 | μA | VDD = 2.0V |
| | | | — | 7.0 | 22 | μA | VDD = 5.0V |
| D023 | ICMP | Comparator Current⁽⁵⁾ | — | 15 | 25 | μA | VDD = 2.0V (per comparator) |
| | | | — | 55 | 75 | μA | VDD = 5.0V (per comparator) |
| D022 | ICVREF | CVREF Current⁽⁵⁾ | — | 30 | 65 | μA | VDD = 2.0V (high range) |
| | | | — | 75 | 135 | μA | VDD = 5.0V (high range) |
| D023 | IFVR | Internal 0.6V Fixed Voltage Reference Current⁽⁵⁾ | — | 85 | 130 | μA | VDD = 2.0V (0.6V reference and 1 comparator enabled) |
| | | | — | 175 | 220 | μA | VDD = 5.0V (0.6V reference and 1 comparator enabled) |
| D024 | ΔIAD | A/D Conversion Current⁽⁵⁾ | — | 120 | 150 | μA | 2.0V |
| | | | — | 200 | 250 | μA | 5.0V |

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

4: The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VSS, TOCKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

5: For standby current measurements, the conditions are the same as IDD, except that the device is in Sleep mode. If a module current is listed, the current is for that specific module enabled and the device in Sleep.

6: Does not include current through REXT. The current through the resistor can be estimated by the formula: $I = VDD/2REXT$ (mA) with REXT in kΩ.

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13.3 DC Characteristics: PIC12F510/16F506 (Industrial, Extended)

| DC CHARACTERISTICS | | Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) | | | | | |
|--------------------|-------------------|---|--------------------------------|------|----------------------|-------|--|
| Param No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
| | V _{IL} | Input Low Voltage | | | | | |
| D030 | | I/O ports with TTL buffer | V _{SS} | — | 0.8V | V | For $4.5 \leq V_{DD} \leq 5.5\text{V}$ otherwise |
| D030A | | | V _{SS} | — | 0.15 V _{DD} | V | |
| D031 | | with Schmitt Trigger buffer | V _{SS} | — | 0.15 V _{DD} | V | |
| D032 | | MCLR, T0CKI | V _{SS} | — | 0.15 V _{DD} | V | |
| D033 | | OSC1 (in EXTRC), EC ⁽¹⁾ | V _{SS} | — | 0.15 V _{DD} | V | |
| D033 | | OSC1 (in HS) | V _{SS} | — | 0.3 V _{DD} | V | |
| D033 | | OSC1 (in XT and LP) | V _{SS} | — | 0.3 V _{DD} | V | |
| | V _{IH} | Input High Voltage | | | | | |
| D040 | | I/O ports with TTL buffer | 2.0 | — | V _{DD} | V | $4.5 \leq V_{DD} \leq 5.5\text{V}$ Otherwise |
| D040A | | | 0.25 V _{DD} + 0.8V | — | V _{DD} | V | |
| D041 | | with Schmitt Trigger buffer | 0.85 V _{DD} | — | V _{DD} | V | For entire V _{DD} range |
| D042 | | MCLR, T0CKI | 0.85 V _{DD} | — | V _{DD} | V | |
| D043 | | OSC1 (in EXTRC), EC ⁽¹⁾ | 0.85 V _{DD} | — | V _{DD} | V | |
| D043 | | OSC1 (in HS) | 0.7 V _{DD} | — | V _{DD} | V | |
| D043 | | OSC1 (in XT and LP) | 1.6 | — | V _{DD} | V | |
| D070 | IPUR | GPIO/PORTB Weak Pull-up Current | 50 | 250 | 400 | μA | V _{DD} = 5V, V _{PIN} = V _{SS} |
| | I _{IL} | Input Leakage Current^{(2), (3)} | | | | | |
| D060 | | I/O ports | — | — | ±1 | μA | V _{SS} ≤ V _{PIN} ≤ V _{DD} , Pin at high-impedance |
| D062 | | GP3/RB3/MCLR ⁽⁵⁾ | 50 | 250 | 400 | μA | V _{DD} = 5V |
| D061A | | GP3/RB3/MCLR ⁽⁴⁾ | — | +0.7 | ±5 | μA | V _{SS} ≤ V _{PIN} ≤ V _{DD} |
| D063 | | OSC1 | — | — | ±5 | μA | V _{SS} ≤ V _{PIN} ≤ V _{DD} , XT, HS and LP oscillator configuration |
| | V _{OL} | Output Low Voltage | | | | | |
| D080 | | I/O ports/CLKOUT | — | — | 0.6 | V | I _{OL} = 8.5 mA, V _{DD} = 4.5V, -40°C to $+85^{\circ}\text{C}$ |
| D080A | | | — | — | 0.6 | V | I _{OL} = 7.0 mA, V _{DD} = 4.5V, -40°C to $+125^{\circ}\text{C}$ |
| D083 | | OSC2 | — | — | 0.6 | V | I _{OL} = 1.6 mA, V _{DD} = 4.5V, -40°C to $+85^{\circ}\text{C}$ |
| D083A | | | — | — | 0.6 | V | I _{OL} = 1.2 mA, V _{DD} = 4.5V, -40°C to $+125^{\circ}\text{C}$ |
| | V _{OH} | Output High Voltage | | | | | |
| D090 | | I/O ports/CLKOUT ⁽³⁾ | V _{DD} - 0.7 | — | — | V | I _{OH} = -3.0 mA, V _{DD} = 4.5V, -40°C to $+85^{\circ}\text{C}$ |
| D090A | | | V _{DD} - 0.7 | — | — | V | I _{OH} = -2.5 mA, V _{DD} = 4.5V, -40°C to $+125^{\circ}\text{C}$ |
| D092 | | OSC2 | V _{DD} - 0.7 | — | — | V | I _{OH} = -1.3 mA, V _{DD} = 4.5V, -40°C to $+85^{\circ}\text{C}$ |
| D092A | | | V _{DD} - 0.7 | — | — | V | I _{OH} = -1.0 mA, V _{DD} = 4.5V, -40°C to $+125^{\circ}\text{C}$ |
| | | Capacitive Loading Specs on Output Pins | | | | | |
| D100 | C _{osc2} | OSC2 pin | — | — | 15 | pF | In XT, HS and LP modes when external clock is used to drive OSC1. |
| D101 | C _{IO} | All I/O pins | — | — | 50 | pF | |

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note**
- 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12F510/16F506 be driven with external clock in RC mode.
 - 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
 - 3: Negative current is defined as coming out of the pin.
 - 4: This specification applies when GP3/MCLR is configured as an input with the pull-up disabled. The leakage current for the GP3/RB3/MCLR pin is higher than for the standard I/O port pins.
 - 5: This specification applies when GP3/RB3/MCLR is configured as the MCLR Reset pin function with the weak pull-up always enabled.

TABLE 13-1: COMPARATOR SPECIFICATIONS

| Sym | Characteristics | Min | Typ | Max | Units | Comments |
|-------|------------------------------|-------|-----|-----------|-------|----------------|
| VOS | Input Offset Voltage | — | ±3 | ±10 | mV | (VDD - 1.5V)/2 |
| VCM | Input Common Mode Voltage | 0 | — | VDD - 1.5 | V | |
| CMRR | Common Mode Rejection Ratio | +55* | — | — | dB | |
| TRT | Response Time ⁽¹⁾ | — | 150 | 400* | ns | Internal |
| VIVRF | Internal Voltage Reference | 0.550 | 0.6 | 0.650 | V | |

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (VDD - 1.5)/2, while the other input transitions from VSS to VDD - 1.5V.

TABLE 13-2: COMPARATOR VOLTAGE REFERENCE (CVREF) SPECIFICATIONS

| Sym | Characteristics | Min | Typ | Max | Units | Comments |
|-------------------------|------------------------------|-----|---------|-------|-------|----------------------|
| CVRES | Resolution | — | VDD/24* | — | LSb | Low Range (VRR = 1) |
| | | — | VDD/32 | — | LSb | High Range (VRR = 0) |
| | Absolute Accuracy | — | — | ±1/2* | LSb | Low Range (VRR = 1) |
| | | — | — | ±1/2* | LSb | High Range (VRR = 0) |
| Unit Resistor Value (R) | — | 2K* | — | Ω | | |
| | Settling Time ⁽¹⁾ | — | — | 10* | μs | |

* These parameters are characterized but not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from 0000 to 1111.

TABLE 13-3: A/D CONVERTER CHARACTERISTICS (PIC16F506/PIC12F510)

| Param No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|-----------|------|--|------|---------------------------|----------------|-------|---------------------------------------|
| A01 | NR | Resolution | — | — | 8 bits | bit | |
| A03 | EIL | Integral Error | — | — | ± 1.5 | LSb | VDD = 5.0V |
| A04 | EDL | Differential Error | — | — | -1 < EDL ≤ 1.5 | LSb | No missing codes to 8 bits VDD = 5.0V |
| A05 | EFS | Full-scale Range | 2 | — | 5.5* | V | VDD |
| A06 | EOFF | Offset Error | — | — | ± 1.5 | LSb | VDD = 5.0V |
| A07 | EGN | Gain Error | -0.5 | — | +1.75 | LSb | VDD = 5.0V |
| A10 | — | Monotonicity | — | guaranteed ⁽¹⁾ | — | — | VSS ≤ VAIN ≤ VDD |
| A25 | VAIN | Analog Input Voltage | VSS | — | VDD | V | |
| A30 | ZAIN | Recommended Impedance of Analog Voltage Source | — | — | 10 | kΩ | |

* These parameters are characterized but not tested.

† Data in the "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only are not tested.

Note 1: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

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13.4 Timing Parameter Symbolology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

| | | |
|----------|-------------|--------|
| T | F Frequency | T Time |
|----------|-------------|--------|

Lowercase (pp) and their meanings:

| | | |
|-----------|--------------------|-----------------------------|
| pp | 2 To | mc $\overline{\text{MCLR}}$ |
| ck | CLKOUT | osc Oscillator |
| cy | Cycle Time | os OSC1 |
| drt | Device Reset Timer | t0 T0CKI |
| io | I/O port | wdt Watchdog Timer |

Uppercase letters and their meanings:

| | | |
|----------------------------|---------|------------------|
| S | F Fall | P Period |
| H High | R Rise | V Valid |
| I Invalid (high-impedance) | V Valid | Z High-impedance |
| L Low | | |

FIGURE 13-5: LOAD CONDITIONS

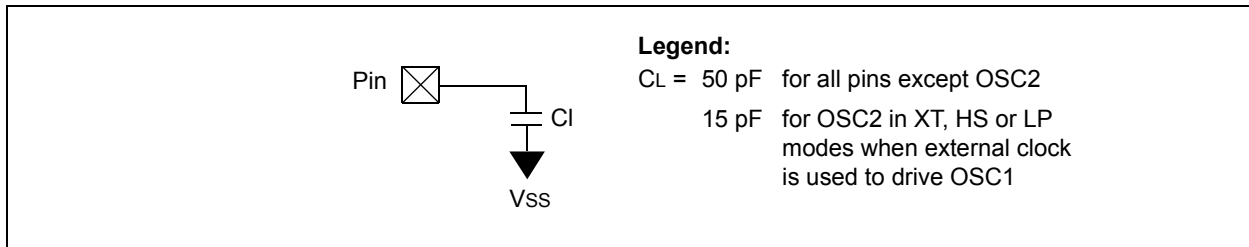


FIGURE 13-6: EXTERNAL CLOCK TIMING

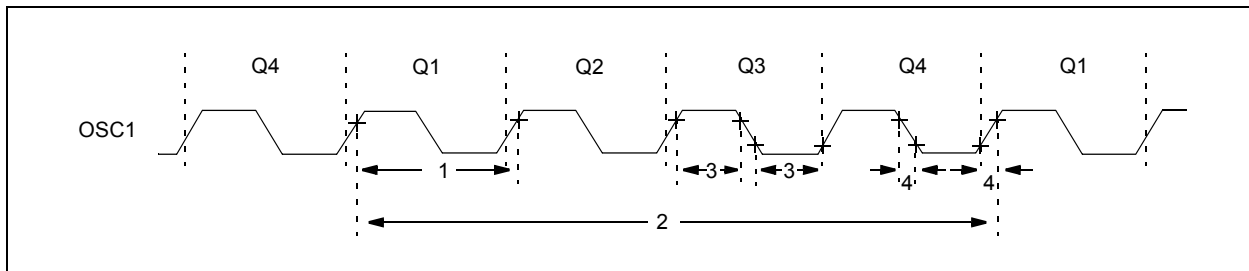


TABLE 13-4: EXTERNAL CLOCK TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial), $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) | | | | |
|--------------------|---------------|---|--|--------------------|--------|-------|---|
| Para No. | Sym | Characteristic | Min | Typ ⁽¹⁾ | Max | Units | Conditions |
| 1A | Fosc | External CLKIN Frequency ⁽²⁾ | DC | — | 4 | MHz | XT Oscillator mode |
| | | | DC | — | 20 | MHz | HS/EC Oscillator mode (PIC16F506 only) |
| | | | DC | — | 200 | kHz | LP Oscillator mode |
| | | Oscillator Frequency ⁽²⁾ | — | — | 4 | MHz | EXTRC Oscillator mode |
| | | | 0.1 | — | 4 | MHz | XT Oscillator mode |
| | | | 4 | — | 20 | MHz | HS/EC Oscillator mode (PIC16F506 only) |
| — | — | 200 | kHz | LP Oscillator mode | | | |
| 1 | Tosc | External CLKIN Period ⁽²⁾ | 250 | — | — | ns | XT Oscillator mode |
| | | | 50 | — | — | ns | HS/EC Oscillator mode (PIC16F506 only) |
| | | | 5 | — | — | μs | LP Oscillator mode |
| | | Oscillator Period ⁽²⁾ | 250 | — | — | ns | EXTRC Oscillator mode |
| | | | 250 | — | 10,000 | ns | XT Oscillator mode |
| | | | 50 | — | 250 | ns | HS/EC Oscillator mode (PIC16F506 only) |
| | | | 5 | — | — | μs | LP Oscillator mode |
| | | | — | — | — | — | — |
| 2 | Tcy | Instruction Cycle Time | 200 | 4/Fosc | — | ns | |
| 3 | TosL, TosH | Clock in (OSC1) Low or High Time | 50* | — | — | ns | XT Oscillator |
| | | | 2* | — | — | μs | LP Oscillator |
| | | | 10 | — | — | ns | HS/EC Oscillator (PIC16F506 only) |
| 4 | TosR, TosF | Clock in (OSC1) Rise or Fall Time | — | — | 25* | ns | XT Oscillator |
| | | | — | — | 50* | ns | LP Oscillator |
| | | | — | — | 15 | ns | HS/EC Oscillator (PIC16F506 only) |

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- 2:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

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TABLE 13-5: CALIBRATED INTERNAL RC FREQUENCIES

| AC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial), $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) | | | | | |
|--------------------|------|---|--|----------------------|----------------------|----------------------|-------------------|---|
| Param No. | Sym | Characteristic | Freq. Tolerance | Min | Typ ⁽¹⁾ | Max* | Units | Conditions |
| F10 | Fosc | Internal Calibrated INTOSC Frequency ⁽¹⁾ | $\pm 1\%$ $\pm 2\%$ $\pm 5\%$ | 7.92 7.84 7.60 | 8.00 8.00 8.00 | 8.08 8.16 8.40 | MHz MHz MHz | $V_{DD} = 3.5\text{V}$ $T_A = 25^{\circ}\text{C}$ $2.5\text{V} \leq V_{DD} \leq 5.5\text{V}$ $0^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ $2.0\text{V} \leq V_{DD} \leq 5.5\text{V}$ $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (Ind.) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (Ext.) |

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 13-7: I/O TIMING

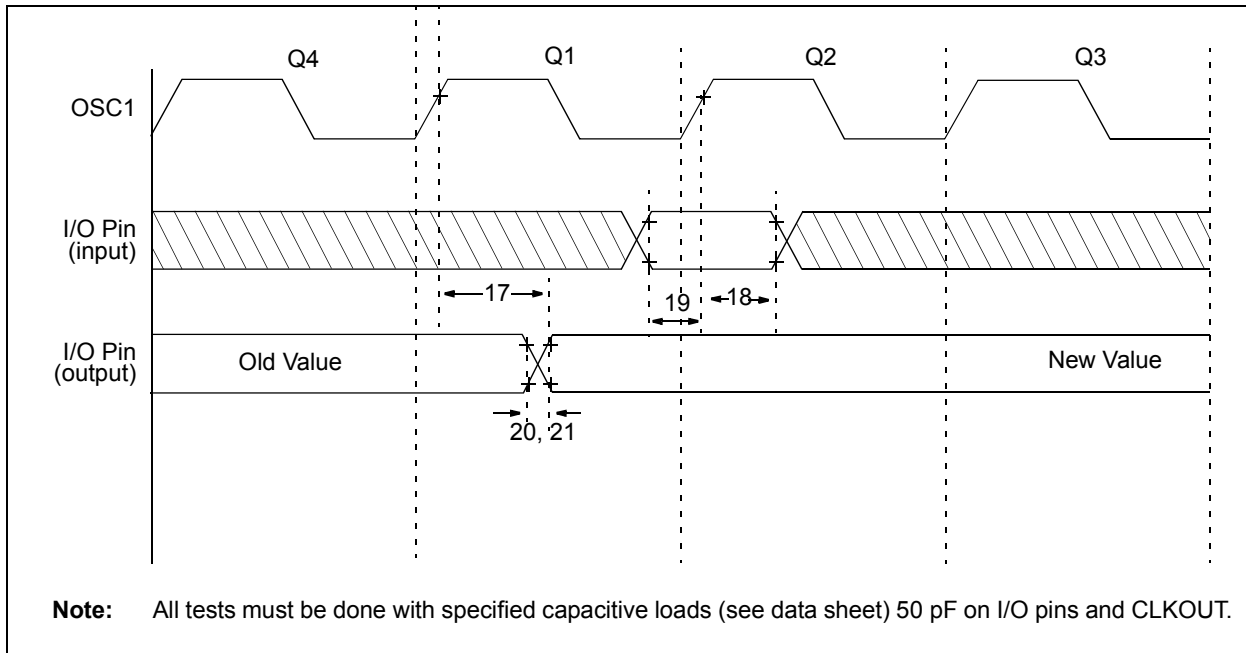


TABLE 13-6: TIMING REQUIREMENTS

| AC CHARACTERISTICS | | Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) | | | | |
|--------------------|----------|---|-----|--------------------|------|-------|
| Param No. | Sym | Characteristic | Min | Typ ⁽¹⁾ | Max | Units |
| 17 | TosH2ioV | OSC1 \uparrow (Q1 cycle) to Port out valid ^{(2), (3)} | — | — | 100* | ns |
| 18 | TosH2ioI | OSC1 \uparrow (Q2 cycle) to Port input invalid (I/O in hold time) ⁽²⁾ | 50 | — | — | ns |
| 19 | TioV2osH | Port input valid to OSC1 \uparrow (I/O in setup time) | 20 | — | — | ns |
| 20 | TioR | Port output rise time ^{(2), (3)} | — | 10 | 25** | ns |
| 21 | TioF | Port output fall time ^{(2), (3)} | — | 10 | 25** | ns |

* These parameters are characterized but not tested.

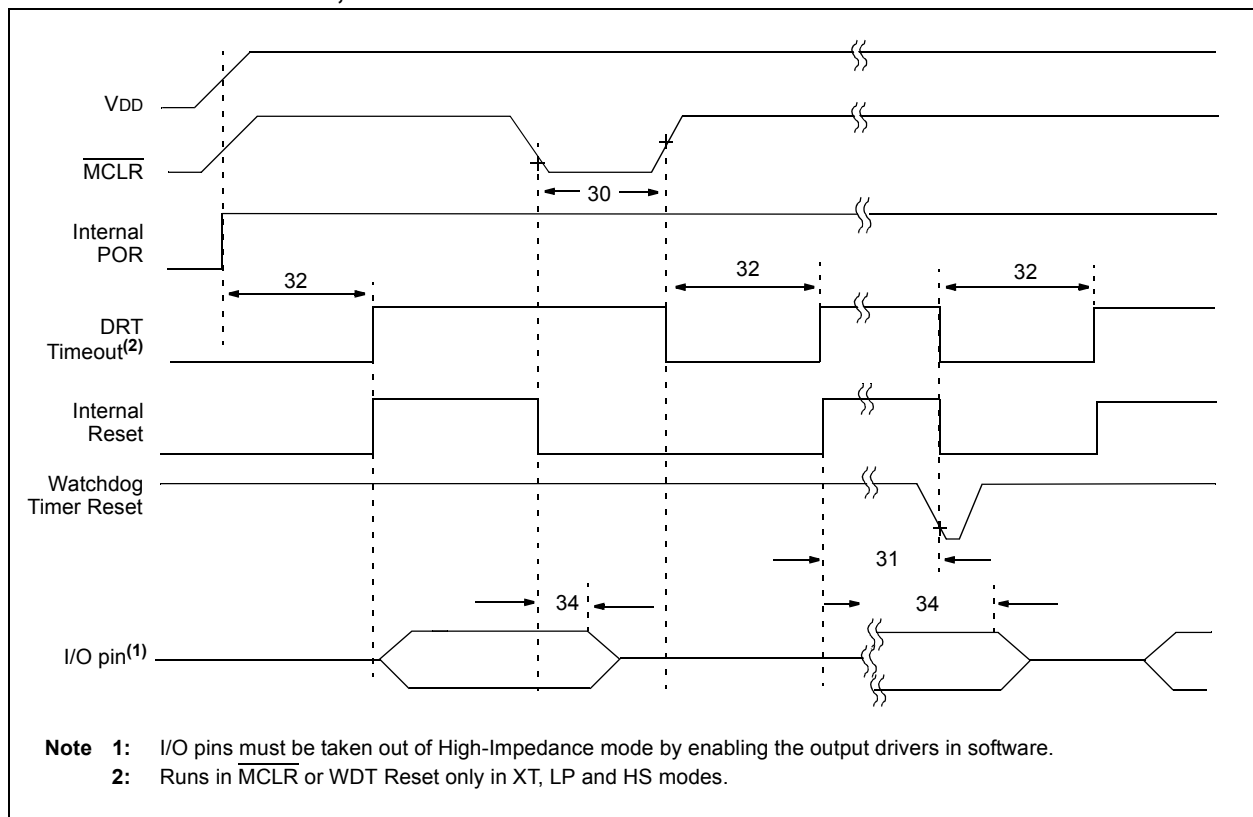
** These parameters are design targets and are not tested.

Note 1: Data in the Typical (“Typ”) column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in EXTRC mode.

3: See Figure 13-5 for loading conditions.

FIGURE 13-8: RESET, WATCHDOG TIMER AND DEVICE RESET TIMER TIMING



Note 1: I/O pins must be taken out of High-Impedance mode by enabling the output drivers in software.

2: Runs in $\overline{\text{MCLR}}$ or WDT Reset only in XT, LP and HS modes.

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TABLE 13-7: RESET, WATCHDOG TIMER AND DEVICE RESET TIMER

| AC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended) | | | | |
|--------------------|------|---|---|--------------------|-------------------------|-------|-------------------------|
| Param No. | Sym | Characteristic | Min | Typ ⁽¹⁾ | Max | Units | Conditions |
| 30 | TMCL | MCLR Pulse Width (low) | 2000* | — | — | ns | VDD = 5.0V |
| 31 | TWDT | Watchdog Timer Time-out Period (No Prescaler) | 9* | 18* | 30* | ms | VDD = 5.0V (Industrial) |
| | | | 9* | 18* | 40* | ms | VDD = 5.0V (Extended) |
| 32 | TDRT | Device Reset Timer Period | | | | | |
| | | Standard | 9* | 18* | 30* | ms | VDD = 5.0V (Industrial) |
| | | | 9* | 18* | 40* | ms | VDD = 5.0V (Extended) |
| Short | 0.5* | 1.125* | 2* | ms | VDD = 5.0V (Industrial) | | |
| | 0.5* | 1.125* | 2.5* | ms | VDD = 5.0V (Extended) | | |
| 34 | TIOZ | I/O high-impedance from MCLR low | — | — | 2000* | ns | |

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 13-9: TIMER0 CLOCK TIMINGS

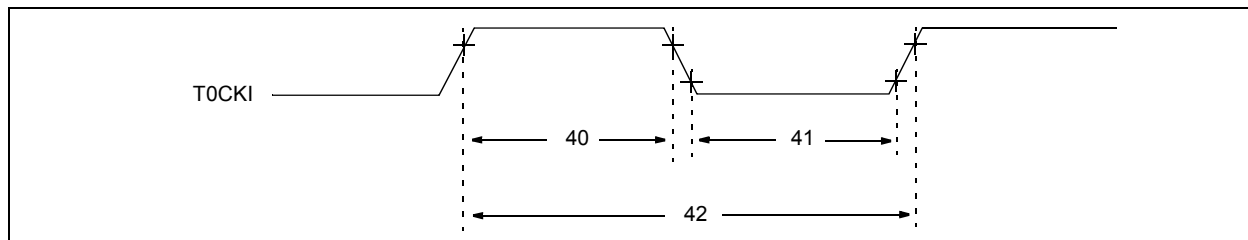


TABLE 13-8: TIMER0 CLOCK REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended) | | | | |
|--------------------|------|------------------------|---|--------------------|-----|-------|--|
| Param No. | Sym | Characteristic | Min | Typ ⁽¹⁾ | Max | Units | Conditions |
| 40 | Tt0H | T0CKI High Pulse Width | No Prescaler | 0.5 TcY + 20* | — | — | ns |
| | | With Prescaler | 10* | — | — | ns | |
| 41 | Tt0L | T0CKI Low Pulse Width | No Prescaler | 0.5 TcY + 20* | — | — | ns |
| | | With Prescaler | 10* | — | — | ns | |
| 42 | Tt0P | T0CKI Period | 20 or TcY + 40* N | — | — | ns | Whichever is greater. N = Prescale Value (1, 2, 4, ..., 256) |

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 13-9: PULL-UP RESISTOR RANGES

| VDD (Volts) | Temperature (°C) | Min | Typ | Max | Units |
|----------------------------|------------------|-----|------|------|-------|
| RB0 (GP0)/RB1 (GP1) | | | | | |
| 2.0 | -40 | 73K | 105K | 186K | Ω |
| | 25 | 73K | 113K | 187K | Ω |
| | 85 | 82K | 123K | 190K | Ω |
| | 125 | 86K | 132k | 190K | Ω |
| 5.5 | -40 | 15K | 21K | 33K | Ω |
| | 25 | 15K | 22K | 34K | Ω |
| | 85 | 19K | 26k | 35K | Ω |
| | 125 | 23K | 29K | 35K | Ω |
| RB3 (GP3) | | | | | |
| 2.0 | -40 | 63K | 81K | 96K | Ω |
| | 25 | 77K | 93K | 116K | Ω |
| | 85 | 82K | 96k | 116K | Ω |
| | 125 | 86K | 100K | 119K | Ω |
| 5.5 | -40 | 16K | 20k | 22K | Ω |
| | 25 | 16K | 21K | 23K | Ω |
| | 85 | 24K | 25k | 28K | Ω |
| | 125 | 26K | 27K | 29K | Ω |

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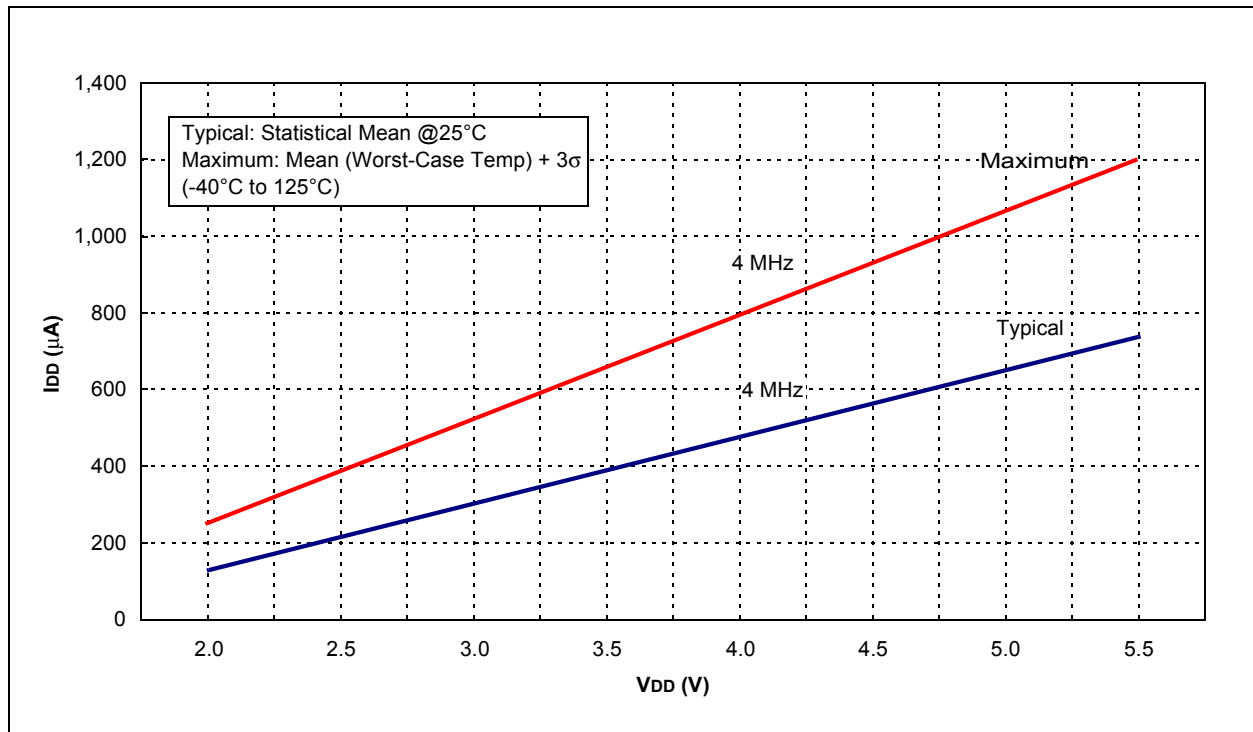
NOTES:

14.0 DC AND CHARACTERISTICS GRAPHS AND CHARTS.

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

“Typical” represents the mean of the distribution at 25°C. “Maximum” or “minimum” represents (mean + 3σ) or (mean - 3σ) respectively, where s is a standard deviation, over each temperature range.

FIGURE 14-1: IDD vs. VDD OVER Fosc



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FIGURE 14-2: TYPICAL IPD vs. VDD (SLEEP MODE, ALL PERIPHERALS DISABLED)

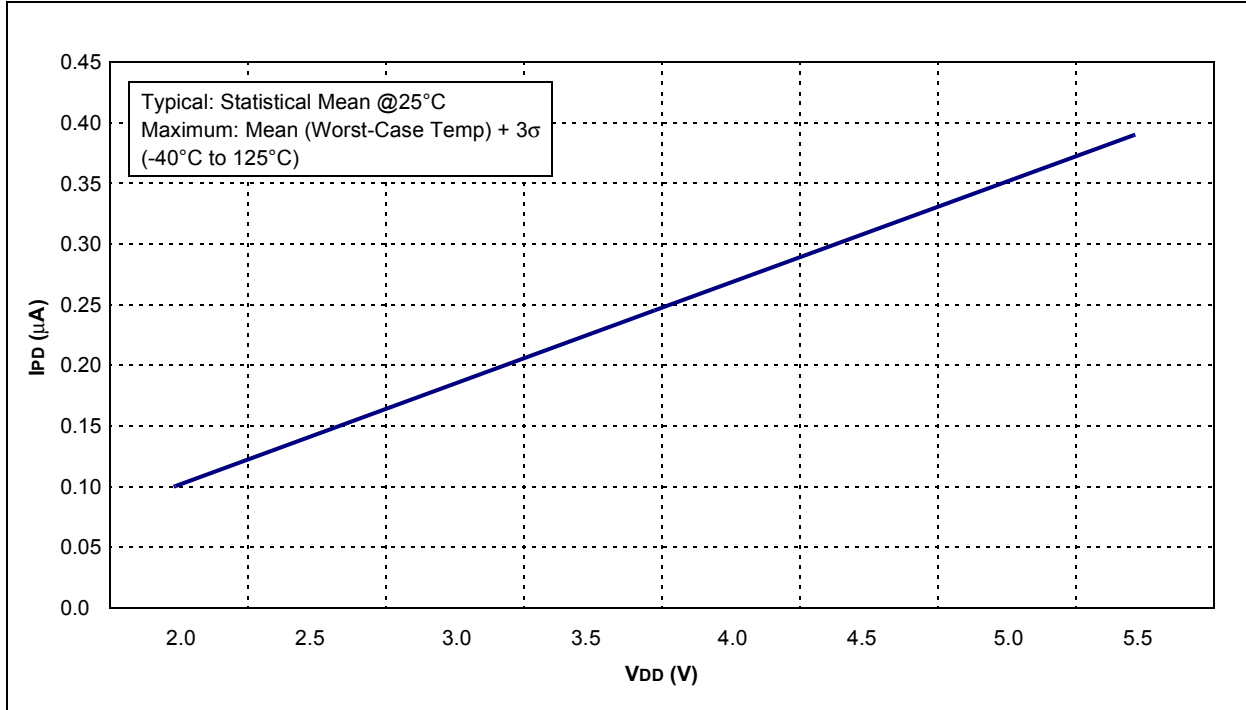


FIGURE 14-3: MAXIMUM IPD vs. VDD (SLEEP MODE, ALL PERIPHERALS DISABLED)

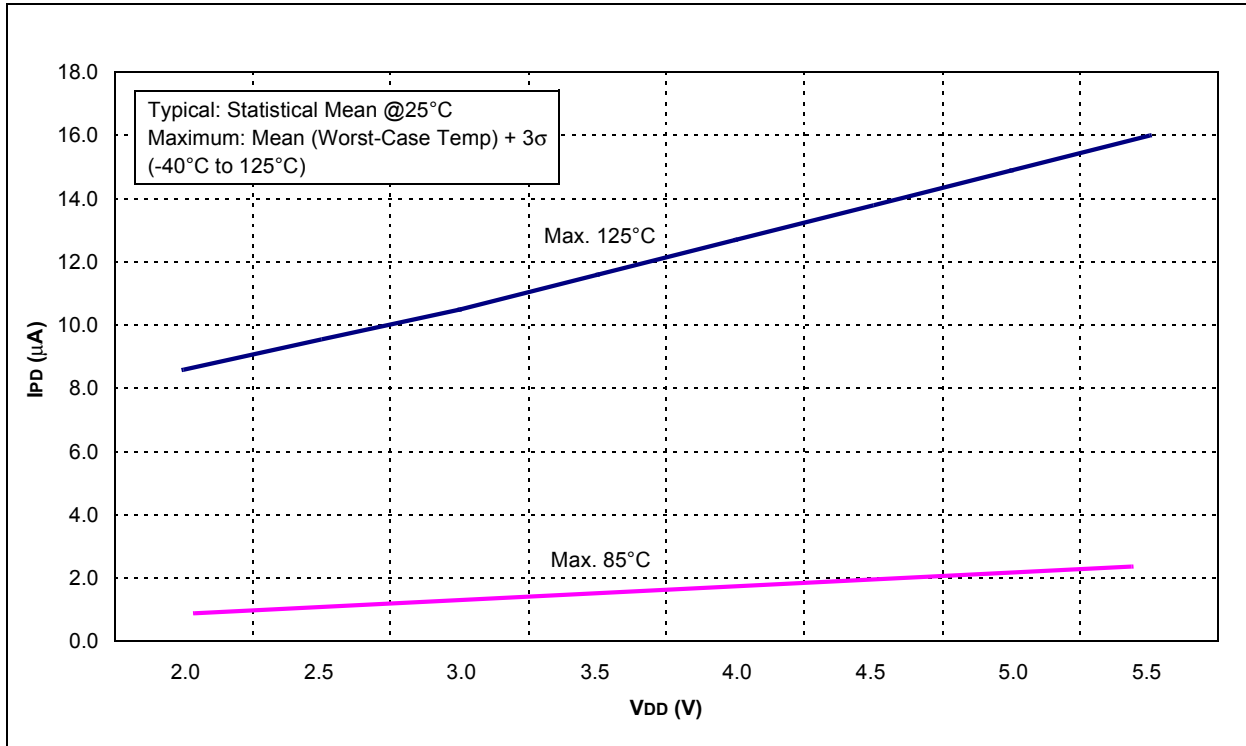


FIGURE 14-4: COMPARATOR IPD vs. VDD (COMPARATOR ENABLED)

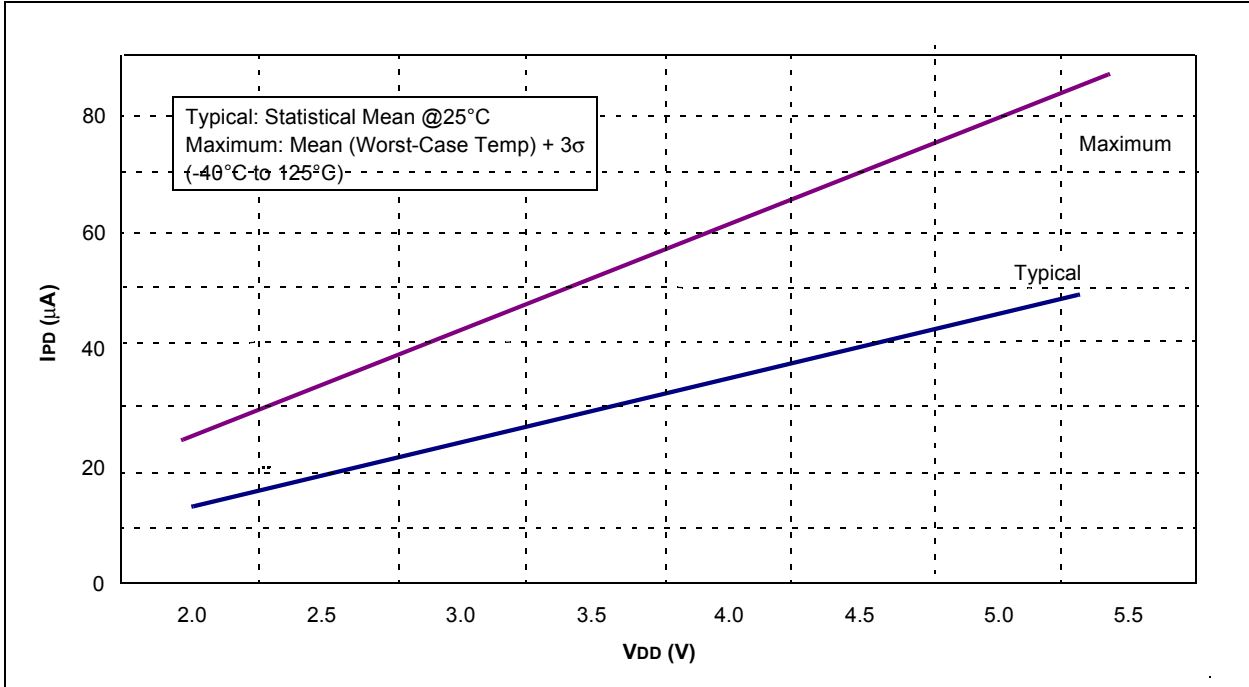
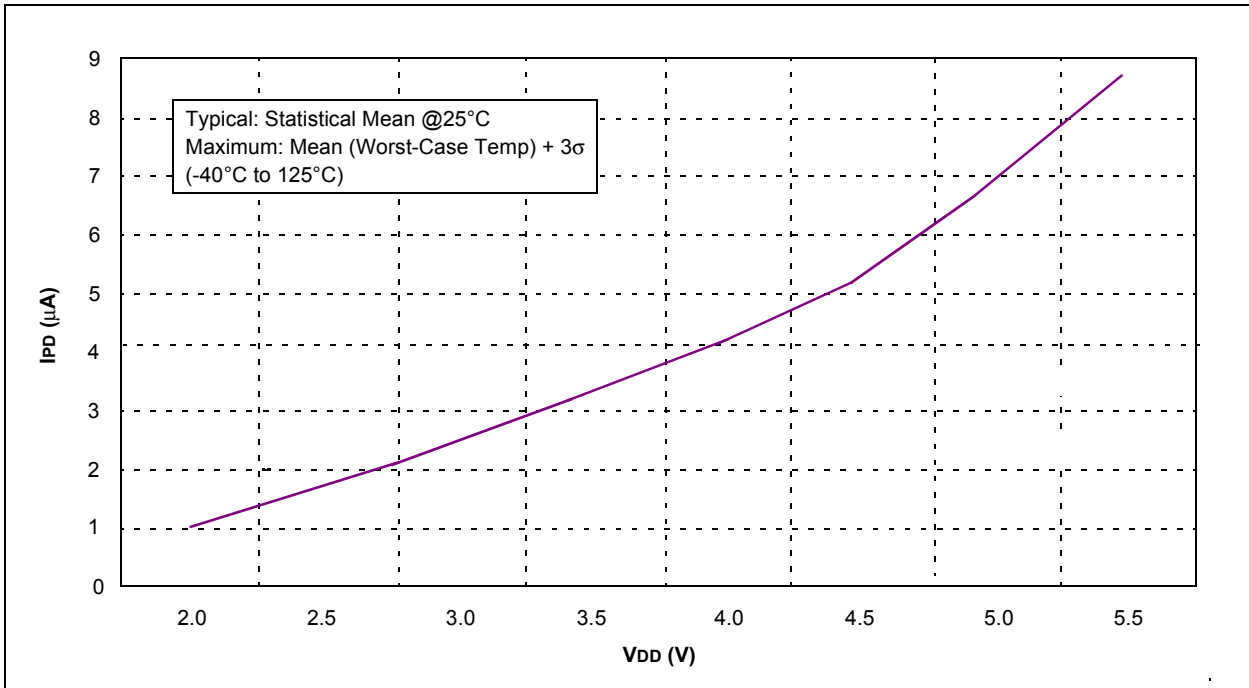


FIGURE 14-5: TYPICAL WDT IPD vs. VDD



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FIGURE 14-6: MAXIMUM WDT IPD vs. VDD OVER TEMPERATURE

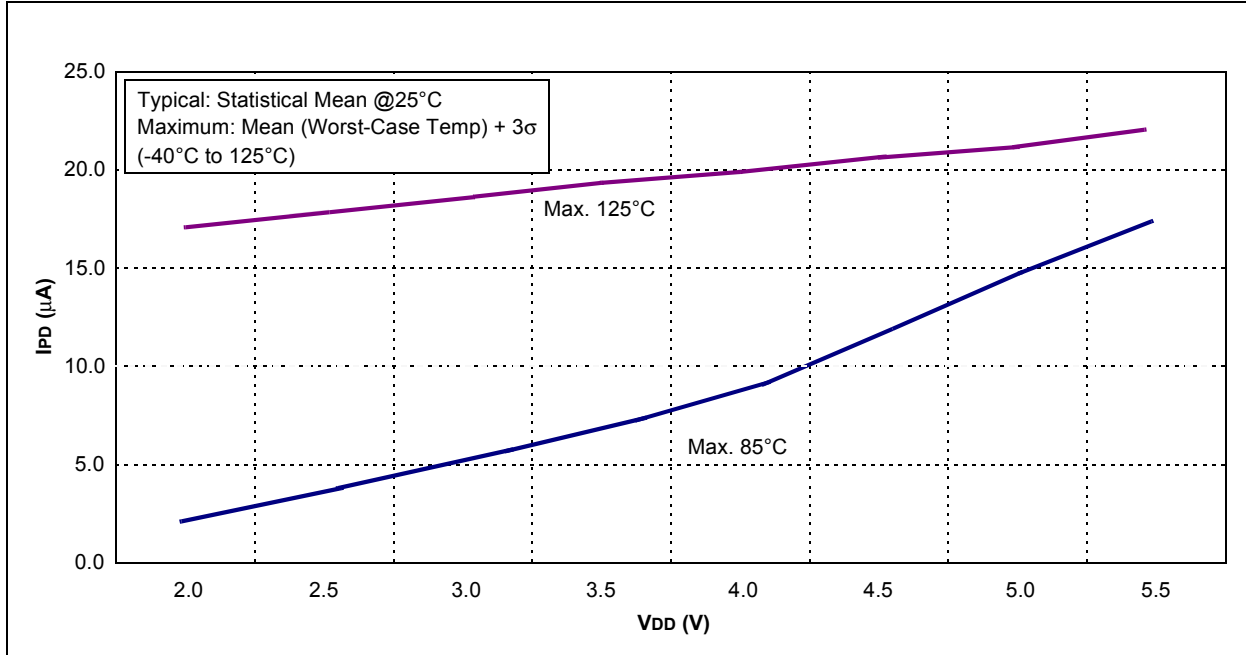


FIGURE 14-7: WDT TIME-OUT vs. VDD OVER TEMPERATURE (NO PRESCALER)

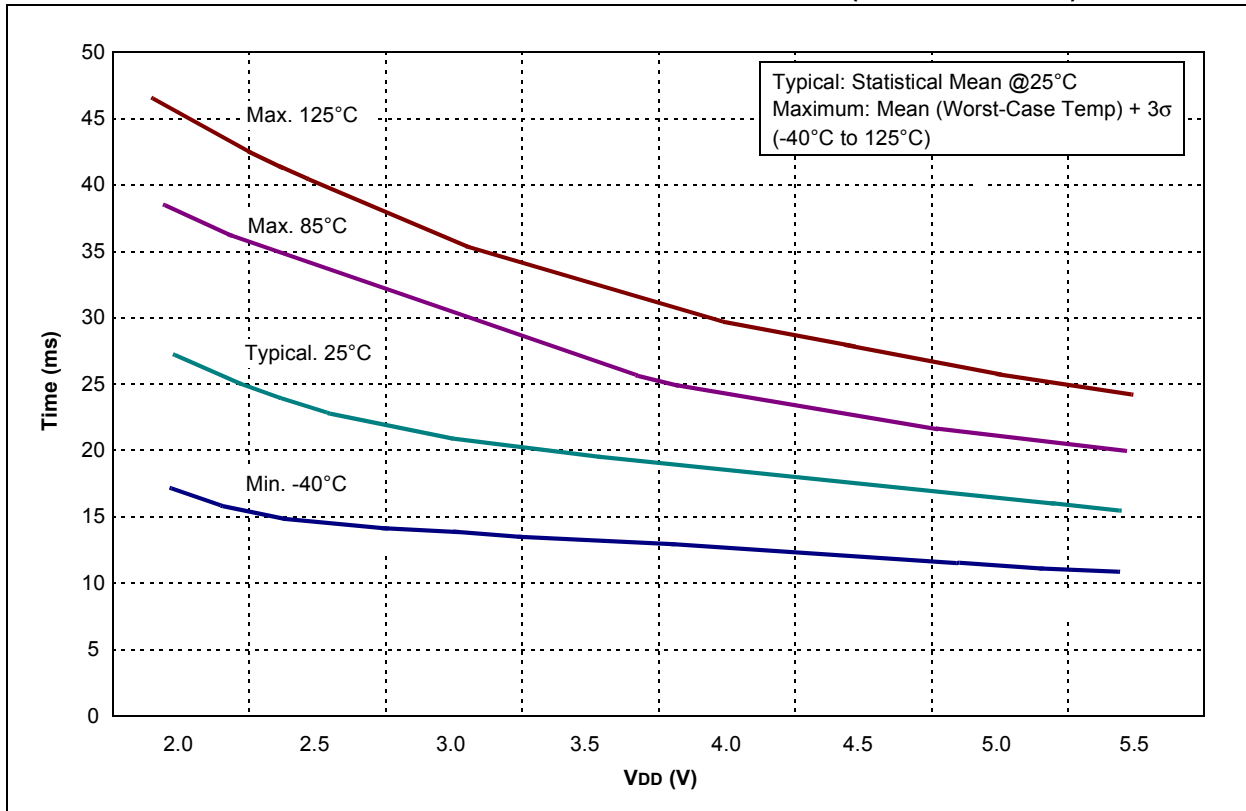


FIGURE 14-8: VOL vs. IOL OVER TEMPERATURE (VDD = 3.0V)

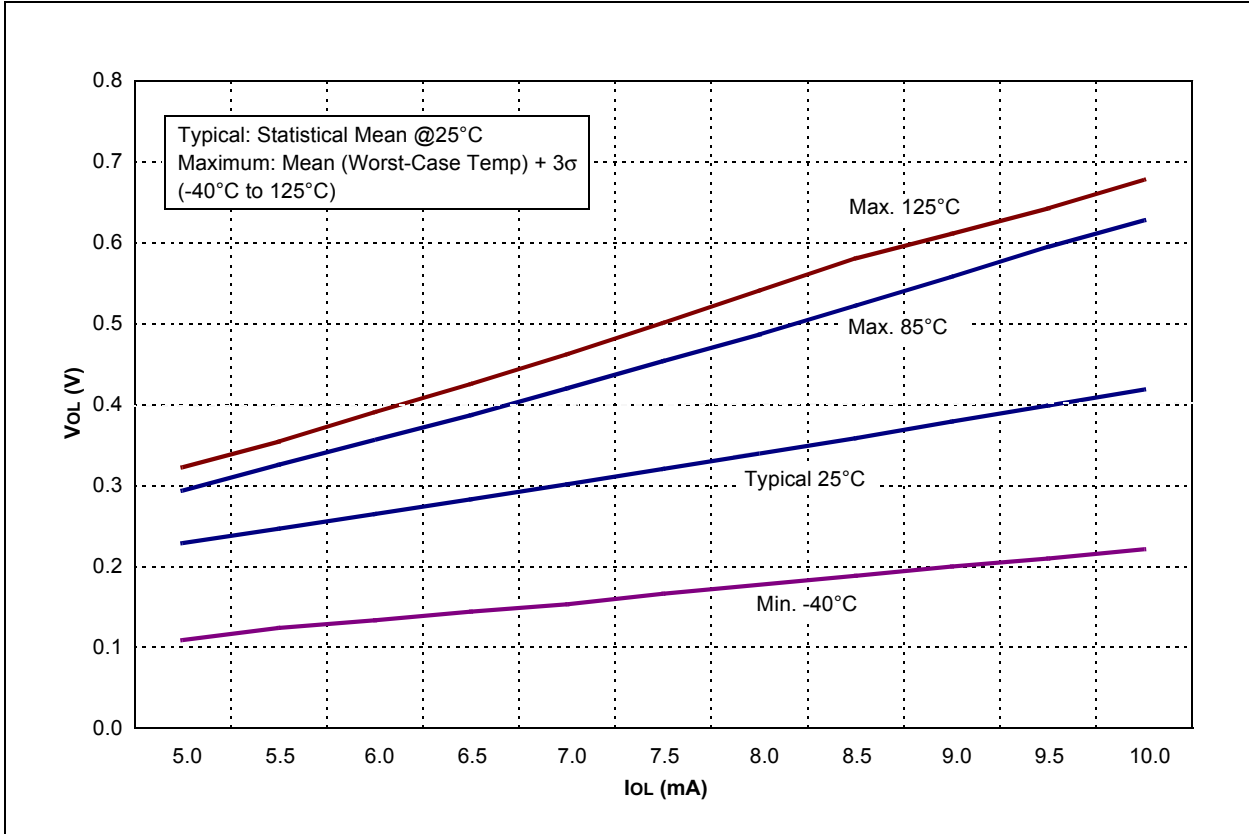
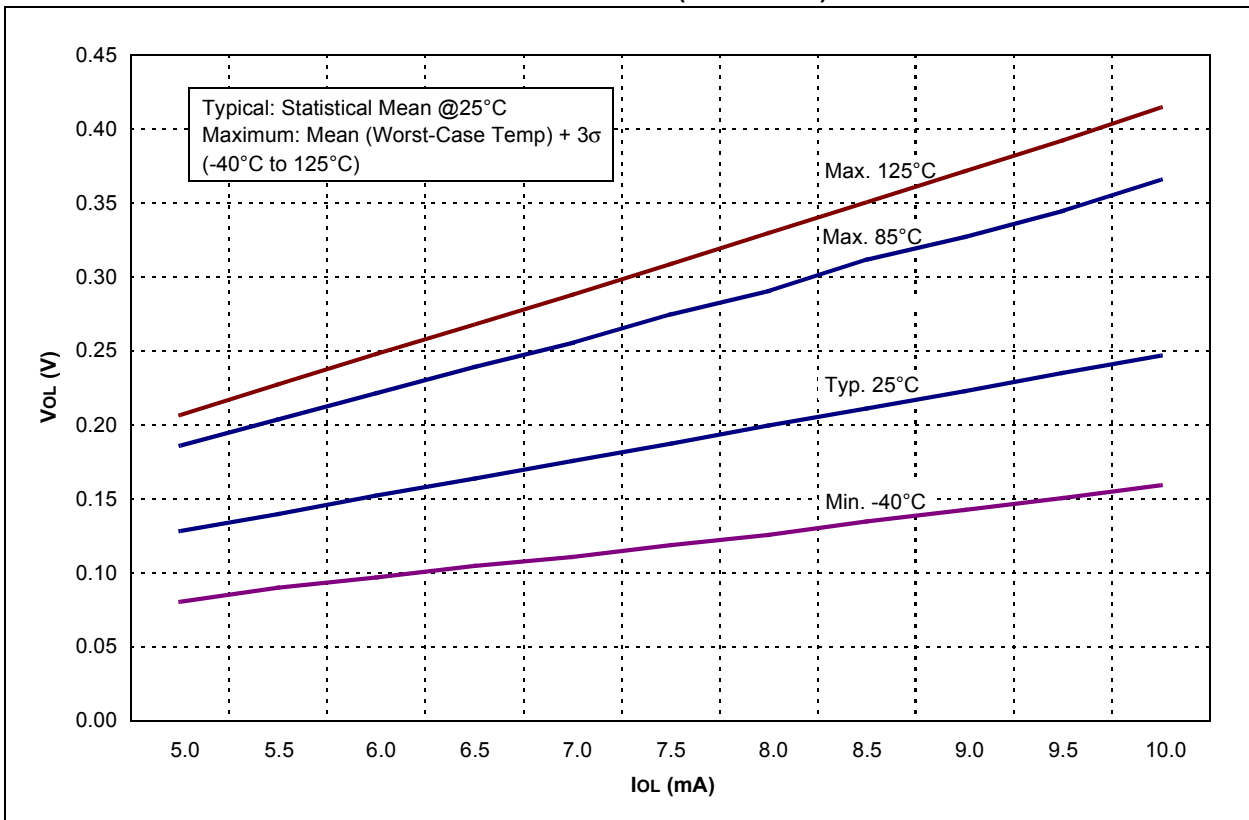


FIGURE 14-9: VOL vs. IOL OVER TEMPERATURE (VDD = 5.0V)



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FIGURE 14-10: V_{OH} vs. I_{OH} OVER TEMPERATURE ($V_{DD} = 3.0V$)

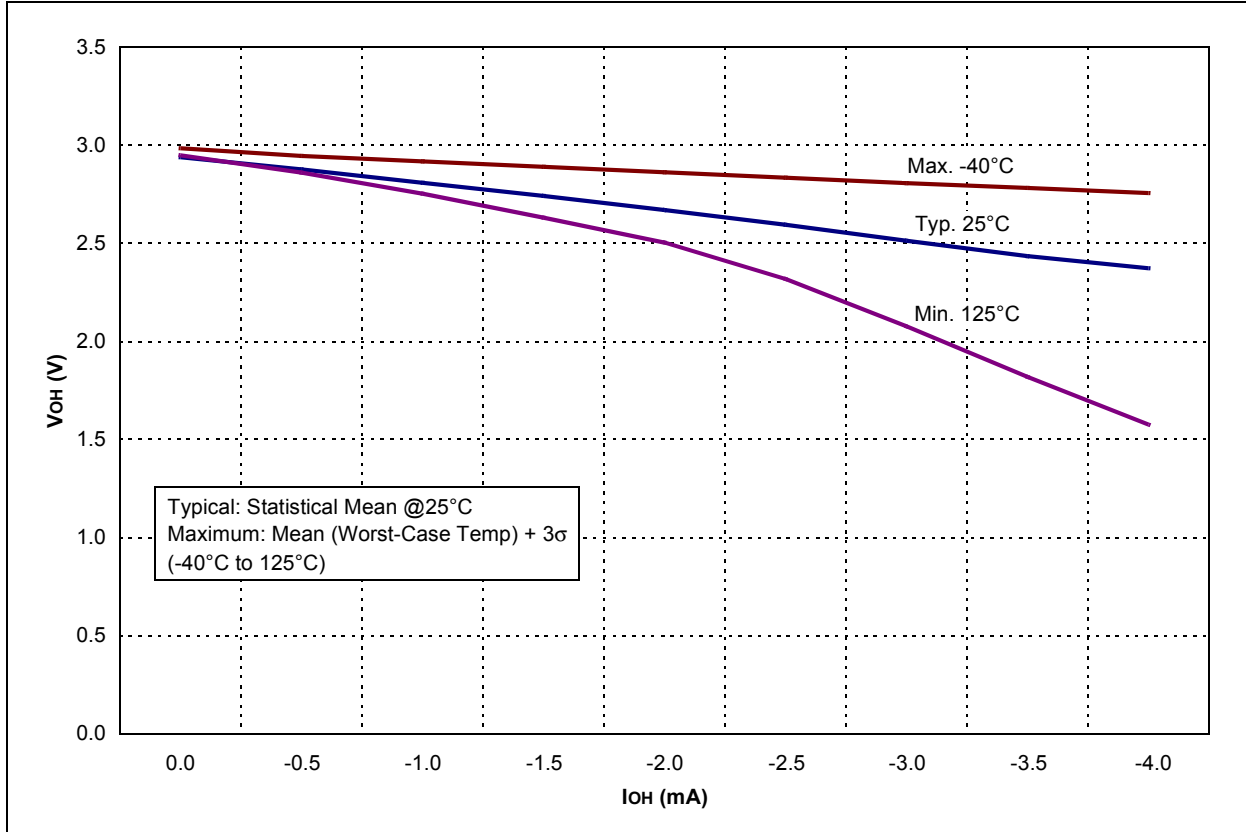


FIGURE 14-11: V_{OH} vs. I_{OH} OVER TEMPERATURE ($V_{DD} = 5.0V$)

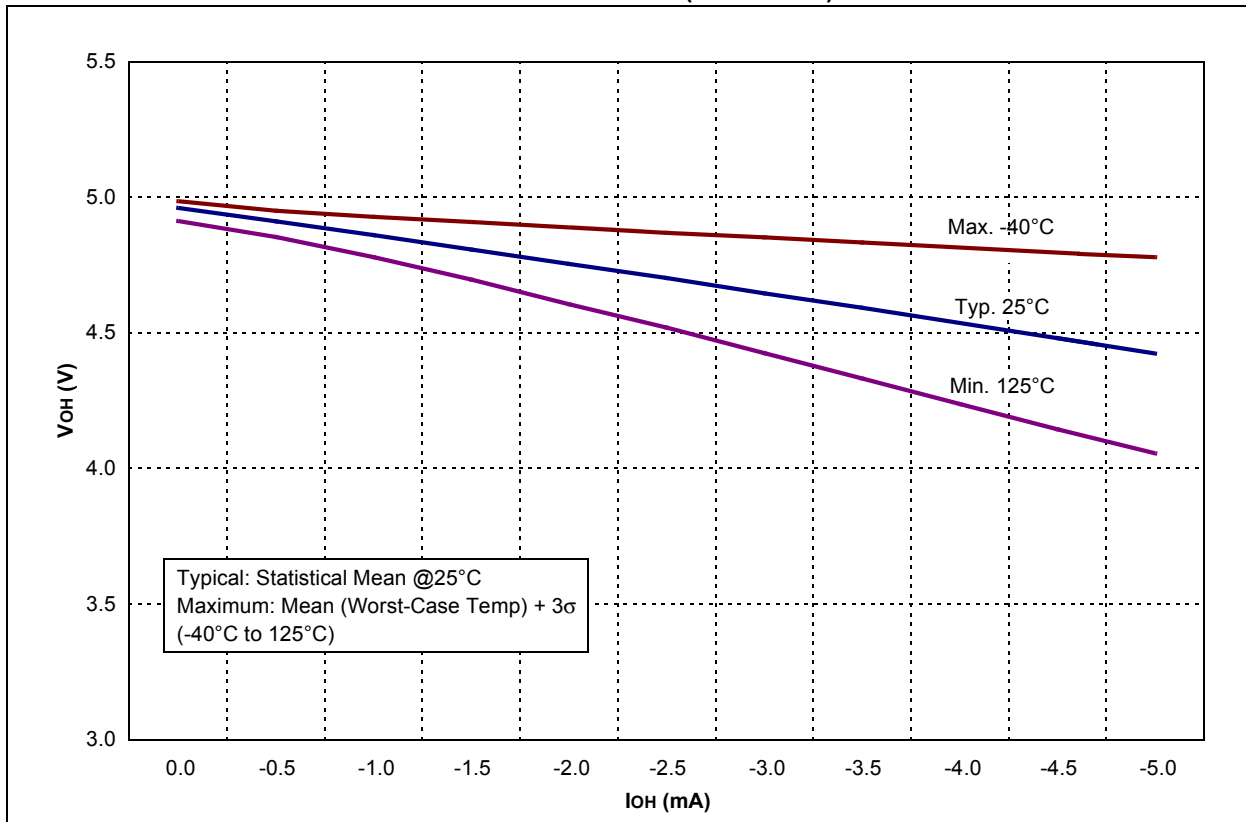


FIGURE 14-12: TTL INPUT THRESHOLD V_{IN} vs. V_{DD}

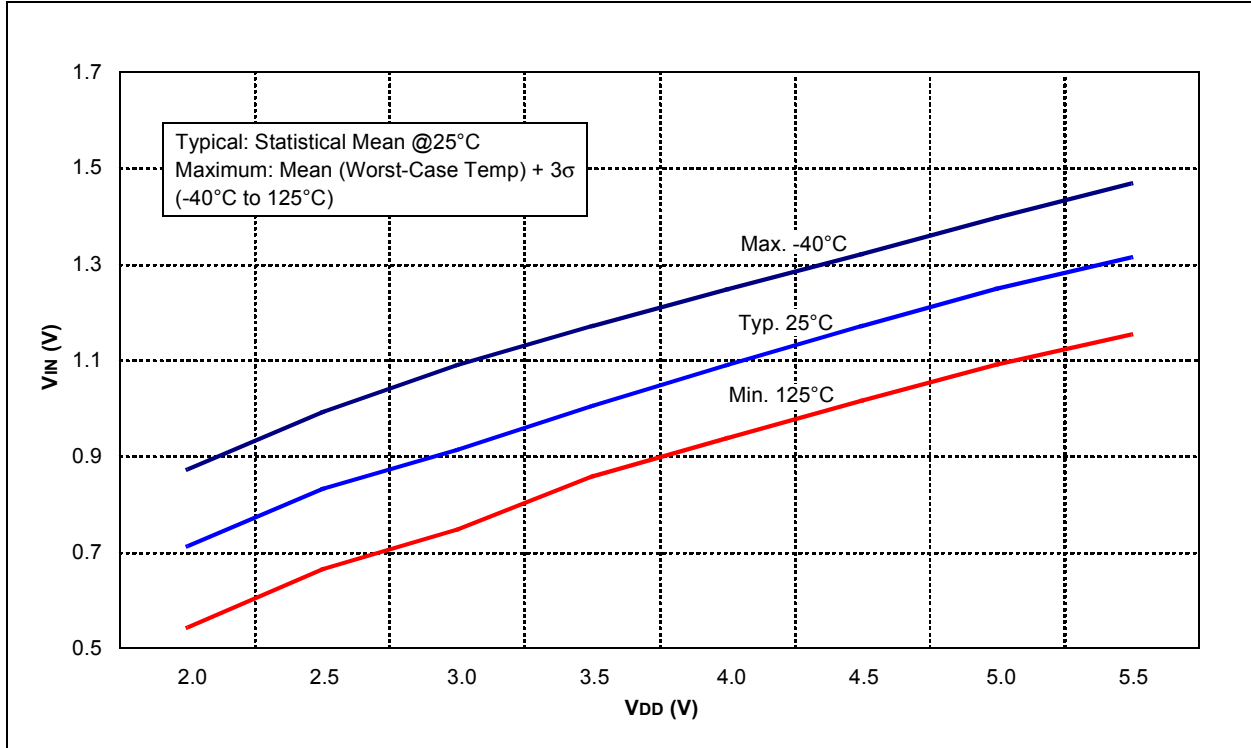
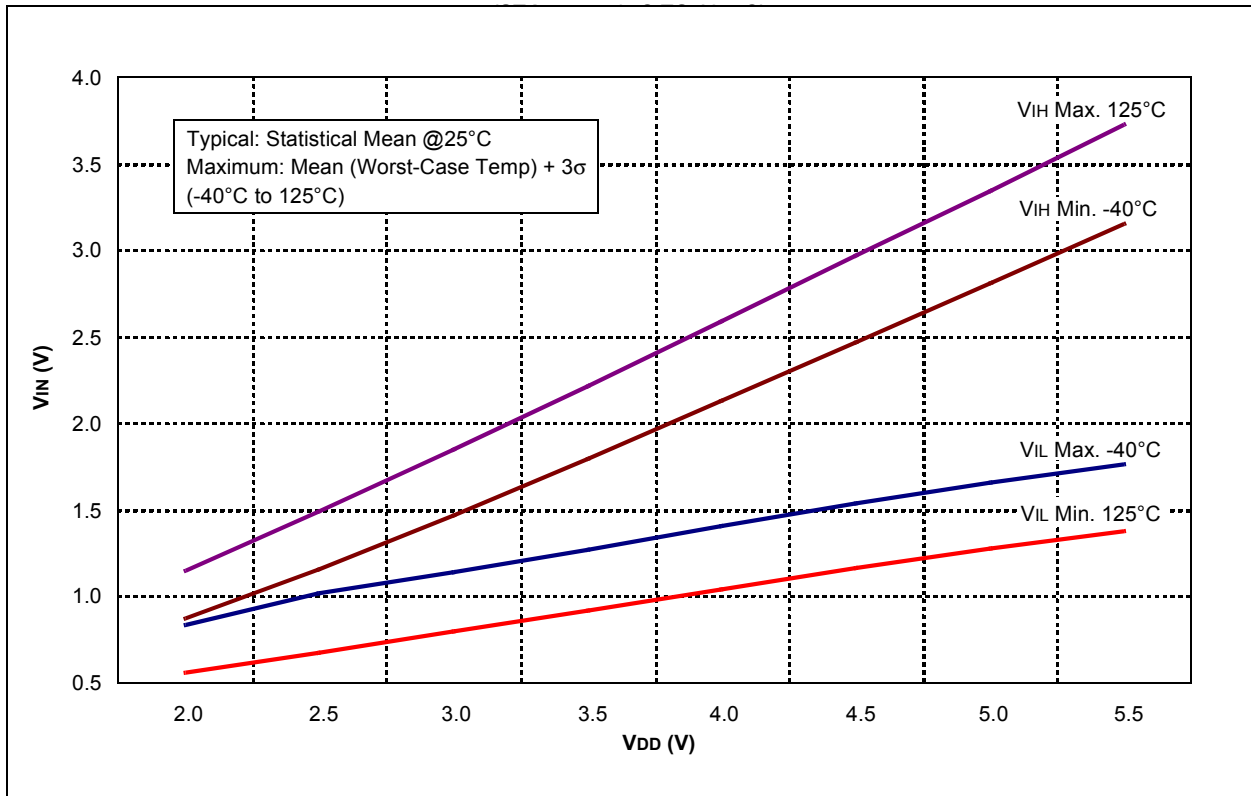
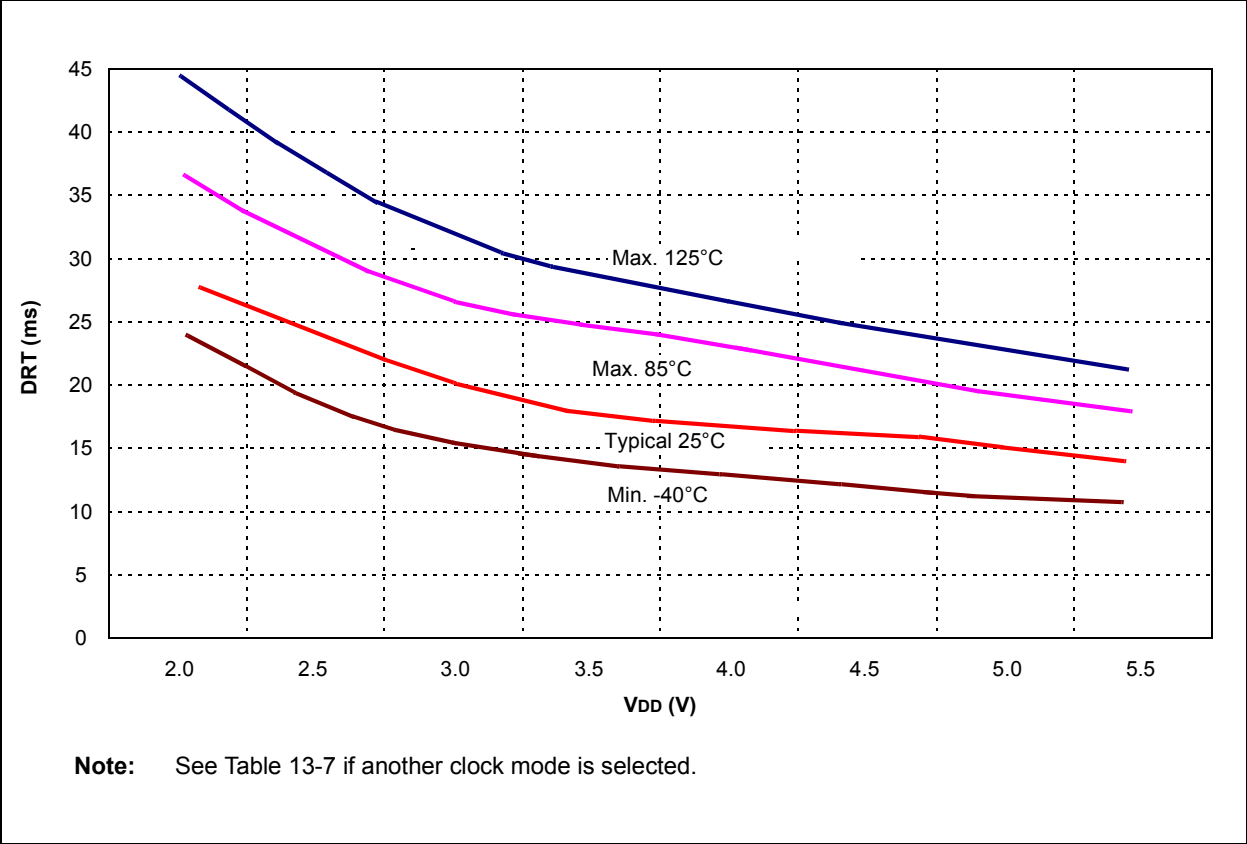


FIGURE 14-13: SCHMITT TRIGGER INPUT THRESHOLD V_{IN} vs. V_{DD}



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FIGURE 14-14: DEVICE RESET TIMER (HS, XT AND LP) vs. VDD



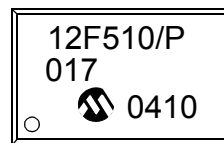
15.0 PACKAGING

15.1 Package Marking Information

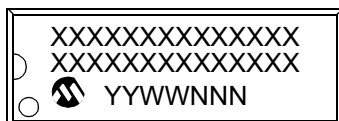
8-Lead PDIP



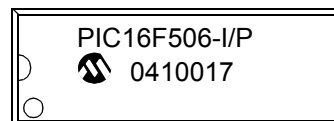
Example



14-Lead PDIP



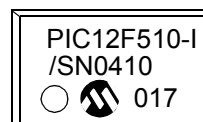
Example



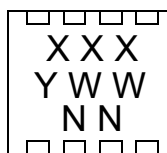
8-Lead SOIC (3.90 mm)



Example



8-Lead 2x3 DFN*



Example

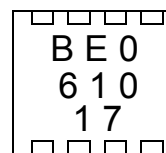


TABLE 15-1: 8-LEAD 2X3 DFN (MC) TOP MARKING

| Part Number | Marking |
|-------------------|---------|
| PIC12F510(T)-I/MC | BS0 |
| PIC12F510-E/MC | BT0 |

| | | |
|----------------|--------|--|
| Legend: | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

* Standard PIC[®] device marking consists of Microchip part number, year code, week code and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

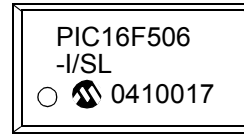
PIC12F510/16F506

15.2 Package Marking Information (Cont'd)

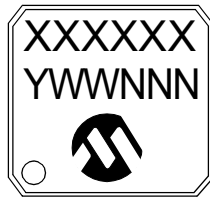
14-Lead SOIC (3.90 mm)



Example



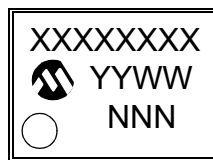
8-Lead MSOP



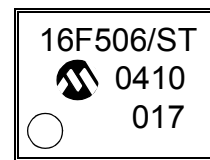
Example



14-Lead TSSOP (4.4 mm)

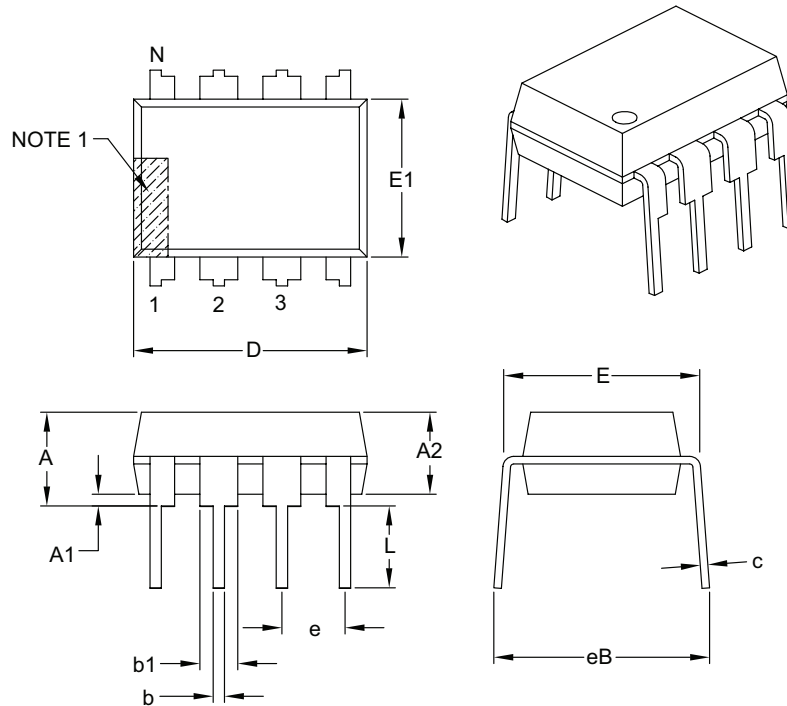


Example



8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| | | Units | INCHES | | |
|----------------------------|----|-------|----------|-----|------|
| Dimension Limits | | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | | |
| Pitch | e | | .100 BSC | | |
| Top to Seating Plane | A | – | – | | .210 |
| Molded Package Thickness | A2 | .115 | .130 | | .195 |
| Base to Seating Plane | A1 | .015 | – | | – |
| Shoulder to Shoulder Width | E | .290 | .310 | | .325 |
| Molded Package Width | E1 | .240 | .250 | | .280 |
| Overall Length | D | .348 | .365 | | .400 |
| Tip to Seating Plane | L | .115 | .130 | | .150 |
| Lead Thickness | c | .008 | .010 | | .015 |
| Upper Lead Width | b1 | .040 | .060 | | .070 |
| Lower Lead Width | b | .014 | .018 | | .022 |
| Overall Row Spacing § | eB | – | – | | .430 |

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

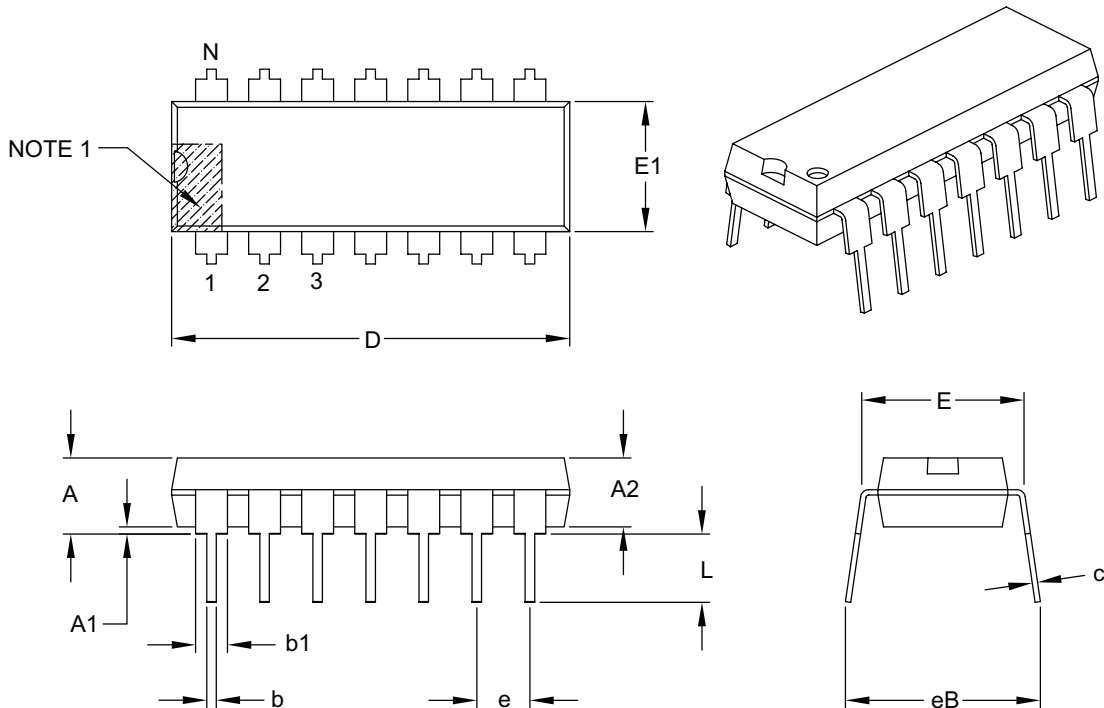
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

PIC12F510/16F506

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packageing>



| Dimension Limits | Units | INCHES | | |
|----------------------------|-------|----------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 14 | | |
| Pitch | e | .100 BSC | | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .735 | .750 | .775 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .045 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

Notes:

- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

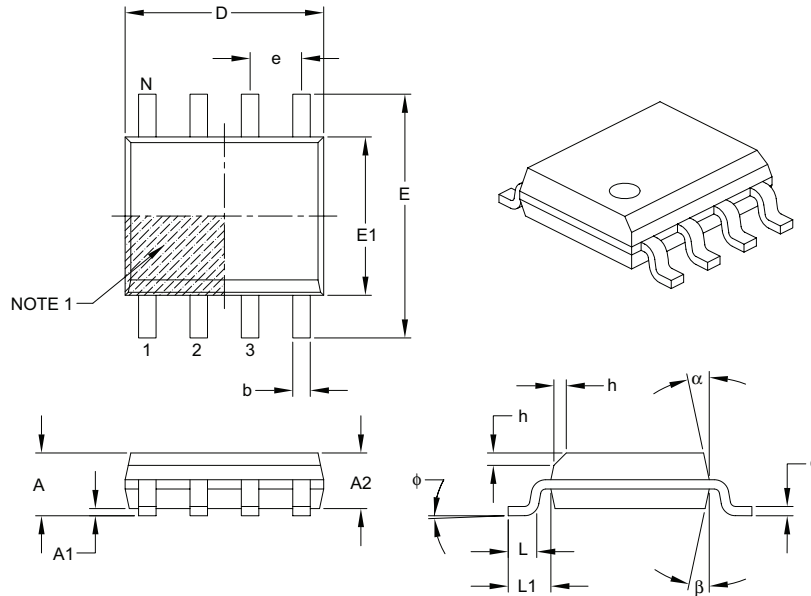
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

PIC12F510/16F506

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|----------|-------------|-----|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 1.27 BSC | | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | – |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | 6.00 BSC | | |
| Molded Package Width | E1 | 3.90 BSC | | |
| Overall Length | D | 4.90 BSC | | |
| Chamfer (optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | 1.04 REF | | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Mold Draft Angle Top | α | 5° | – | 15° |
| Mold Draft Angle Bottom | β | 5° | – | 15° |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

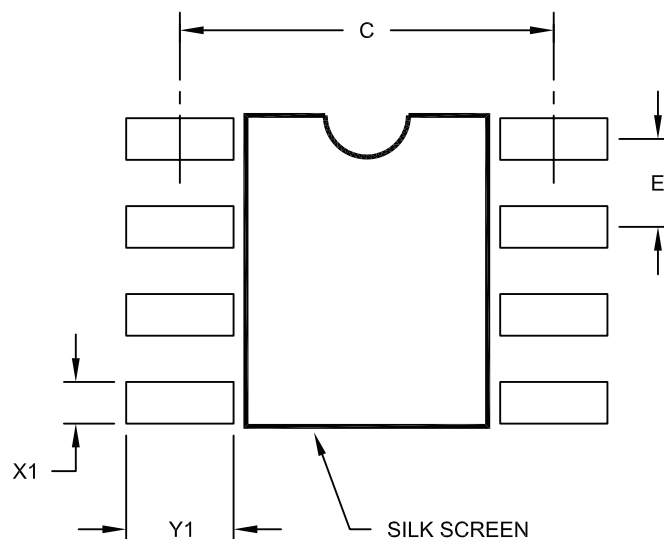
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

PIC12F510/16F506

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|-------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 1.27 BSC | | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

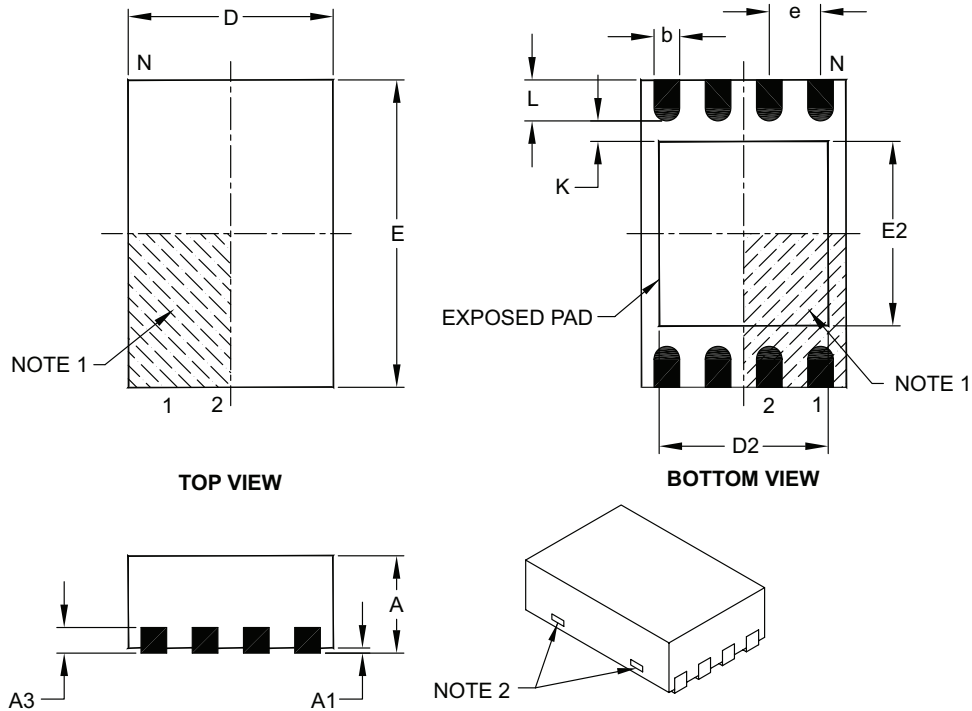
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

PIC12F510/16F506

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 0.50 BSC | | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | 0.20 REF | | |
| Overall Length | D | 2.00 BSC | | |
| Overall Width | E | 3.00 BSC | | |
| Exposed Pad Length | D2 | 1.30 | – | 1.75 |
| Exposed Pad Width | E2 | 1.50 | – | 1.90 |
| Contact Width | b | 0.18 | 0.25 | 0.30 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package may have one or more exposed tie bars at ends.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

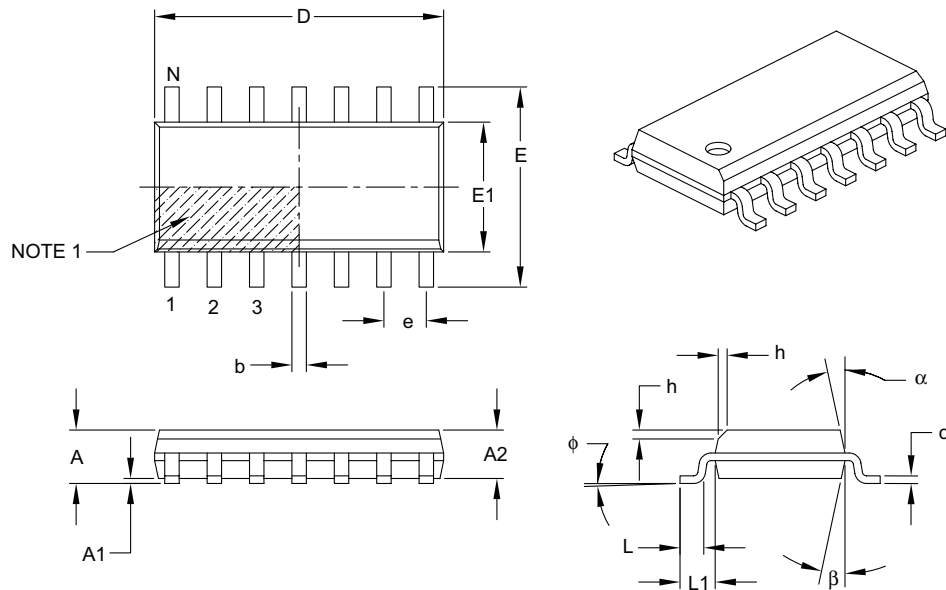
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123B

PIC12F510/16F506

14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|----------|-------------|-----|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 14 | | |
| Pitch | e | 1.27 BSC | | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | – |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | 6.00 BSC | | |
| Molded Package Width | E1 | 3.90 BSC | | |
| Overall Length | D | 8.65 BSC | | |
| Chamfer (optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | 1.04 REF | | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Mold Draft Angle Top | α | 5° | – | 15° |
| Mold Draft Angle Bottom | β | 5° | – | 15° |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

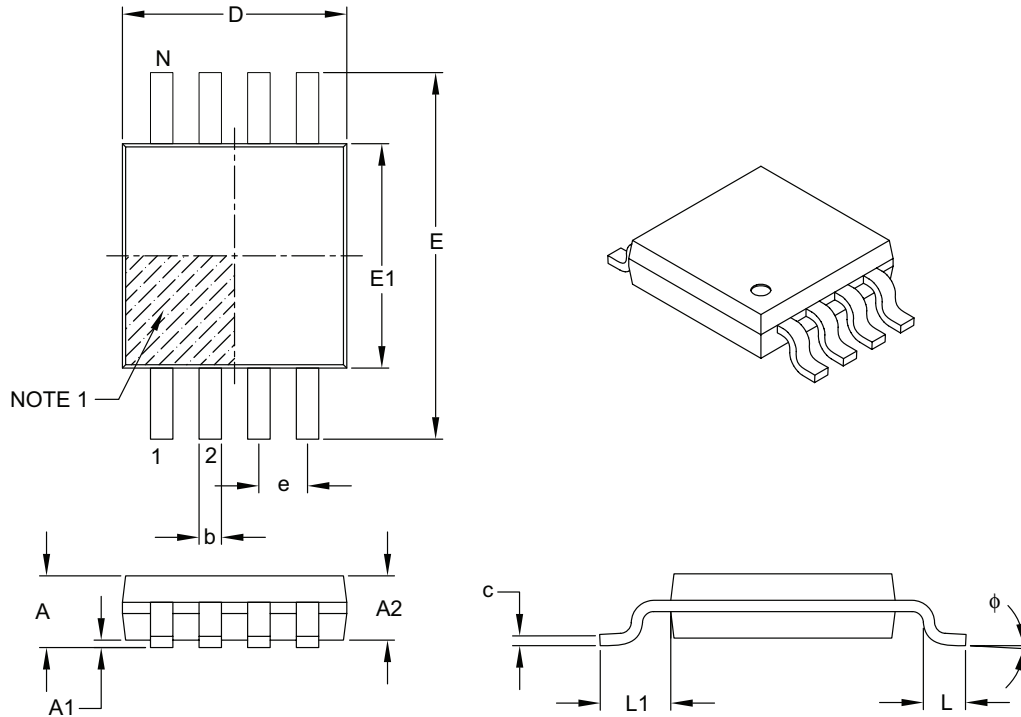
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|--------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | – | – | 1.10 |
| Molded Package Thickness | A2 | 0.75 | 0.85 | 0.95 |
| Standoff | A1 | 0.00 | – | 0.15 |
| Overall Width | E | 4.90 BSC | | |
| Molded Package Width | E1 | 3.00 BSC | | |
| Overall Length | D | 3.00 BSC | | |
| Foot Length | L | 0.40 | 0.60 | 0.80 |
| Footprint | L1 | 0.95 REF | | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.08 | – | 0.23 |
| Lead Width | b | 0.22 | – | 0.40 |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

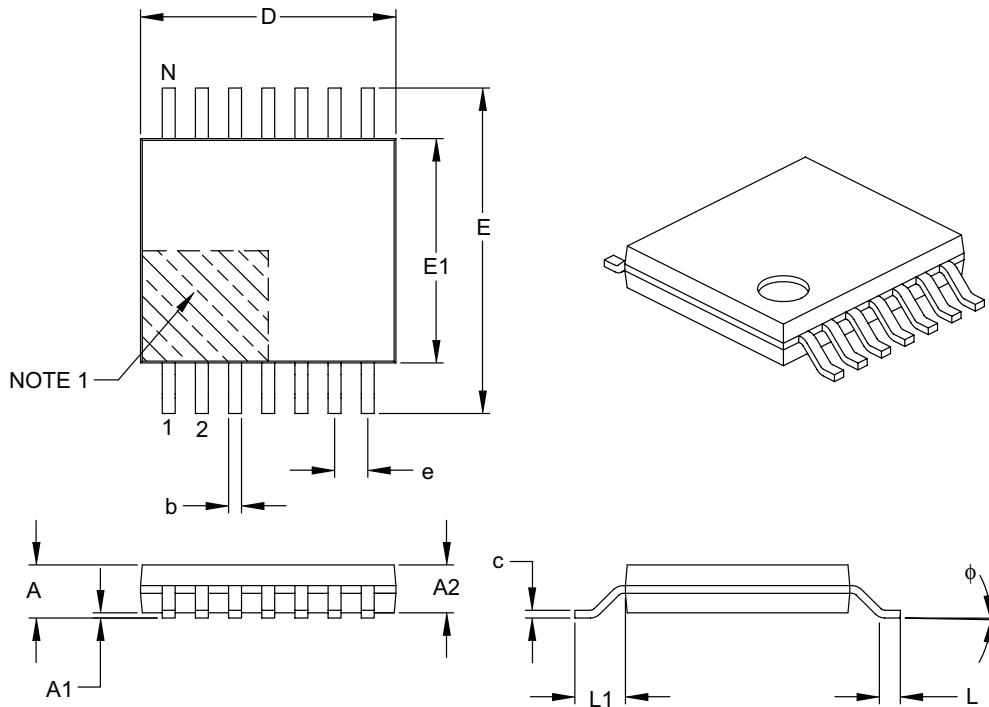
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

PIC12F510/16F506

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|--------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 14 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.80 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Overall Width | E | 6.40 BSC | | |
| Molded Package Width | E1 | 4.30 | 4.40 | 4.50 |
| Molded Package Length | D | 4.90 | 5.00 | 5.10 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | 1.00 REF | | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.19 | – | 0.30 |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087B

APPENDIX A: REVISION HISTORY

Revision A

Original release.

Revision B

Page 3 – Special Microcontroller Features and Low-Power Features sections.

PIC12F510 Pin Diagram.

Section 3.0 – Figure 3-1, Figure 3-2, Table 3-2, Table 3-3.

Section 4.0 – First paragraph, Section 4.2 - Figure references, Tables 4-1 and 4-2 (Note 1).

Section 5.0 – Table 5-2, Table 5-6 Title.

Section 6.0

Section 7.0 – First paragraph, Section 7.7, Register 7-1, Register 7-2, Register 7-3, Figure 7-1, Figure 7-2, Sections 7.4 through 7.7, Table 7-1.

Section 8.0 – Sections 8.0 through 8.2, Figure 8-1, Table 8-1.

Section 9.0 – Table 9-2, Register 9-1, Register 9-2, Table 9-3.

Section 10.0 – Registers 10-1 and 10-2 (Note 1), Table 10-2 (Note 2), Section 10.2.5, Section 10.3, Table 10-3, Table 10-4, Table 10-5, Section 10.4, Section 10.5, Section 10.6.1, Section 10.9, 10.9.1, 10.9.2, Section 10.11.

Section 13.0 – 13.1 DC Characteristics, 13.2 DC Characteristics, Table 13-1, Table 13-3, Table 13-4.

Revision C (03/2007)

Revised Table 3-2 GP3 and Legend; Revised Table 3-3 RB3 and Legend; Updated Registers to new format; Revised Section 9.1; Revised Table 9-2; Revised 13.1 DC Characteristics D025; Revised Table 13-2 and Table 13-3 and Notes; Replaced Package Drawings (Rev. AN); Added DFN package; Replaced Development Support Section; Revised Product ID System.

Revision D (11/2007)

Revised Table 1-1; Table 4-1, Table 4-2; Figure 4-5; Register 7-1 (Note 1); Register 8-1; Figure 13-4; 13.1 - 13.3; Table 13-1, Table 13-3, Table 13-6, Table 13-7, Table 13-9; Figure 14-4, Figure 14-14; Section 14.0; Packaging; Product ID System.

PIC12F510/16F506

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PIC12F510/16F506

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| <u>PART NO.</u> | <u>X</u> | <u>/XX</u> | <u>XXX</u> |
|--|--|--|--|
| Device | Temperature Range | Package | Pattern |
| Device: PIC16F506 PIC12F510 PIC16F506T ⁽¹⁾ PIC12F510T ⁽²⁾ VDD range 2.0V to 5.5V | Temperature Range: I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended) | Package: MC = 8L DFN 2x3 (DUAL Flatpack No-Leads) ^(3, 4) MS = Micro-Small Outline Package (MSOP) ^(3, 4) P = Plastic (PDIP) ⁽⁴⁾ SL = 14L Small Outline, 3.90 mm (SOIC) ⁽⁴⁾ SN = 8L Small Outline, 3.90 mm Narrow (SOIC) ⁽⁴⁾ ST = Thin Shrink Small Outline (TSSOP) ⁽⁴⁾ | Pattern: QTP, SQTP Code or Special Requirements (blank otherwise) |
| Examples: a) PIC16F506-E/P 301 = Extended Temp., PDIP package, QTP pattern #301 b) PIC16F506-I/SN = Industrial Temp., SOIC package c) PIC16F506T-E/P = Extended Temp., PDIP package, Tape and Reel | | | |
| Note 1: T = in tape and reel SOIC and TSSOP packages only 2: T = in tape and reel SOIC and MSOP packages only. 3: PIC12F510 only. 4: Pb-free. | | | |



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10/05/07



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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