MORE THAN 16,057 SECTORS (271,299,072 BITS) CMOS 3.3V-ONLY SERIAL READ FLASH MEMORY

DESCRIPTION

The MITSUBISHI M5M29F25611 is a CMOS Flash Memory with AND type multi-level memory cells.

It has fully automatic programming and erase capabilities with a single 3.3V power supply.

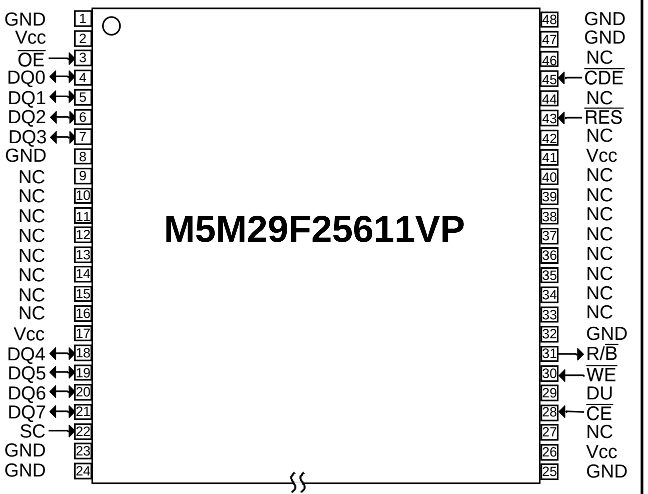
The functions are controlled by simple external commands. To fit the I/O card applications, the unit of programming and erase is as small as (2048+64) bytes.

Available sectors of M5M29F25611 are more than 16,057(98% of all sector address) and less than 16,384 sectors.

FEATURES

- On-board single power supply(Vcc) :
  Vcc=3.0V to 3.6V
- Organization
  AND Flash Memory :
  (2048+64)bytes x (More than 16,057 sectors)
  Data register : (2048+64)bytes
- Multi-level memory cell:
  2bit / per memory cell.
- Automatic programming :
  Sector program time : 2.5 ms typ.
  System bus free
  Address,data latch function
  Internal automatic program verify function
  Status data polling function
- Automatic erase :
  Single sector erase time : 1.0 ms typ.
  System bus free
  Internal automatic erase verify function
  Status data polling function
- Erase mode :
  Single sector erase ((2048+64)byte unit)
- Fast access time :
  Serial read First access time : 50µs max.
  Serial access time : 50ns max.
- Low power dissipation :
  I_{CC2} = 30mA typ. / 50mA max. (Read)
  I_{SB2} = 30µA typ. / 50µA max. (Standby)
  I_{CC3} = 20mA typ. / 40mA max. (Program)
  I_{CC4} = 20mA typ. / 40mA max. (Erase)
  I_{SB3} = 1µA typ. / 10µA max. (Deep standby)
- Package : 48pin-TSOP(I) (12.0 x 20.0mm2)

PIN CONFIGURATION(TOP VIEW)



Outline 48P3R-B

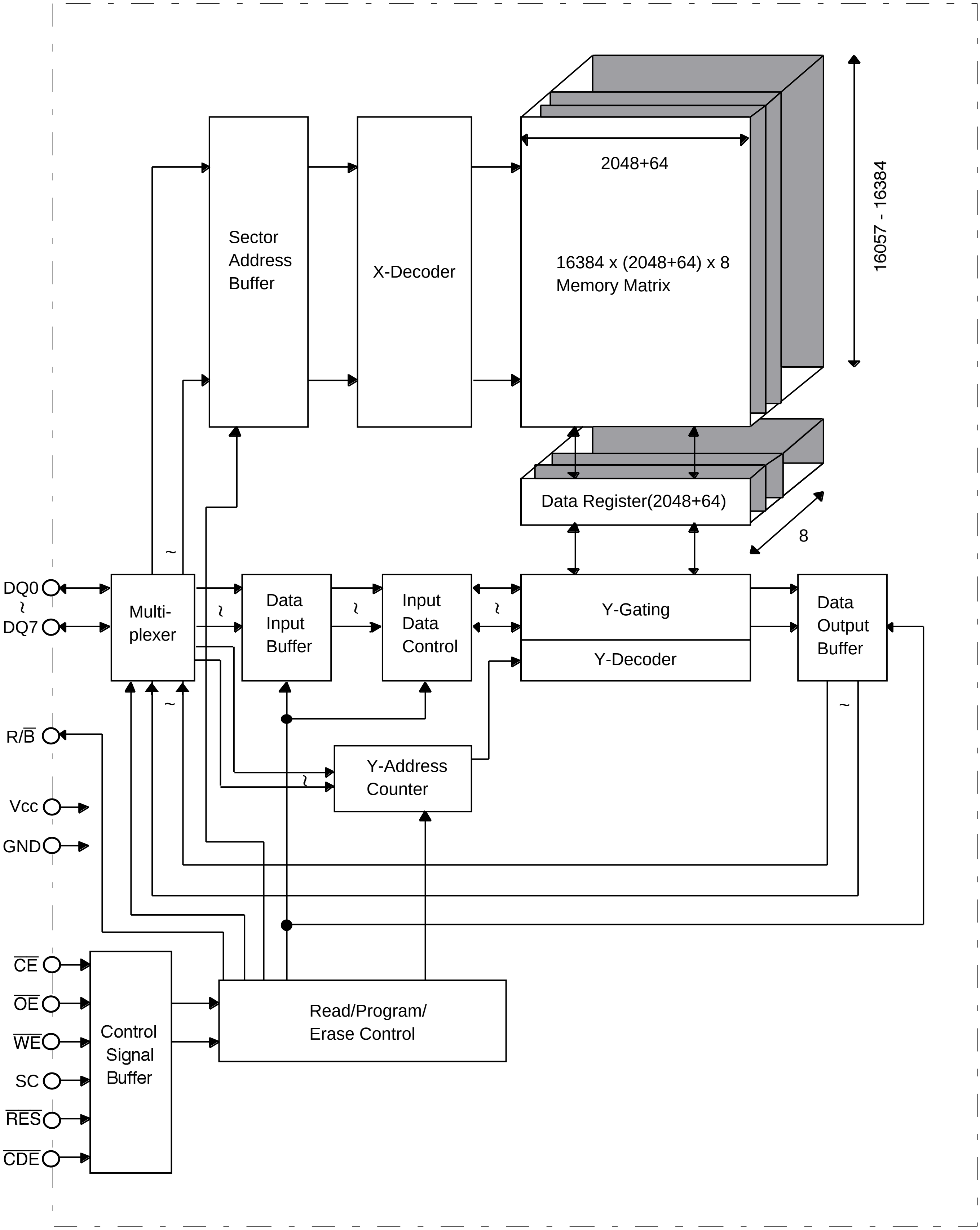
Pin Description

Pin name	Function
DQ0-7	Input / Output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
$\overline{CDE}$	Command data enable
Vcc note1	Power supply
GND note1	Ground
R/$\overline{B}$	Ready / $\overline{\text{BUSY}}$
$\overline{RES}$	Reset
SC	Serial clock
NC	No connect
DU note2	Don't Use

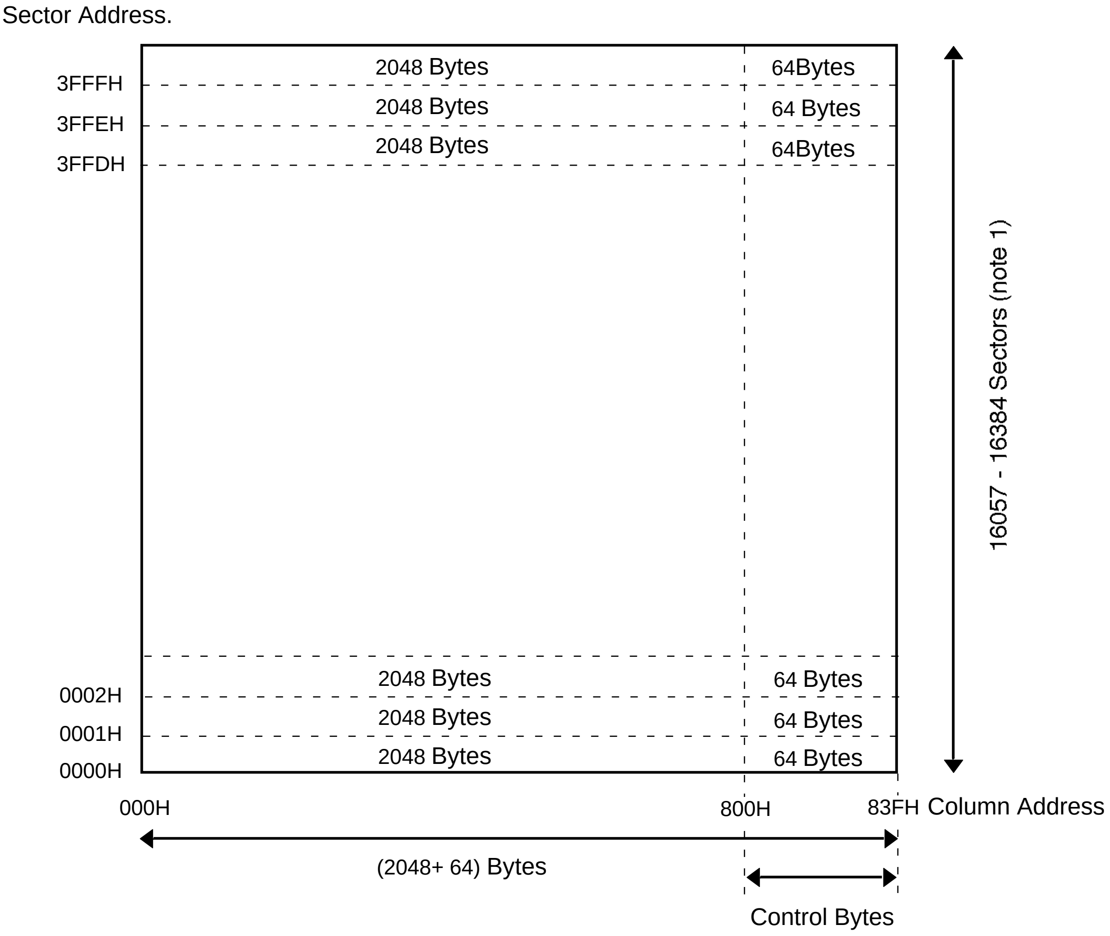
Note1:All Vcc and GND pins should be connected to a common power supply and a ground, respectively.

Note2:Pin should not be connected to anything.

Block Diagram



Memory Map & Address



		DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7
Sector address	SA(1) : First Cycle	SA0	SA1	SA2	SA3	SA4	SA5	SA6	SA7
	SA(2) : Second Cycle	SA8	SA9	SA10	SA11	SA12	SA13	X	X
Column address	CA(1) : First Cycle	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7
	CA(2) : Second Cycle	CA8	CA9	CA10	CA11	X	X	X	X

(Note2)

Note 1: Some failed sectors may exist in the device.
The failed sectors can be recognized by reading the sector valid data written in a part of the column address 820H - 825H. The sector valid data must be read and kept outside of the sector before the sector erase.
When the sector is programmed, the sector valid data should be written back to the sector.

2: An X means “Don’t care”. The pin level can be set to either V_{IL} or V_{IH}, as shown on page 12.

Mode Selection

Pin Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	SC	$\overline{RES}$	$\overline{CDE}$	(note3) R/$\overline{B}$	DQ0 - DQ7
Deep Standby (note4)	X	X	X	X	V_{ILR}	X	V_{OH}	Hi - Z
Standby	V_{IH}	X	X	X	V_{IHR}	X	V_{OH}	Hi - Z
Output disable	V_{IL}	V_{IH}	V_{IH}	X	V_{IHR}	X	V_{OH}	Hi - Z
Status register read (note1)	V_{IL}	V_{IL}	V_{IH}	X	V_{IHR}	X	V_{OH}	Status register outputs
Command Write (note2)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IHR}	V_{IL}	V_{OH}	Din

Notes: 1. Default mode after the power on is the status register read mode(refer to status transition P.11).
From DQ0 to DQ7 pins output the status when $\overline{CE}$=V_{IL} and $\overline{OE}$=V_{IL}.
2. Refer to the command definition(P.5). Data can be read, programmed and erased after commands are written in this mode.
3. The R/$\overline{B}$ bus should be pulled up to Vcc to maintain the V_{OH} level while the R/$\overline{B}$ pin outputs a high impedance.
4. An X means “Don’t care”. The pin level can be set to either V_{IL} or V_{IH} as shown on page 12.

Pin Description

$\overline{CE}$

$\overline{CE}$ is used to select the device. The status returns to the Standby at the rising edge of $\overline{CE}$ in the reading operation. However, the status does not return to the Standby at the rising edge of $\overline{CE}$ in the busy state in programming and erase operation.

$\overline{OE}$

Memory data, status register data and identifier code (ID code) can be read, when $\overline{OE}$ is V_{IL}.

$\overline{WE}$

Commands and address are latched at the rising edge of $\overline{WE}$.

SC

Programming and reading data is latched at the rising edge of SC.

$\overline{RES}$

$\overline{RES}$ pin must be kept at the V_{ILR} (GND±0.2V) level when Vcc is turned on and off. In this way, data in the memory is protected against unintentional erase and programming. $\overline{RES}$ must be kept at the V_{IHR} (Vcc±0.2V) level during any operations such as programming, erase and read

$\overline{CDE}$

Commands and data are latched when $\overline{CDE}$ is V_{IL} and Address is latched when $\overline{CDE}$ is V_{IH}.

R/$\overline{B}$

The R/$\overline{B}$ indicates the program/erase status of the flash memory. The R/$\overline{B}$ signal is initially at a high impedance state. It turns to a V_{OL} level after the (40H) command in programming operation or the(B0H) command in erase operation. No commands can be written during the R/$\overline{B}$ pin outputs a V_{OL}. After the erase or programming operation finishes, the R/$\overline{B}$ signal turns back to the high impedance state.

The R/$\overline{B}$ indicates the first access status of the flash memory in serial read (1) and (2). It turns to a V_{OL} level after the sector address (SA(2)) in serial read (1) and serial read (2) operation.
No commands can be written during the R/$\overline{B}$ pin outputs a V_{OL}. Also, no serial clock can be input during the R/$\overline{B}$ pin outputs a V_{OL}. After the first access operation finishes, the R/$\overline{B}$ signal turns back to the high impedance state.

DQ0-DQ7

The DQ pins are used to input data, address and command, and are used to output memory data, status register data and identifier code (ID code).

Command Definition (note 1,2)

Command				First		Second cycle		
			Bus cycles	Operation mode (note 3)	Data in	Operation mode	Data in	Data out
Serial read(1)	Without CA		3	Write	00H	Write	SA(1) (note 4)	-
	With CA		3+2h(note6)	Write	00H	Write	SA(1) (note 4)	-
Serial read(2)			3	Write	F0H	Write	SA(1) (note 4)	-
Read identifier codes			1	Write	90H	Read	-	ID (note8,9)
Data Recovery Read			1	Write	01H	Read	-	Recovery Data
Auto Erase	Single sector		4	Write	20H	Write	SA(1) (note 4)	-
Auto Program	Program (1)	Without CA (note 7)	4	Write	10H	Write	SA(1) (note 4)	-
		With CA (note 7)	4+2h(note6)	Write	10H	Write	SA(1) (note 4)	-
	Program (2) (note 10)		4	Write	1FH	Write	SA(1) (note 4)	-
	Program (3) (control bytes) (note 7)		4	Write	0FH	Write	SA(1) (note 4)	-
	Program (4)	Without CA (note 7)	4	Write	11H	Write	SA(1) (note 4)	-
		With CA (note 7)	4+2h(note6)	Write	11H	Write	SA(1) (note 4)	-
Reset			1	Write	FFH	-	-	-
Clear status register			1	Write	50H	-	-	-
Data Recovery Write			4	Write	12H	Write	SA(1) (note 4)	-

Command				Third cycle		Fourth cycle	
			Bus cycles	Operation mode	Data in	Operation mode	Data in
Serial read(1)	Without CA		3	Write	SA(2) (note4)	-	-
	With CA		3+2h(note6)	Write	SA(2) (note4)	Write	CA(1) (note5)
Serial read(2)			3	Write	SA(2) (note4)	-	-
Auto Erase	Single sector		4	Write	SA(2) (note4)	Write	B0H (note11)
Auto Program	Program (1)	Without CA (note 7)	4	Write	SA(2) (note4)	Write	40H (note11,12)
		With CA (note 7)	4+2h(note6)	Write	SA(2) (note4)	Write	CA(1) (note5)
	Program (2) (note 10)		4	Write	SA(2) (note4)	Write	40H (note11,12)
	Program (3) (control bytes) (note 7)		4	Write	SA(2) (note4)	Write	40H (note11,12)
	Program (4)	Without CA (note 7)	4	Write	SA(2) (note4)	Write	CA(1) (note5)
		With CA (note 7)	4+2h(note6)	Write	SA(2) (note4)	Write	40H (note11,12)
Data Recovery Write			4	Write	SA(2) (note4)	Write	40H (note11,12)

Command				Fifth cycle		Sixth cycle	
			Bus cycles	Operation mode	Data in	Operation mode	Data in
Serial read(1)	With CA		3+2h(note6)	Write	CA(2) (note5)	-	-
Auto Program	Program (1)	With CA (note 7)	4+2h(note6)	Write	CA(2) (note5)	Write	40H (note11,12)
	Program (4)	With CA (note 7)	4+2h(note6)	Write	CA(2) (note5)	Write	40H (note11,12)

Notes :
1. Commands, sector address and column address are latched at rising edge of $\overline{WE}$ pulses.
   Program data is latched at rising edge of SC pulses.
2. The chip is in the read status register mode when $\overline{RES}$ is set to V_{IHR} first time after the power up.
3. Refer to the command read and write mode in mode selection table (P.4).
4. SA(1)=Sector address (SA0 - SA7), SA(2)=Sector address (SA8 - SA13).
5. CA(1)=Column address (CA0 - CA7), CA(2)=Column address (CA8 - CA11).(0≤CA11 - CA0≤83FH)
6. The variable h is the input number of times of set of CA(1) and CA(2).(1≤h≤2048+64)
   Set of CA(1) and CA(2) can be input not only one time but free times.
7. By using program(1) and (3), data can additionally be programmed for each sector before erase.
8. ID=Identifier code; Manufacturer code (1CH), Device code (6CH).
9. The manufacturer identifier code is output when $\overline{CDE}$ is low and the device identifier code is output when $\overline{CDE}$ is high.
10. Before program (2) operations, data in the programmed sector must be erased.
11. No commands can be written during auto program and erase (when the R/$\overline{B}$ pin outputs a V_{OL}).
12. The fourth cycle or sixth cycle of the auto program comes after the program data input is complete.

Mode Description

Read

Serial read(1)

Memory data D0-D2111 in the sector of address SA is sequentially read. Output data is not valid after the number of the serial clock SC pulse exceeds 2112. When the column address CA is input after SA, memory data D(m) -D(m+j) in the sector of address SA is sequentially read. Then output data is not valid after the number of the SC pulse exceeds (2112-m).

The mode turns back to the Standby mode at any time when $\overline{CE}$ is V_{IH}.

Serial read(2)

Memory data D2048-D2111 in the sector of address SA is sequentially read. Output data is not valid after the number of the SC pulse exceeds 64.The mode turns back to the Standby mode at any time when $\overline{CE}$ is V_{IH}.

Automatic Erase

Single sector Erase

Memory data D0-D2111 in the sector of address SA is erased automatically by internal control circuits. After the sector erase starts, the erasure completion can be checked through the R/$\overline{B}$ signal and status data polling. All the bits in the sector are “1” after the erase. The sector valid data stored in a part of memory data D2048-D2111 must be read and kept outside of the sector before the sector erase.

Automatic program

Program(1)

Program data PD0-PD2111 is programmed into the sector of address SA automatically by internal control circuits. When CA is input after SA, program data PD(m) -PD(m+j) is programmed form CA into the sector of address SA automatically by internal control circuits. By using program(1), data can additionally be programmed for each sector before the following erase. When the column is programmed, the data of the column must be [FF].

After the programming starts, the program completion can be checked through the R/$\overline{B}$ signal and status data polling. Programmed bits in the sector turn from “1” to “0” when they are programmed. The sector valid data should be included in the program data PD2048-PD2111. In this mode, E/W number of times must be counted whenever program(1) execute.

Program(2)

Program data PD0-PD2111 is programmed into the sector of address SA automatically by internal control circuits. After the programming starts, the program completion can be checked through the R/$\overline{B}$ signal and status data polling. Programmed bits in the sector turn from “1” to “0” when they are programmed. The sector must be erased before programming. The sector valid data should be included in the program data PD2048-PD2111. In this mode, Write number of times must be counted whenever program(2) execute.

Program(3)

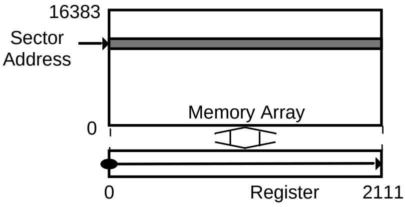
Program data PD2048-PD2111 is programmed into the sector of address SA automatically by internal control circuits. By using program(3), data can additionally be programmed for each sector before the following erase. When the column is programmed, the data of the column must be [FF].

After the programming starts, the program completion can be checked through the R/$\overline{B}$ signal and status data polling. Programmed bits in the sector turn from “1” to “0” when they programmed. In this mode, E/W number of times must be counted whenever program(3) execute.

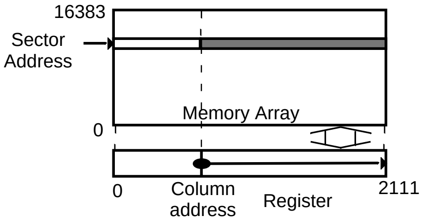
Program(4)

Program data PD0-PD2111 is programmed into the sector of address SA automatically by internal control circuits. When CA is input after SA, program data PD(m) -PD(m+j) is programmed from CA into the sector of address SA automatically by internal control circuits. By using program(4), data can be rewritten for each sector before the following erase. So the column data before programming operation are either “1” to “0”.

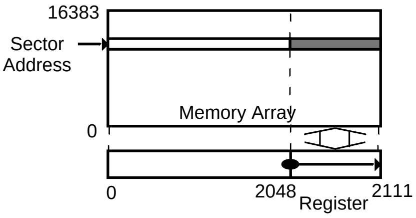
After the programming starts,the program completion can be checked through the R/$\overline{B}$ single and status data polling. The sector valid data should be included in the program data PD2048-PD2111. In this mode, E/W number of times must be counted whenever program(4) execute.



Serial read(1), (Without CA)
Program(1), (Without CA)
Program(2)
Program(4), (Without CA)



Serial read(1), (With CA)
Program(1), (With CA)
Program(4), (With CA)



Serial read(2)
Program(3)

Status Register Read

The status returns to the register read mode from Standby mode ,when $\overline{CE}$ and $\overline{OE}$ is V_{IL}. In the status register read mode, DQ pins output the same operation status as in the status data polling defined in the function description, table 1 (page 34).

Identifier Read

The manufacturer and device identifier code can be read in the identifier read mode. The manufacturer and device identifier code is selected with $\overline{CDE}$ V_{IL} and V_{IH}, respectively.

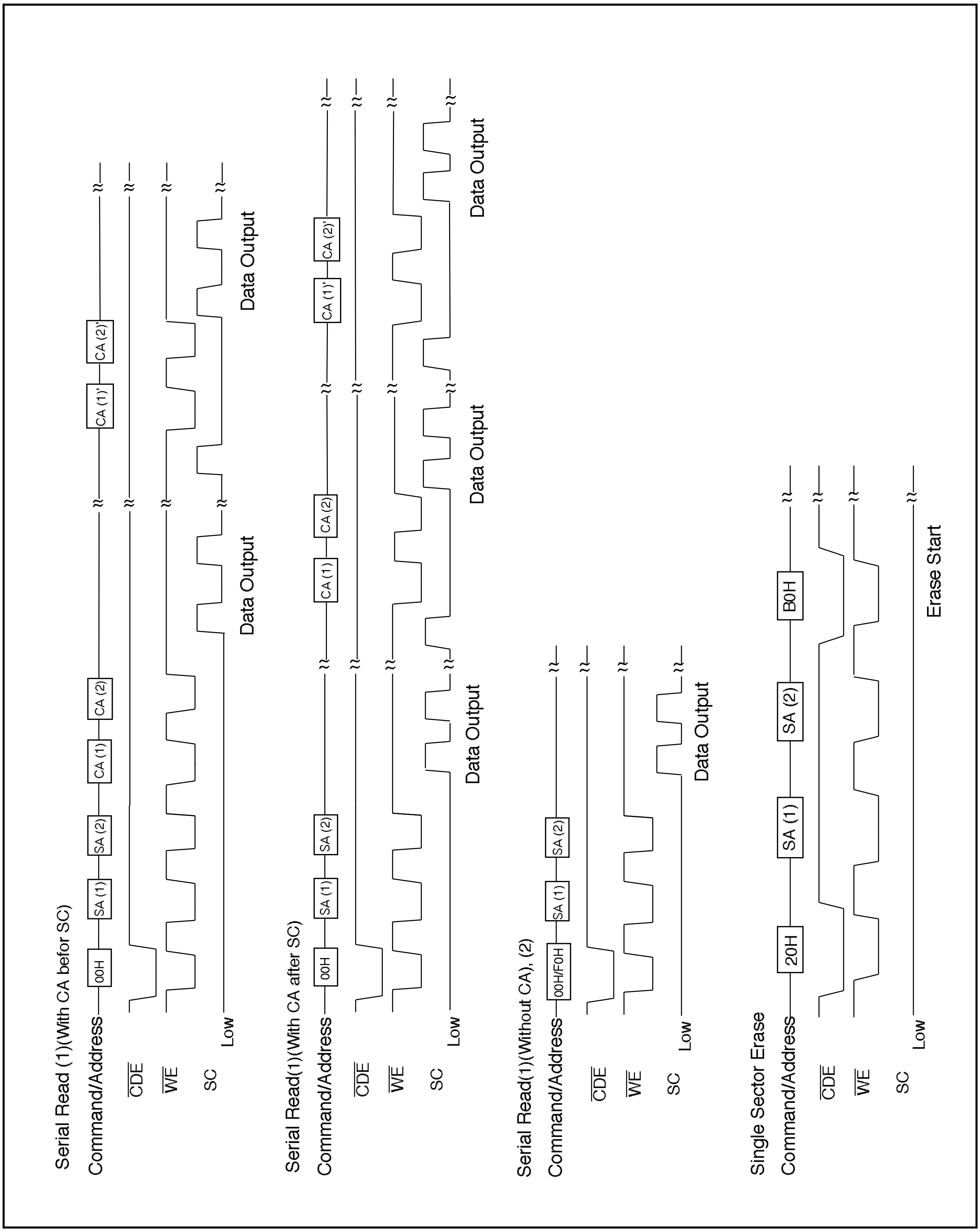
Data Recovery Read

When programming was error, the program data can be read. When additional programming (Program(1),(3),(4))was error, the data compounded of the program data and the original data in the sector of address SA can be read. Output data is not valid after the number of SA pulse exceeds 2112. The mode turns back to the Standby mode at any time when $\overline{CE}$ is V_{IH}. (See timing waveform in page 31)

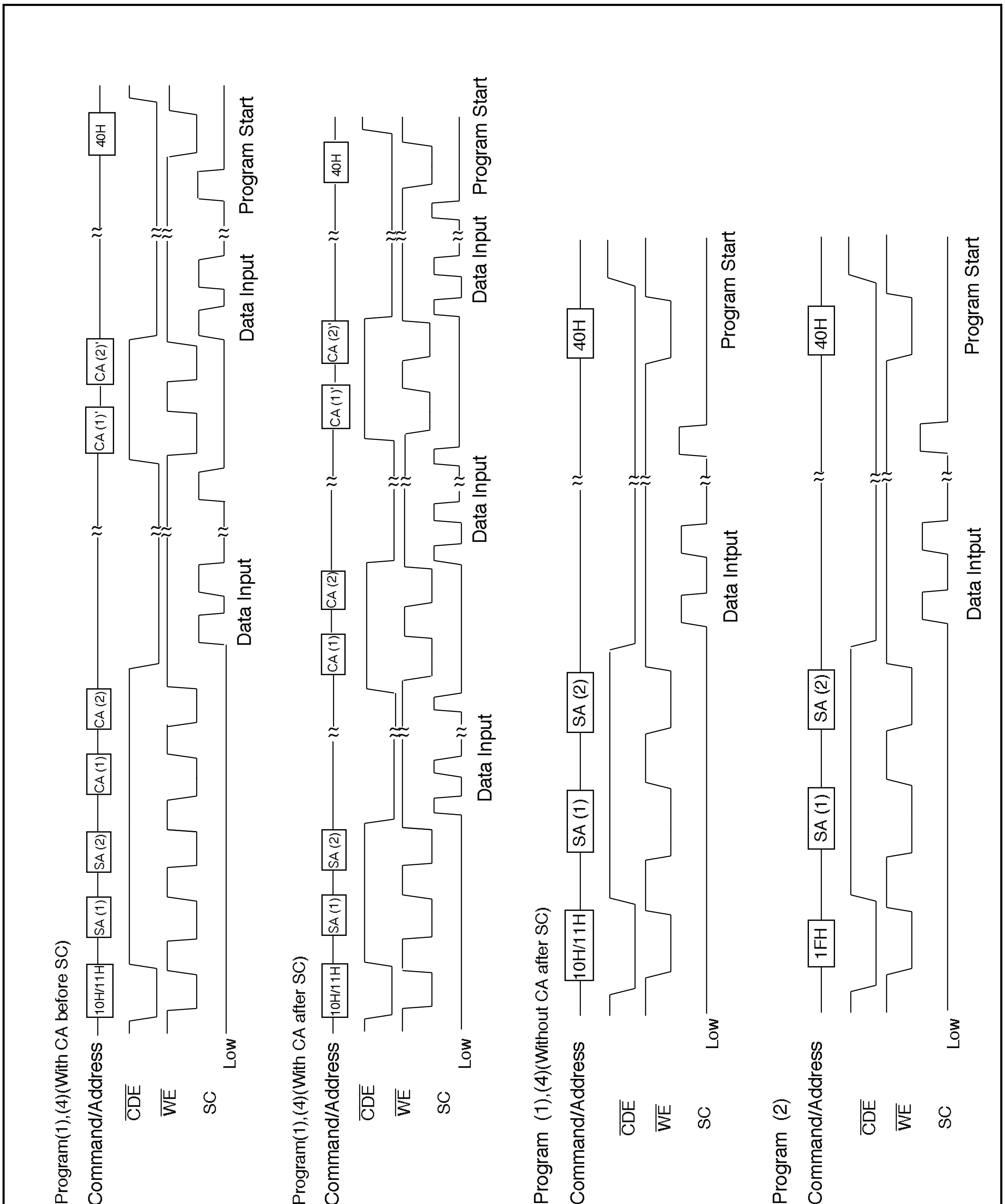
Data Recovery Write

When programming into a sector of address SA was an error,the program data can be re-written automatically by selecting the other sector SA'.In this Case,top address [SA13] of sector of address SA' must be the same as SA.Since the data recovery write mode utilizes program(4),rewritten sector of address SA' needs no sector erase before rewritten.After the data recovery write mode starts,the program completion can be checked through R/$\overline{B}$ signal and the status data polling.

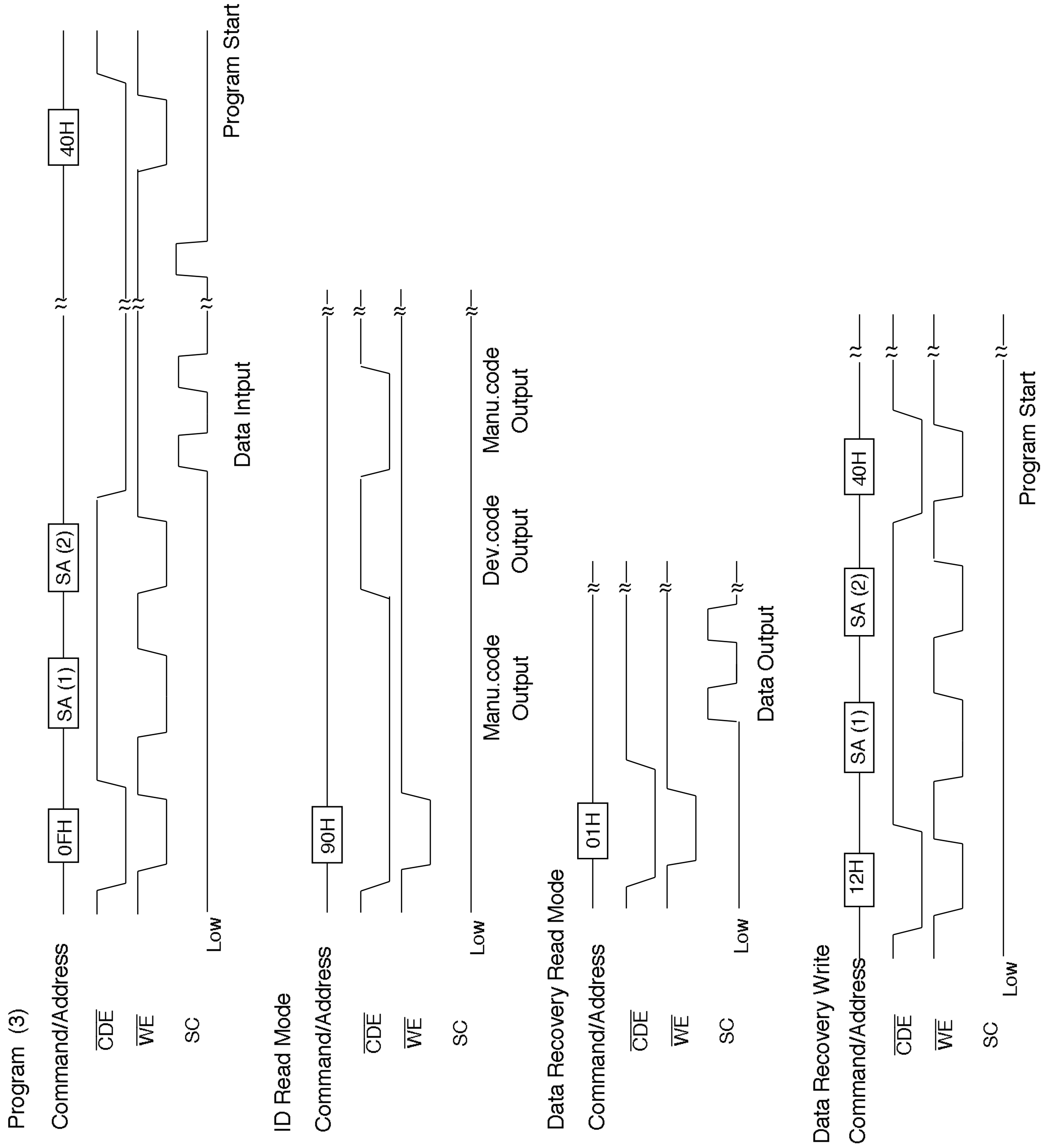
Command / Address / Data Input Sequence



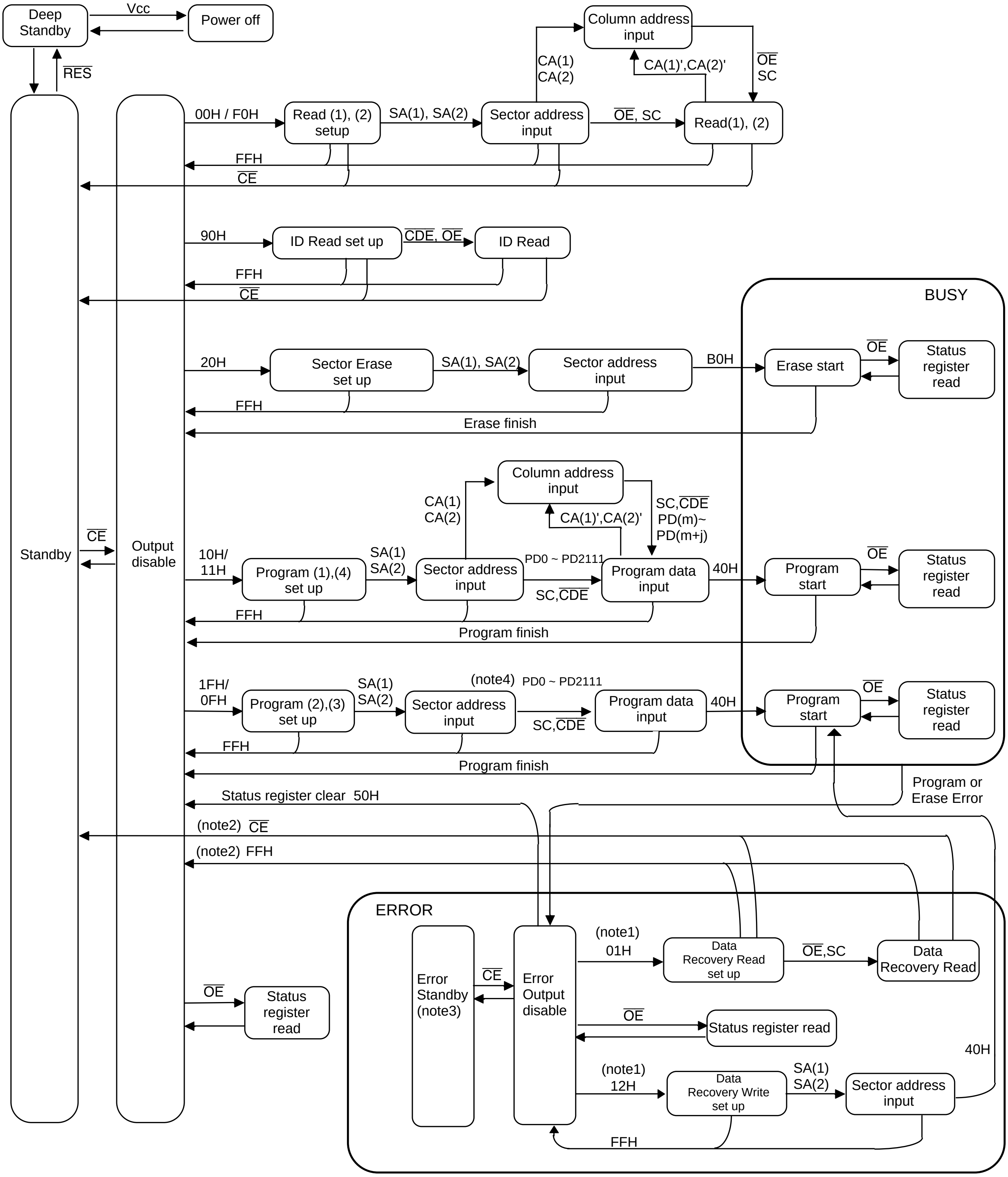
Command / Address / Data Input Sequence



Command / Address / Data Input Sequence



Status Transition



Note 1: (01H)/(12H) Data Recovery Read/Write can be used only for Program(1),(2),(3),(4) Errors.
2: When Reset is done by CE or FFH, Error Status Flag is cleared.
3: When Error Standby, Icc3 level is current.
4: When Program(3) mode, input data is PD2048 ~ PD2111.

Absolute Maximum Ratings

Symbol	Parameter	Test conditions	Ratings	Unit
V_{IN}, V_{OUT}	All input and output voltages	With respect to GND	-0.6 to +7 1)	V
V_{cc}	Vcc voltage		-0.6 to +7	V
T_{opr}	Operating temperature range		0 to +70	°C
T_{stg}	Storage temperature range 2)		-65 to +125	°C
T_{bias}	Storage temperature under bias		-10 to +80	°C

Notes : 1. V_{IN} , V_{OUT} = -2.0V for pulse width ≤ 20ns
2. Device storage temperature range before programming.

Capacitance (Ta = 25°C , f = 1MHz)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{in}	Input capacitance	Ta = 25°C, f = 1MHz, V_{IN} = V_{OUT} = 0V	-	-	6	pF
C_{out}	Output capacitance		-	-	12	pF

Read Operation

DC Characteristics (Vcc = 3.0V to 3.6V , Ta = 0 to +70°C)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	GND ≤ V_{IN} ≤ V_{CC}	-	-	2	µA
I_{LO}	Output leakage current	GND ≤ V_{OUT} ≤ V_{CC}	-	-	2	µA
I_{SB1}	Standby Vcc current	$\overline{CE}$ = V_{IH}	-	0.3	1	mA
I_{SB2}		$\overline{CE}$ = V_{CC} ± 0.2V $\overline{RES}$ = V_{CC} ± 0.2V	-	30	50	µA
I_{SB3}	Deep Standby Vcc current	$\overline{RES}$ = GND ± 0.2V	-	1	10	µA
I_{CC1}	Operating Vcc current	I_{OUT} = 0mA, f = 0.2MHz	-	20	25	mA
I_{CC2}		I_{OUT} = 0mA, f = 20MHz	-	30	50	mA
V_{IL}	Input low voltage		-0.3 1)	-	0.8	V
V_{IH}	Input high voltage		2.0	-	V_{CC} + 0.3 2)	V
V_{ILR}	Input low voltage($\overline{RES}$ pin)		-0.2	-	0.2	V
V_{IHR}	Input high voltage($\overline{RES}$ pin)		V_{CC} - 0.2	-	V_{CC} + 0.2	V
V_{OL}	Output low voltage	I_{OL} = 2mA	-	-	0.4	V
V_{OH}	Output high voltage	I_{OH} = -2mA	2.4	-	-	V

Notes : 1. V_{IL}min = -1.0V for pulse width ≤ 50ns. V_{IL}min = -2.0V for pulse width ≤ 20ns.
2. V_{IH}max = Vcc + 1.5V for pulse width ≤ 20ns. If V_{IH} is over the specified maximum value, the read operations are not guaranteed.

AC Characteristics (for power on and off, serial read) (Vcc =3.0 to 3.6V, Ta = 0 to +70°C)

Test Conditions

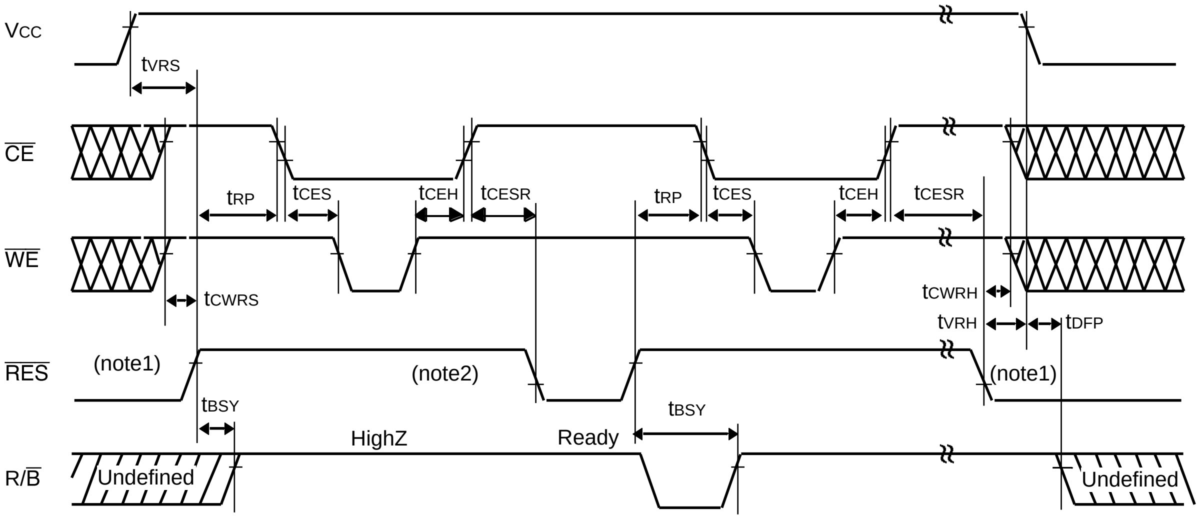
- Input pulse levels : 0.4V/2.4V
- Input pulse levels for RES : 0.2V/Vcc-0.2V
- Input rise and fall times : ≤ 5ns
- Output load : 1 TTL gate + 100pF
  (Including scope and jig.)
- Reference levels for measuring timing : 0.8V, 1.8V

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{CWC}	Write cycle time		120	-	-	ns
t_{SCC}	Serial clock cycle time		50	-	-	ns
t_{CES}	$\overline{\text{CE}}$ setup time		0	-	-	ns
t_{CEH}	$\overline{\text{CE}}$ hold time		0	-	-	ns
t_{WP}	Write pulse time	$\overline{\text{CE}}$ = V_{IL}, $\overline{\text{OE}}$ = V_{IH}	60	-	-	ns
t_{WPH}	Write pulse high time		40	-	-	ns
t_{AS}	Address setup time		50	-	-	ns
t_{AH}	Address hold time		10	-	-	ns
t_{DS}	Data setup time		50	-	-	ns
t_{DH}	Data hold time		10	-	-	ns
t_{SAC}	SC to output delay	$\overline{\text{CE}}$ = $\overline{\text{OE}}$ = V_{IL}, $\overline{\text{WE}}$ = V_{IH}	-	-	50	ns
t_{OES}	$\overline{\text{OE}}$ setup time for SC		0	-	-	ns
t_{OEL}	$\overline{\text{OE}}$ low to output low-z		0	-	40	ns
t_{OER}	$\overline{\text{OE}}$ setup time before read		250	-	-	ns
t_{OEWS}	$\overline{\text{OE}}$ setup time before command write		0	-	-	ns
t_{SH}	SC to output hold	$\overline{\text{CE}}$ = $\overline{\text{OE}}$ = V_{IL}, $\overline{\text{WE}}$ = V_{IH}	15	-	-	ns
t_{DF} 1)	$\overline{\text{OE}}$ hight to output float	$\overline{\text{CE}}$ = V_{IL}, $\overline{\text{WE}}$ = V_{IH}	-	-	40	ns
t_{WSD} 2)	$\overline{\text{WE}}$ to SC delay time		50	-	-	µs
t_{RP}	$\overline{\text{RES}}$ to $\overline{\text{CE}}$ setup time		1	-	-	ms
t_{SOH}	SC to $\overline{\text{OE}}$ hold time		50	-	-	ns
t_{SP}	SC pulse width		20	-	-	ns
t_{SPL}	SC pulse low time		20	-	-	ns
t_{SCS}	SC setup time for $\overline{\text{CE}}$		0	-	-	ns
t_{CDS}	$\overline{\text{CDE}}$ setup time for $\overline{\text{WE}}$		0	-	-	ns
t_{CDH}	$\overline{\text{CDE}}$ hold time for $\overline{\text{WE}}$		20	-	-	ns
t_{VRS}	Vcc setup time for $\overline{\text{RES}}$	$\overline{\text{CE}}$ = V_{IH}	1	-	-	µs
t_{VRH}	$\overline{\text{RES}}$ to Vcc hold time	$\overline{\text{CE}}$ = V_{IH}	1	-	-	µs
t_{CESR}	$\overline{\text{CE}}$ setup time for $\overline{\text{RES}}$		1	-	-	µs
t_{DFP}	R/$\overline{\text{B}}$ undefined for Vcc off		0	-	-	ns
t_{BSY}	$\overline{\text{RES}}$ high to device ready		-	-	1	ms
t_{CPH}	$\overline{\text{CE}}$ pulse high time		200	-	-	ns
t_{CWRS}	$\overline{\text{CE}}$,$\overline{\text{WE}}$ setup time for $\overline{\text{RES}}$		0	-	-	ns
t_{CWRH}	$\overline{\text{RES}}$ to $\overline{\text{CE}}$,$\overline{\text{WE}}$ hold time		0	-	-	ns
t_{SW}	SC setup for $\overline{\text{WE}}$		50	-	-	ns
t_{COH}	$\overline{\text{CE}}$ hold time for $\overline{\text{OE}}$		0	-	-	ns
t_{SCD}	SA(2)to CA(2)delay time		-	-	30	µs
t_{RS}	R/$\overline{\text{B}}$ setup time for SC		200	-	-	ns
t_{DBR}	Time to device Busy on Read mode		-	-	1	µs
t_{RBSY}	Busy time on Read mode		-	45	-	µs

Notes : 1. tDF is a time after which the DQ pins become open.

2. tWSD(min) is specified as a reference point only for SC, if tWSD is greater than the specified tWSD(min) limit, then access time is controlled exclusively by tSAC.

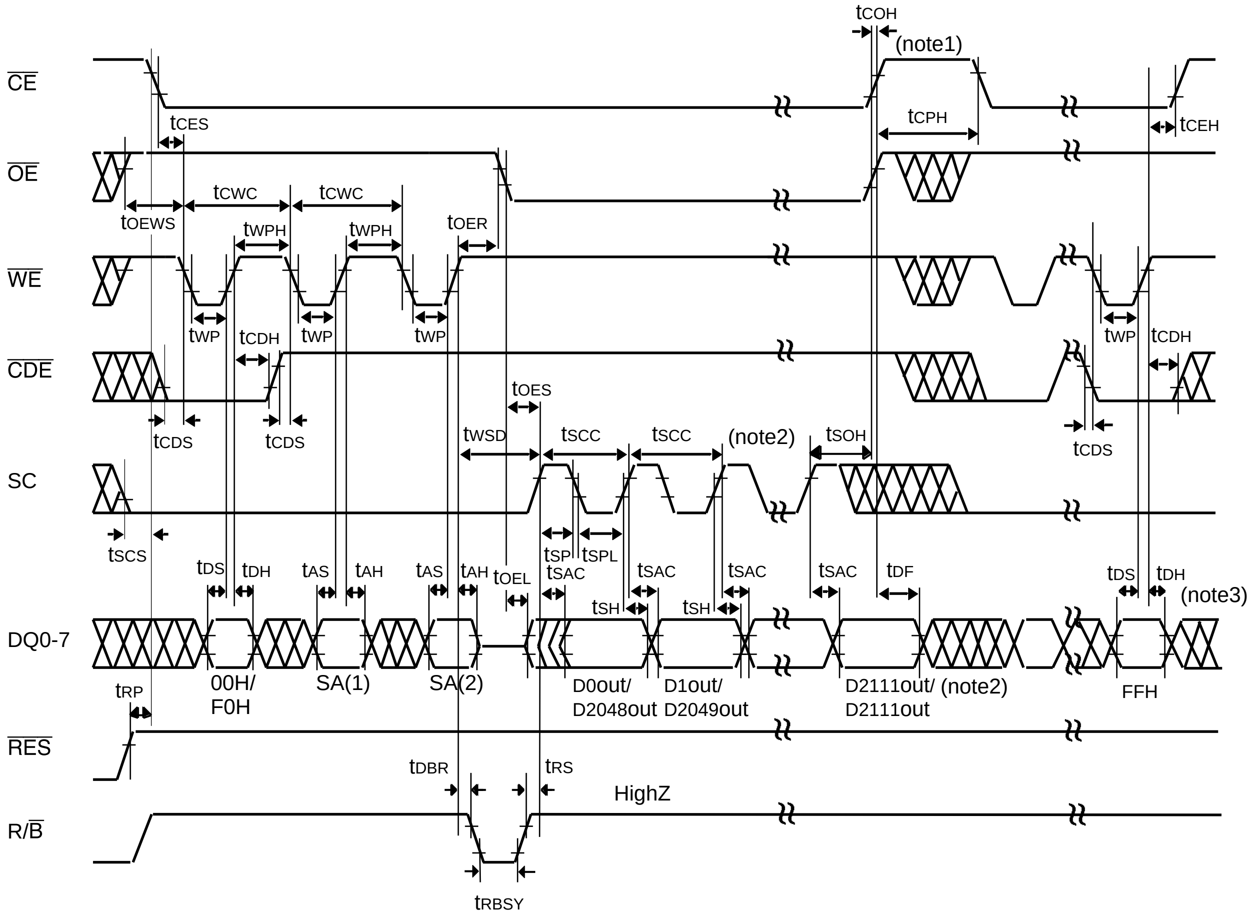
Power on and off Sequence



note1 : $\overline{\text{RES}}$ must be kept at the VILR level as shown in page 12 at the rising and falling edges of Vcc to guarantee data stored in the chip.

note2 : $\overline{\text{RES}}$ must be kept at the VIHR level specified in page 12 while DQ7 outputs the VOL level in the status data polling and R/$\overline{\text{B}}$ outputs the VOL level.

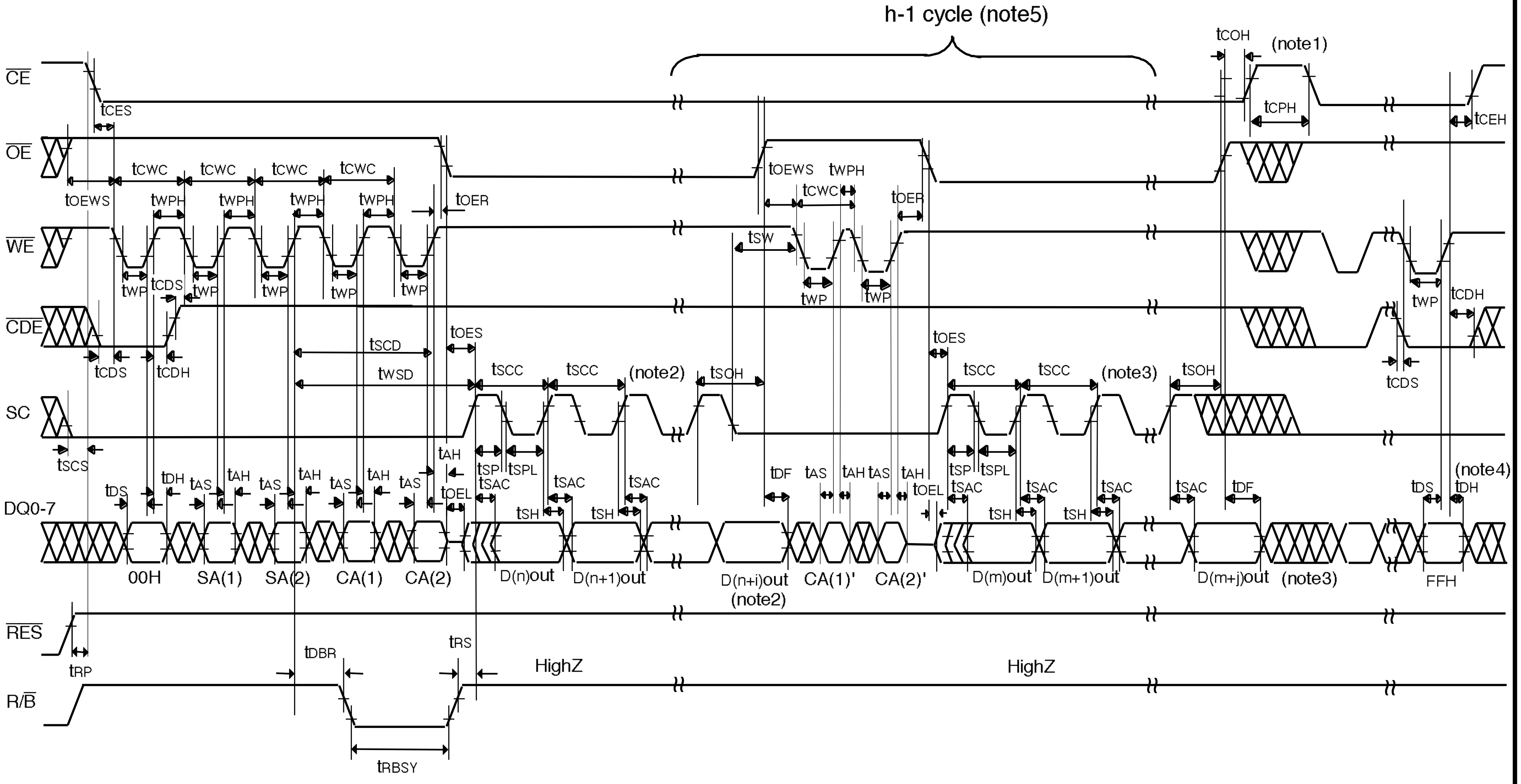
Serial Read (1)/(2) Timing Waveforms



Note 1. The status returns to the Standby at the rising edge of $\overline{\text{CE}}$.

2. Output data is not valid after the number of the SC pulse exceed 2112 and 64 in the serial read mode (1) and (2), respectively.
3. The status can return to the Ready after the command FFH is input.

Serial Read(1)with CA before SC Timing Waveforms



Note 1. The status returns to the Standby at the rising edge of $\overline{CE}$.

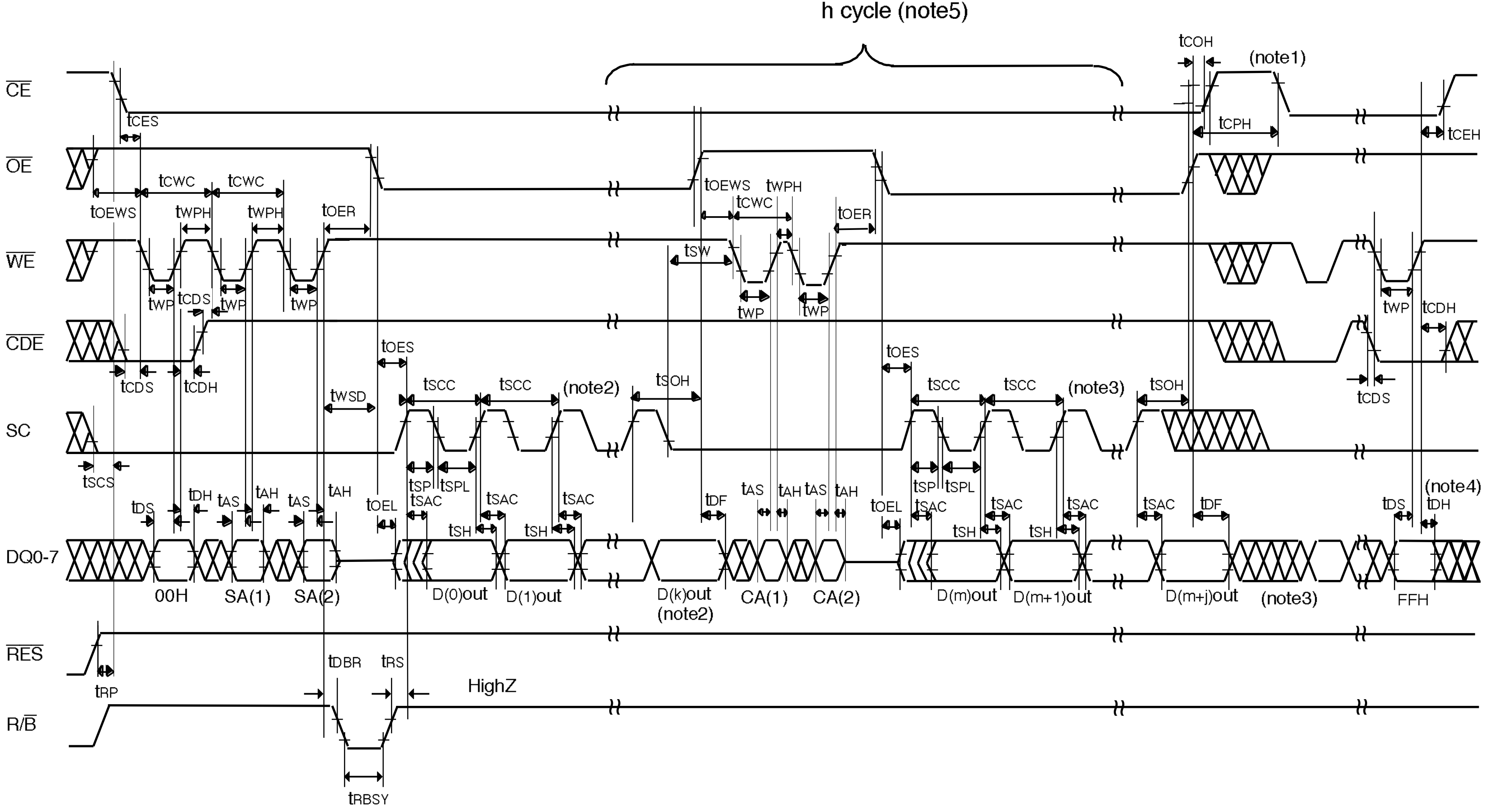
2. Output data is not valid after the number of the SC pulse exceed (2112-n).(i ≤ 2111-n, 0 ≤ n ≤ 2111)

3. Output data is not valid after the number of the SC pulse exceed (2112-m).(j ≤ 2111-m, 0 ≤ m ≤ 2111)

4. The status can return to the Ready after the command FFH is input.

5. This interval can be repeated (h-1)cycle.(1 ≤ h ≤ 2048+64)

Serial Read(1)with CA after SC Timing Waveforms



Note 1. The status returns to the Standby at the rising edge of $\overline{CE}$.
2. Output data is not valid after the number of the SC pulse exceed 2112.(0 ≤ k ≤ 2111)
3. Output data is not valid after the number of the SC pulse exceed (2112-m).(j ≤ 2111-m, 0 ≤ m ≤ 2111)
4. The status can return to the Ready after the command FFH is input.
5. This interval can be repeated h cycle.(1 ≤ h ≤ 2048+64)

Erase and Programming Operations

DC Characteristics (Vcc = 3.0V to 3.6V , Ta = 0 to +70°C)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	GND ≤ V_{IN} ≤ V_{CC}	-	-	2	µA
I_{LO}	Output leakage current	GND ≤ V_{OUT} ≤ V_{CC}	-	-	2	µA
I_{SB1}	Standby Vcc current	$\overline{CE}$ = V_{IH}	-	0.3	1	mA
I_{SB2}		$\overline{CE}$ = V_{CC} ± 0.2V $\overline{RES}$ = V_{CC} ± 0.2V	-	30	50	µA
I_{SB3}	Deep Standby Vcc current	$\overline{RES}$ = GND ± 0.2V	-	1	10	µA
I_{CC3}	Operating Vcc current	In programming	-	20	40	mA
I_{CC4}		In erase	-	20	40	mA
V_{IL}	Input low voltage		-0.3 1)	-	0.8	V
V_{IH}	Input high voltage		2.0	-	V_{CC} + 0.3 2)	V
V_{OL}	Output low voltage	I_{OL} = 2mA	-	-	0.4	V
V_{OH}	Output high voltage	I_{OH} = -2mA	2.4	-	-	V

Notes : 1. V_{IL}min = -0.6V for pulse width ≤ 20ns.
2. If V_{IH} is over the specified maximum value, the Erase and Programming operations are not guaranteed.

AC Characteristics (for Erase,program,ID read,status register read , data recovery read and data recovery write.)
(Vcc =3.0V to 3.6V, Ta = 0 to +70°C)

Test Conditions

- Input pulse levels : 0.4V/2.4V
- Input pulse levels for RES : 0.2V/Vcc - 0.2V
- Input rise and fall times : ≤ 5ns
- Output load : 1 TTL gate + 100pF
  (Including scope and jig.)
- Reference levels for measuring timing : 0.8V, 1.8V

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
t_{CWC}	Write cycle time		120	-	-	ns
t_{SCC}	Serial clock cycle time		50	-	-	ns
t_{CES}	$\overline{CE}$ setup time		0	-	-	ns
t_{CEH}	$\overline{CE}$ hold time		0	-	-	ns
t_{WP}	Write pulse width		60	-	-	ns
t_{WPH}	Write pulse high time		40	-	-	ns
t_{AS}	Address setup time		50	-	-	ns
t_{AH}	Address hold time		10	-	-	ns
t_{DS}	Data setup time		50	-	-	ns
t_{DH}	Data hold time		10	-	-	ns
t_{OEWS}	$\overline{OE}$ setup time before command write		0	-	-	ns
t_{OEPS}	$\overline{OE}$ setup time before status polling		40	-	-	ns
t_{OER}	$\overline{OE}$ setup time before read		250	-	-	ns
t_{DB}	Time to device busy		-	-	150	ns
t_{DBR}	Time to device busy on Read Mode		-	-	1	µs
t_{ASE}	Auto erase time		-	1.0	10	ms
$t_{ASP(1)}$	Auto program time (1)		-	3.0	40	ms
$t_{ASP(2)}$	Auto program time (2)		-	2.5	40	ms
$t_{ASP(3)}$	Auto program time (3)		-	3.0	40	ms
$t_{ASP(4)}$	Auto program time (4)		-	3.5	40	ms
t_{ASRW}	Data Recovery Write time		-	3.5	40	ms
t_{WSD}	$\overline{WE}$ to SC delay time		50	-	-	µs
t_{RBSY}	Busy Time on Read Mode		-	45	-	µs
t_{WSDR}	$\overline{WE}$ to SC delay time on Recovery Read Mode		2	-	-	µs
t_{CPH}	$\overline{CE}$ pulse high time		200	-	-	ns
t_{SP}	SC pulse width		20	-	-	us
t_{SPL}	SC pulse low time		20	-	-	ns
t_{SDS}	Data setup time for SC		0	-	-	ns
t_{SDH}	Data hold time for SC	$\overline{CDE}$ = V_{IL}	30	-	-	ns
t_{SW}	SC setup for $\overline{WE}$		50	-	-	ns
t_{SCS}	SC setup for $\overline{CE}$		0	-	-	ns
t_{SCHW}	SC hold time for $\overline{WE}$		20	-	-	ns
t_{CE}	$\overline{CE}$ to output delay		-	-	120	ns
t_{OE}	$\overline{OE}$ to output delay		-	-	60	ns
t_{DF} 1)	$\overline{OE}$ high to output float		-	-	40	ns
t_{RP}	$\overline{RES}$ to $\overline{CE}$ setup time		1	-	-	ms

Notes : 1. tDF is a time after which the DQ pins become open.

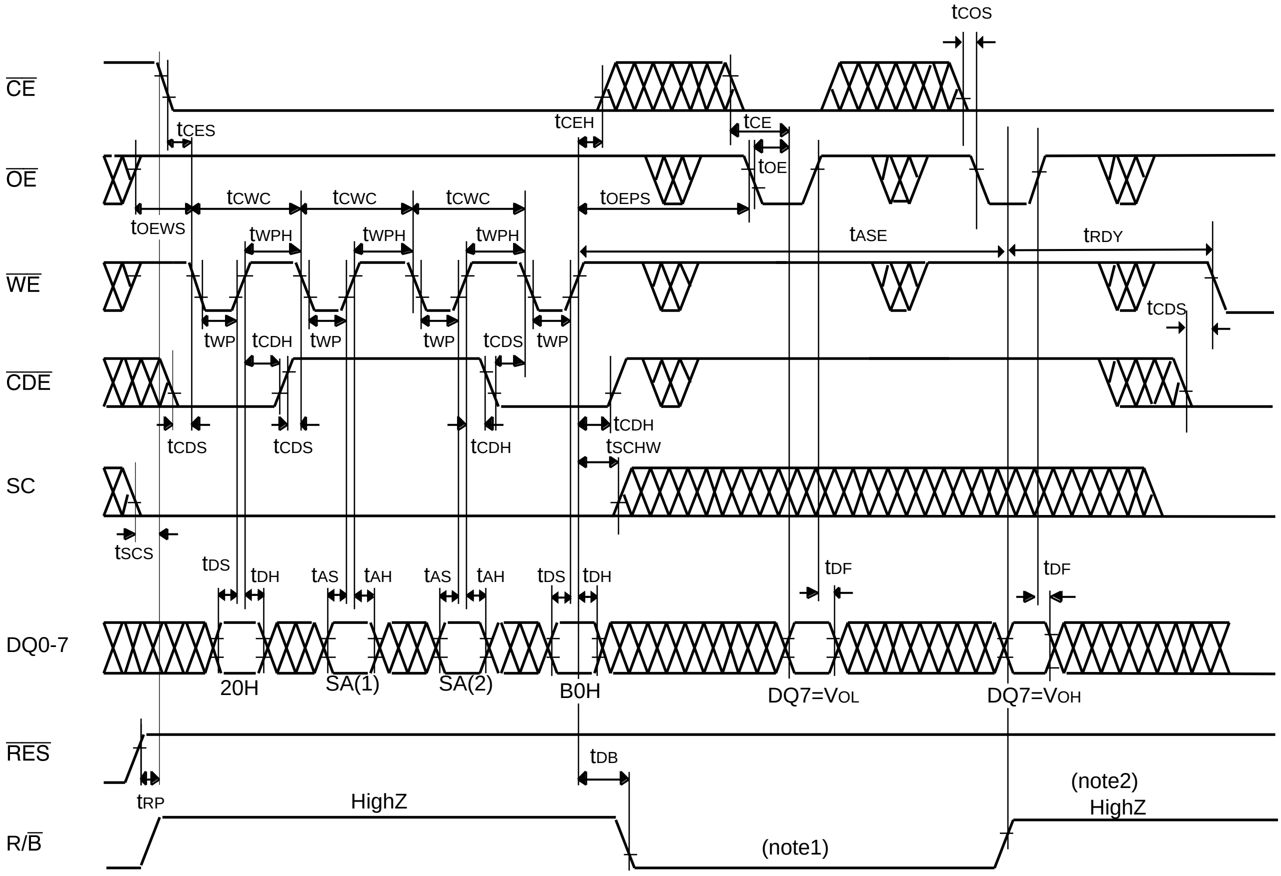
AC Characteristics (for Erase,program,ID read,status register read , data recovery read and data recovery write.)
(Vcc =3.0V to 3.6V, Ta = 0 to +70°C)

Test Conditions

- Input pulse levels : 0.4V/2.4V
- Input pulse levels for RES : 0.2V/Vcc - 0.2V
- Input rise and fall times : ≤ 5ns
- Output load : 1 TTL gate + 100pF
  (Including scope and jig.)
- Reference levels for measuring timing : 0.8V, 1.8V

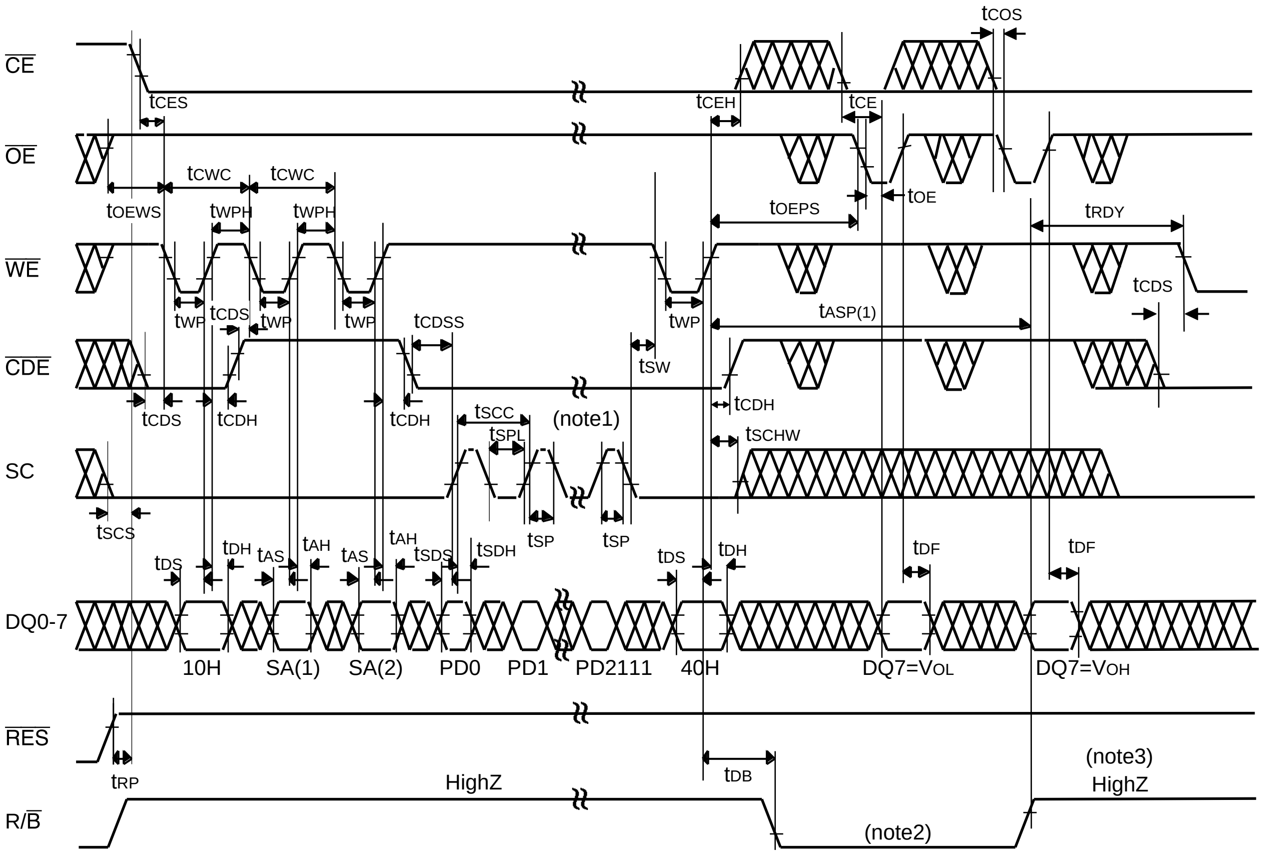
Symbol	parameter	Test condition	Limits			Unit
			Min	Typ	Max	
t_{CDS}	$\overline{\text{CDE}}$ setup time for $\overline{\text{WE}}$		0	-	-	ns
t_{CDH}	$\overline{\text{CDE}}$ hold time for $\overline{\text{WE}}$		20	-	-	ns
t_{CDSS}	$\overline{\text{CDE}}$ setup time for SC		1.5	-	-	µs
t_{CDSH}	$\overline{\text{CDE}}$ hold time for SC		30	-	-	ns
t_{RDY}	Next cycle ready time		0	-	-	ns
t_{CDOH}	$\overline{\text{CDE}}$ to $\overline{\text{OE}}$ hold time		50	-	-	ns
t_{CDAC}	$\overline{\text{CDE}}$ to output delay		-	-	50	ns
t_{CDF}	$\overline{\text{CDE}}$ to output invalid		0	-	100	ns
t_{COS}	$\overline{\text{CE}}$ setup time for $\overline{\text{OE}}$		0	-	-	ns
t_{COH}	$\overline{\text{CE}}$ hold time for $\overline{\text{OE}}$		0	-	-	ns
t_{CDOS}	$\overline{\text{CDE}}$ to $\overline{\text{OE}}$ setup time		20	-	-	ns
t_{OES}	$\overline{\text{OE}}$ setup time for SC		0	-	-	ns
t_{OEL}	$\overline{\text{OE}}$ low to output low-z		0	-	40	ns
t_{SAC}	SC to output delay		-	-	50	ns
t_{SH}	SC to output hold		15	-	-	ns
t_{RS}	R/$\overline{\text{B}}$ setup for SC		200	-	-	ns
t_{CWH}	$\overline{\text{CE}}$ hold time for $\overline{\text{WE}}$		1	-	-	µs
t_{CWHR}	$\overline{\text{CE}}$ hold time for $\overline{\text{WE}}$ on Recovery Read Mode		2	-	-	µs
t_{WWH}	$\overline{\text{WE}}$ hold time for $\overline{\text{WE}}$		1	-	-	µs

Erase and Status Data Polling Timing Waveforms (Sector Erase)



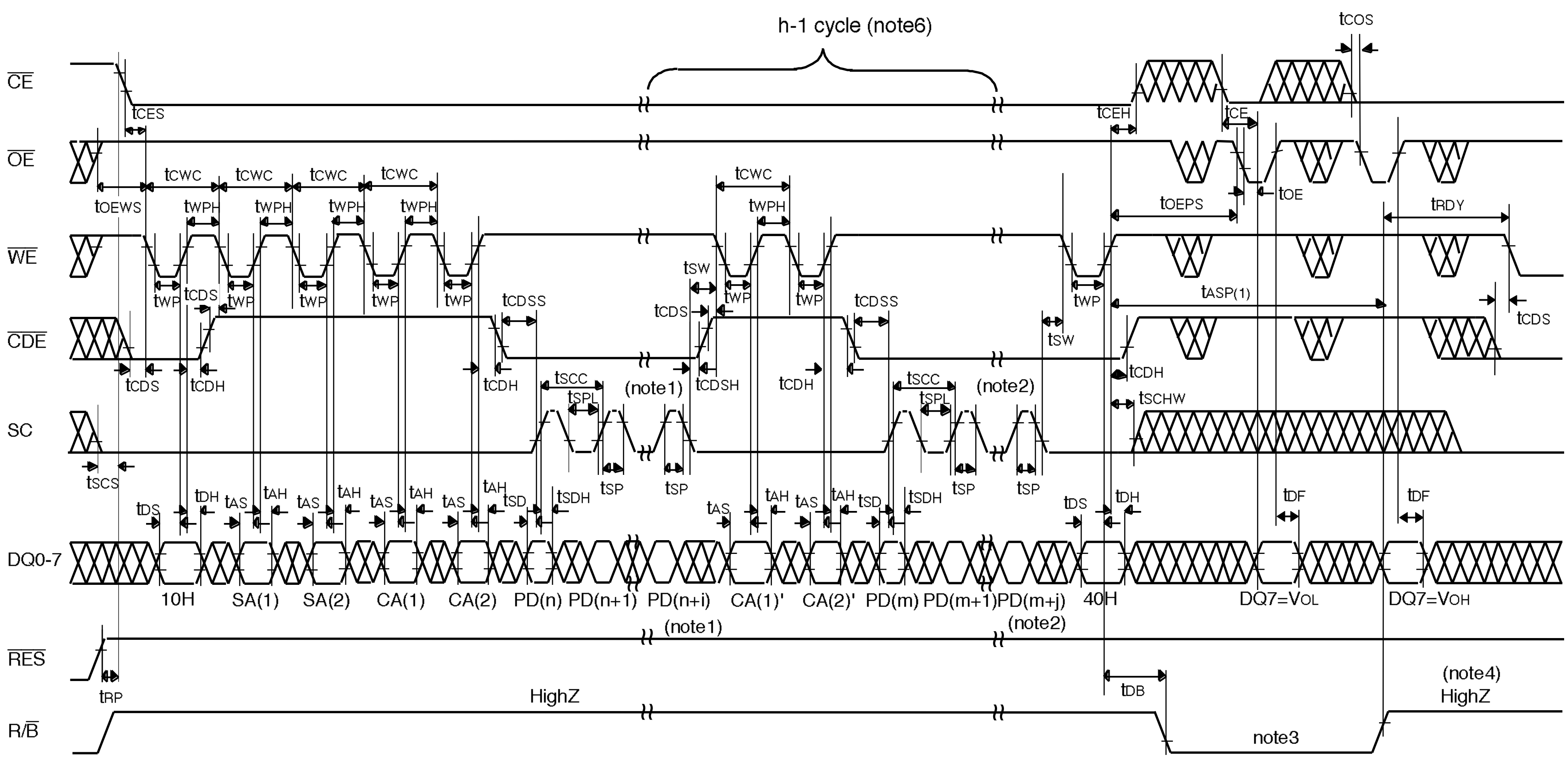
Note : 1. Any commands, including reset command FFH, cannot be input while R/B outputs a VOL.
2. The status returns to the Standby or the Output disable after R/B returns to HighZ.

Program(1) and Status Data Polling Timing Waveforms



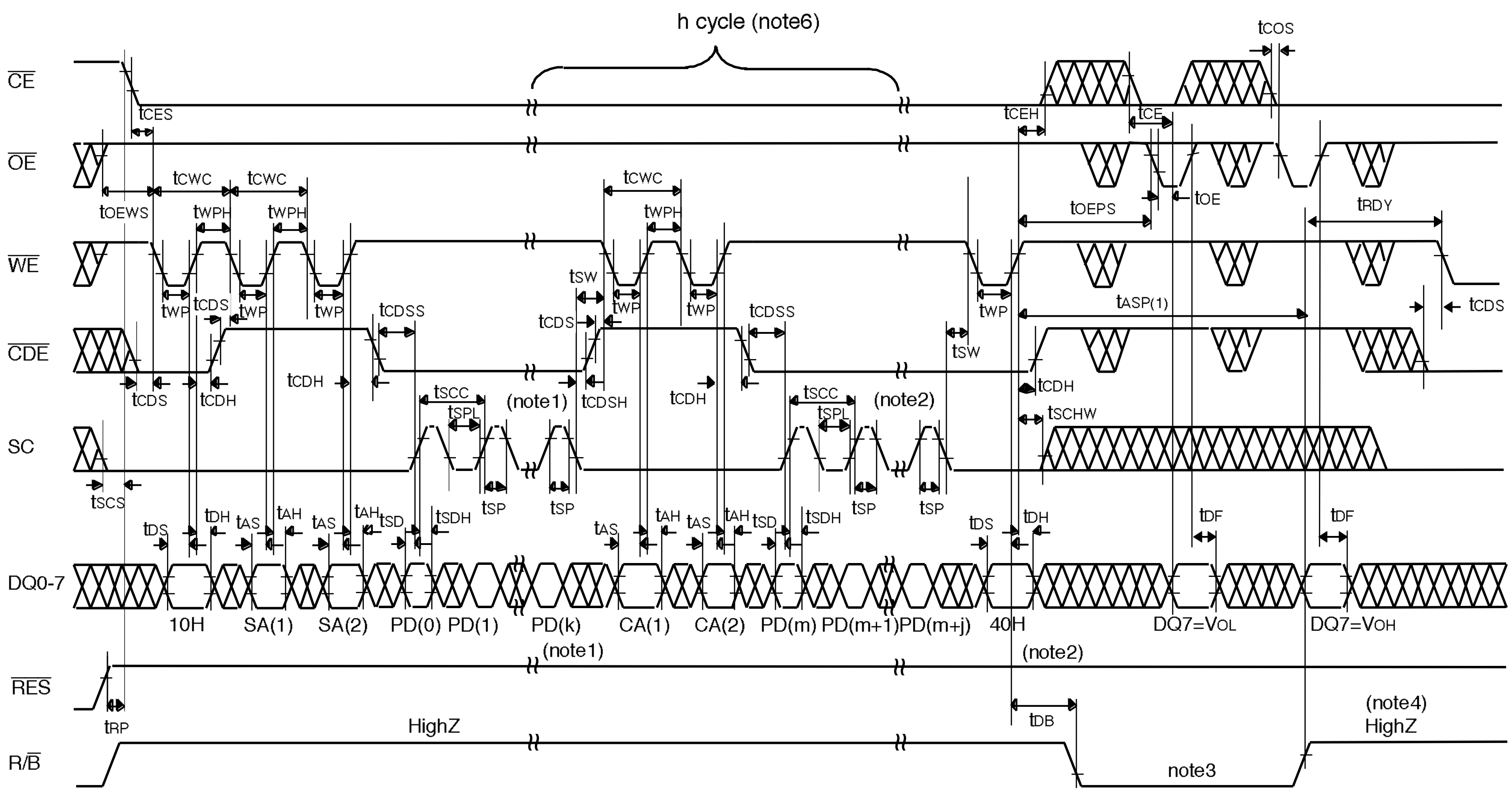
Notes : 1. The programming operation is not guaranteed when the number of the SC pulse exceeds 2112.
2. Any commands, including reset command FFH, cannot be input while R/$\overline{B}$ is V_{OL}.
3. The status returns to the Standby or the Output disable after R/$\overline{B}$ returns to HighZ.
4. By using program(1), data can be programmed additionally for each sector before erase.

Program(1) with CA before SC and Status Data Polling Timing Waveforms



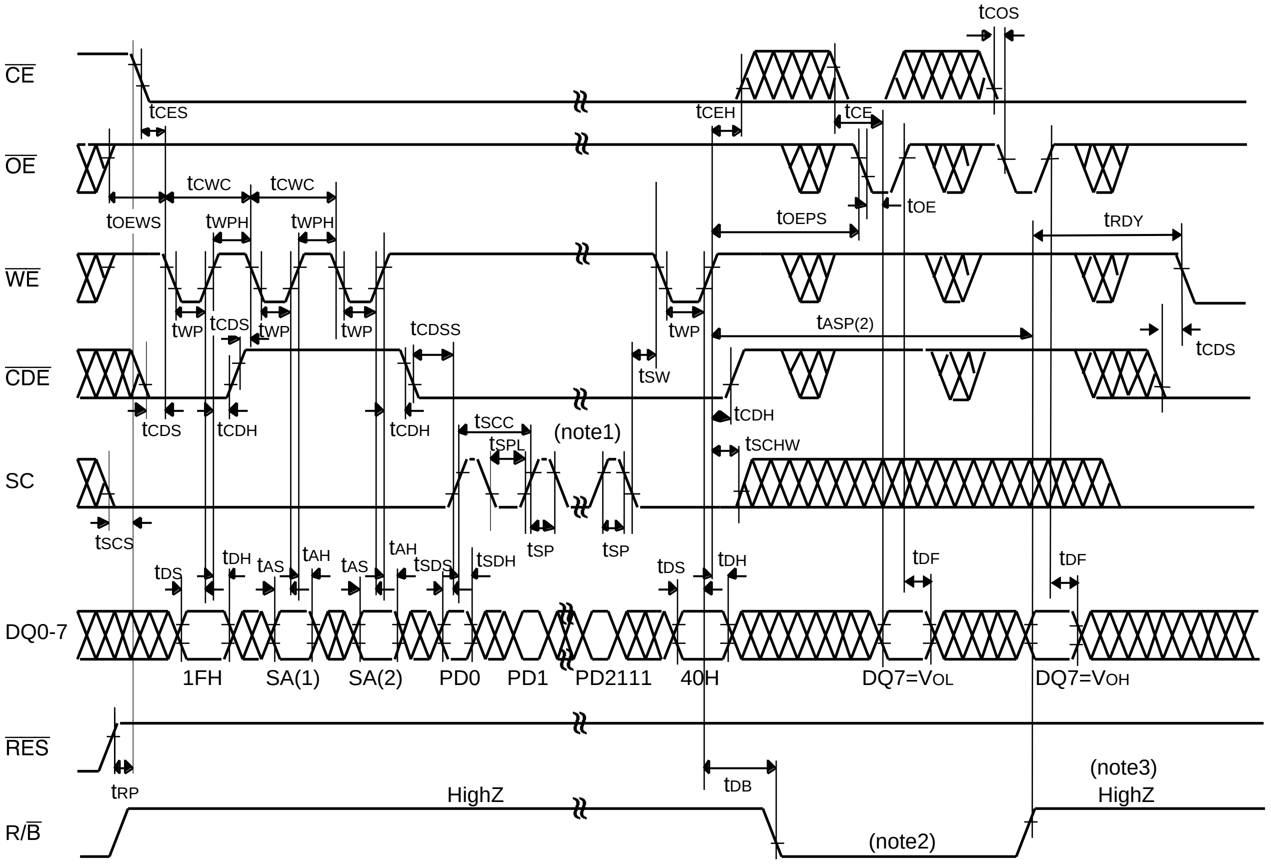
Notes : 1. The programming operation is not guaranteed when the number of the SC pulse exceeds (2112-n).($i \leq 2111-n$, $0 \leq n \leq 2111$)
2. The programming operation is not guaranteed when the number of the SC pulse exceeds (2112-m).($j \leq 2111-m$, $0 \leq m \leq 2111$)
3. Any commands, including reset command FFH, cannot be input while R/$\overline{B}$ is V_{OL}.
4. The status returns to the Standby or the Output disable after R/$\overline{B}$ returns to HighZ.
5. By using program(1), data can be programmed additionally for each sector before erase.
6.This interval can be repeated (h-1)cycle.($1 \leq h \leq 2048+64$)

Program(1) with CA after SC and Status Data Polling Timing Waveforms



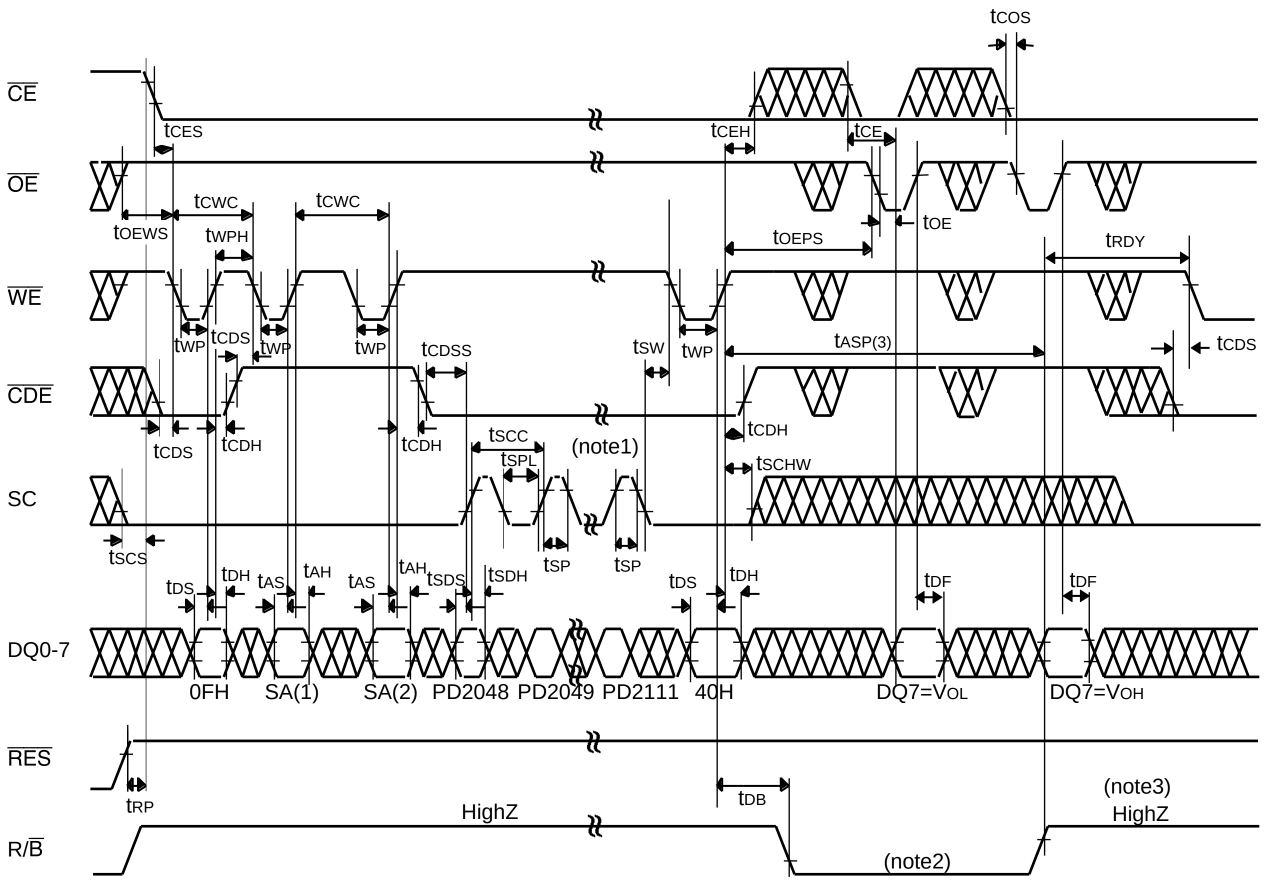
Notes : 1. The programming operation is not guaranteed when the number of the SC pulse exceeds 2112.(0 ≤ k ≤ 2111)
2. The programming operation is not guaranteed when the number of the SC pulse exceeds (2112-m).(j ≤ 2111-m , 0 ≤ m ≤ 2111)
3. Any commands, including reset command FFH, cannot be input while R/B̄ is VOL.
4. The status returns to the Standby or the Output disable after R/B̄ returns to HighZ.
5. By using program(1), data can be programmed additionally each sector before erase.
6.This interval can be repeated h cycle.(1 ≤ h ≤ 2048+64)

Program(2) and Status Data Polling Timing Waveforms



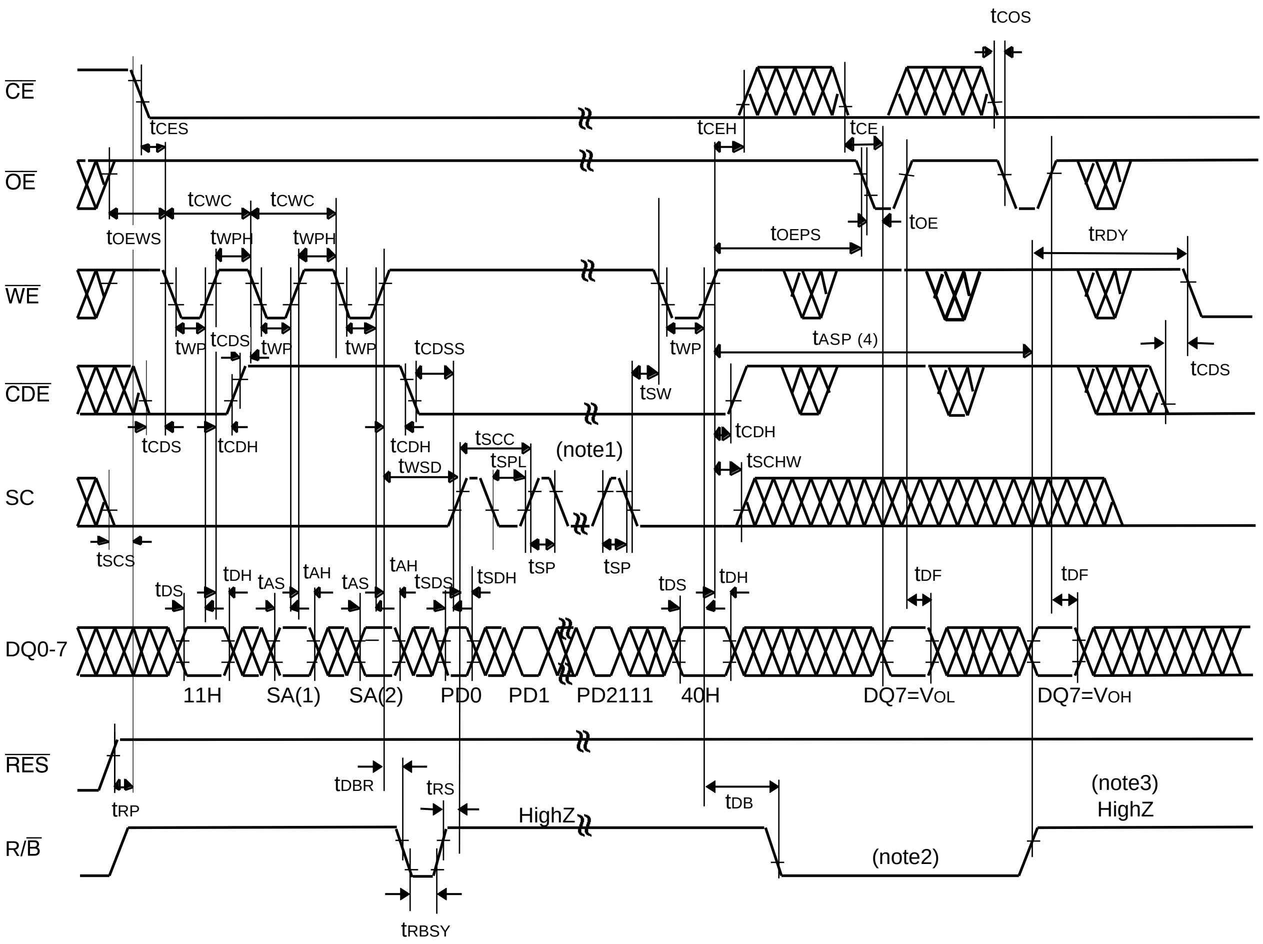
Notes : 1. The programming operation is not guaranteed when the number of the SC pulse exceeds 2112.
2. Any commands, including reset command FFH, cannot be input while R/B is VOL.
3. The status returns to the Standby or the Output disable after R/B returns to HighZ.
4. By using program(2), the programmed data of each sector must be erased before programming next data.

Program(3) and Status Data Polling Timing Waveforms



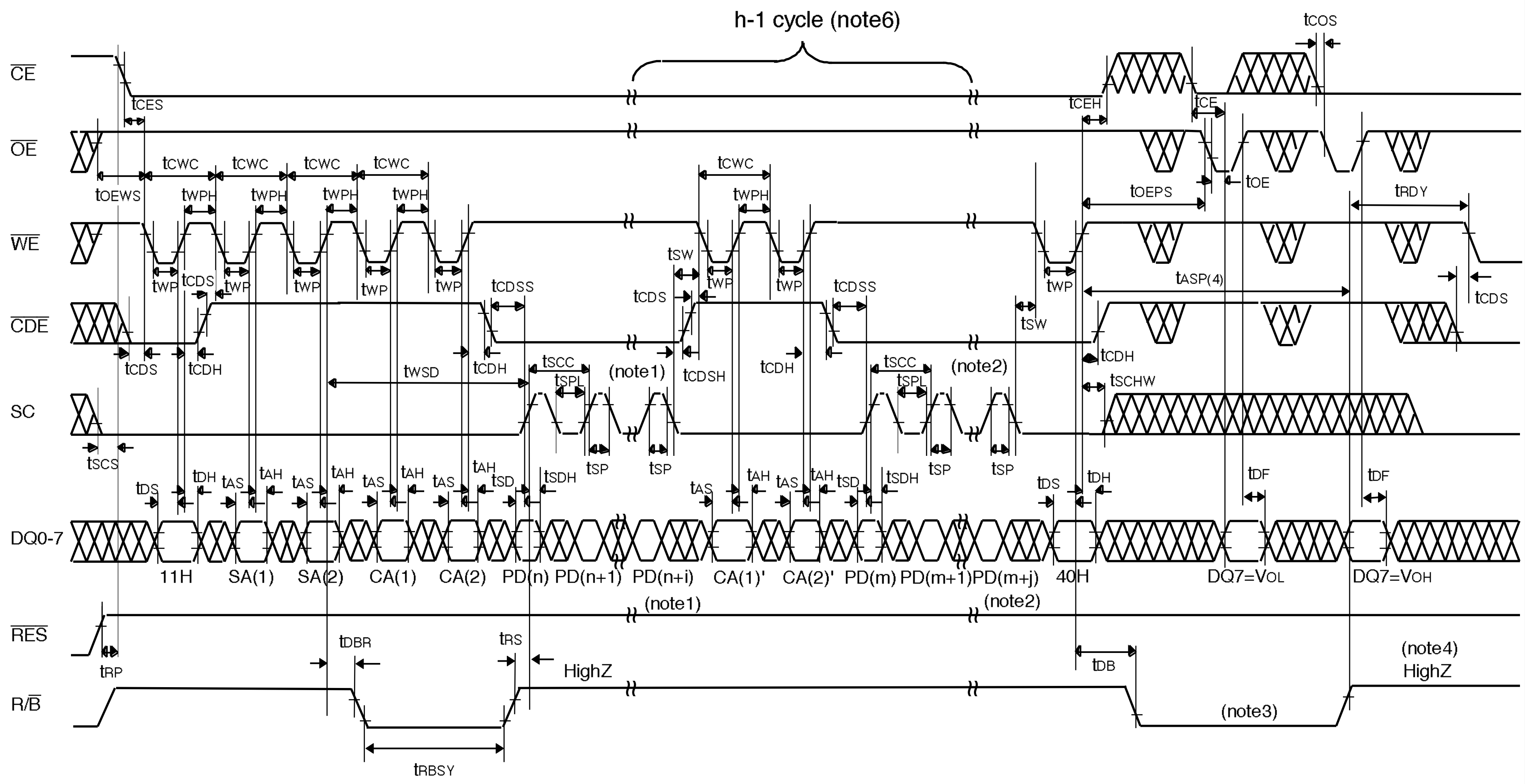
Notes : 1. The programming operation is not guaranteed when the number of the SC pulse exceeds 64.
2. Any commands, including reset command FFH, cannot be input while R/$\overline{\text{B}}$ is V_{OL}.
3. The status returns to the Standby or the Output disable after R/$\overline{\text{B}}$ returns to HighZ.
4. By using program(3), data can be programmed additionally for each sector before erase.

Program(4) and Status Data Polling Timing Waveforms



Notes : 1. The programming operation is not guaranteed when the number of the SC pulse exceeds 2112.
2. Any commands, including reset command FFH, cannot be input while R/B is VOL.
3. The status returns to the Standby or the Output disable after R/B returns to HighZ.
4. By using program(4), data can be rewritten for each sector.

Program(4) with CA before SC and Status Data Polling Timing Waveforms



Notes : 1. The programming operation is not guaranteed when the number of the SC pulse exceeds (2112-n).($i \le 2111-n$, $0 \le n \le 2111$)

2. The programming operation is not guaranteed when the number of the SC pulse exceeds (2112-m).($j \le 2111-m$, $0 \le n \le 2111$)

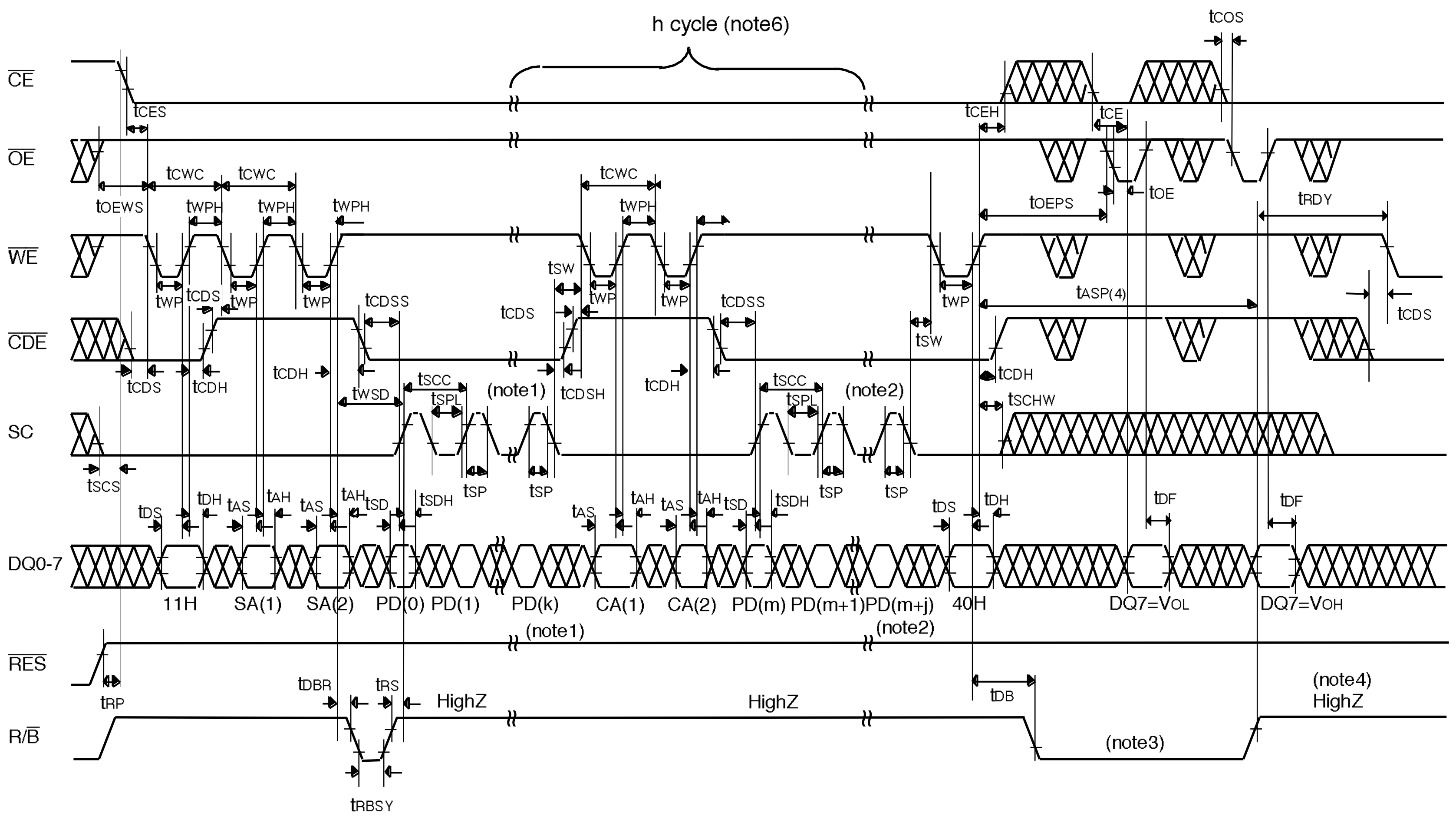
3. Any commands, including reset command FFH, cannot be input while R/$\overline{B}$ is V_{OL}.

4. The status returns to the Standby or the Output disable after R/$\overline{B}$ returns to HighZ.

5. By using program(4), data can be rewritten for each sector.

6.This interval can be repeated (h-1)cycle.($1 \le h \le 2048+64$)

Program(4) with CA after SC and Status Data Polling Timing Waveforms



Notes : 1. The programming operation is not guaranteed when the number of the SC pulse exceeds 2112.($0 \le k \le 2111$)

2. The programming operation is not guaranteed when the number of the SC pulse exceeds (2112-m).($j \le 2111-m$, $0 \le m \le 2111$)

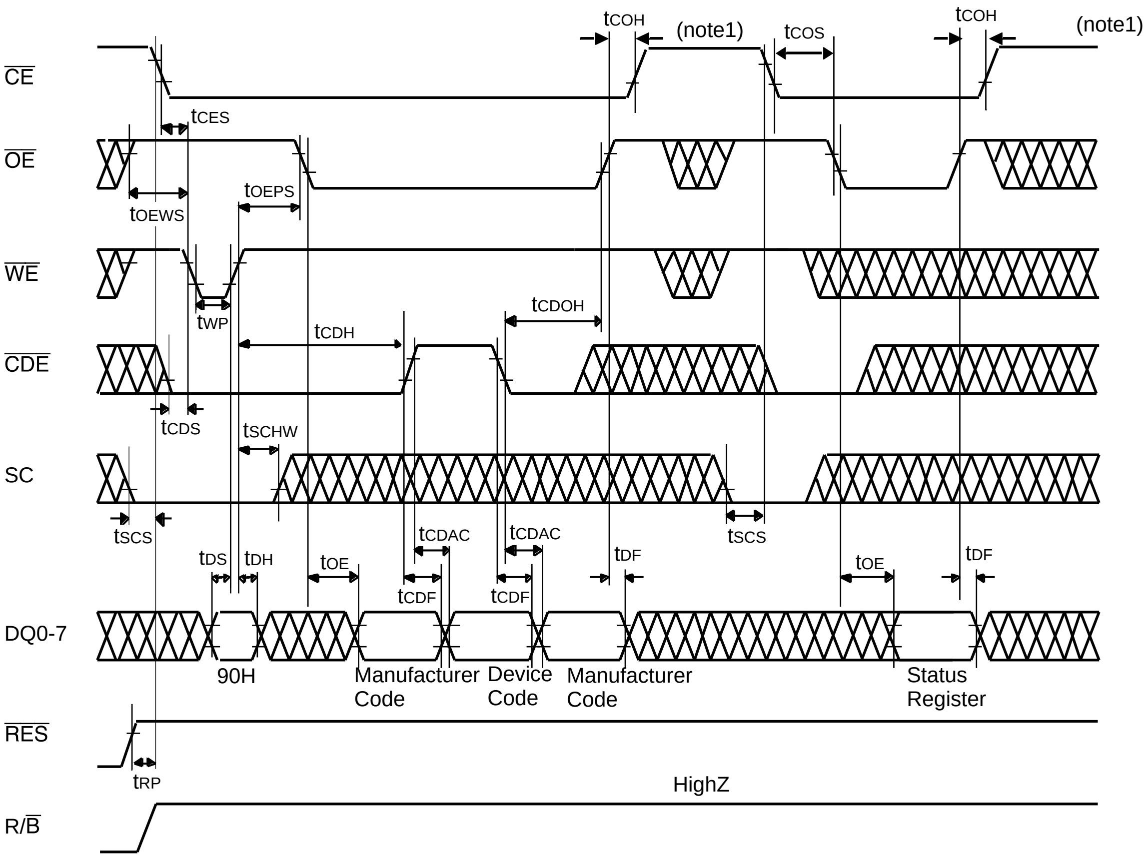
3. Any commands, including reset command FFH, cannot be input while R/$\overline{B}$ is V_{OL}

4. The status returns to the Standby or the Output disable after R/$\overline{B}$ returns to HighZ.

5. By using program(4), data can be rewritten each sector.

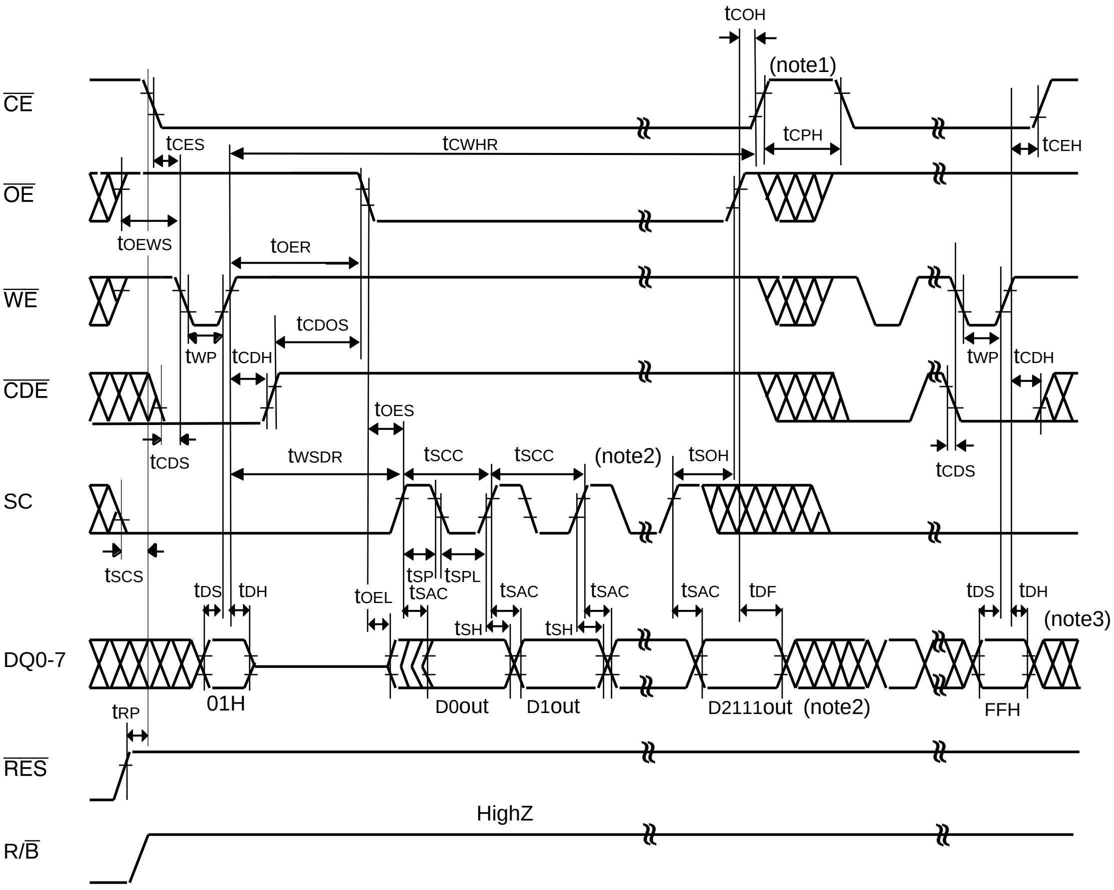
6.This interval can be repeated h cycle.($1 \le h \le 2048+64$)

ID and Status Register Read Timing Waveforms



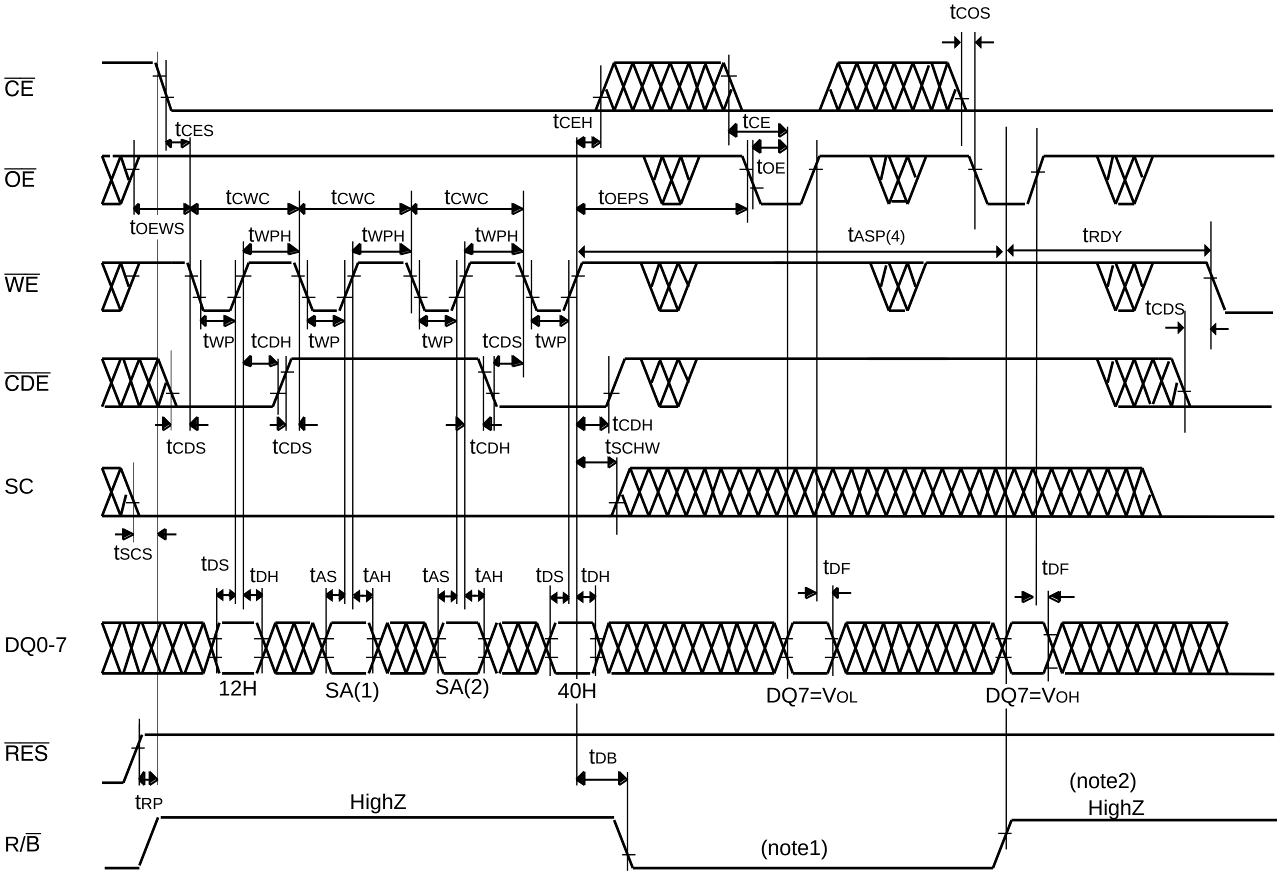
Note : 1. The status returns to the Standby at the rising edge of $\overline{\text{CE}}$.

Data Recovery Read Timing Waveforms



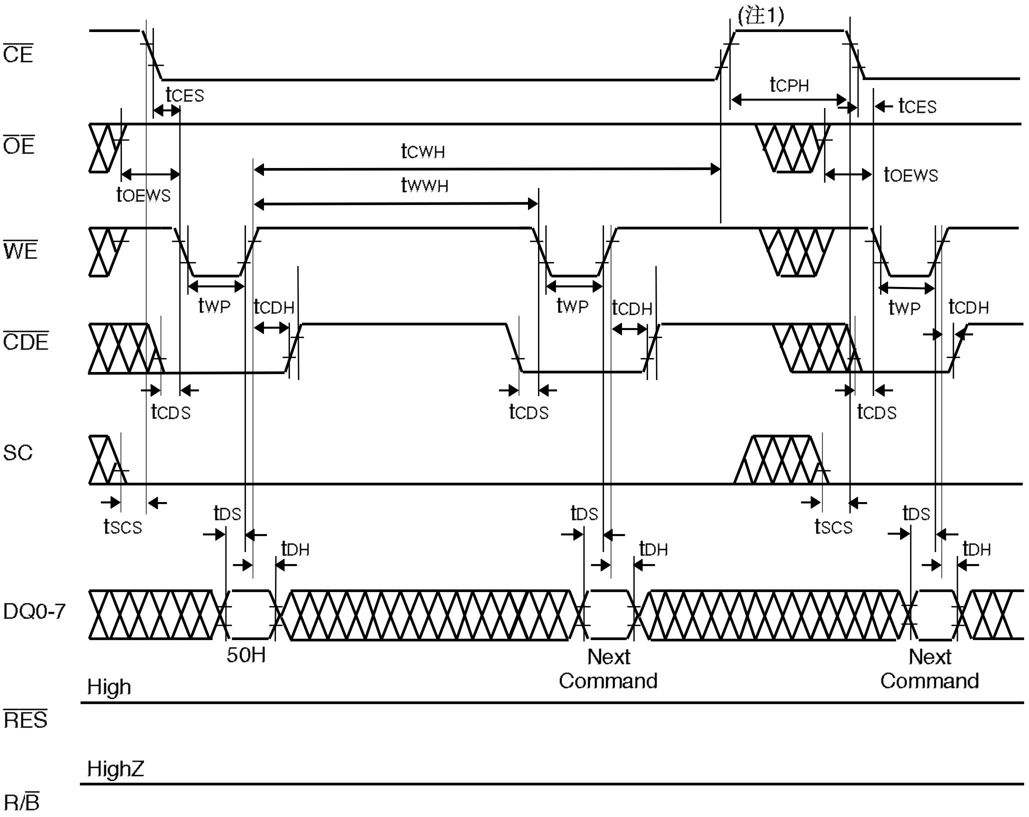
Note 1. The status returns to the Standby at the rising edge of $\overline{CE}$.
2. Output data is not valid after the number of the SC pulse exceeds 2112 and 64 in the Data Recovery Read mode.
3. The status can return to the Ready after the command FFH is input.

Data Recovery Write and Status Data Polling Timing Waveforms



Note : 1. Any commands, including reset command FFH, cannot be input while R/$\overline{B}$ outputs a VOL.
2. The status returns to the Standby or the Output disable after R/$\overline{B}$ returns to HighZ.

Clear Status Register Timing Waveforms



Note 1. The status returns to the Standby at the rising edge of $\overline{\text{CE}}$.

Status Register

The M5M29F25611 outputs the operation status data as follows: DQ7 pin outputs a V_{OL} to indicate that the memory is in either erase or program operation. The level of DQ7 pin turns to a V_{OH} when the operation finishes. DQ5 and DQ4 pins output V_{OL}s to indicate that the erase and program operations are successfully completed or not, respectively. If these pins output V_{OH}s, it indicates that these operations have timed out. When these pins are monitored, DQ7 pin must turn to a V_{OH}. To execute other erase and program operation, the status data must be cleared after a time out occurs. From DQ0 to DQ3 and DQ6 pins are reserved for future use. The pins output V_{OL}s and should be masked out during the status data read mode.

The function of the status register is summarized in the following table.

Table 1.

	Flag Definition	Definition
DQ7	Ready/Busy	"V_{OH}" = Ready "V_{OL}" = Busy
DQ6	Reserved	Outputs a V_{OL} and should be masked out during the status data polling mode.
DQ5	Erase Check	"V_{OH}" = Fail "V_{OL}" = Pass
DQ4	Program Check	"V_{OH}" = Fail "V_{OL}" = Pass
DQ3	Reserved	Outputs a V_{OL} and should be masked out during the status data polling mode.
DQ2	Reserved	
DQ1	Reserved	
DQ0	Reserved	

Notes

Unusable Sector

Initially, the M5M29F25611 contains unusable sectors.Due to the nature of the device architecture, the device can also be screened and tested for partial invalid sectors for selected systems that can utilize the devices.

1. Tested for partial invalid sectors. The usable sectors were programmed the following data.

Column address	820H	821H	822H	823H	824H	825H
Data	1CH	71H	C7H	1CH	71H	C7H

2. No erase and program for the partial invalid sectors by the system.

Item	Min
Usable sectors (initially)	16,057 (98%)

Enable High System Reliability

The device may fail during a program or erase operation due to program or erase cycle. The following architecture will enable high system reliability if a failure occurs.

1. Error in read : Error correction that more than 3 bit error correction per each sector read is required for data reliability.

2. Error in program or erase operation : The device may fail during a program or erase operation due to program or erase cycle. The status register indicates that the program and erase operations are successfully completed or not. After every program and erase operations, read status register to confirm the program and erase operations are successfully completed.
When the error happens in sector, try to reprogram the data into another sector. Then, prevent further system access to sector that error happens. Typically, recommended number of a spare sectors are 1.8% within initial usable 16,057 sectors by each device.If the number of failed sectors exceed the number of the spare sectors,usable data area in the device decreases.In the case of reprogramming to the spare sector ,do not use the data from the failed sector.The reprogram data must be the data reloaded from outer buffer,or use the Data recovery read mode or the Data recovery write mode(see the "Mode Description").To avoid consecutive sector failurechoose addresses of spare sectors as far as possible from the failed sectors.

3. The write/erase endurance is 1 x 10^5 cycles.

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- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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