

MSM518122

131,072-Word × 8-Bit Multiport DRAM

DESCRIPTION

The MSM518122 is an 1-Mbit CMOS multiport DRAM composed of a 131,072-word by 8-bit dynamic RAM and a 256-word by 8-bit SAM. Its RAM and SAM operate independently and asynchronously.

The MSM518122 supports three types of operation : random access to RAM port, high speed serial access to SAM port and bidirectional transfer of data between any selected row in the RAM port and the SAM port. In addition to the conventional multiport DRAM operating modes, the MSM518122 features the block write and flash write functions on the RAM port and a split data transfer capability on the SAM port. The SAM port requires no refresh operation because it uses static CMOS flip-flops.

FEATURES

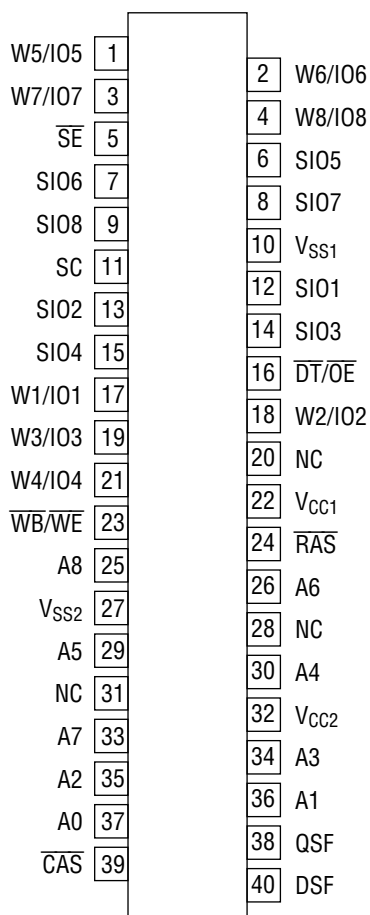
- Single power supply: 5 V $\pm$ 10%
 - Full TTL compatibility
 - Multiport organization
 - RAM: 128K word $\times$ 8 bits
 - SAM: 256 word $\times$ 8 bits
 - Fast page mode
 - Write per bit
 - Masked flash write
 - Masked block write
 - $\overline{\text{RAS}}$ only refresh
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
 - Hidden refresh
 - Serial read/write
 - 256 tap location
 - Bidirectional data transfer
 - Split transfer
 - Masked write transfer
 - Refresh: 512 cycles/8 ms
 - Package options:

40-pin 475 mil plastic ZIP	(ZIP40-P-475-1.27)	(Product : MSM518122-xxZS)
40-pin 400 mil plastic SOJ	(SOJ40-P-400-1.27)	(Product : MSM518122-xxJS)
- xx indicates speed rank.

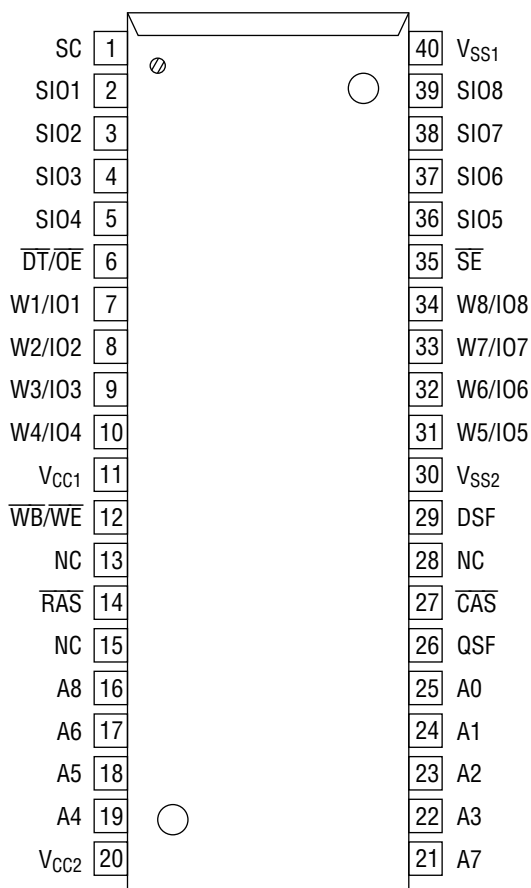
PRODUCT FAMILY

Family	Access Time		Cycle Time		Power Dissipation	
	RAM	SAM	RAM	SAM	Operating	Standby
MSM518122-70	70 ns	25 ns	140 ns	30 ns	120 mA	8 mA
MSM518122-80	80 ns	25 ns	150 ns	30 ns	110 mA	8 mA
MSM518122-10	100 ns	25 ns	180 ns	30 ns	100 mA	8 mA

PIN CONFIGURATION (TOP VIEW)



40-Pin Plastic ZIP

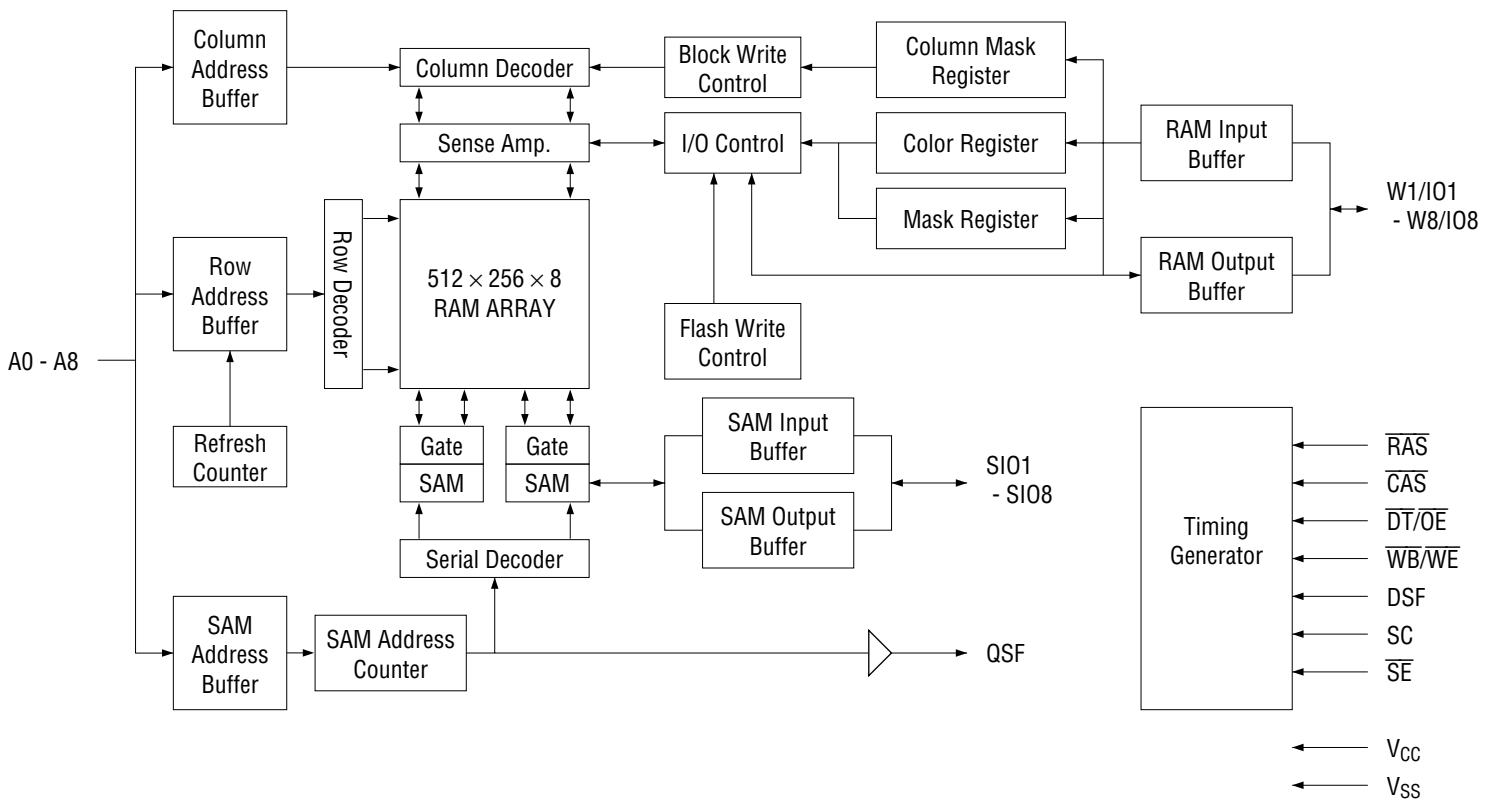


40-Pin Plastic SOJ

Pin Name	Function	Pin Name	Function
A0 - A8	Address Input	SC	Serial Clock
W1/I01 - W8/I08	RAM Inputs/Outputs	$\overline{SE}$	SAM Port Enable
SI01 - SI08	SAM Inputs/Outputs	DSF	Special Function Input
$\overline{RAS}$	Row Address Strobe	QSF	Special Function Output
$\overline{CAS}$	Column Address Strobe	V _{CC}	Power Supply (5 V)
$\overline{WB/WE}$	Write per Bit/Write Enable	V _{SS}	Ground (0 V)
$\overline{DT/OE}$	Transfer/Output Enable	NC	No Connection

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(Note: 16)

Parameter	Symbol	Condition	Rating	Unit
Input Output Voltage	V_T	$T_a = 25^\circ\text{C}$	-1.0 to 7.0	V
Output Current	I_{OS}	$T_a = 25^\circ\text{C}$	50	mA
Power Dissipation	P_D	$T_a = 25^\circ\text{C}$	1	W
Operating Temperature	T_{opr}	—	0 to 70	$^\circ\text{C}$
Storage Temperature	T_{stg}	—	-55 to 150	$^\circ\text{C}$

Recommended Operating Condition

 $(T_a = 0^\circ\text{C to } 70^\circ\text{C})$ (Note: 17)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

Capacitance

 $(V_{CC} = 5\text{ V} \pm 10\%, f = 1\text{ MHz}, T_a = 25^\circ\text{C})$

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance	C_I	—	7	pF
Input/Output Capacitance	$C_{I/O}$	—	9	pF
Output Capacitance	$C_{O(QSF)}$	—	9	pF

Note: This parameter is periodically sampled and is not 100% tested.

DC Characteristics 1

Parameter	Symbol	Condition	Min.	Max.	Unit
Output "H" Level Voltage	V_{OH}	$I_{OH} = -2\text{ mA}$	2.4	—	V
Output "L" Level Voltage	V_{OL}	$I_{OL} = 2\text{ mA}$	—	0.4	
Input Leakage Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$ All other pins not under test = 0 V	-10	10	μA
Output Leakage Current	I_{LO}	$0 \leq V_{OUT} \leq 5.5\text{ V}$ Output Disable	-10	10	

DC Characteristics 2

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C)

Item (RAM)	SAM	Symbol	-70	-80	-10	Unit	Note
			Max.	Max.	Max.		
Operating Current ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ Cycling, $t_{\text{RC}} = t_{\text{RC min.}}$)	Standby	I _{CC1}	85	75	65	mA	1, 2
	Active	I _{CC1A}	120	110	100		1, 2
Standby Current ($\overline{\text{RAS}}$, $\overline{\text{CAS}} = V_{\text{IH}}$)	Standby	I _{CC2}	8	8	8		3
	Active	I _{CC2A}	50	45	40		1, 2
$\overline{\text{RAS}}$ Only Refresh Current ($\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} = V_{\text{IH}}$, $t_{\text{RC}} = t_{\text{RC min.}}$)	Standby	I _{CC3}	85	75	65		1, 2
	Active	I _{CC3A}	120	110	100		1, 2
Page Mode Current ($\overline{\text{RAS}} = V_{\text{IL}}$, $\overline{\text{CAS}}$ Cycling, $t_{\text{PC}} = t_{\text{PC min.}}$)	Standby	I _{CC4}	70	65	60		1, 2
	Active	I _{CC4A}	120	110	100		1, 2
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Current ($\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, $t_{\text{RC}} = t_{\text{RC min.}}$)	Standby	I _{CC5}	85	75	65		1, 2
	Active	I _{CC5A}	120	110	100		1, 2
Data Transfer Current ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ Cycling, $t_{\text{RC}} = t_{\text{RC min.}}$)	Standby	I _{CC6}	85	75	65		1, 2
	Active	I _{CC6A}	120	110	100		1, 2
Flash Write Current ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ Cycling, $t_{\text{RC}} = t_{\text{RC min.}}$)	Standby	I _{CC7}	85	75	65		1, 2
	Active	I _{CC7A}	120	110	100		1, 2
Block Write Current ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ Cycling, $t_{\text{RC}} = t_{\text{RC min.}}$)	Standby	I _{CC8}	85	75	65		1, 2
	Active	I _{CC8A}	120	110	100		1, 2

AC Characteristics (1/3)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 4, 5, 6

Parameter	Symbol	-70		-80		-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	140	—	150	—	180	—	ns	
Read Modify Write Cycle Time	t _{RWC}	195	—	195	—	235	—	ns	
Fast Page Mode Cycle Time	t _{PC}	45	—	50	—	55	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{PRWC}	90	—	90	—	100	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	70	—	80	—	100	ns	7, 13
Access Time from Column Address	t _{AA}	—	35	—	40	—	55	ns	7, 13
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	20	—	25	—	25	ns	7, 14
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	40	—	45	—	50	ns	7, 14
Output Buffer Turn-off Delay	t _{OFF}	0	20	0	20	0	20	ns	9
Transition Time (Rise and Fall)	t _T	3	35	3	35	3	35	ns	6
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	60	—	60	—	70	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	70	10k	80	10k	100	10k	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode Only)	t _{RASP}	70	100k	80	100k	100	100k	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	20	—	25	—	25	—	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	70	—	80	—	100	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	20	10k	25	10k	25	10k	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	50	20	55	20	75	ns	13
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	35	15	40	20	50	ns	13
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	35	—	40	—	55	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	10	—	10	—	10	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	15	—	15	—	15	—	ns	
Column Address Hold Time referenced to $\overline{\text{RAS}}$	t _{AR}	55	—	55	—	70	—	ns	
Read Command Set-up Time	t _{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	ns	10
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t _{WCH}	15	—	15	—	15	—	ns	
Write Command Hold Time referenced to $\overline{\text{RAS}}$	t _{WCR}	55	—	55	—	70	—	ns	
Write Command Pulse Width	t _{WP}	15	—	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	20	—	20	—	25	—	ns	

AC Characteristics (2/3)

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 4, 5, 6

Parameter	Symbol	-70		-80		-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Data Set-up Time	t _{DS}	0	—	0	—	0	—	ns	11
Data Hold Time	t _{DH}	15	—	15	—	15	—	ns	11
Data Hold Time referenced to $\overline{\text{RAS}}$	t _{DHR}	55	—	55	—	70	—	ns	
Write Command Set-up Time	t _{WCS}	0	—	0	—	0	—	ns	12
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	100	—	100	—	130	—	ns	12
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	65	—	65	—	80	—	ns	12
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	45	—	45	—	55	—	ns	12
Data to $\overline{\text{CAS}}$ Delay Time	t _{DZC}	0	—	0	—	0	—	ns	
Data to $\overline{\text{OE}}$ Delay Time	t _{DZO}	0	—	0	—	0	—	ns	
Access Time from $\overline{\text{OE}}$	t _{OEa}	—	20	—	20	—	25	ns	7
Output Buffer Turn-off Delay from $\overline{\text{OE}}$	t _{OEZ}	0	10	0	10	0	20	ns	9
$\overline{\text{OE}}$ to Data Delay Time	t _{OEED}	10	—	10	—	20	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OEh}	10	—	10	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t _{ROH}	15	—	15	—	15	—	ns	
$\overline{\text{CAS}}$ Set-up Time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle	t _{CSR}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle	t _{CHR}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t _{RPC}	0	—	0	—	0	—	ns	
Refresh Period	t _{REF}	—	8	—	8	—	8	ms	
$\overline{\text{WB}}$ Set-up Time	t _{WSR}	0	—	0	—	0	—	ns	
$\overline{\text{WB}}$ Hold Time	t _{RWH}	15	—	15	—	15	—	ns	
DSF Set-up Time referenced to $\overline{\text{RAS}}$	t _{FSR}	0	—	0	—	0	—	ns	
DSF Hold Time referenced to $\overline{\text{RAS}}$ (1)	t _{RFH}	15	—	15	—	15	—	ns	
DSF Hold Time referenced to $\overline{\text{RAS}}$ (2)	t _{FHR}	55	—	55	—	70	—	ns	
DSF Set-up Time referenced to $\overline{\text{CAS}}$	t _{FSC}	0	—	0	—	0	—	ns	
DSF Hold Time referenced to $\overline{\text{CAS}}$	t _{CFH}	15	—	15	—	15	—	ns	
Write Per Bit Mask Data Set-up Time	t _{MS}	0	—	0	—	0	—	ns	
Write Per Bit Mask Data Hold Time	t _{MH}	15	—	15	—	15	—	ns	
$\overline{\text{DT}}$ High Set-up Time	t _{THS}	0	—	0	—	0	—	ns	
$\overline{\text{DT}}$ High Hold Time	t _{THH}	15	—	15	—	15	—	ns	
$\overline{\text{DT}}$ Low Set-up Time	t _{TLS}	0	—	0	—	0	—	ns	
$\overline{\text{DT}}$ Low Hold Time	t _{TLH}	15	10k	15	10k	15	10k	ns	
$\overline{\text{DT}}$ Low Hold Time referenced to $\overline{\text{RAS}}$ (Real Time Read Transfer)	t _{RTH}	60	10k	65	10k	80	10k	ns	
$\overline{\text{DT}}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	t _{ATH}	25	—	30	—	30	—	ns	
$\overline{\text{DT}}$ Low Hold Time referenced to $\overline{\text{CAS}}$ (Real Time Read Transfer)	t _{CTH}	20	—	25	—	25	—	ns	
$\overline{\text{SE}}$ Set-up Time referenced to $\overline{\text{RAS}}$	t _{ESR}	0	—	0	—	0	—	ns	
$\overline{\text{SE}}$ Hold Time referenced to $\overline{\text{RAS}}$	t _{REH}	15	—	15	—	15	—	ns	

AC Characteristics (3/3)

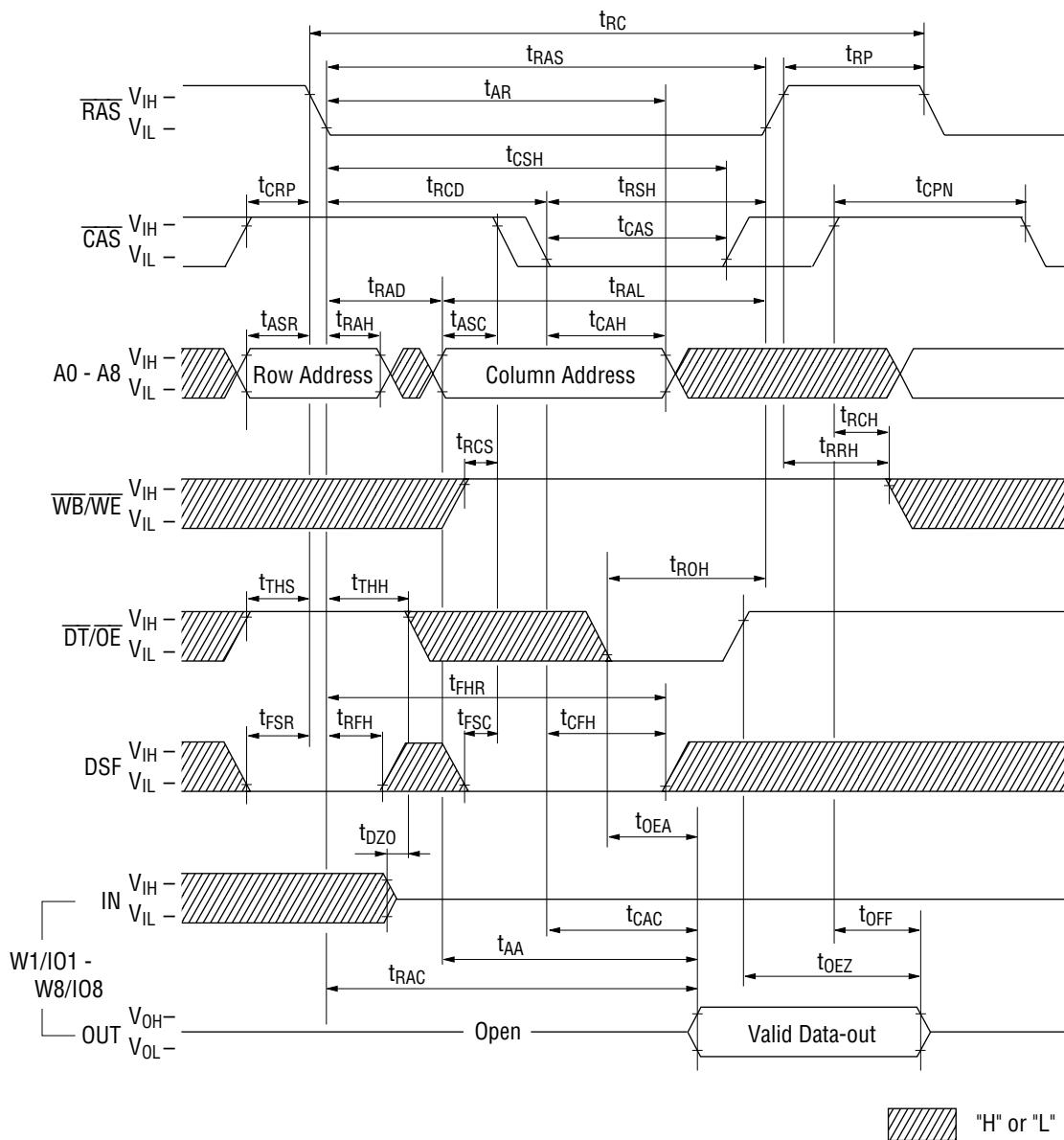
(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 4, 5, 6

Parameter	Symbol	-70		-80		-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{DT}$ to $\overline{RAS}$ Precharge Time	t _{TRP}	60	—	60	—	70	—	ns	
$\overline{DT}$ Precharge Time	t _{TP}	20	—	20	—	30	—	ns	
$\overline{RAS}$ to First SC Delay Time (Read Transfer)	t _{RSD}	70	—	80	—	100	—	ns	
Column Address to First SC Delay Time (Read Transfer)	t _{ASD}	45	—	45	—	50	—	ns	
$\overline{CAS}$ to First SC Delay Time (Read Transfer)	t _{CSD}	20	—	25	—	25	—	ns	
Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	t _{TSL}	5	—	5	—	5	—	ns	
$\overline{DT}$ to First SC Delay Time (Read Transfer)	t _{TSD}	15	—	15	—	15	—	ns	
Last SC to $\overline{RAS}$ Set-up Time (Serial Input)	t _{SRS}	25	—	25	—	30	—	ns	
$\overline{RAS}$ to First SC Delay Time (Serial Input)	t _{SRD}	20	—	20	—	25	—	ns	
$\overline{RAS}$ to Serial Input Delay Time	t _{SDD}	40	—	40	—	50	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{RAS}$ (Pseudo Write Transfer)	t _{SDZ}	10	40	10	40	10	50	ns	9
SC Cycle Time	t _{SCC}	30	—	30	—	30	—	ns	
SC Pulse Width (SC High Time)	t _{SC}	10	—	10	—	10	—	ns	
SC Precharge Time (SC Low Time)	t _{SCP}	10	—	10	—	10	—	ns	
Access Time from SC	t _{SCA}	—	25	—	25	—	25	ns	8
Serial Output Hold Time from SC	t _{SOH}	5	—	5	—	5	—	ns	
Serial Input Set-up Time	t _{SDS}	0	—	0	—	0	—	ns	
Serial Input Hold Time	t _{SDH}	15	—	15	—	15	—	ns	
Access Time from $\overline{SE}$	t _{SEA}	—	25	—	25	—	25	ns	8
$\overline{SE}$ Pulse Width	t _{SE}	25	—	25	—	25	—	ns	
$\overline{SE}$ Precharge Time	t _{SEP}	25	—	25	—	25	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{SE}$	t _{SEZ}	0	20	0	20	0	20	ns	9
Serial Input to $\overline{SE}$ Delay Time	t _{SZE}	0	—	0	—	0	—	ns	
Serial Input to First SC Delay Time	t _{SZS}	0	—	0	—	0	—	ns	
Serial Write Enable Set-up Time	t _{SWS}	5	—	5	—	5	—	ns	
Serial Write Enable Hold Time	t _{SWH}	15	—	15	—	15	—	ns	
Serial Write Disable Set-up Time	t _{SWIS}	5	—	5	—	5	—	ns	
Serial Write Disable Hold Time	t _{SWIH}	15	—	15	—	15	—	ns	
Split Transfer Set-up Time	t _{STS}	25	—	30	—	30	—	ns	
Split Transfer Hold Time	t _{STH}	25	—	30	—	30	—	ns	
SC-QSF Delay Time	t _{SQD}	—	20	—	25	—	25	ns	
$\overline{DT}$ -QSF Delay Time	t _{TQD}	—	20	—	25	—	25	ns	
$\overline{CAS}$ -QSF Delay Time	t _{CQD}	—	30	—	35	—	35	ns	
$\overline{RAS}$ -QSF Delay Time	t _{RQD}	—	70	—	75	—	85	ns	

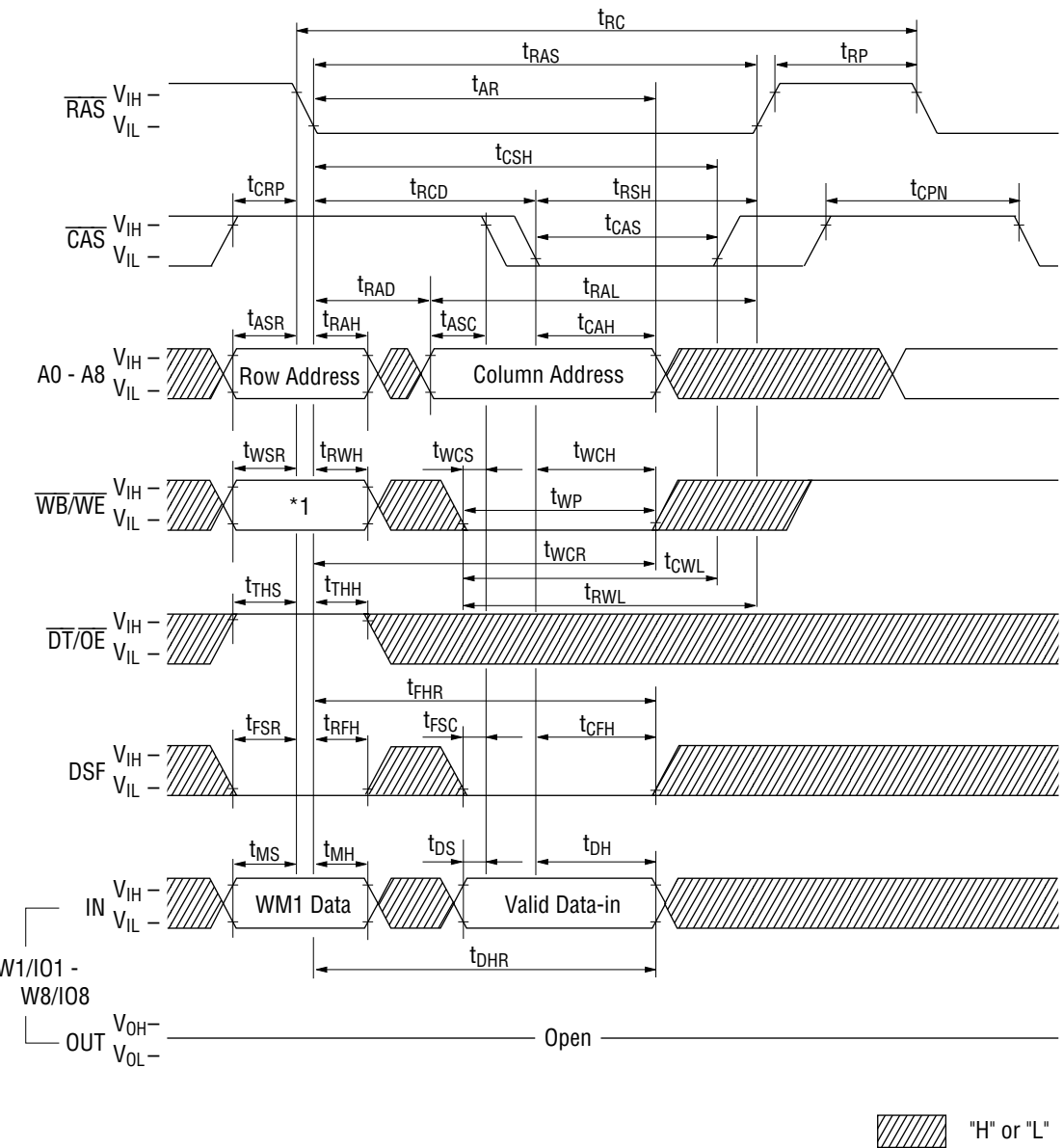
- Notes:
1. These parameters depend on output loading. Specified values are obtained with the output open.
 2. These parameters are measured at minimum cycle test.
 3. I_{CC2} (Max.) are measured under the condition of TTL input level.
 4. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 5. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{RAS}$ cycles ($\overline{DT}/\overline{OE}$ "high") and any 8 SC cycles before proper device operation is achieved. In the case of using an internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles in stead of 8 $\overline{RAS}$ cycles are required.
 6. AC measurements assume $t_T = 5$ ns.
 7. RAM port outputs are measured with a load equivalent to 1 TTL load and 100 pF. Output reference levels are $V_{OH}/V_{OL} = 2.4$ V/1.0 V.
 8. SAM port outputs are measured with a load equivalent to 1 TTL load and 30 pF. Output reference levels are $V_{OH}/V_{OL} = 2.0$ V/1.0 V.
 9. t_{OFF} (Max.), t_{OEZ} (Max.), t_{SDZ} (Max.) and t_{SEZ} (Max.) define the time at which the outputs achieve the open circuit condition and are not reference to output voltage levels.
 10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 11. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}/\overline{WE}$ leading edge in $\overline{OE}$ controlled write cycles and read modify write cycles.
 12. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only.
If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an early write cycle, and the data out pin will remain open circuit (high impedance) throughout the entire cycle : If $t_{RWD} \geq t_{RWD}$ (Min.), $t_{CWD} \geq t_{CWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.) the cycle is a read-write cycle and the data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 13. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled by t_{CAC} .
 14. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then access time is controlled by t_{AA} .
 15. Input levels at the AC parameter measurement are 3.0 V/0 V.
 16. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
 17. All voltages are referenced to V_{SS} .

TIMING WAVEFORM

Read Cycle



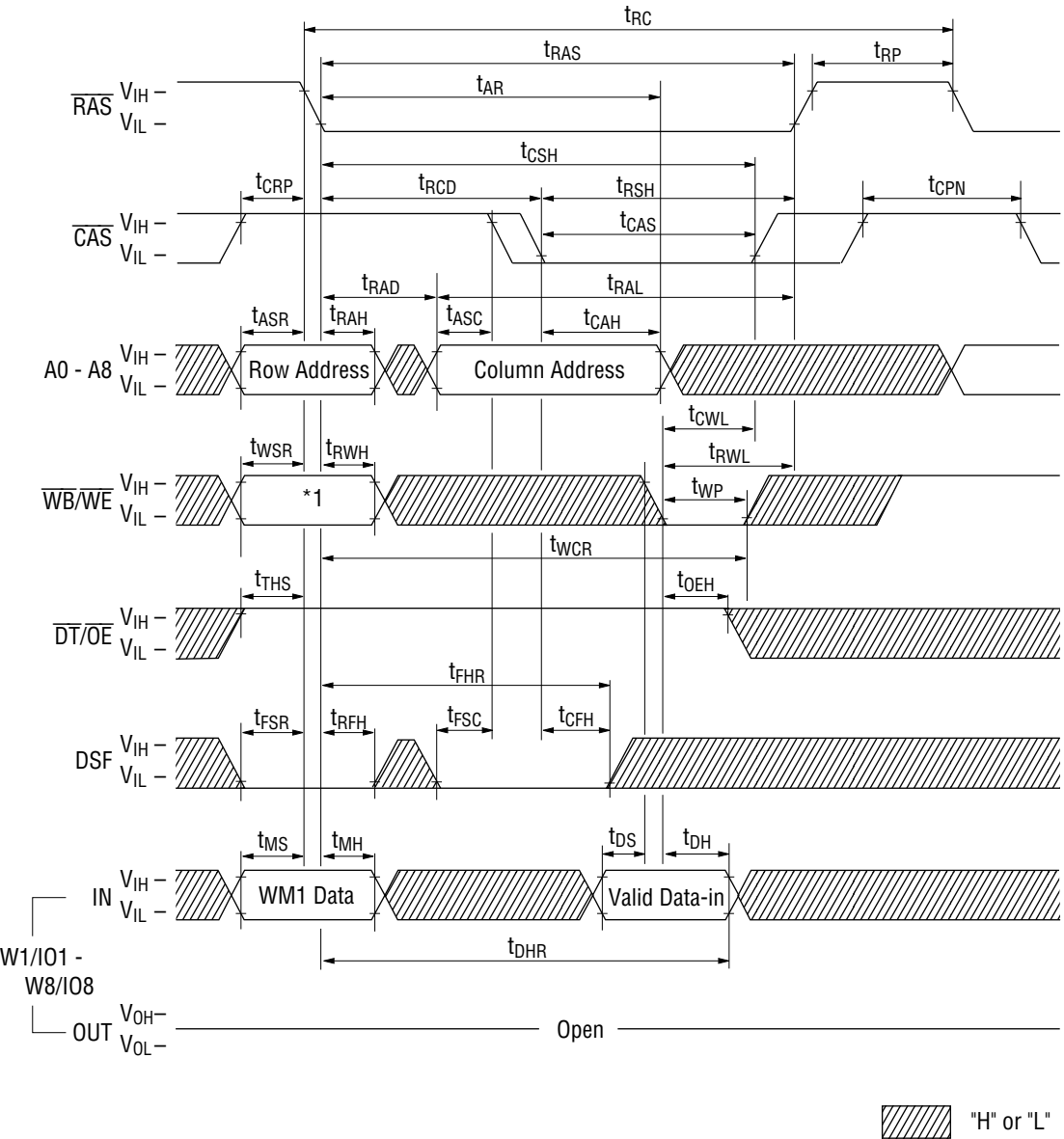
Write Cycle (Early Write)



*1 WB/WE	W1/I01 - W8/I08	Cycle
0	WM1 data	Write per Bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

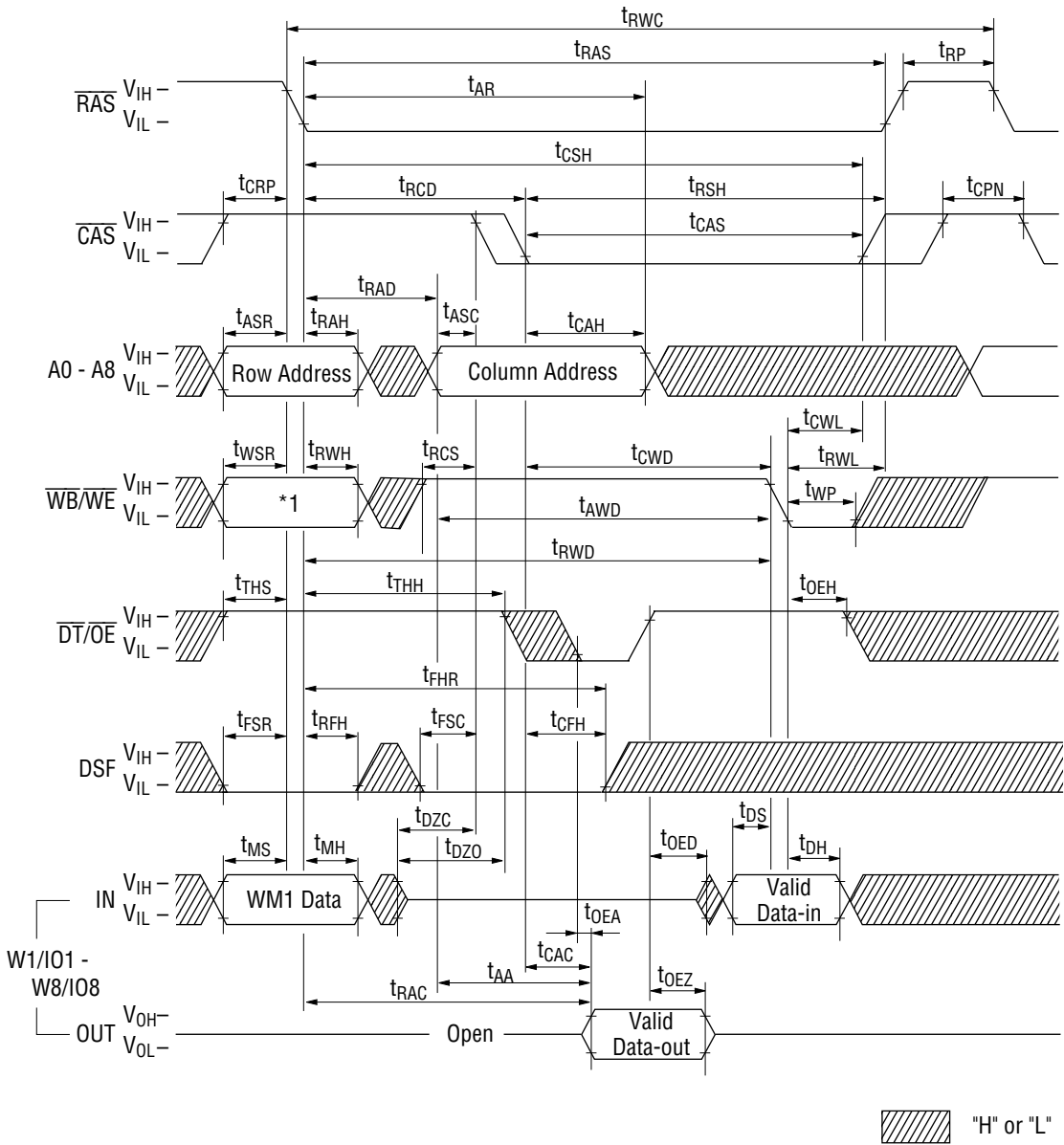
Write Cycle ($\overline{\text{OE}}$ Controlled Write)



*1 WB/WE	W1/I01 - W8/I08	Cycle
0	WM1 data	Write per Bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

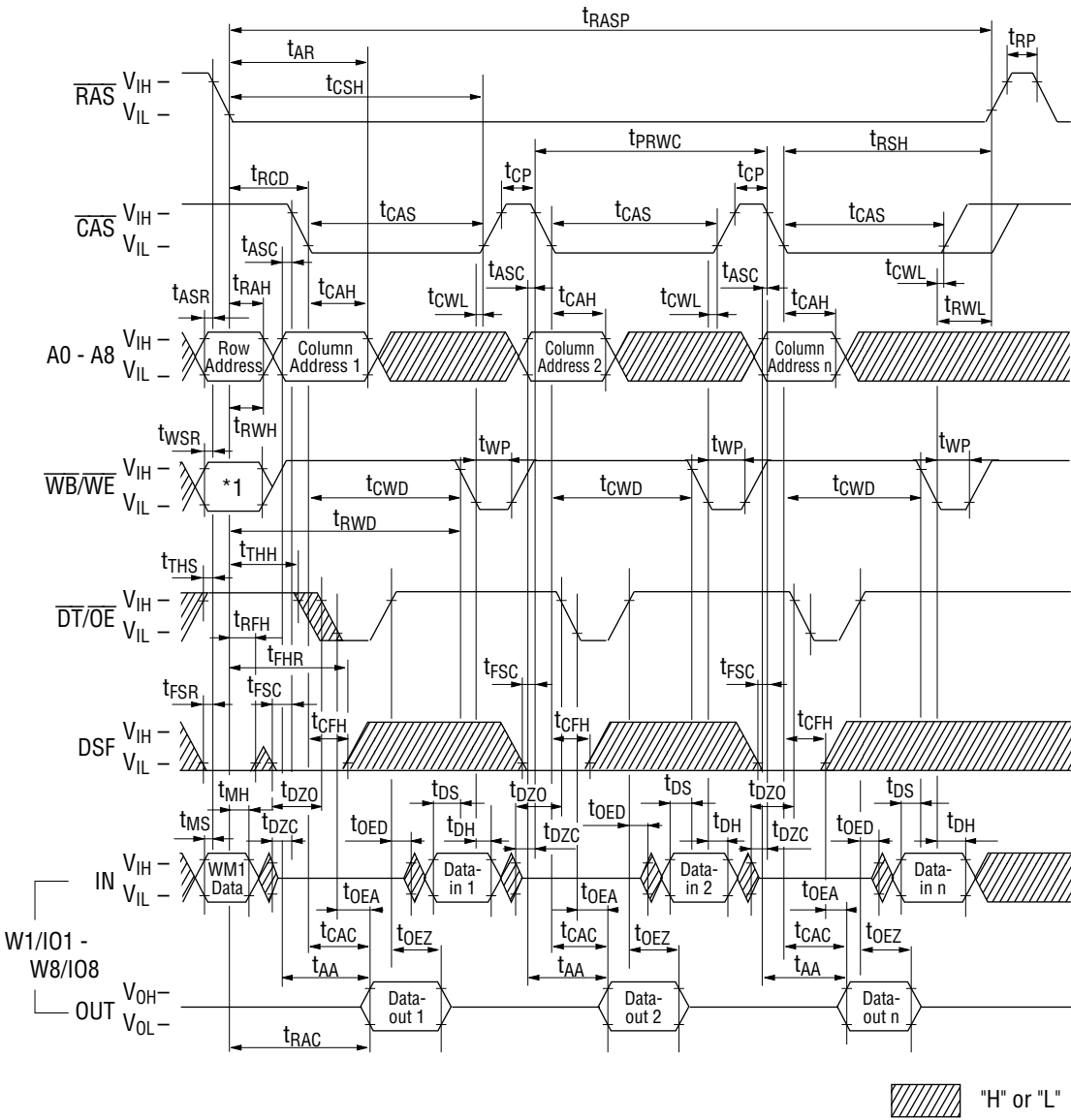
Read Modify Write Cycle



*1 WB/WE	W1/I01 - W8/I08	Cycle
0	WM1 data	Write per Bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

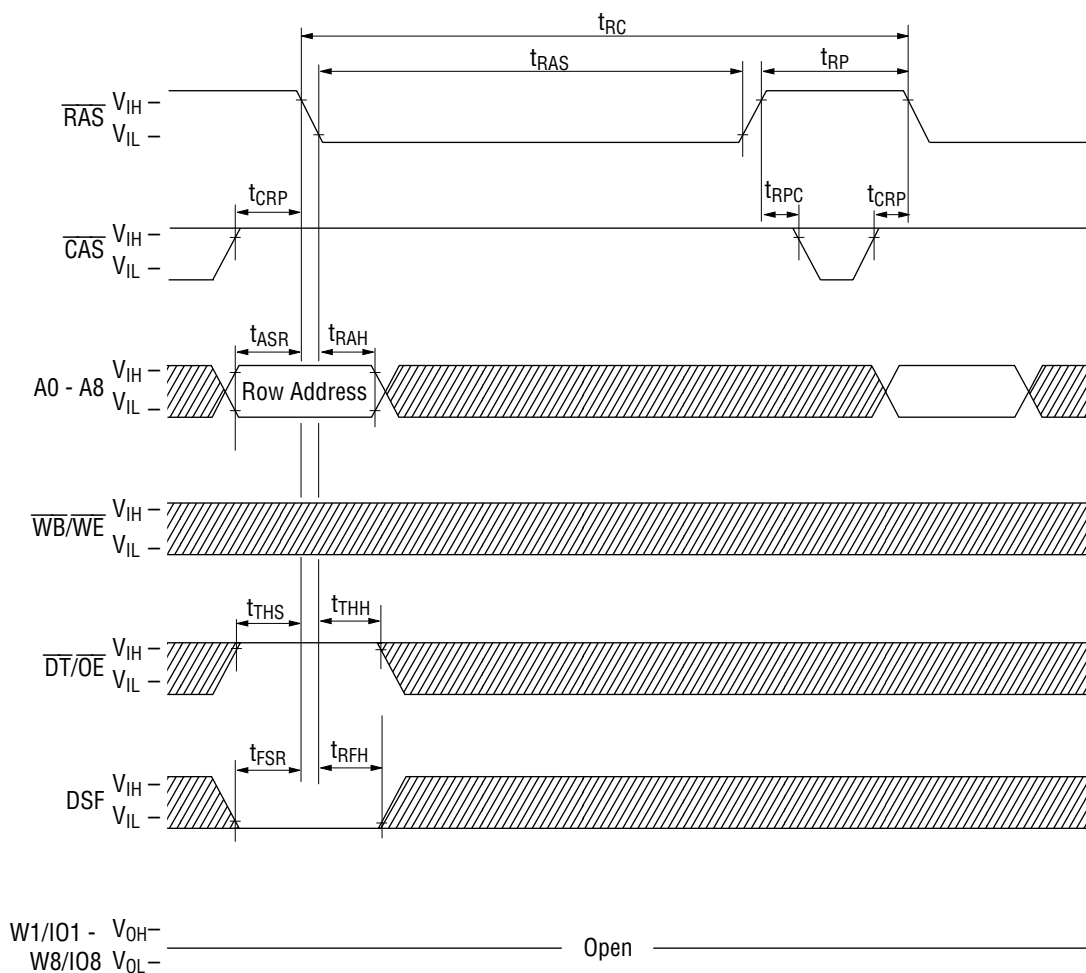
Fast Page Mode Read Modify Write Cycle



*1 WB/WE	W1/I01 - W8/I08	Cycle
0	WM1 data	Write per Bit
1	Don't Care	Normal Write

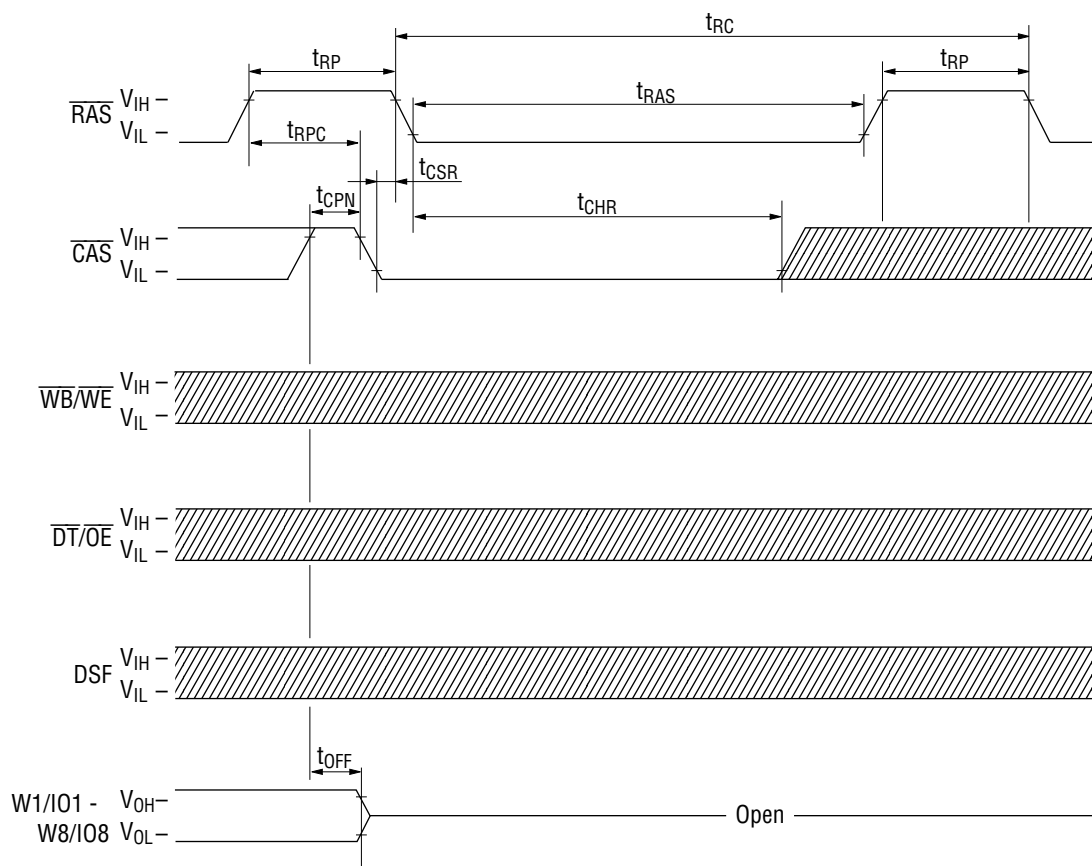
WM1 data: 0: Write Disable
1: Write Enable

RAS Only Refresh Cycle



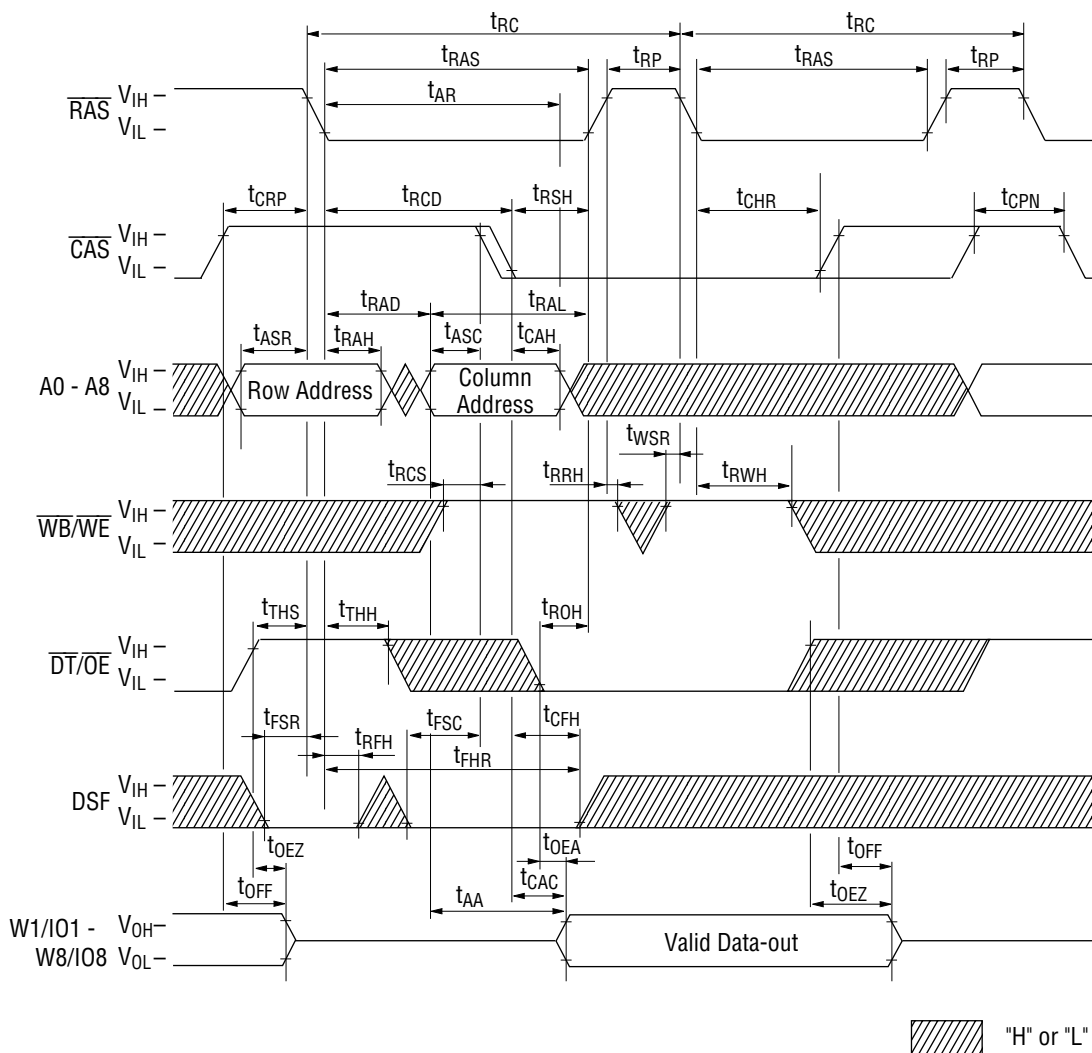
 "H" or "L"

CAS before RAS Refresh Cycle

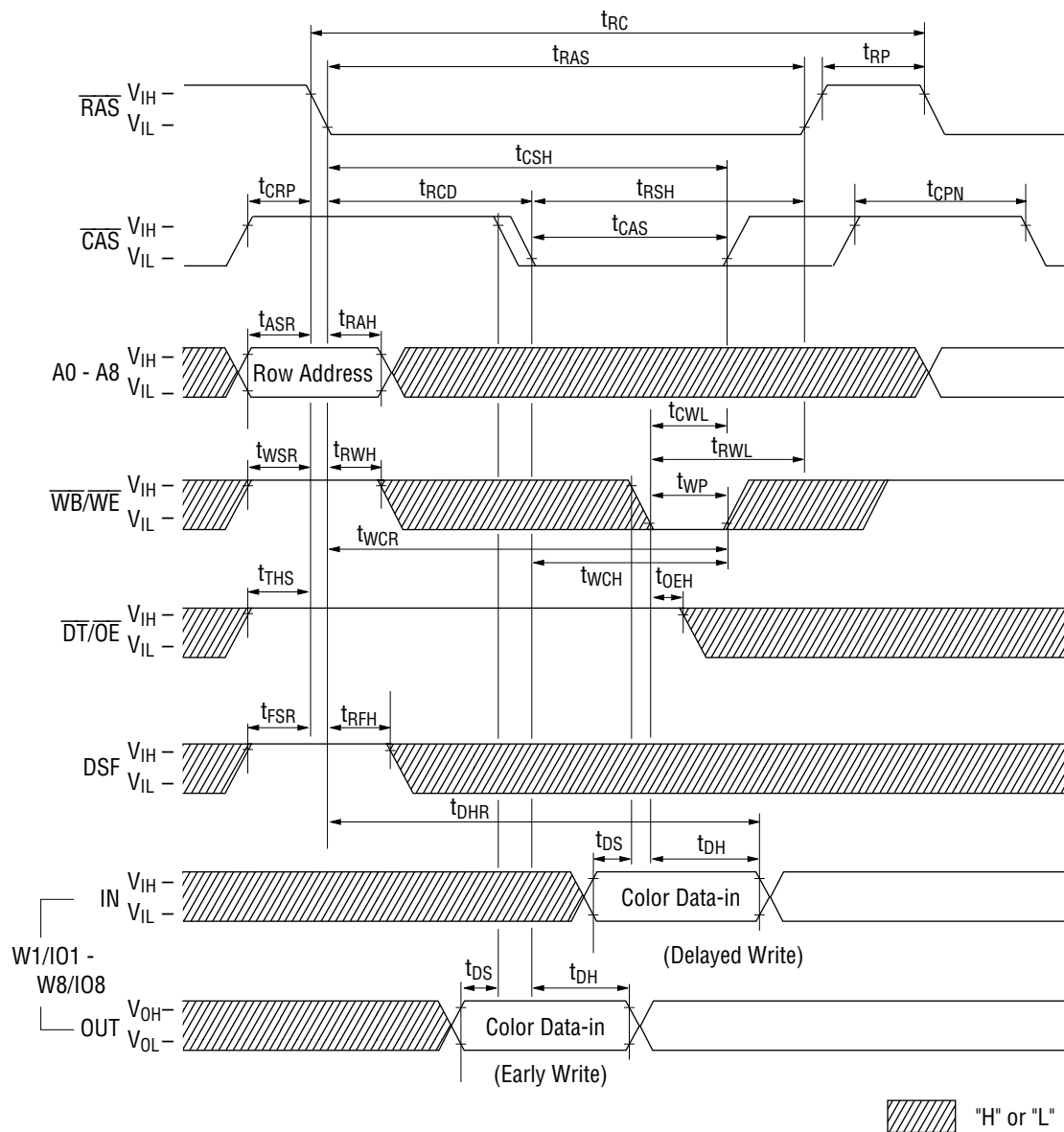


Note: A0 - A8 = Don't care ("H" or "L")  "H" or "L"

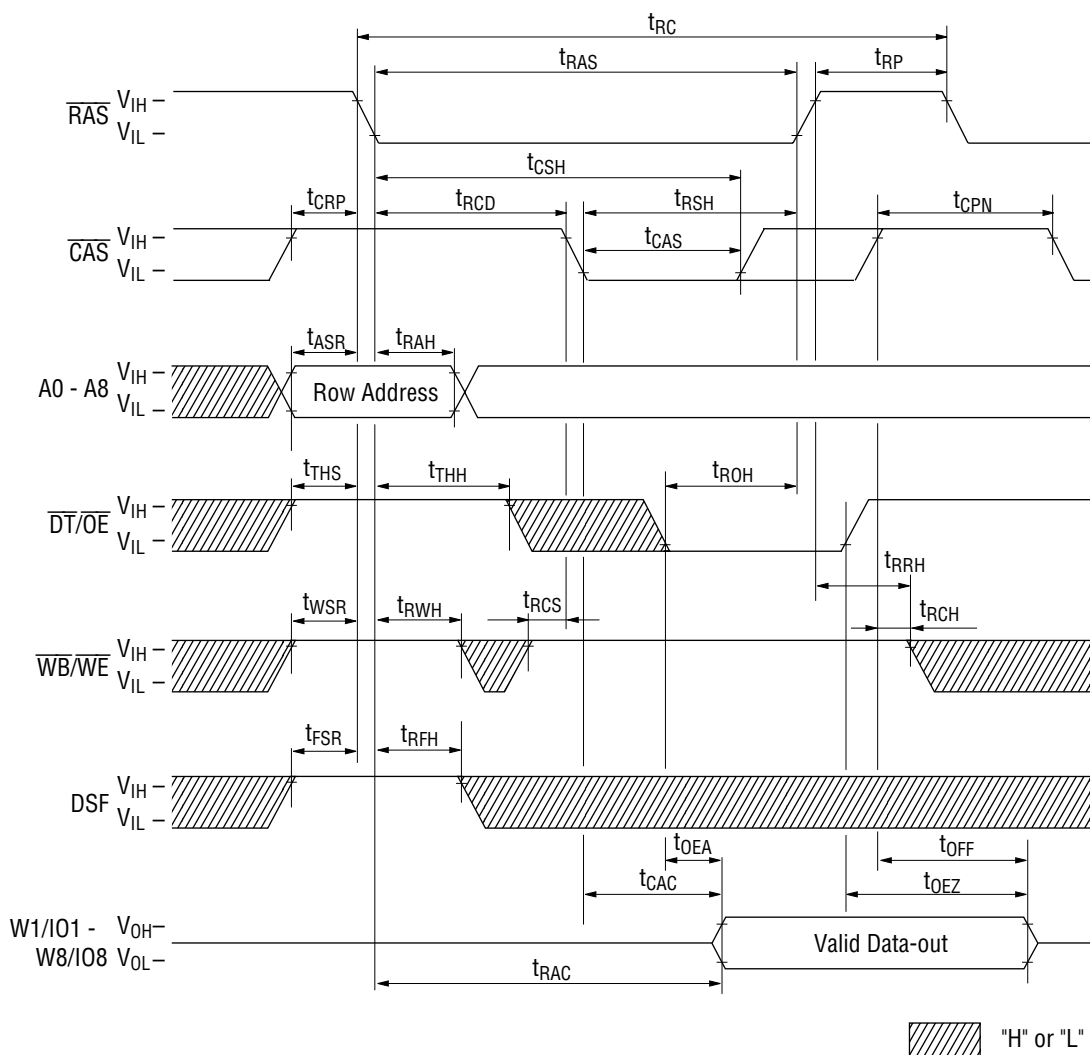
Hidden Refresh Cycle



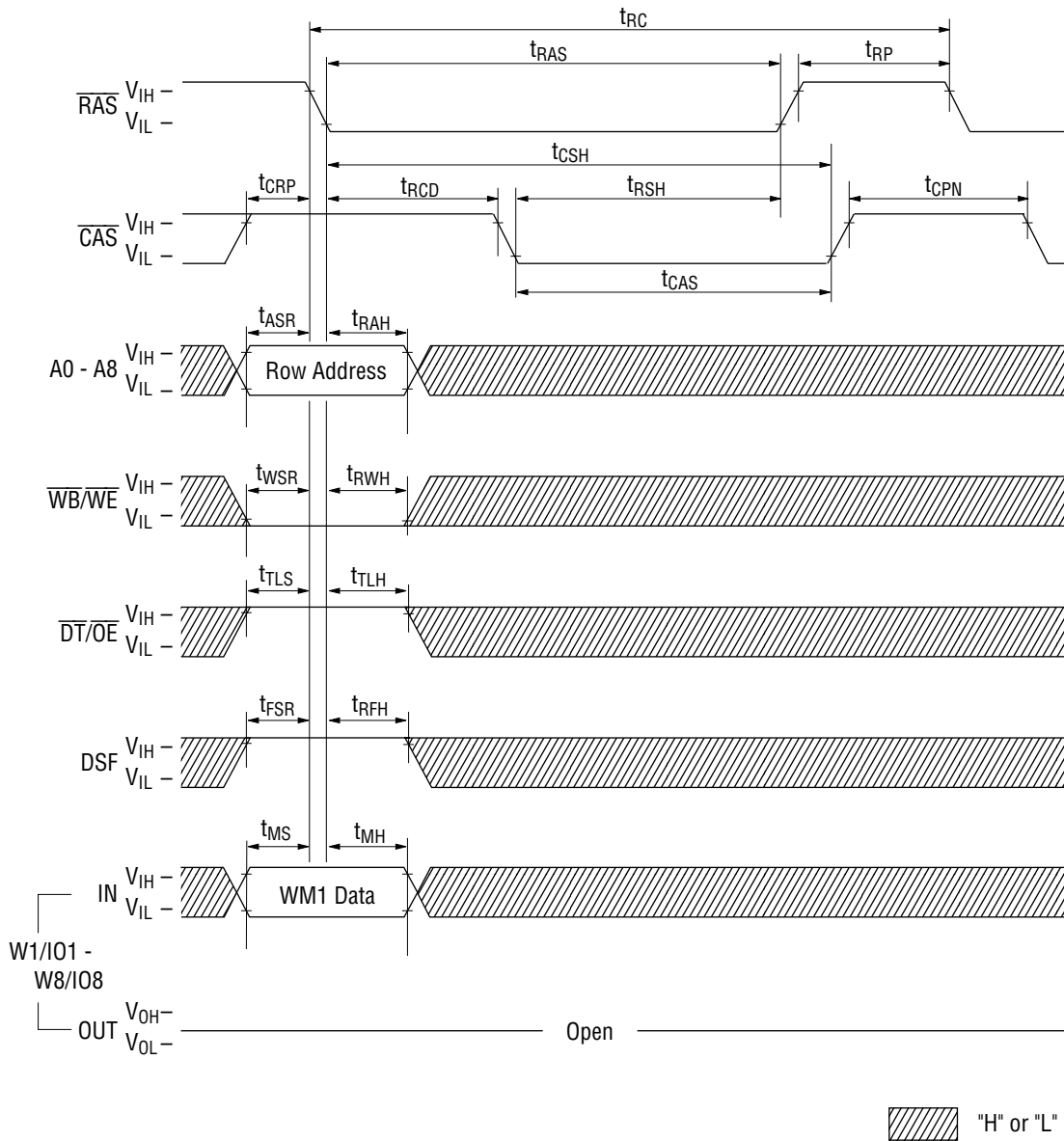
Load Color Register Cycle



Read Color Register Cycle

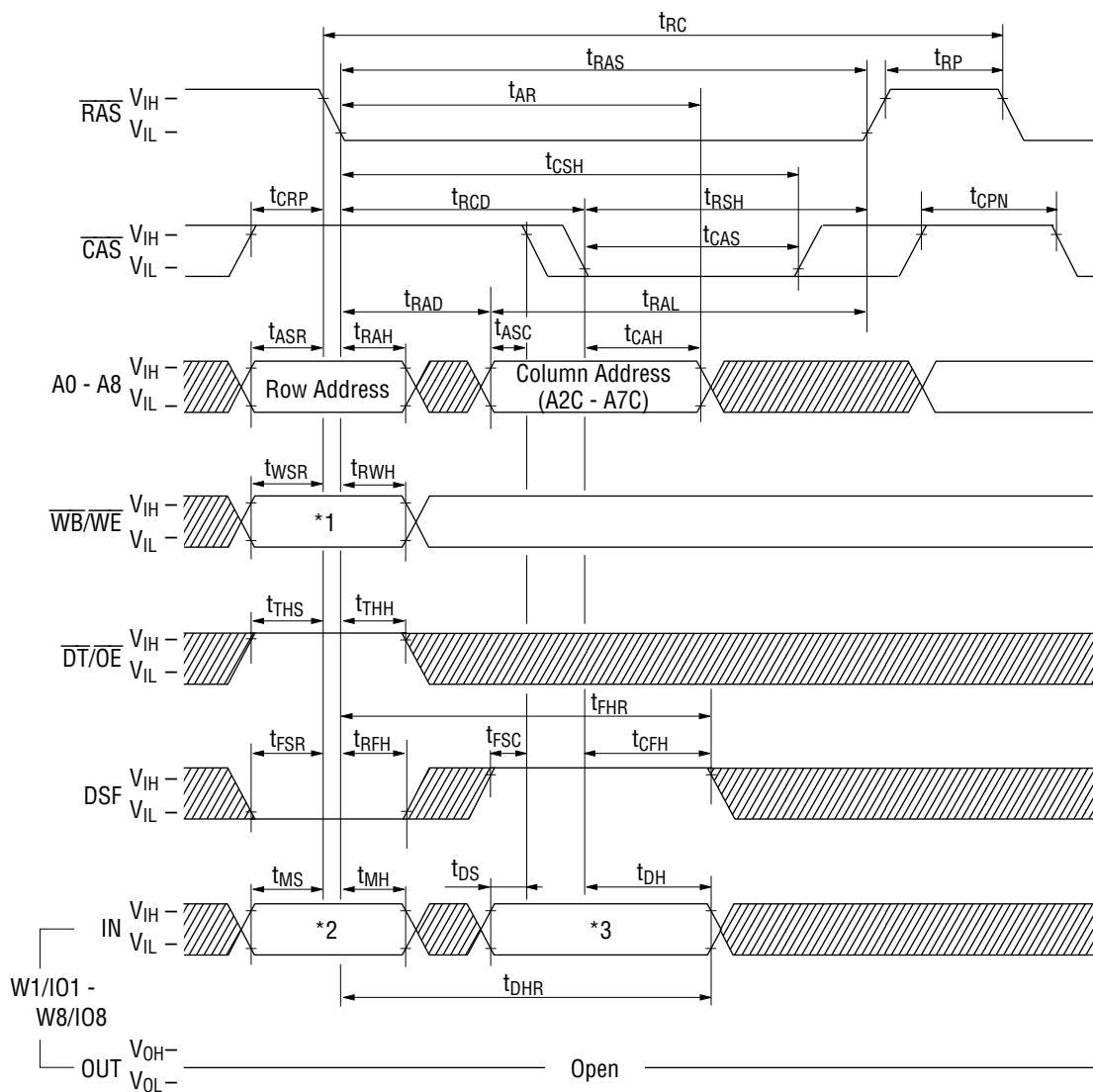


Flash Write Cycle



WM1 Data	Cycle
0	Flash Write Disable
1	Flash Write Enable

Block Write Cycle



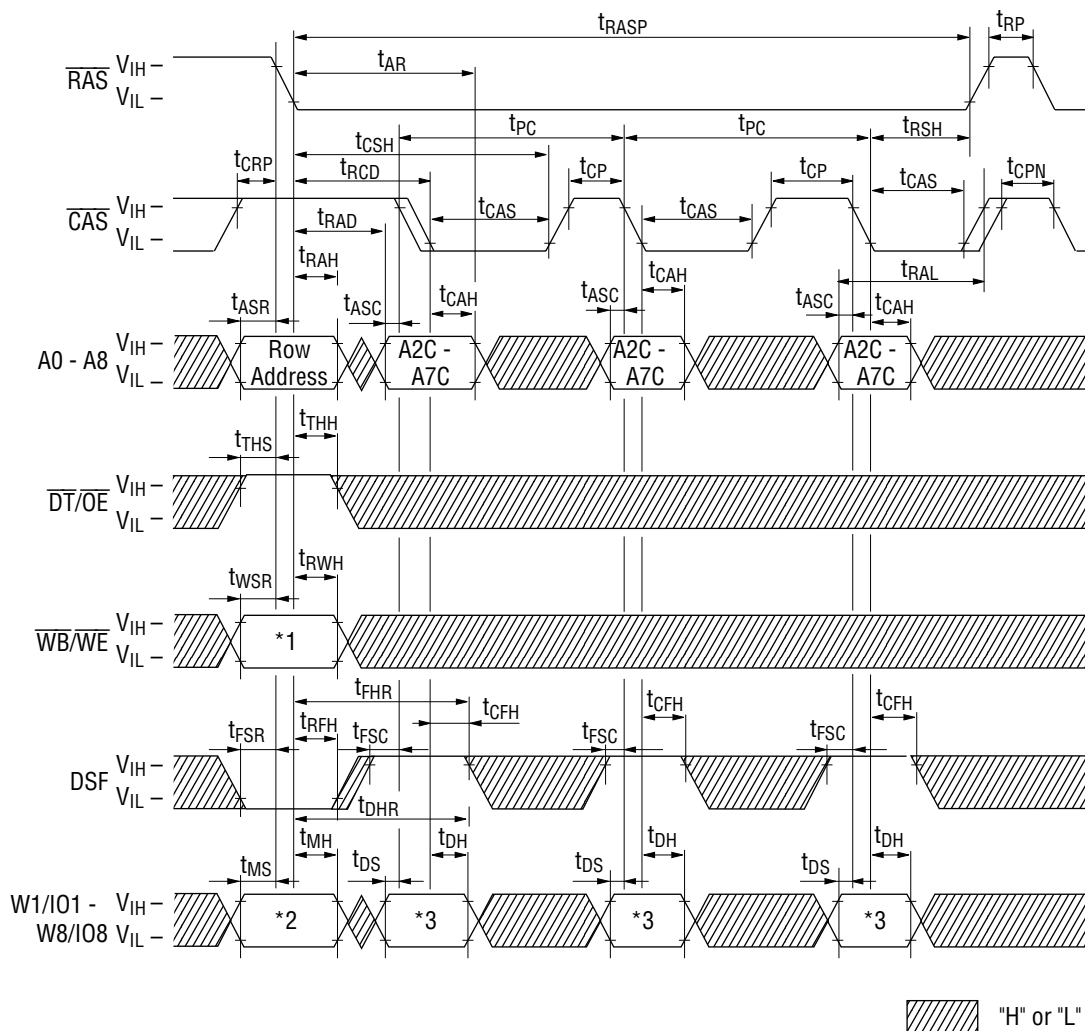
*1 $\overline{WB/WE}$	*2 W1/I01 - W8/I08	Cycle
0	WM1 data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

WM1 data: 0: Write Disable
1: Write Enable

*3) COLUMN SELECT

$\left. \begin{array}{l} \text{W1/I01 - Column 0 (A1C = 0, A0C = 0)} \\ \text{W2/I02 - Column 1 (A1C = 0, A0C = 1)} \\ \text{W3/I03 - Column 2 (A1C = 1, A0C = 0)} \\ \text{W4/I04 - Column 3 (A1C = 1, A0C = 1)} \end{array} \right\} \begin{array}{l} \text{Wn/On} \\ = 0 : \text{Disable} \\ = 1 : \text{Enable} \end{array}$

Fast Page Mode Block Write Cycle



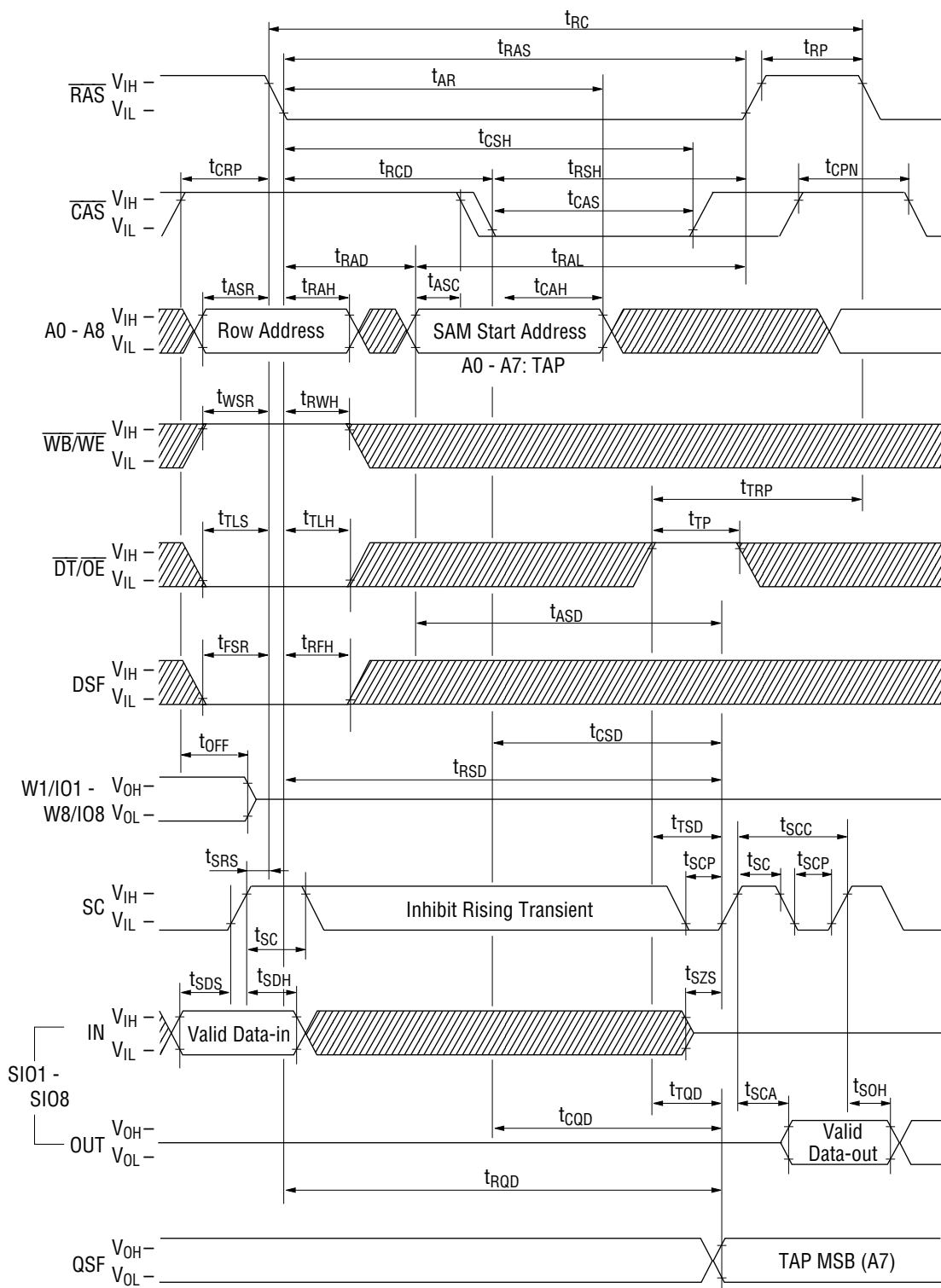
*1 WB/WE	*2 W1/I01 - W8/I08	Cycle
0	WM1 data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

WM1 data: 0: Write Disable
 1: Write Enable

*3) COLUMN SELECT

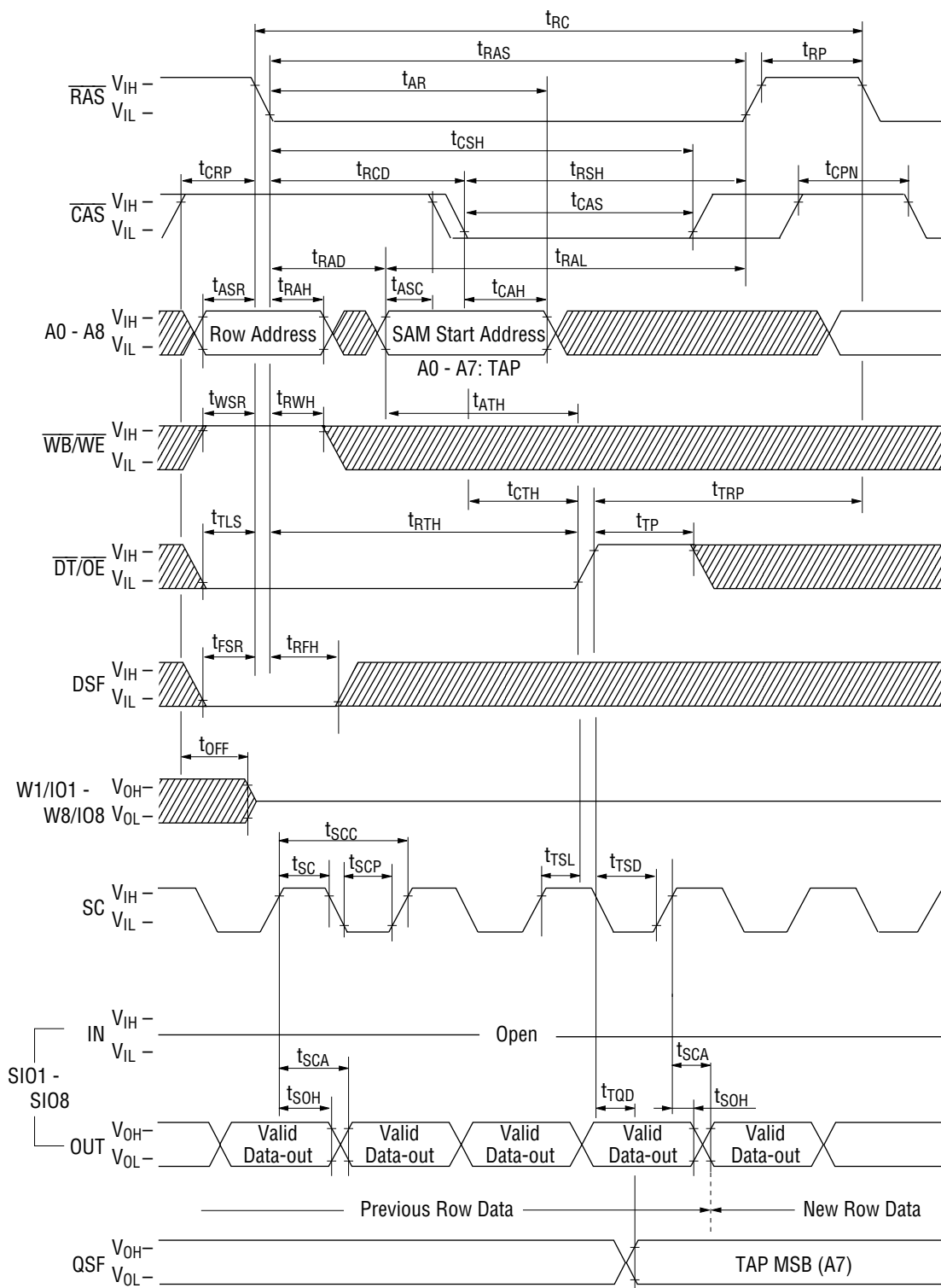
W1/I01 - Column 0 (A1C = 0, A0C = 0)	} Wn/On = 0 : Disable = 1 : Enable
W2/I02 - Column 1 (A1C = 0, A0C = 1)	
W3/I03 - Column 2 (A1C = 1, A0C = 0)	
W4/I04 - Column 3 (A1C = 1, A0C = 1)	

Read Transfer Cycle (Previous Transfer is Write Transfer Cycle)



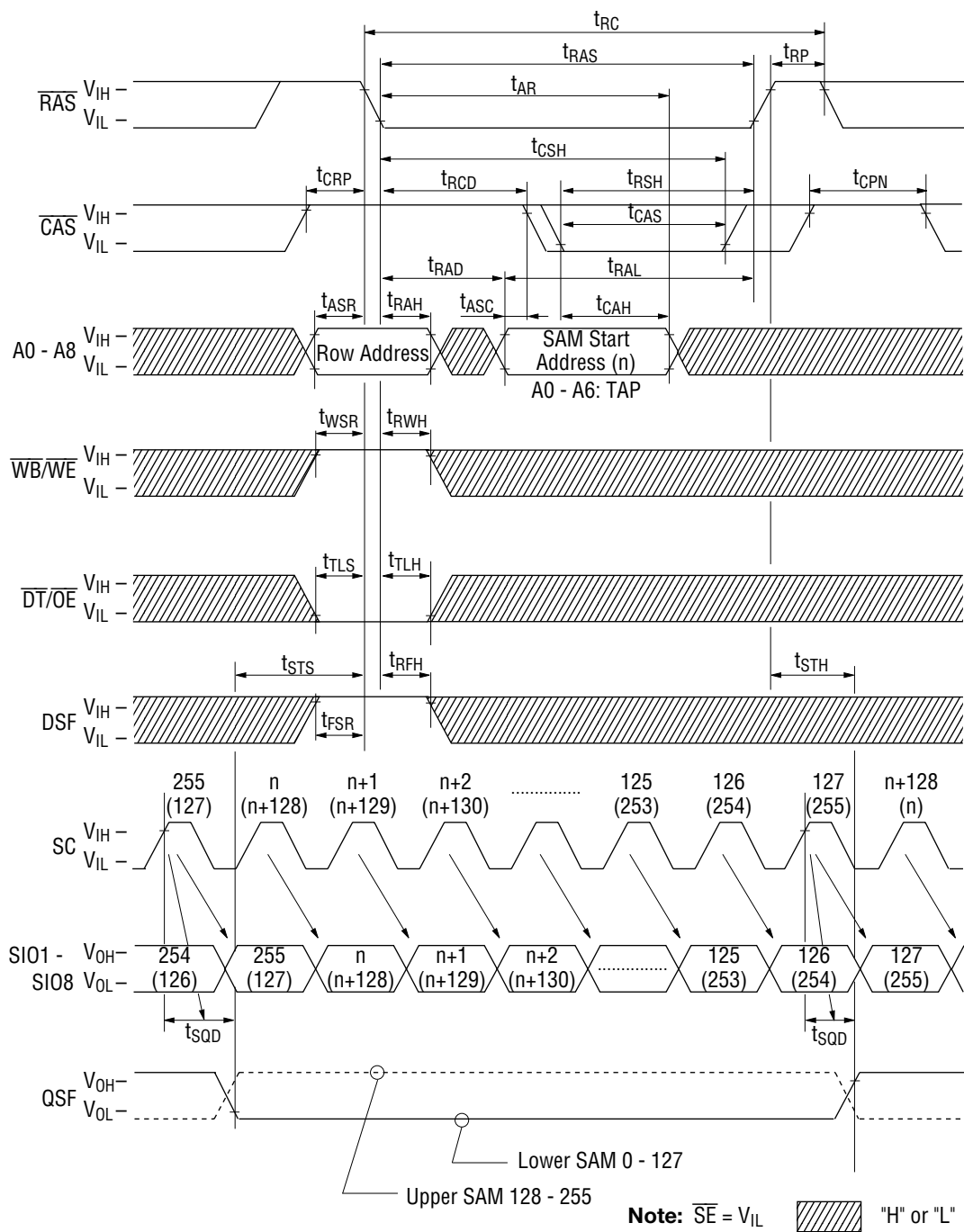
Note: $\overline{SE} = V_{IL}$  "H" or "L"

Real Time Read Transfer Cycle

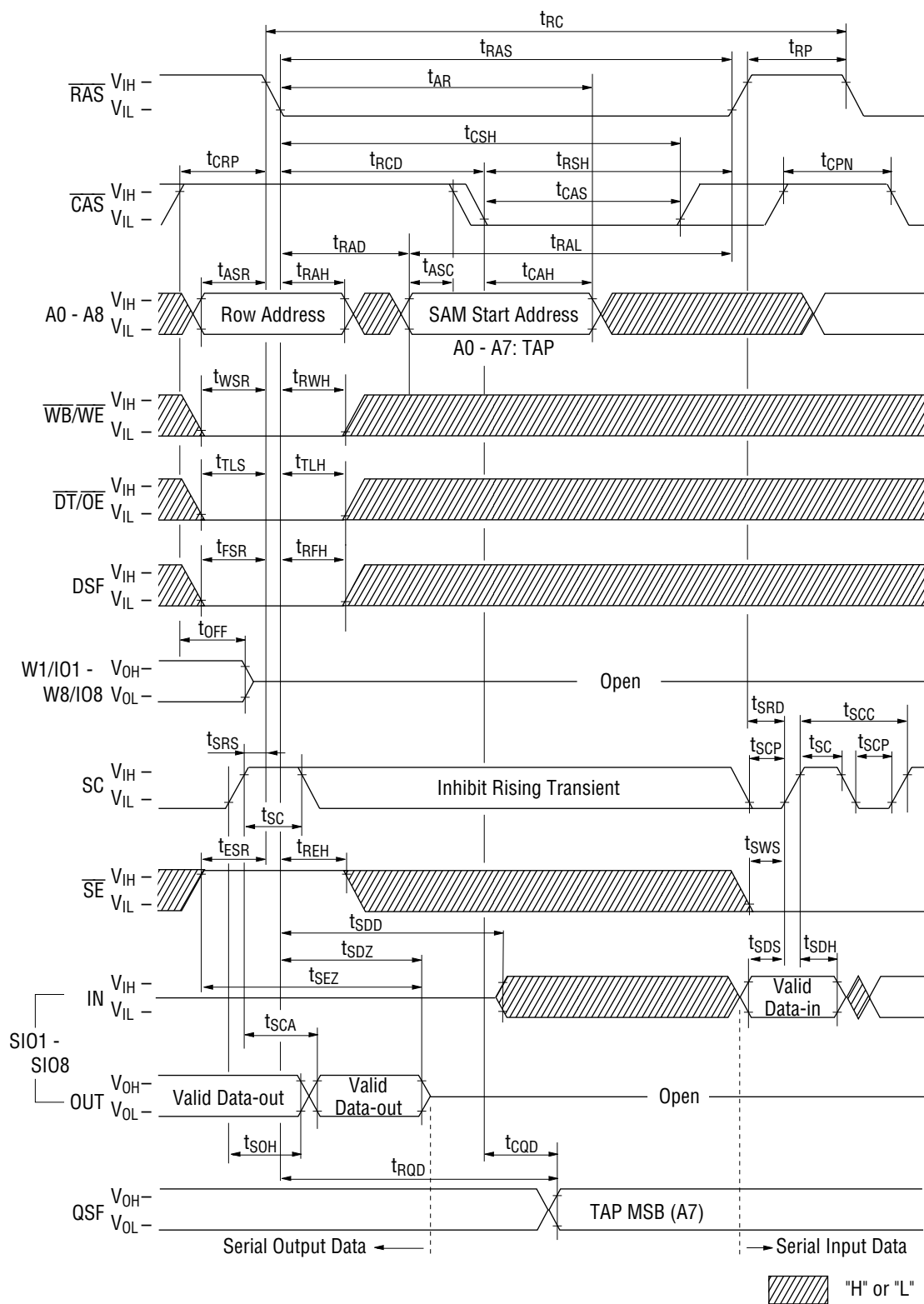


Note: $\overline{SE} = V_{IL}$  "H" or "L"

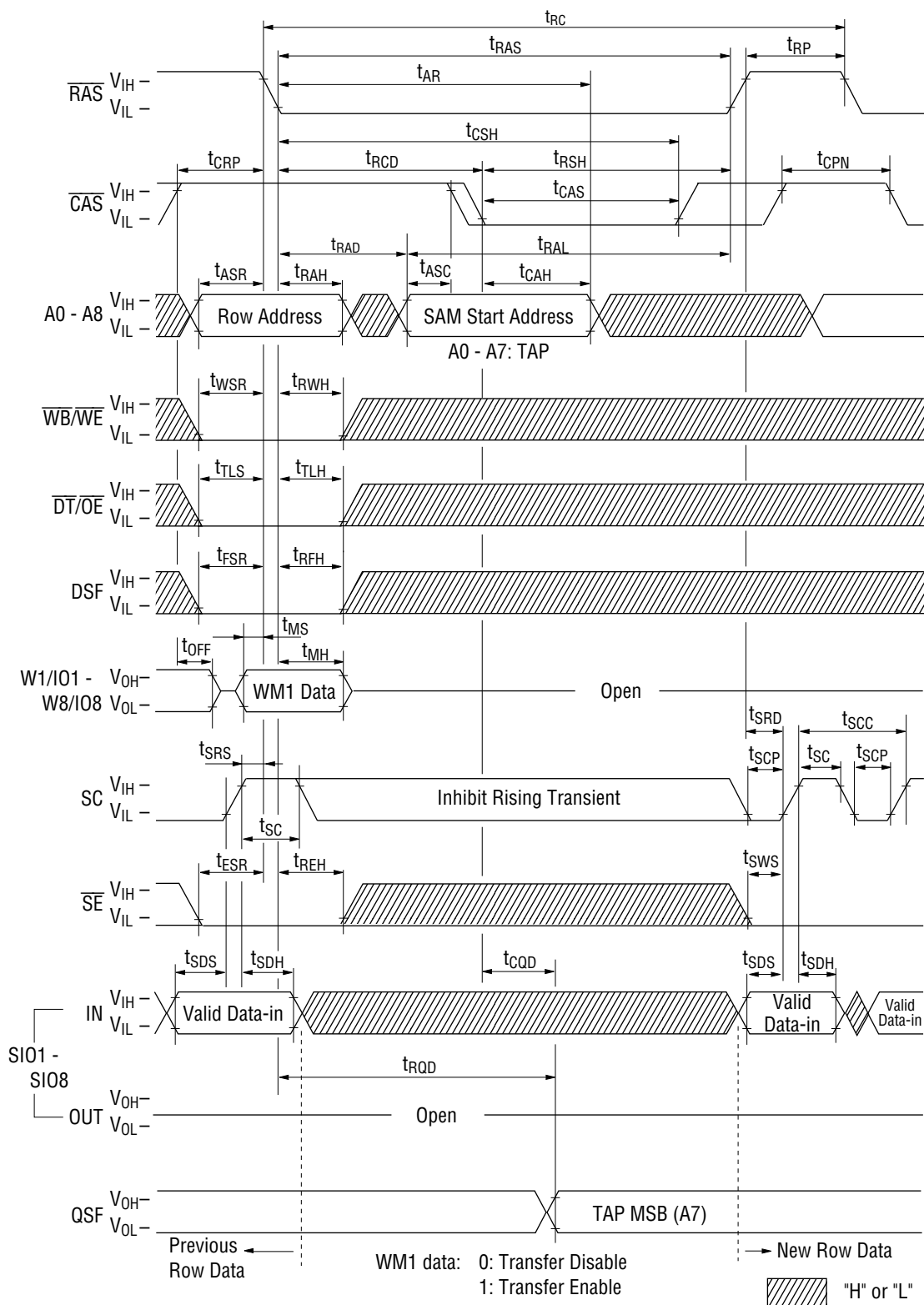
Split Read Transfer Cycle



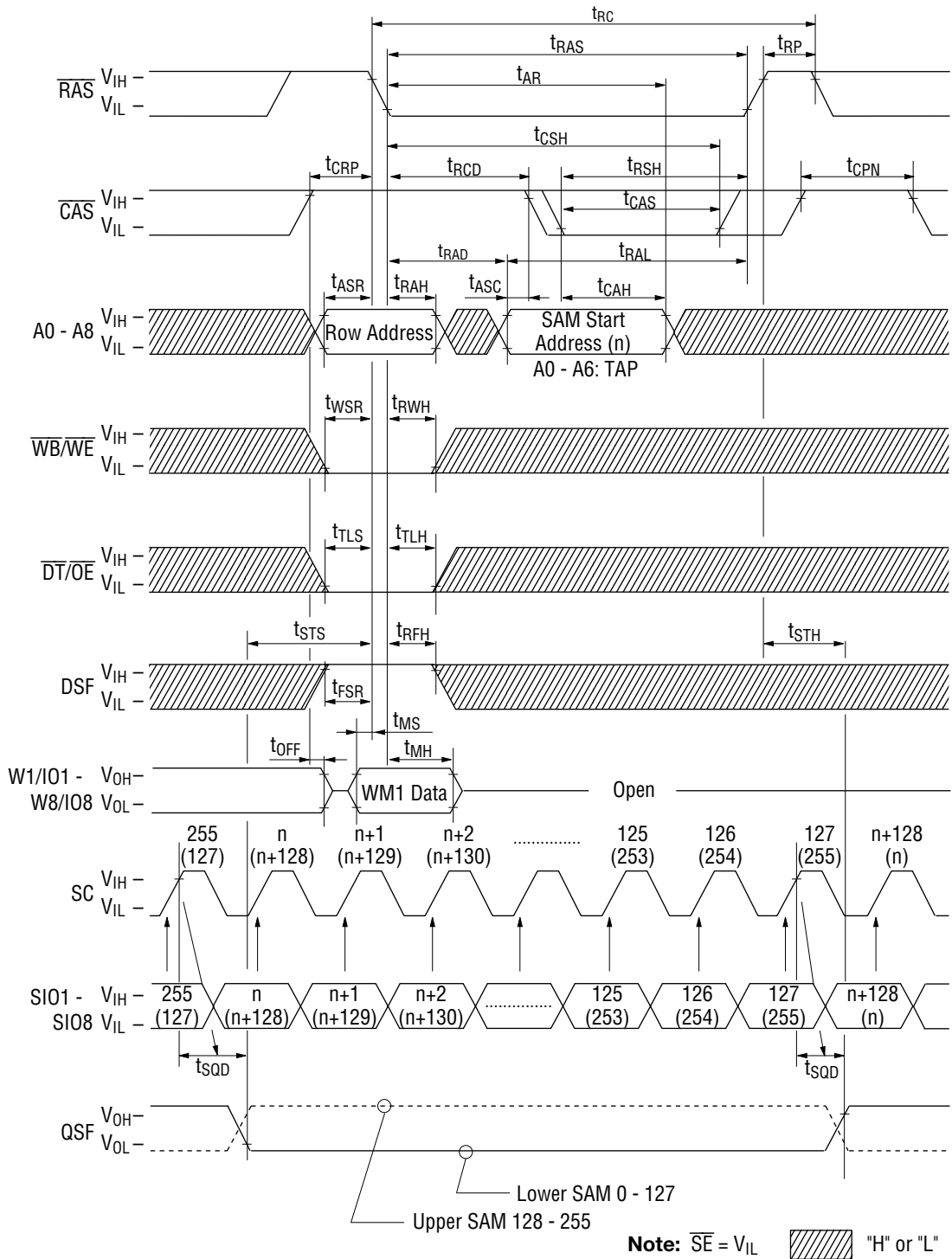
Pseudo Write Transfer Cycle



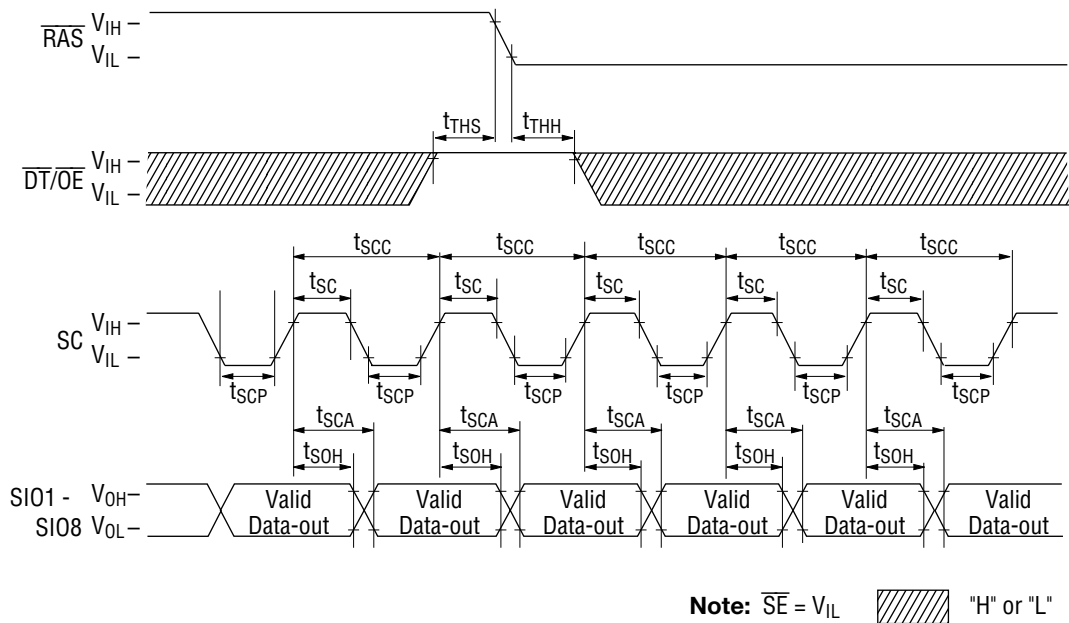
Write Transfer Cycle



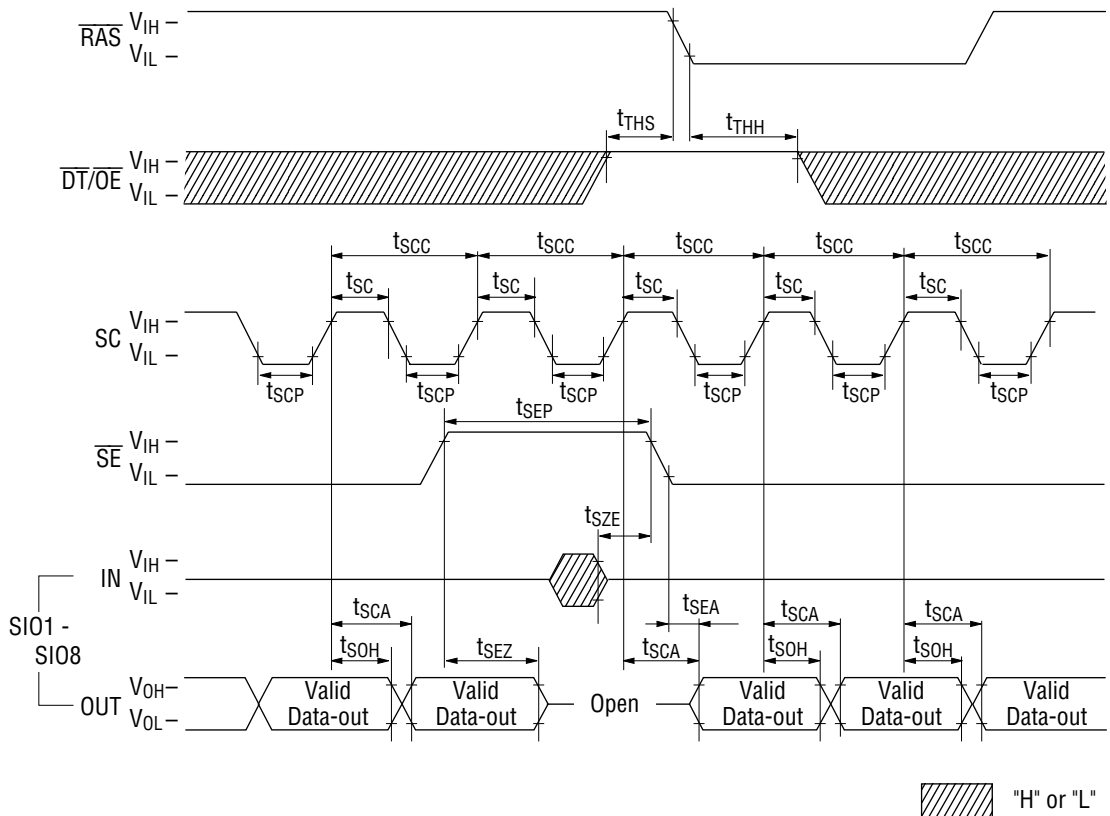
Split Write Transfer Cycle



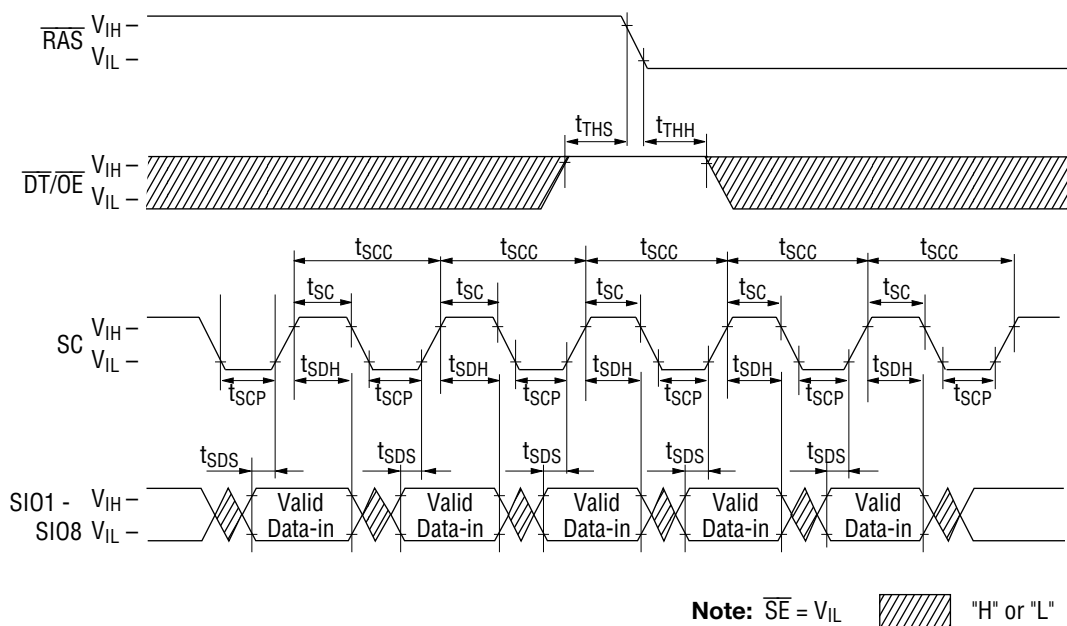
Serial Read Cycle ($\overline{SE} = V_{IL}$)



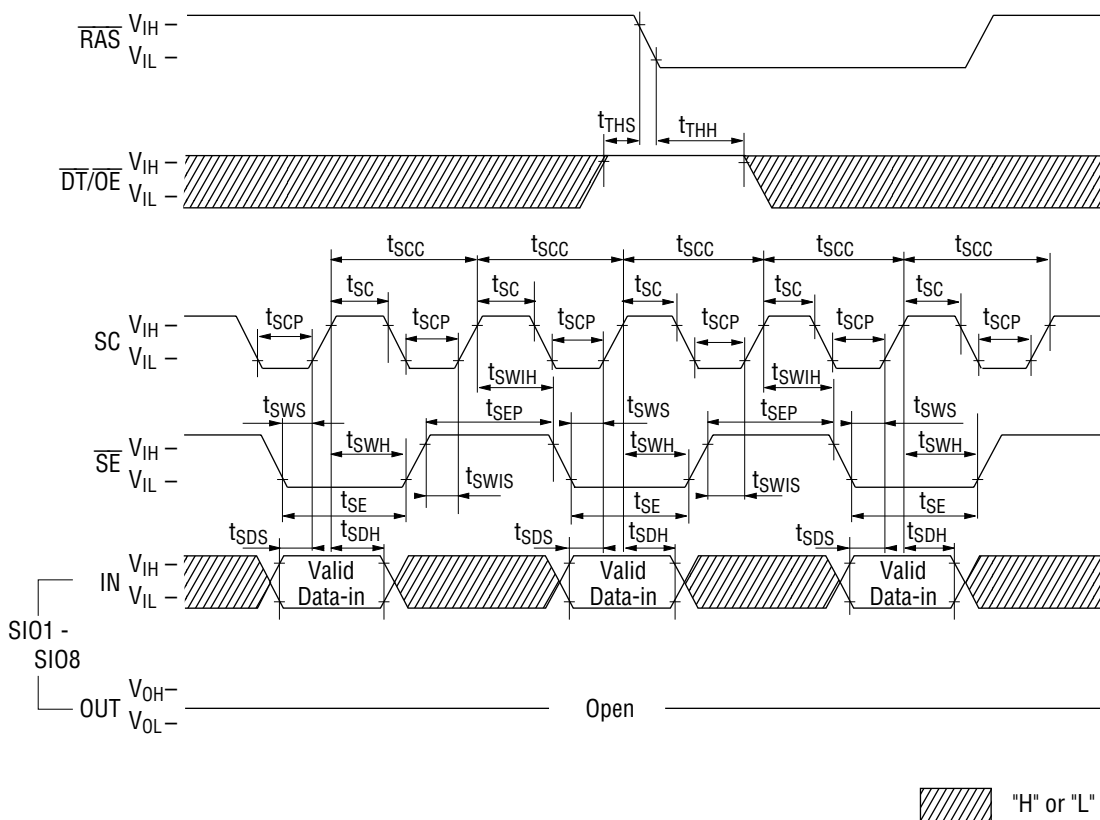
Serial Read Cycle ($\overline{SE}$ Controlled Outputs)



Serial Write Cycle ($\overline{SE} = V_{IL}$)



Serial Write Cycle ($\overline{SE}$ Controlled Inputs)



PIN FUNCTION

Address Input : A0 - A8

The 17 address bits decode an 8-bit location of the 1,048,576 locations in the MSM518122 memory array. The address bits are multiplexed to 9 address input pins (A0 - A8) as standard DRAM. 9 row address bits are latched at the falling edge of $\overline{\text{RAS}}$. The following 8 column address bits are latched at the falling edge of $\overline{\text{CAS}}$.

Row Address Strobe : $\overline{\text{RAS}}$

$\overline{\text{RAS}}$ is a basic RAM control signal. The RAM port is in standby mode when the $\overline{\text{RAS}}$ level is "high". As the standard DRAM's $\overline{\text{RAS}}$ signal function, $\overline{\text{RAS}}$ is control input that latches the row address bits and a random access cycle begins at the falling edge of $\overline{\text{RAS}}$.

In addition to the conventional $\overline{\text{RAS}}$ signal function, the level of the input signals, $\overline{\text{CAS}}$, $\overline{\text{DT/OE}}$, $\overline{\text{WB/WE}}$, DSF and $\overline{\text{SE}}$ at the falling edge of $\overline{\text{RAS}}$, determines the MSM518122 operation modes.

Column Address Strobe : $\overline{\text{CAS}}$

As the standard DRAM's $\overline{\text{CAS}}$ signal function, $\overline{\text{CAS}}$ is the control input signal that latches the column address input and the state of the special function input DSF to select, in conjunction with the $\overline{\text{RAS}}$ control, either read/write operations or the special block write feature on the RAM port when the DSF is held "low" at the falling edge of $\overline{\text{RAS}}$.

$\overline{\text{CAS}}$ also acts as a RAM port output enable signal.

Data Transfer/Output Enable : $\overline{\text{DT/OE}}$

$\overline{\text{DT/OE}}$ is also a control input signal having multiple functions. As the standard DRAM's $\overline{\text{OE}}$ signal function, $\overline{\text{DT/OE}}$ is used as an output enable control when $\overline{\text{DT/OE}}$ is "high" at the falling edge of $\overline{\text{RAS}}$.

In addition to the conventional $\overline{\text{OE}}$ signal function, a data transfer operation is started between the RAM port and the SAM port when $\overline{\text{DT/OE}}$ is "low" at the falling edge of $\overline{\text{RAS}}$.

Write per Bit/Write Enable : $\overline{\text{WB/WE}}$

$\overline{\text{WB/WE}}$ is a control input signal having multiple functions. As the standard DRAM's $\overline{\text{WE}}$ signal function, it is used to write data into the memory on the RAM port when $\overline{\text{WB/WE}}$ is "high" at the falling edge of $\overline{\text{RAS}}$.

In addition to the conventional $\overline{\text{WE}}$ signal function, the $\overline{\text{WB/WE}}$ determines the write-per-bit function when $\overline{\text{WB/WE}}$ is "low" at the falling edge of $\overline{\text{RAS}}$, during RAM port operations. The $\overline{\text{WB/WE}}$ also determines the direction of data transfer between the RAM and SAM.

When $\overline{\text{WB/WE}}$ is "high" at the falling edge of $\overline{\text{RAS}}$, the data is transferred from RAM to SAM (read transfer). When $\overline{\text{WB/WE}}$ is "low" at the falling edge of $\overline{\text{RAS}}$, the data is transferred SAM to RAM (write transfer).

Write Mask Data/Data Input and Output : W1/IO1 - W8/IO8

W1/IO1 - W8/IO8 have the functions of both Input/Output and a control input signal. As the standard DRAM's I/O pins, input data on the W1/IO1 - W8/IO8 are written into the RAM port during the write cycle. The input data is latched at the falling edge of either $\overline{\text{CAS}}$ or $\overline{\text{WB}}/\overline{\text{WE}}$, whichever occurs later. The RAM data out buffers, which will output read data from the W1/IO1 - W8/IO8 pins, becomes low impedance state after the specified access times from $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{DT}}/\overline{\text{OE}}$ and column address are satisfied and the output data will remain valid as long as $\overline{\text{CAS}}$ and $\overline{\text{DT}}/\overline{\text{OE}}$ are kept "low". The outputs will return to the high impedance state at the rising edge of either $\overline{\text{CAS}}$ or $\overline{\text{DT}}/\overline{\text{OE}}$, whichever occurs earlier.

In addition to the conventional I/O function, the W1/IO1 - W8/IO8 have the function to set the mask data, which select mask input pins out of four input pins, W1/IO1 - W8/IO8, at the falling edge of $\overline{\text{RAS}}$. Data is written to the DRAM on data lines where the Write-mask data is a logic "1". The write-mask data is valid for only one cycle.

Serial Clock : SC

SC is a main serial cycle control input signal. All operations of SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SIO pins after the maximum specified serial access time t_{SCA} from the rising edge of SC.

The SC also increments the 9 bits serial pointer which is used to select the SAM address. The pointer address is incremented in a wrap-around mode to select sequential locations after the setting location which is determined by the column address in the read transfer cycle. When the pointer reaches the most significant address location (decimal 255), the next SC clock will place it at the least significant address location (decimal 0).

The SC must be held data constant V_{IH} or V_{IL} level during read /pseudo write /write-transfer operations and should not be clocked while the SAM port is the standby mode to prevent the SAM pointer from being increment.

Serial Enable : $\overline{\text{SE}}$

The $\overline{\text{SE}}$ is a serial access enable control and serial read/write control signal. In a serial read cycle, $\overline{\text{SE}}$ is used as an output control. In a serial write cycle, $\overline{\text{SE}}$ is used as write enable control. When $\overline{\text{SE}}$ is "high", serial access is disable, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{\text{SE}}$ is "high".

Special Function Input : DSF

The DSF is latched at the falling edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ and allows for the selection of several RAM port and transfer operating modes. In addition to the conventional multiport DRAM, the special function consisting of flash write, block write, load/read resistor and read/write transfer can be invoked.

Special Function Output : QSF

QSF is an output signal which, during split resister mode, indicates which half of the split SAM is being accessed. QSF “low” indicates that the lower split SAM (0 - 127) is being accessed. QSF “high” indicates that the upper SAM (128 - 255) is being accessed.

QSF is monitored so that after it toggles and after allowing for a delay of t_{STS} , split read/write transfer operation can be performed on the non-active SAM.

Serial Input/Output : SIO1 - SIO8

Serial input/output mode is determined by the most recent read, write or pseudo write transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a write or pseudo write transfer cycle is performed, the SAM port is switched from output mode to input mode.

OPERATION MODES

Table-1 shows the function truth table for a listing of all available RAM ports and transfer operation of MSM518122.

The RAM port and data transfer operations are determined by the state of $\overline{\text{CAS}}$, $\overline{\text{DT/OE}}$, $\overline{\text{WB/WE}}$, $\overline{\text{SE}}$ and DSF at the falling edge of $\overline{\text{RAS}}$ and by the level of DSF at the falling edge of $\overline{\text{CAS}}$.

Table-1. Function Truth Table

$\overline{\text{RAS}} \downarrow$					$\overline{\text{CAS}} \downarrow$	ADDRESS		W/IO			Write Mask	Register		Function
CAS	DT/OE	WB/WE	DSF	SE	DSF	RAS	CAS	RAS	CAS	CAS/WE		WM	Color	
0	*	*	*	*	—	*	—	*	—	—	—	—	—	C.B.R Refresh
1	0	0	0	0	*	Row	TAP	WM1	*	*	WM1	Load Use	—	Masked Write Transfer
1	0	0	0	1	*	Row	TAP	*	*	*	—	—	—	Pseudo Write Transfer
1	0	0	1	*	*	Row	TAP	WM1	—	*	WM1	Load Use	—	Split Write Transfer
1	0	1	0	*	*	Row	TAP	*	*	*	—	—	—	Read Transfer
1	0	1	1	*	*	Row	TAP	*	*	*	—	—	—	Split Read Transfer
1	1	0	0	*	0	Row	Column	WM1	—	Din	WM1	Load Use	—	Write per Bit
1	1	0	0	*	1	Row	Column A2c-7c	WM1	Column Select	—	WM1	Load Use	Use	Masked Block Write
1	1	0	1	*	*	Row	*	WM1	—	*	WM1	Load Use	Use	Masked Flash Write
1	1	1	0	*	0	Row	Column	*	—	Din	—	—	—	Read Write
1	1	1	0	*	1	Row	Column A2c-7c	*	Column Select	—	—	—	Use	Block Write
1	1	1	1	*	*	Row	*	*	—	Color	—	—	Load	Load Color Register

If the DSF is "high" at the falling edge of $\overline{\text{RAS}}$, special functions such as split transfer, flash write, and load/read color register can be invoked. If the DSF is "low" at the falling edge of $\overline{\text{RAS}}$ and "high" at the falling edge of $\overline{\text{CAS}}$, the block write feature can be invoked.

If the DSF is "low" at the falling edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$, only the conventional multiport DRAM operating feature can be invoked.

RAM PORT OPERATION

Fast Page Mode

Fast page mode allows data to be transferred into or out of multiple column locations of the same row by performing multiple $\overline{\text{CAS}}$ cycle during a signal active for a period up to 100 μ s. For the initial fast page mode access, the output data is valid after the specified access times from $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, column address and $\overline{\text{DT}}/\overline{\text{OE}}$.

For all subsequent fast page mode read operations, the output data is valid after the specified access times from $\overline{\text{CAS}}$, column address and $\overline{\text{DT}}/\overline{\text{OE}}$. When the write-per bit function is enable, the mask data latched at the falling edge of $\overline{\text{RAS}}$ is maintained throughout the fast page mode write or read or read modify write cycle.

$\overline{\text{RAS}}$ Only Refresh

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of the 512 rows in the DRAM array within the specified 8ms refresh period.

Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with “ $\overline{\text{RAS}}$ -only” cycle.

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh

The MSM518122 also offers an internal refresh function. When $\overline{\text{CAS}}$ is held “low” for a specified period (t_{CSR}) before $\overline{\text{RAS}}$ goes “low”, an internal refresh address counter and on-chip refresh control clock generators are enable refresh operation take place.

When the refresh operation is completed, the internal refresh address counter is automatically incremented in preparation for the next $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycle. For successive $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle, $\overline{\text{CAS}}$ can remain “low” while cycling $\overline{\text{RAS}}$.

Hidden Refresh

A hidden refresh is a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh performed by holding $\overline{\text{CAS}}$ “low” from a previous read cycle. This allows for the output data from the previous memory cycle to remain valid while performing a refresh.

The internal refresh address counter provides the address and the refresh is accomplished by cycling $\overline{\text{RAS}}$ after the specified $\overline{\text{RAS}}$ precharge period.

Write per Bit Function

The write per bit selectively controls the internal write enable circuits of the RAM port. Write per bit enabled when $\overline{\text{WB}}/\overline{\text{WE}}$ held “low” at the falling edge of $\overline{\text{RAS}}$ in a random write operation. Also, at the falling edge of $\overline{\text{RAS}}$, the mask data on the Wi/IOi pins are latched into a write mask register. The write mask data must be presented at the Wi/IOi pins at every falling edge of $\overline{\text{RAS}}$. A “0” on any of the Wi/IOi pins will disable the corresponding write circuits and new data will not be written into the RAM. A “1” on any of Wi/IOi pins will enable the corresponding write circuits and new data will be written into the RAM.

Load / Read Color Register

The MSM518122 is provided with an on-chip 4 bits color register for use during the flash write or block write operation. Each bit of the color register corresponds to one of the DRAM I/O blocks.

The load color register cycle is initiated by holding $\overline{\text{CAS}}$, $\overline{\text{WB}}/\overline{\text{WE}}$, $\overline{\text{DT}}/\overline{\text{OE}}$ and DSF "high" at the falling edge of $\overline{\text{RAS}}$. The data presented on the Wi/IOi lines is subsequently latched into the color register at the falling edge of either $\overline{\text{CAS}}$ or $\overline{\text{WB}}/\overline{\text{WE}}$ whichever occurs later.

The read color register cycle is activated by holding $\overline{\text{CAS}}$, $\overline{\text{WB}}/\overline{\text{WE}}$, $\overline{\text{DT}}/\overline{\text{OE}}$ and DSF "high" at the falling edge of $\overline{\text{RAS}}$ and by holding $\overline{\text{WB}}/\overline{\text{WE}}$ "high" at the falling edge of $\overline{\text{CAS}}$ and throughout the remainder of the cycle. The data in the color register becomes valid on the Wi/IOi lines after the specified access times from $\overline{\text{RAS}}$ and $\overline{\text{DT}}/\overline{\text{OE}}$ are satisfied.

During the load/read color register cycle, the memory cells on the row address latched at the falling edge of $\overline{\text{RAS}}$ are refreshed.

Flash Write

Flash write allows for the data in the color register to be written into all the memory locations of a selected row.

Each bit of the color register corresponds to the DRAM I/O blocks and the flash write operation can be selectively controlled on an I/O basis in the same manner as the write per bit operation. A flash write cycle is performed by holding $\overline{\text{CAS}}$ "high" $\overline{\text{WB}}/\overline{\text{WE}}$ "low" and DSF "high" at the falling edge of $\overline{\text{RAS}}$. The mask data must also be provided on the Wi/IOi lines at the falling edge of $\overline{\text{RAS}}$ in order to enable the flash write operation for selected I/O blocks.

Block Write

Block write allows for the data in the color register to be written into 4 consecutive column address locations starting from a selected row. The block write operation can be selectively controlled on an I/O basis and a column mask capability is also available.

Block write cycle is performed by holding $\overline{\text{CAS}}$, $\overline{\text{DT}}/\overline{\text{OE}}$ "high" and DSF "low" at the falling edge of $\overline{\text{RAS}}$ and by holding DSF "high" at the falling edge of $\overline{\text{CAS}}$. The state of the $\overline{\text{WB}}/\overline{\text{WE}}$ input at the falling edge of $\overline{\text{RAS}}$ determines whether or not the I/O data mask is enabled ($\overline{\text{WB}}/\overline{\text{WE}}$ must be "low" to enable the I/O data mask or "high" to disable mask). At the falling edge of $\overline{\text{RAS}}$, a valid row address and I/O mask data are also specified. At the falling edge of $\overline{\text{CAS}}$, the starting column address location and column address data must be provided. During a block write cycle, the 2 least significant column address locations (A0C, A1C) are internally controlled and only the 6 most significant column addresses (A2C - A7C) are latched at the falling edge of $\overline{\text{CAS}}$.

SAM PORT OPERATION

Single Register Mode

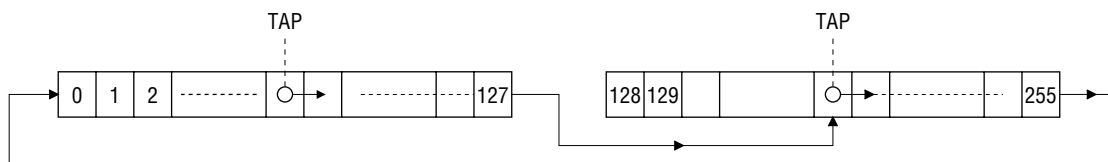
High speed serial read or write operation can be reformed through the SAM port independent of the RAM port operation, except during read/write transfer cycles. The preceding transfer operation determines the direction of data flow through the SAM port. If the preceding transfer is a read transfer, the SAM port is in the output mode. If the preceding transfer is write or pseudo write transfer, the SAM port is in the input mode. The pseudo write transfer only switches the SAM port from output mode into mode (Data is not transferred from SAM port to RAM port). Serial data can be read out of the SAM after a read transfer has been performed. The data is shifted out to the SAM starting at any of the 256 bits locations.

The TAP location corresponds to the column address selected at the falling edge of $\overline{\text{CAS}}$ during the read or write transfer cycle. The SAM registers are configured as circular data register. The data is shifted out sequentially starting from the selected TAP location to the most significant bit (255) and then wraps around to the least significant bit (0).

Split Register Mode

In split register mode, data can be shifted into or out of one half of the SAM while a split read or split write transfer is being performed on the other half of the SAM.

Conventional (non split) read, write, or pseudo write transfer cycle must precede any split read or split write transfers. The split read and write transfers will not change the SAM port mode set by preceding conventional transfer operation. In the split register mode, serial data can be shifted in or out of the split SAM registers starting from any at the 128 TAP locations, excluding the last address of each split SAM, data is shifted in or out sequentially starting from the selected TAP location to the most significant bit (127 or 255) of the first split SAM and, then the SAM pointer moves to the TAP location selected for the second split SAM to shift data in or out sequentially starting from this TAP location to the most significant bit (255 or 127) and finally wraps around to the least significant bit.



DATA TRANSFER OPERATION

The MSM518122 features two types of bidirectional data transfer capability between RAM and SAM, as shown in Figure 1 below.

- 1) Conventional (non split) transfer : 256 words by 8 bits of data can be loaded from RAM to SAM (Read transfer) or from SAM to RAM (Write transfer).
- 2) Split transfer : 128 words by 8 bits of data can be loaded from the lower/upper half of the RAM to the lower/upper half of the SAM (Split read transfer) or from the lower/upper half of SAM to the lower/upper half of RAM (Split write transfer).

The conventional transfer and split transfer modes are controlled by the DSF input signal.

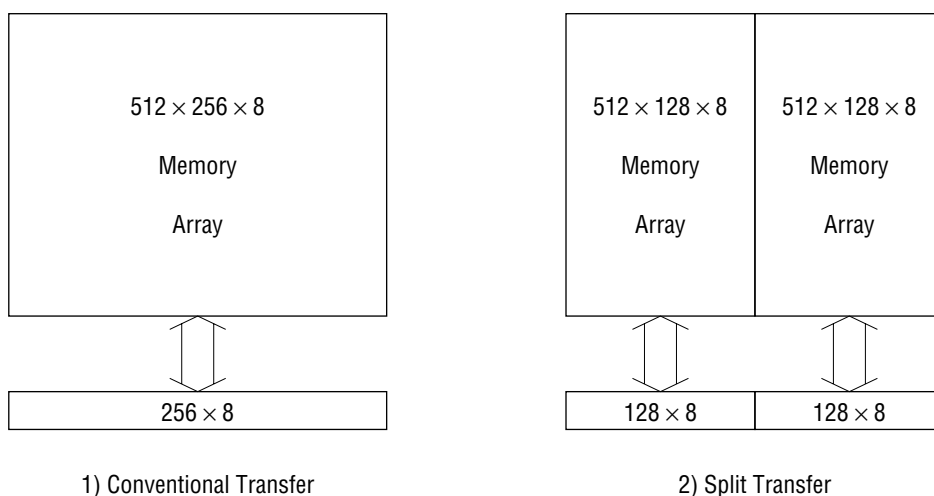


Figure 1.

The MSM518122 supports five types of transfer operation : Read transfer , Split read transfer, Write transfer, Pseudo write transfer and Split write transfer as shown in truth table. Data transfer are invoked by holding the $\overline{DT}/\overline{OE}$ signal "low" at the falling edge of $\overline{RAS}$. The type of transfer operation is determined by the state of $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{SE}$ and DSF latched at the falling edge of $\overline{RAS}$. During conventional transfer operations, the SAM port is switched from input to output mode (Read transfer) or output to input mode (Write/Pseudo write transfer) Whereas it remains unchanged during split transfer operation (Split read transfer or Split write transfer).

Read Transfer Operation

Read transfer consists of loading a selected row of data from the RAM into the SAM register. A read transfer is invoked by holding $\overline{\text{CAS}}$ "high", $\overline{\text{DT}}/\overline{\text{OE}}$ "low", $\overline{\text{WB}}/\overline{\text{WE}}$ "high" and DSF "low" at the falling edge of $\overline{\text{RAS}}$. The row address selected at the falling edge of $\overline{\text{RAS}}$ determines the RAM row to be transferred into the SAM. The transfer cycle is completed at the rising edge of $\overline{\text{DT}}/\overline{\text{OE}}$. When the transfer is completed, the SAM port is set into the output mode. In a read/real time read transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{\text{DT}}/\overline{\text{OE}}$ and this data becomes valid on the SIO lines after the specified access time t_{SCA} from the rising edge of the subsequent SC cycles. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{\text{CAS}}$. In a read transfer cycle (which is preceded by a write transfer cycle), SC clock must be held at a constant V_{IL} or V_{IH} , after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{\text{DT}}/\overline{\text{OE}}$.

In a real time read transfer cycle (which is preceded by another read transfer cycle), the previous row data appears on the SIO lines until the $\overline{\text{DT}}/\overline{\text{OE}}$ signal goes "high" and the serial access time t_{SCA} from the following serial clock is satisfied. This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed without any timing loss. To make this continuous data flow possible, the rising edge of $\overline{\text{DT}}/\overline{\text{OE}}$ must be synchronized with $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and the subsequent rising edge of SC (t_{RTH} , t_{CTH} and $t_{\text{TSL}}/t_{\text{TSD}}$ must be satisfied).

Write Transfer Operation

Write transfer cycle consists of loading the content of the SAM register into a selected row of the RAM. If the SAM data to be transferred must first be loaded through the SAM, a pseudo write transfer operation must precede the write transfer cycles. A write transfer is invoked by holding $\overline{\text{CAS}}$ "high", $\overline{\text{DT}}/\overline{\text{OE}}$ "low", $\overline{\text{WB}}/\overline{\text{WE}}$ "low", $\overline{\text{SE}}$ "low" at the falling edge of $\overline{\text{RAS}}$. This write transfer is selectively controlled per RAM I/O block by setting the mask data on the Wi/IOi lines at the falling edge of $\overline{\text{RAS}}$. The row address selected at the falling edge of $\overline{\text{RAS}}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{\text{CAS}}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SIO lines are set in the input mode so that serial data synchronized with the SC clock can be loaded. When consecutive write transfer operation are performed, new data must not be written into the serial register until the $\overline{\text{RAS}}$ cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant V_{IL} or V_{IH} during the $\overline{\text{RAS}}$ cycle. A rising edge of the SC clock is only allowed after the specified delay t_{SRD} from rising edge of the $\overline{\text{RAS}}$, at which time a new row of data can be written in the serial register.

Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other address of RAM by write transfer cycle, however, the address to write data must be the same as that of the read transfer cycle or the split read transfer cycle (row address AX8).

Pseudo Write Transfer Operation

Pseudo write transfer cycle must be performed before loading data into the serial register after a read transfer operation has been executed. The only purpose of a pseudo write transfer is to change the SAM port mode from output mode to input mode (A data transfer from SAM to RAM does not occur). After the serial register is loaded with new data, a write transfer cycle must be performed to transfer the data from SAM to RAM. A pseudo write transfer is invoked by holding $\overline{\text{CAS}}$ "high", $\overline{\text{DT}}/\overline{\text{OE}}$ "low", $\overline{\text{WB}}/\overline{\text{WE}}$ "low", $\overline{\text{SE}}$ "high" and DSF "low" at the falling edge of $\overline{\text{RAS}}$. The timing conditions are the same as the one for the write transfer cycle except for the state of SE at the falling edge of $\overline{\text{RAS}}$.

Split Data Transfer and QSF

The MSM518122 features a bidirectional split data transfer capability between the RAM and SAM. During split data transfer operation, the serial register is split into two halves which can be controlled independently. Split read or write transfer operation can be performed to or from one half of the serial register while serial data can be shifted into or out of the other half of the register. The most significant column address location (A7C) is controlled internally to determine which half of the serial register will be reloaded from the RAM. QSF is an output in which indicates which half of the serial register is in an active state. QSF changes state when the last SC clock is applied to active split SAM.

Split Read Transfer Operation

Split read transfer consists of loading 128 words by 8 bits of data from a selected row of the split RAM into the corresponding non-active split SAM register. Serial data can be shifted out from the other half of the split SAM register simultaneously. During split read transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus eliminating timing restrictions as in the case of real time read transfers. A split read transfer can be performed after a delay of t_{STS} , from the change of state of the QSF output, is satisfied. Conventional (non-split) read transfer operation must precede split read transfer cycles.

Split Write Transfer Operation

Split write transfer consists of loading 128 words by 8 bits of data from the non-active split SAM register into a selected row of the corresponding split RAM. Serial data can be shifted into the other half of the split SAM register simultaneously. During split write transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus allowing for real time transfer. A split write transfer can be performed after a delay of t_{STS} , from the change of state of the QSF output, is satisfied.

A pseudo write transfer operation must precede split write transfer. The purpose of the pseudo write transfer operation is to switch the SAM port from output mode to input mode and to set the initial TAP location prior to split write transfer operations.

Transfer Operation Without $\overline{\text{CAS}}$

During all transfer cycles, the $\overline{\text{CAS}}$ clock must be cycled, so that the column addresses are latched at the falling edge of $\overline{\text{CAS}}$, to set the SAM TAP location.

TAP Location In Split Transfer

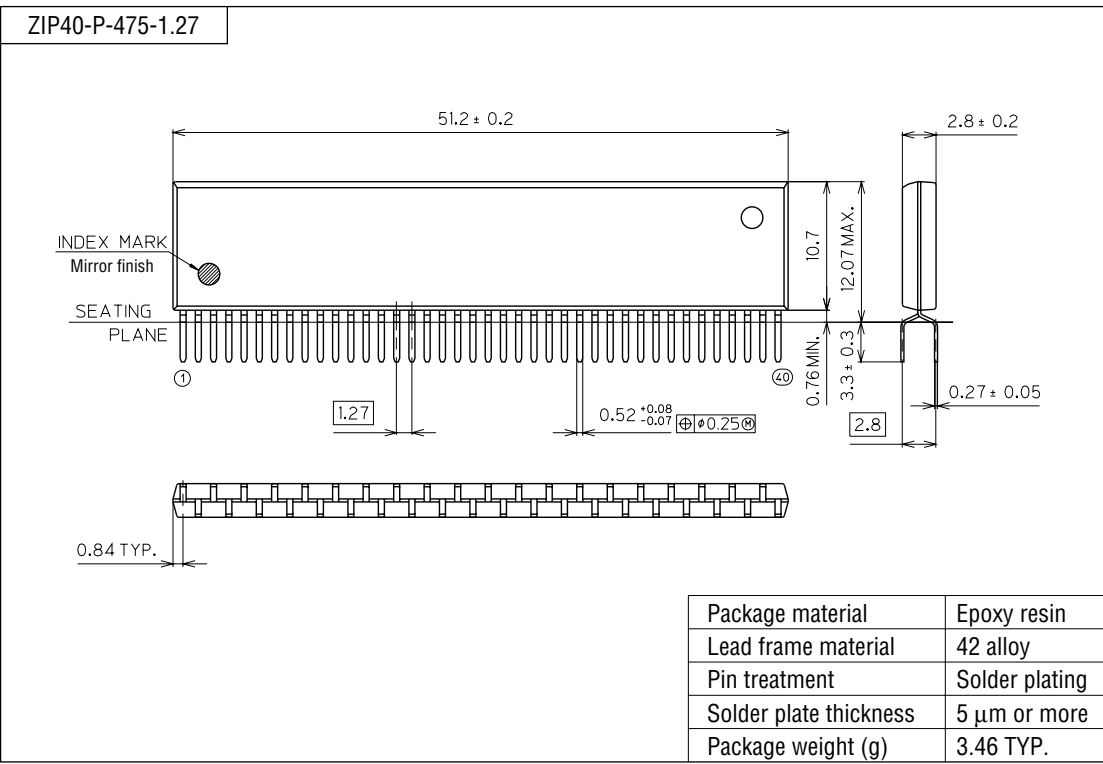
- 1) In a split transfer operation, column address A0C through A6C must be latched at the falling edge of $\overline{\text{CAS}}$ in order to set the TAP location in one of the split SAM registers. During a split transfer, column address A7C is controlled internally and therefore it is ignored internally at the falling edge of $\overline{\text{CAS}}$. During a split transfer, it is not permissible to set the last address location (A0C - A6C = 7F), in either the lower SAM or the Upper SAM, as the TAP location.

POWER-UP

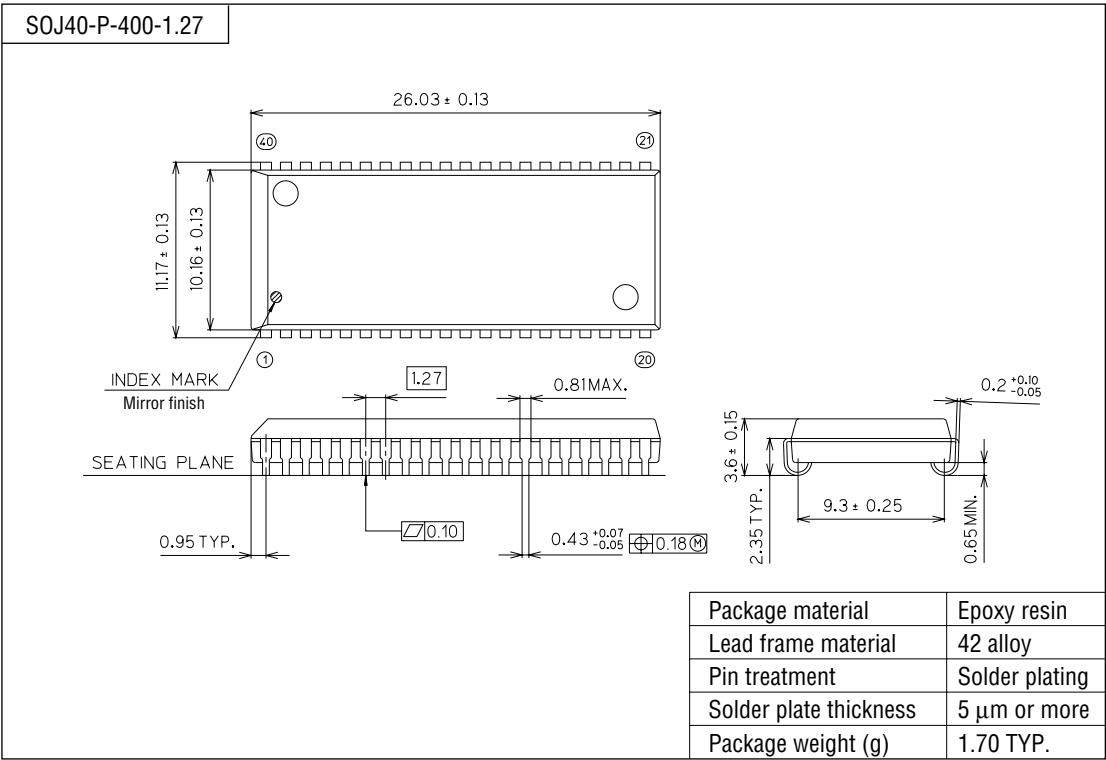
Power must be applied to the $\overline{\text{RAS}}$ and $\overline{\text{DT}}/\overline{\text{OE}}$ input signals to pull them “high” before or at the same time as the V_{CC} supply is turned on. After power-up, a pause of 200 μs minimum is required with $\overline{\text{RAS}}$ and $\overline{\text{DT}}/\overline{\text{OE}}$ held “high”. After the pause, a minimum of 8 $\overline{\text{RAS}}$ and SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{\text{DT}}/\overline{\text{OE}}$ signal must be held “high”. If the internal refresh counter is used, a minimum 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles are required instead of 8 $\overline{\text{RAS}}$ cycles.

PACKAGE DIMENSIONS

(Unit : mm)



(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).



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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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