Freescale Semiconductor
Technical Data

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RoHS

RF LDMOS Wideband Integrated Power Amplifiers

A2I08H040NR1
A2I08H040GNR1

728–960 MHz, 9 W AVG., 28 V
AIRFAST RF LDMOS WIDEBAND INTEGRATED POWER AMPLIFIERS

The A2I08H040N wideband integrated circuit is an asymmetrical Doherty designed with on–chip matching that makes it usable from 728 to 960 MHz. This multi–stage structure is rated for 26 to 32 V operation and covers all typical cellular base station modulation formats.

900 MHz

- Typical Doherty Single–Carrier W–CDMA Performance: V_{DD} = 28 Vdc, I_{DQ1A} = 25 mA, I_{DQ2A} = 105 mA, V_{GS1B} = 2.65 Vdc, V_{GS2B} = 2.3 Vdc, P_{out} = 9 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	PAE (%)	Output PAR (dB)	ACPR (dBc)
920 MHz	30.7	45.9	8.5	–36.0
940 MHz	30.6	46.7	8.4	–39.3
960 MHz	30.4	45.2	8.1	–34.5

700 MHz

- Typical Doherty Single–Carrier W–CDMA Performance: V_{DD} = 28 Vdc, I_{DQ1A} = 25 mA, I_{DQ2A} = 105 mA, V_{GS1B} = 2.65 Vdc, V_{GS2B} = 2.3 Vdc, P_{out} = 9 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	PAE (%)	Output PAR (dB)	ACPR (dBc)
728 MHz	29.1	49.1	7.9	–32.7
748 MHz	28.8	48.6	7.8	–36.4
768 MHz	28.5	46.9	7.8	–36.7

Features

- Advanced High Performance In–Package Doherty
- On–Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (1)
- Designed for Digital Predistortion Error Correction Systems

TO–270WB–15
PLASTIC
A2I08H040NR1



TO–270WBG–15
PLASTIC
A2I08H040GNR1



1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.nxp.com/RF and search for AN1977 or AN1987.

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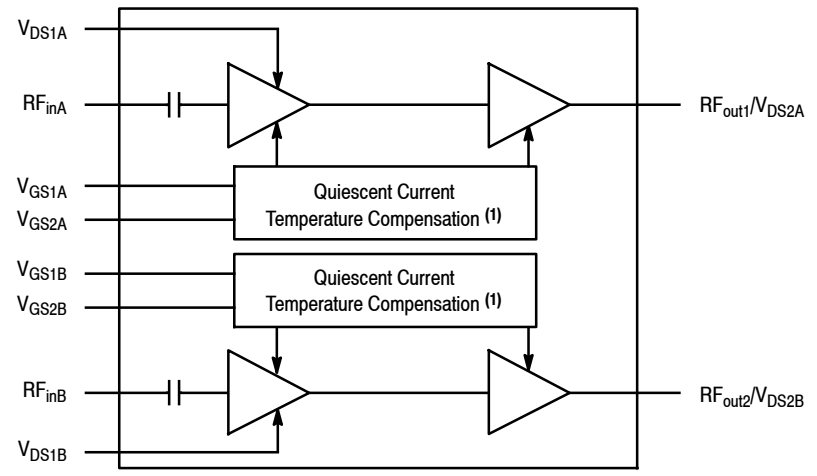
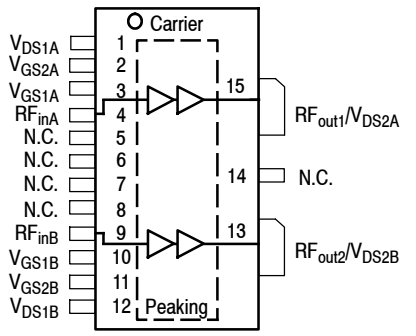


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (2,3)	T_J	–40 to +225	°C
Input Power	P_{in}	20	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (3,4)	Unit
Thermal Resistance, Junction to Case Case Temperature 73°C, 9 W, 940 MHz Stage 1, 28 Vdc, I_{DQ1A} = 24 mA, V_{GS1B} = 1.65 Vdc Stage 2, 28 Vdc, I_{DQ2A} = 145 mA, V_{GS2B} = 1.3 Vdc	$R_{\theta JC}$	 5.5 3.4	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	II

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.nxp.com/RF and search for AN1977 or AN1987.
2. Continuous use at maximum temperature will affect MTTF.
3. MTTF calculator available at http://www.nxp.com/RF/calculators.
4. Refer to AN1955*, Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Carrier Stage 1 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Carrier Stage 1 – On Characteristics					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 4 μAdc)	$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ1A} = 25 mAdc)	$V_{GS(Q)}$	—	2.8	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ1A} = 25 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	3.5	4.1	5.0	Vdc
Carrier Stage 2 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Carrier Stage 2 – On Characteristics					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 19 μAdc)	$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ2A} = 105 mAdc)	$V_{GS(Q)}$	—	2.8	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ2A} = 105 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	3.5	4.1	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 190 mAdc)	$V_{DS(on)}$	0.1	0.2	2.5	Vdc

1. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Peaking Stage 1 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Peaking Stage 1 – On Characteristics (1)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 6 μAdc)	$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Peaking Stage 2 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Peaking Stage 2 – On Characteristics (1)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 34 μAdc)	$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 340 mAdc)	$V_{DS(on)}$	0.1	0.2	2.5	Vdc

1. Each side of device measured separately.

(continued)

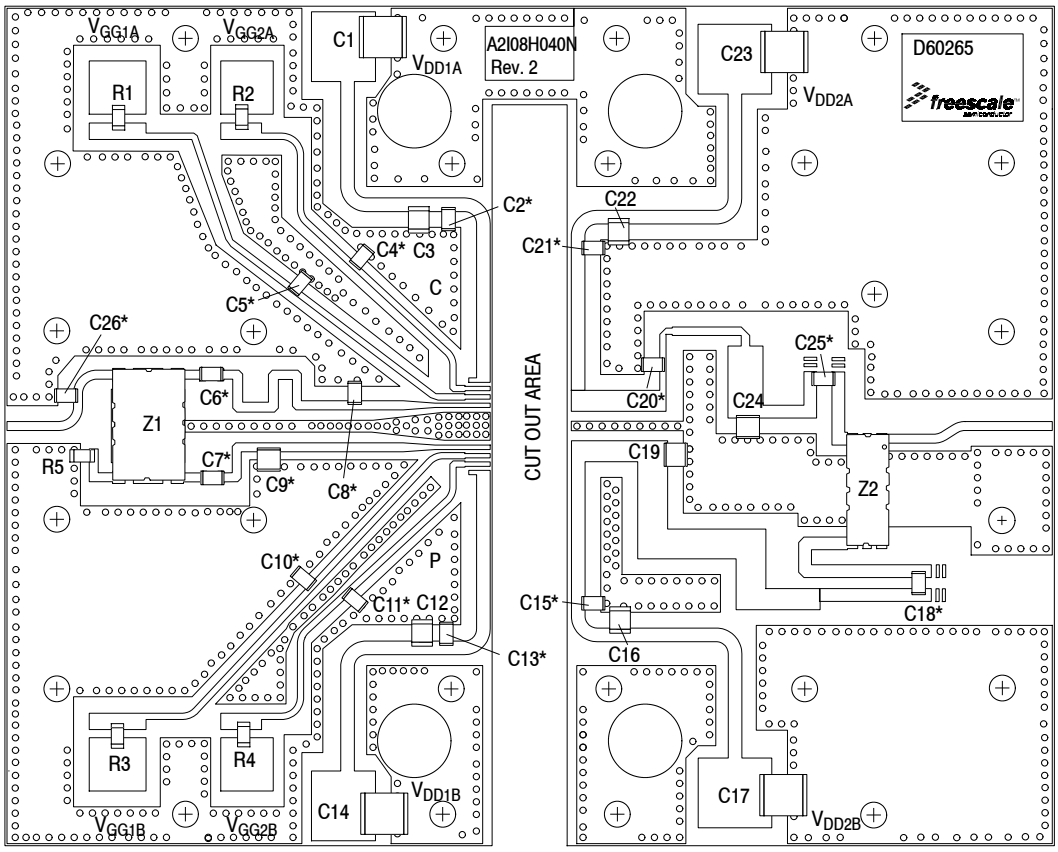
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2,3) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1A} = 25 mA, I_{DQ2A} = 105 mA, V_{GS1B} = 2.65 Vdc, V_{GS2B} = 2.3 Vdc, P_{out} = 9 W Avg., f = 920 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	27.0	30.7	33.0	dB
Power Added Efficiency	PAE	42.0	45.9	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.3	8.5	—	dB
Adjacent Channel Power Ratio	ACPR	—	–36.0	–30.0	dBc
P_{out} @ 3 dB Compression Point, CW	P3dB	42.2	51.8	—	W
Load Mismatch (2) (In Freescale Doherty Test Fixture, 50 ohm system) I_{DQ1A} = 25 mA, I_{DQ2A} = 10.5 mA, V_{GS1B} = 2.65 Vdc, V_{GS2B} = 2.3 Vdc, f = 940 MHz					
VSWR 10:1 at 32 Vdc, 56 W CW Output Power (3 dB Input Overdrive from 48 W CW Rated Power)	No Device Degradation				
Typical Performance (2) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1A} = 25 mA, I_{DQ2A} = 105 mA, V_{GS1B} = 2.65 Vdc, V_{GS2B} = 2.3 Vdc, 920–960 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	46.8	—	W
P_{out} @ 3 dB Compression Point (4)	P3dB	—	56	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 920–960 MHz frequency range.)	Φ	—	–15.9	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	70	—	MHz
Quiescent Current Accuracy over Temperature (5) with 2 kΩ Gate Feed Resistors (–30 to 85°C) Stage 1 with 2 kΩ Gate Feed Resistors (–30 to 85°C) Stage 2	ΔI_{QT}	 — —	 1.1 1.9	 — —	%
Gain Flatness in 40 MHz Bandwidth @ P_{out} = 9 W Avg.	G_F	—	0.3	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.029	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.006	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2I08H040NR1	R1 Suffix = 500 Units, 44 mm Tape Width, 13-inch Reel	TO-270WB-15
A2I08H040GNR1		TO-270WBG-15

1. Part internally input matched.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.
4. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
5. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.nxp.com/RF and search for AN1977 or AN1987.



*C2, C4, C5, C6, C7, C8, C9, C10, C11, C13, C15, C18, C20, C21, C25, and C26 are mounted vertically.

Figure 3. A2I08H040NR1 Test Circuit Component Layout

Table 7. A2I08H040NR1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C14, C17, C23	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C2, C4, C5, C6, C7, C10, C11, C13, C15, C18, C21, C25	47 pF Chip Capacitors	ATC100B470JT500XT	ATC
C3, C12, C16, C22	2.2 μF Chip Capacitors	C3225X7R2A225M230AB	TDK
C8	1.8 pF Chip Capacitor	ATC100B1R8BT500XT	ATC
C9	0.5 pF Chip Capacitor	ATC00B0R5BT500XT	ATC
C19	9.1 pF Chip Capacitor	ATC100B9R1BT500XT	ATC
C20	10 pF Chip Capacitor	ATC100B100GT500XT	ATC
C24	1.1 pF Chip Capacitor	ATC100B1R1BT500XT	ATC
C26	0.7 pF Chip Capacitor	ATC100B0R7BT500XT	ATC
R1, R2, R3, R4	2 kΩ, 1/4 W Chip Resistors	WCR1206-2K0FI	Welwyn
R5	50 Ω, 8 W Termination	C8A50Z4A	Anaren
Z1	800–1000 MHz Band, 5 dB Directional Coupler	XC0900A-05S	Anaren
Z2	925–960 MHz Band, Doherty Combiner	X3DC09E2S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D60265	MTL

TYPICAL CHARACTERISTICS

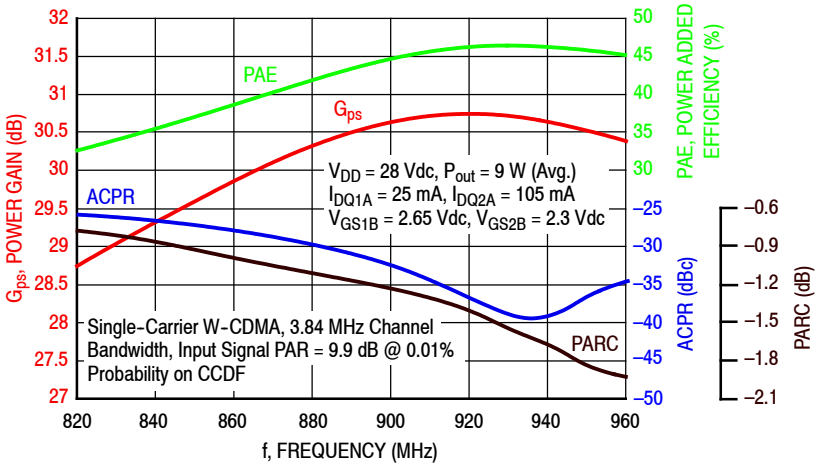


Figure 4. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 9 Watts Avg.

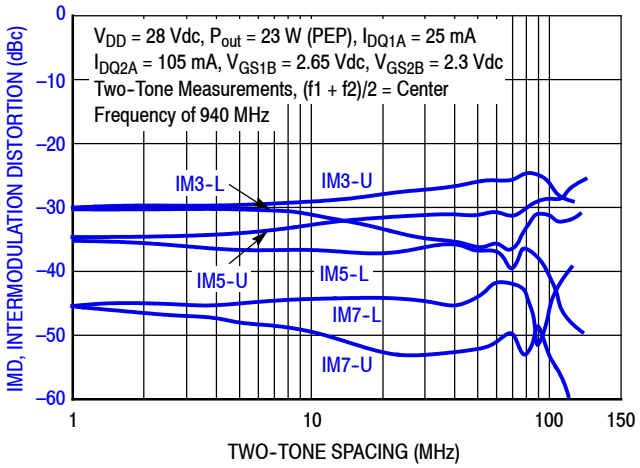


Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing

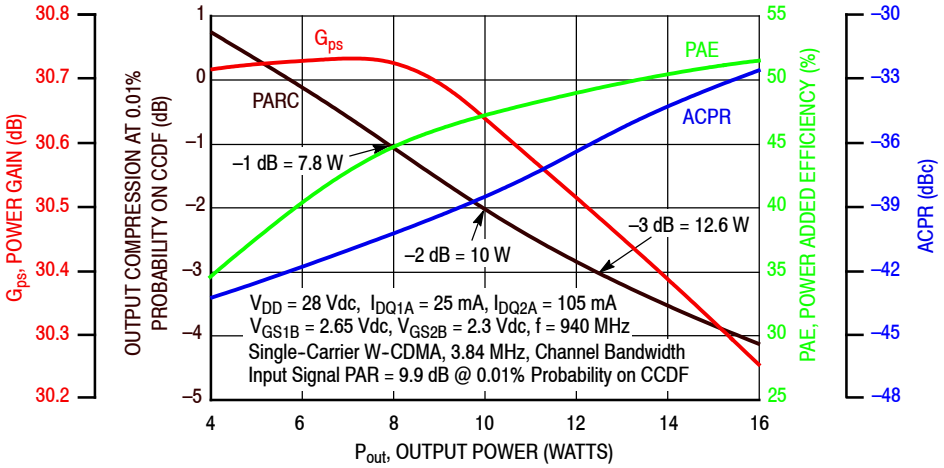


Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

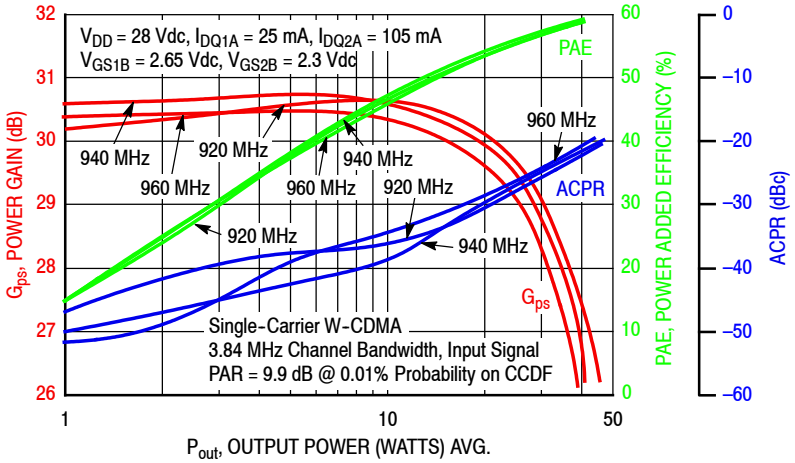


Figure 7. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

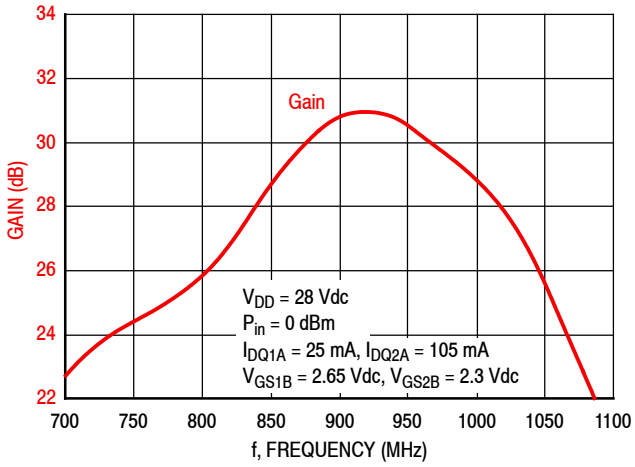


Figure 8. Broadband Frequency Response

Table 8. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ1A} = 25 mA, I_{DQ2A} = 100 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	51.1 – j12.0	58.6 + j15.3	8.16 + j5.47	32.9	43.4	22	58.3	–5
940	54.9 – j7.00	62.0 + j11.7	8.70 + j5.35	32.8	43.4	22	58.6	–5
960	57.0 – j4.01	63.0 + j7.73	9.38 + j4.95	32.7	43.3	21	58.1	–6

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	51.1 – j12.0	58.7 + j12.7	8.80 + j4.28	30.6	44.1	26	58.5	–6
940	54.9 – j7.00	61.6 + j9.15	9.44 + j4.22	30.6	44.1	25	58.9	–7
960	57.0 – j4.01	62.1 + j5.47	9.96 + j3.98	30.5	44.0	25	58.5	–8

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 9. Carrier Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ1A} = 25 mA, I_{DQ2A} = 100 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	51.1 – j12.0	63.7 + j16.2	9.09 + j13.8	35.4	41.2	13	70.1	–9
940	54.9 – j7.00	67.8 + j12.0	8.74 + j14.9	35.5	40.8	12	70.3	–11
960	57.0 – j4.01	67.6 + j7.31	9.78 + j14.6	35.2	41.0	13	69.6	–10

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	51.1 – j12.0	63.5 + j14.8	7.87 + j13.6	33.5	41.7	15	71.3	–15
940	54.9 – j7.00	66.4 + j10.4	8.45 + j14.0	33.4	41.7	15	71.2	–15
960	57.0 – j4.01	66.2 + j5.95	9.24 + j13.7	33.1	41.9	15	70.5	–14

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

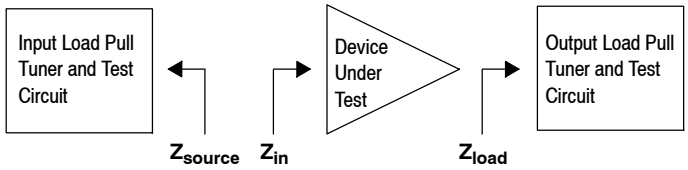


Table 10. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ1B} = 30 mA, V_{GS2B} = 2.3 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	38.7 – j2.27	35.4 + j2.30	4.19 + j1.68	30.0	45.5	36	58.6	–16
940	39.2 – j5.06	36.2 + j0.98	4.27 + j1.85	29.9	45.3	34	59.6	–17
960	38.0 + j0.79	36.1 – j1.16	4.53 + j1.73	29.7	45.1	32	59.4	–18

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	38.7 – j2.27	36.5 + j0.74	4.35 + j1.68	28.0	45.8	38	60.0	–21
940	39.2 – j5.06	37.3 – j0.71	4.51 + j1.85	27.9	45.6	36	61.0	–21
960	38.0 + j0.79	37.3 – j2.62	4.53 + j1.73	27.7	45.3	34	60.2	–20

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

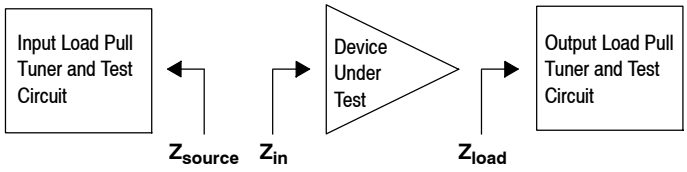
Table 11. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ1B} = 30 mA, V_{GS2B} = 2.3 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	38.7 – j2.27	37.7 + j3.57	4.26 + j6.49	30.9	43.0	20	69.9	–19
940	39.2 – j5.06	38.6 + j1.50	4.13 + j6.62	30.8	42.7	19	70.7	–21
960	38.0 + j0.79	38.0 – j0.71	4.10 + j6.31	30.6	42.7	19	69.5	–21

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	38.7 – j2.27	36.8 + j1.64	4.18 + j5.42	29.0	44.3	27	69.4	–28
940	39.2 – j5.06	37.2 – j0.30	4.20 + j5.43	28.8	44.1	26	69.7	–29
960	38.0 + j0.79	36.6 – j2.33	4.10 + j5.58	28.6	43.7	23	68.4	–30

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER LOAD PULL CONTOURS — 940 MHz

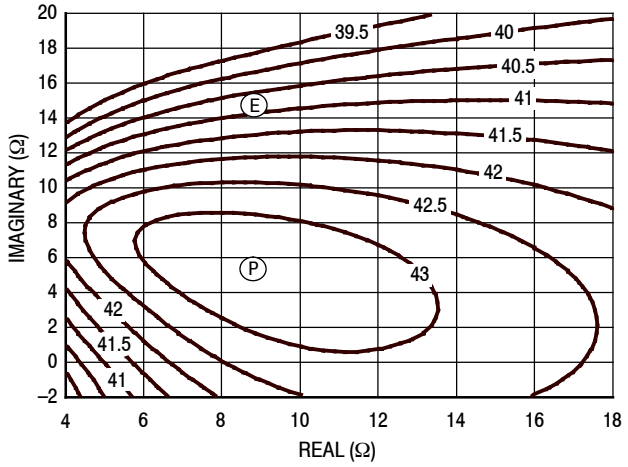


Figure 9. P1dB Load Pull Output Power Contours (dBm)

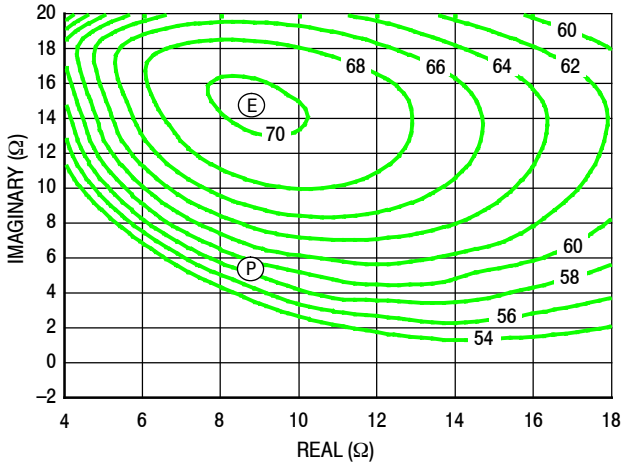


Figure 10. P1dB Load Pull Efficiency Contours (%)

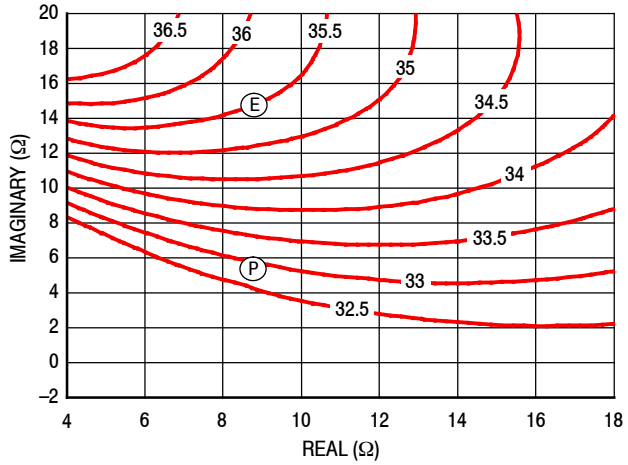


Figure 11. P1dB Load Pull Gain Contours (dB)

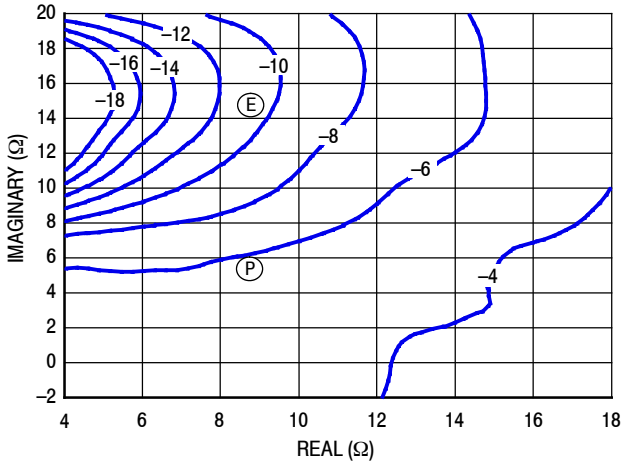


Figure 12. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER LOAD PULL CONTOURS — 940 MHz

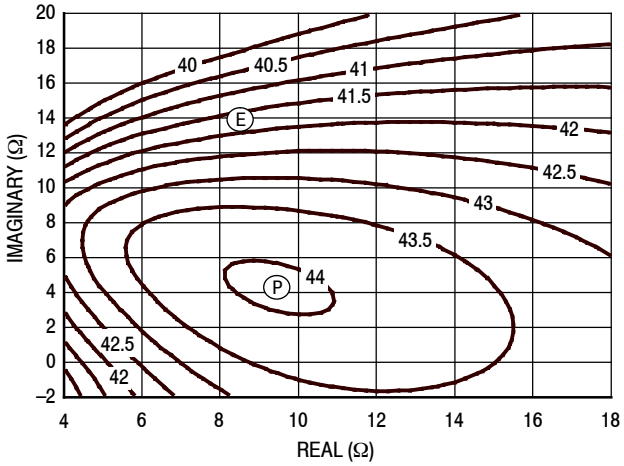


Figure 13. P3dB Load Pull Output Power Contours (dBm)

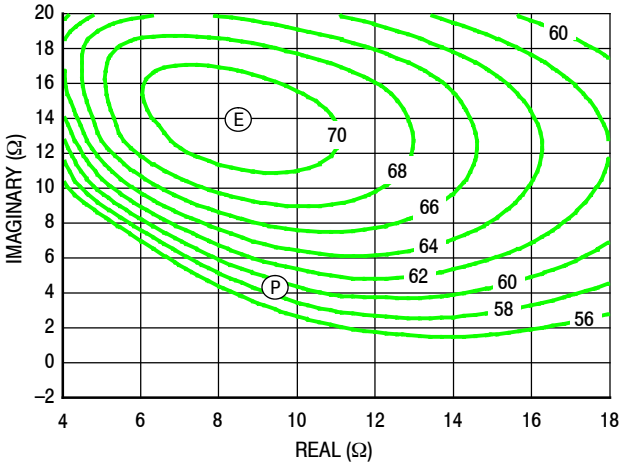


Figure 14. P3dB Load Pull Efficiency Contours (%)

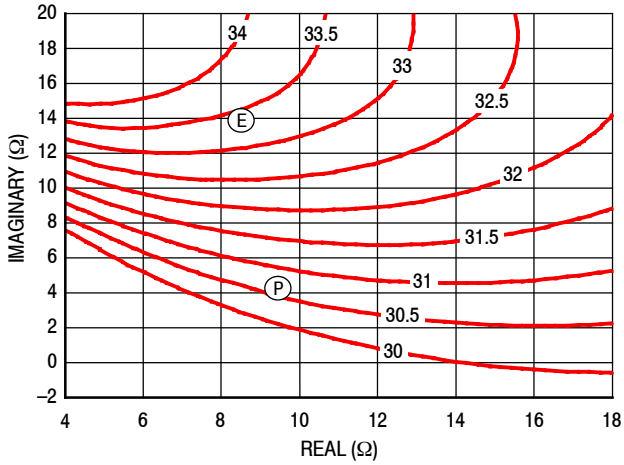


Figure 15. P3dB Load Pull Gain Contours (dB)

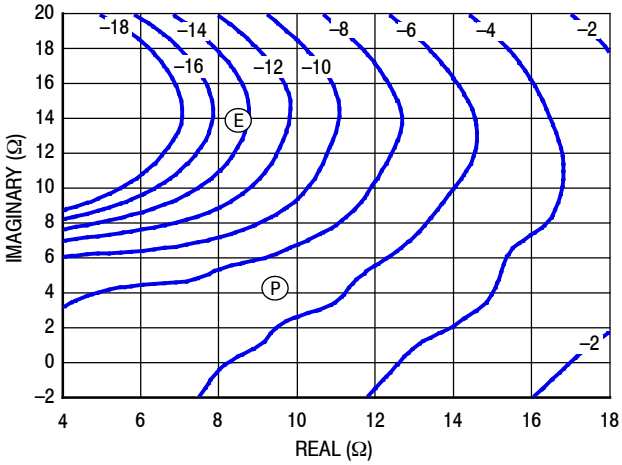


Figure 16. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB – TYPICAL PEAKING LOAD PULL CONTOURS — 940 MHz

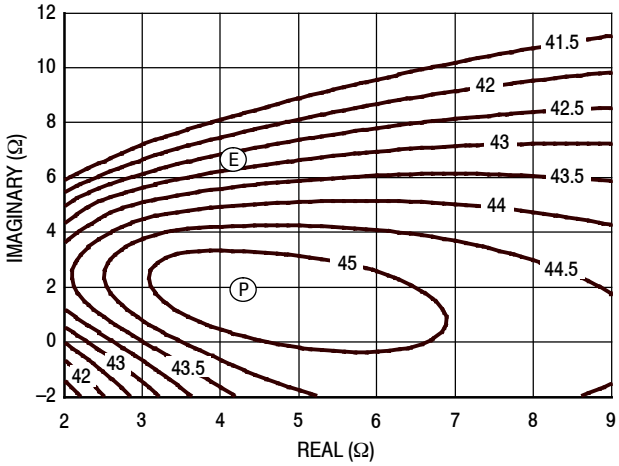


Figure 17. P1dB Load Pull Output Power Contours (dBm)

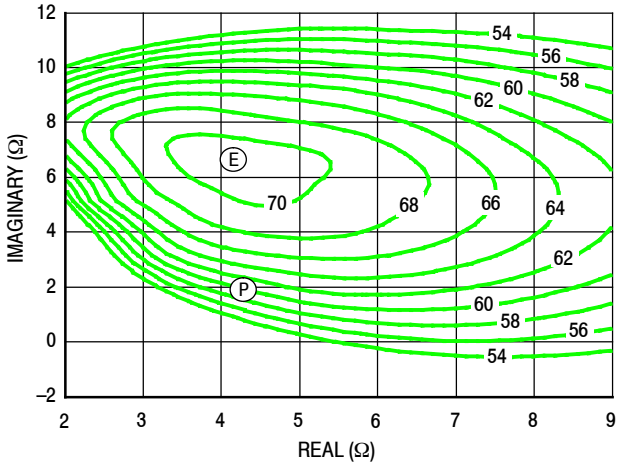


Figure 18. P1dB Load Pull Efficiency Contours (%)

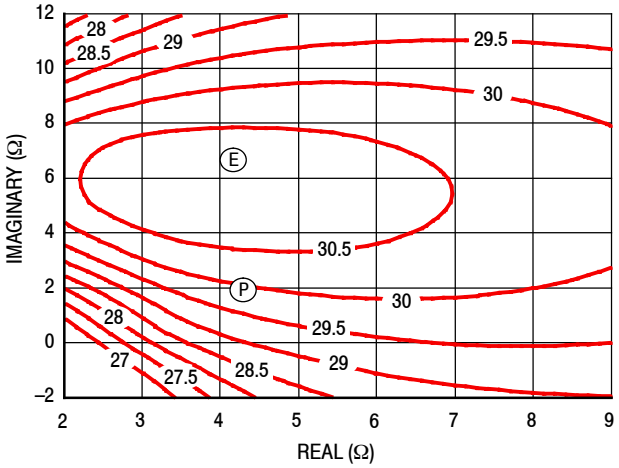


Figure 19. P1dB Load Pull Gain Contours (dB)

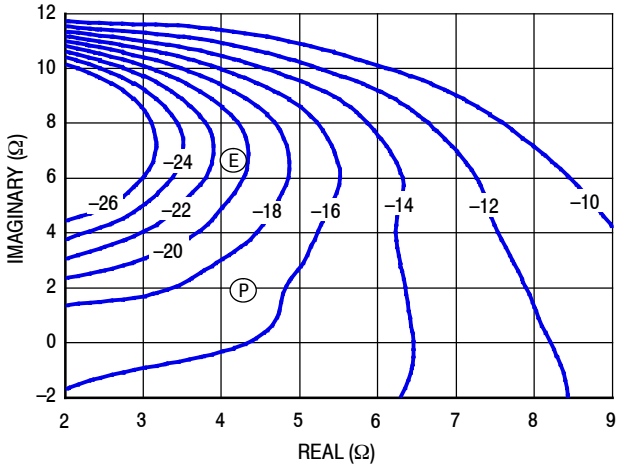


Figure 20. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL PEAKING LOAD PULL CONTOURS — 940 MHz

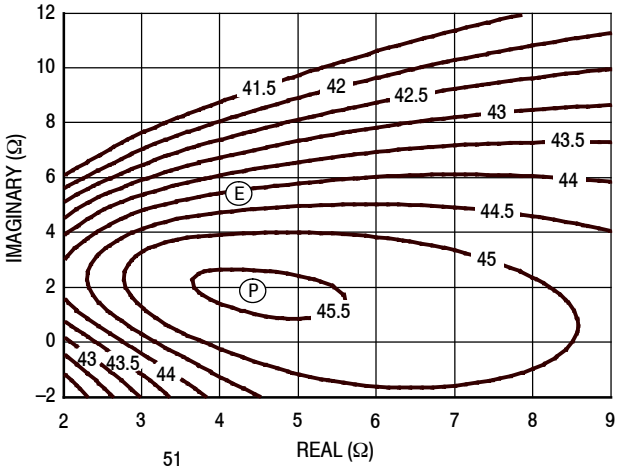


Figure 21. P3dB Load Pull Output Power Contours (dBm)

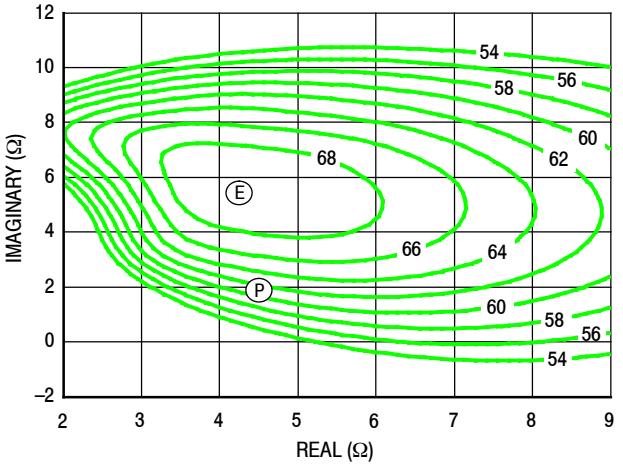


Figure 22. P3dB Load Pull Efficiency Contours (%)

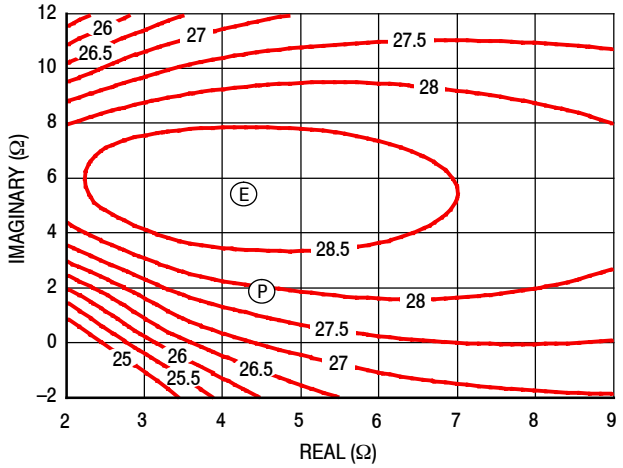


Figure 23. P3dB Load Pull Gain Contours (dB)

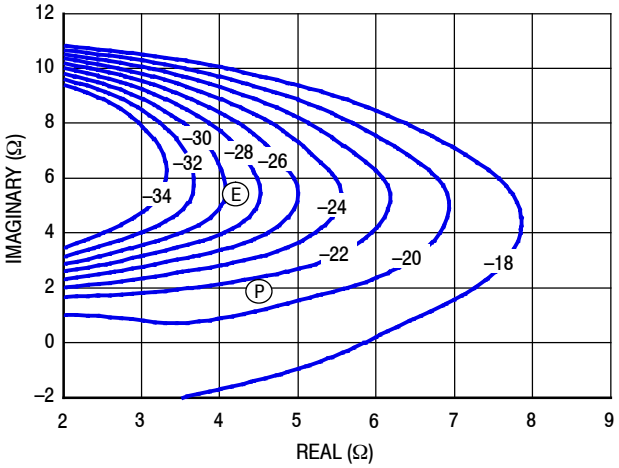


Figure 24. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

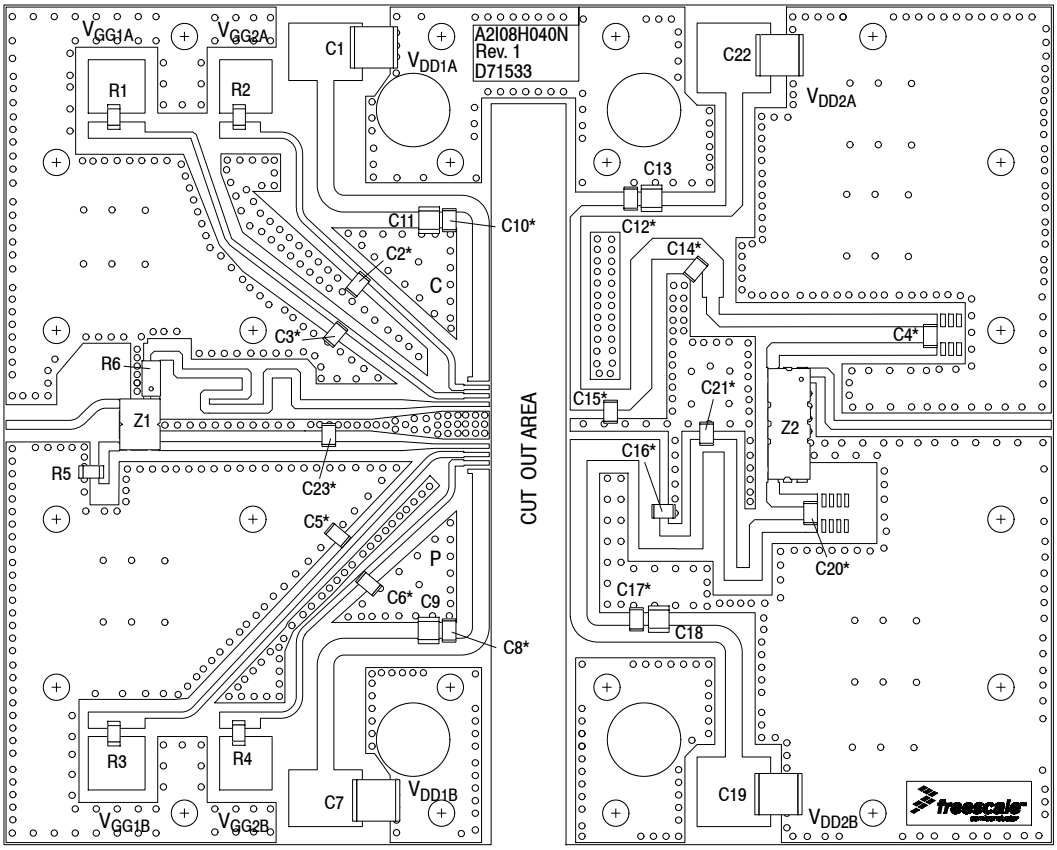
Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power



*C2, C3, C4, C5, C6, C8, C10, C12, C14, C15, C16, C17, C20, C21, and C23 are mounted vertically.

Figure 25. A2I08H040NR1 Production Test Circuit Component Layout — 728–768 MHz

Table 12. A2I08H040NR1 Production Test Circuit Component Designations and Values — 728–768 MHz

Part	Description	Part Number	Manufacturer
C1, C7, C19, C22	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C2, C3, C4, C5, C6, C8, C10, C12, C17, C20	68 pF Chip Capacitors	ATC100B680JT500XT	ATC
C9, C11, C13, C18	2.2 μF Chip Capacitors	C3225X7R2A225M230AB	TDK
C14	5.6 pF Chip Capacitor	ATC100B5R6BT500XT	ATC
C15, C21	4.7 pF Chip Capacitors	ATC100B4R7BT500XT	ATC
C16	12 pF Chip Capacitor	ATC100B120GT500XT	ATC
C23	3.6 pF Chip Capacitor	ATC100B3R6BT500XT	ATC
R1, R2, R3, R4	2 kΩ, 1/4 W Chip Resistors	WCR1206-2K0FI	Welwyn
R5	50 Ω, 8 W Termination	C8A50Z4A	Anaren
R6	3 dB, 10 W Chip Attenuator	D10AA3Z4	Anaren
Z1	600–900 MHz Band, 90°, 4 dB Directional Coupler	X3C07P1-04S	Anaren
Z2	728–768 MHz Band, Doherty Combiner	X3DC07E2S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D71533	MTL

TYPICAL CHARACTERISTICS

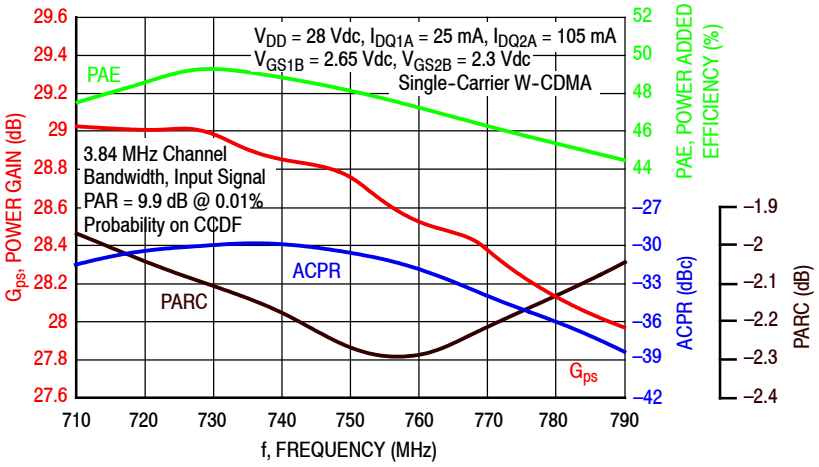


Figure 26. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 9 Watts Avg.

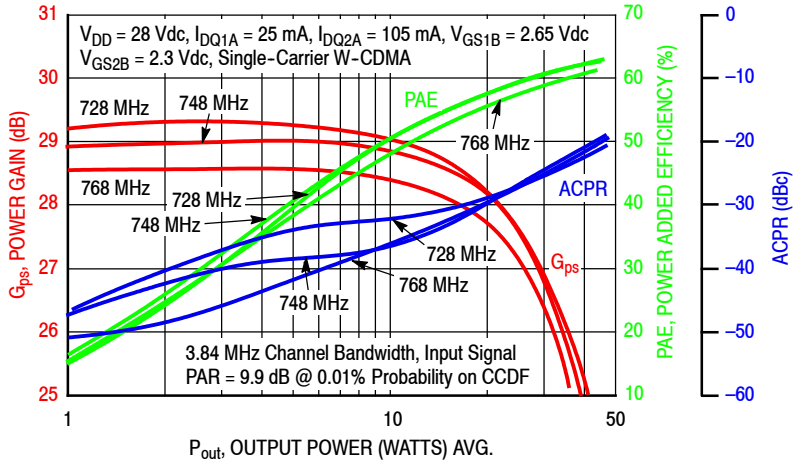


Figure 27. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

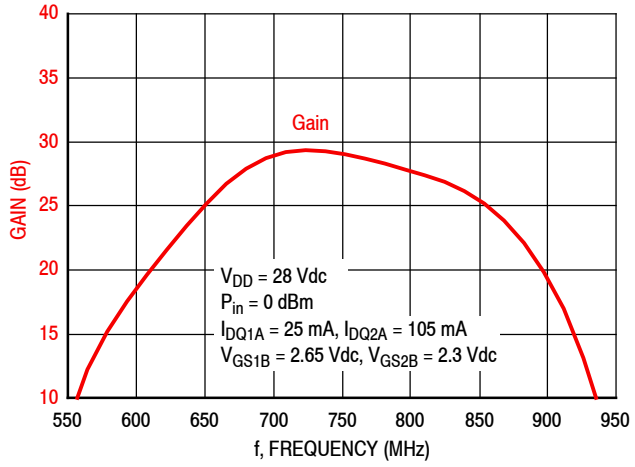


Figure 28. Broadband Frequency Response

Table 13. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ1A} = 25 mA, I_{DQ2A} = 100 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
728	24.7 – j1.50	25.7 + j0.73	4.92 + j5.15	32.2	41.7	15	42.2	–7
748	23.8 – j4.10	26.6 + j4.02	4.92 + j4.60	31.8	41.6	15	40.3	–3
768	24.1 – j7.86	27.0 + j8.40	6.79 + j6.25	33.2	42.6	18	55.2	–2

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
728	24.7 – j1.50	26.7 + j1.45	5.35 + j4.77	30.3	42.9	19	47.1	–9
748	23.8 – j4.10	27.6 + j4.63	5.63 + j4.20	30.0	42.9	19	46.6	–5
768	24.1 – j7.86	28.4 + j8.44	7.45 + j5.33	31.0	43.6	23	59.0	–4

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 14. Carrier Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ1A} = 25 mA, I_{DQ2A} = 100 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
728	24.7 – j1.50	28.1 + j7.23	19.7 + j26.7	35.4	37.8	6	52.4	–5
748	23.8 – j4.10	24.2 + j9.57	8.94 + j17.9	37.7	38.2	7	59.8	–2
768	24.1 – j7.86	26.2 + j11.9	8.70 + j14.0	36.4	40.7	12	68.9	–4

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
728	24.7 – j1.50	27.5 + j6.67	16.6 + j22.7	34.3	39.6	9	65.1	–1
748	23.8 – j4.10	26.0 + j10.0	9.44 + j18.6	35.7	39.6	9	68.8	–5
768	24.1 – j7.86	27.7 + j11.6	8.98 + j13.7	34.3	41.6	15	72.8	–7

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

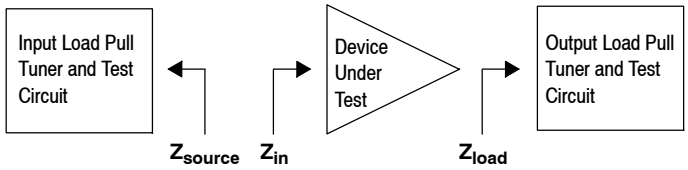


Table 15. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ1B} = 30 mA, V_{GS2B} = 2.3 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
728	22.4 + j1.93	20.3 + j0.94	4.44 + j3.21	29.3	45.0	32	57.7	–5
748	22.1 – j0.64	21.0 + j2.44	3.99 + j2.31	28.8	45.3	34	54.1	–5
768	22.4 – j1.08	21.9 + j4.31	4.32 + j2.46	29.4	45.6	36	58.4	–5

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
728	22.4 + j1.93	21.2 + j0.96	4.74 + j2.36	27.0	46.0	40	58.3	–9
748	22.1 – j0.64	22.0 + j2.51	4.58 + j2.21	26.9	46.2	42	58.8	–10
768	22.4 – j1.08	23.2 + j4.05	4.52 + j1.59	27.0	46.3	43	57.4	–9

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

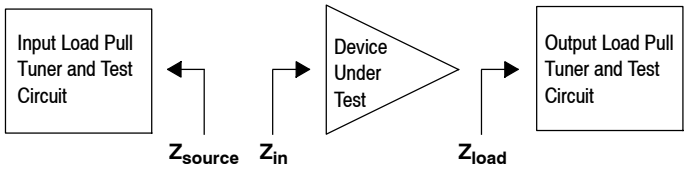
Table 16. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ1B} = 30 mA, V_{GS2B} = 2.3 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
728	22.4 + j1.93	20.1 + j1.53	5.25 + j5.68	30.0	43.9	25	63.8	–8
748	22.1 – j0.64	20.8 + j4.24	5.21 + j9.70	30.2	42.0	16	69.8	–11
768	22.4 – j1.08	21.6 + j5.73	4.94 + j7.47	30.8	43.5	22	71.9	–11

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
728	22.4 + j1.93	20.9 + j1.52	5.89 + j5.15	27.9	45.0	32	66.2	–11
748	22.1 – j0.64	21.6 + j3.60	6.00 + j7.89	28.2	43.9	25	69.5	–13
768	22.4 – j1.08	22.7 + j5.43	5.81 + j7.57	28.6	44.1	26	72.9	–15

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER LOAD PULL CONTOURS — 748 MHz

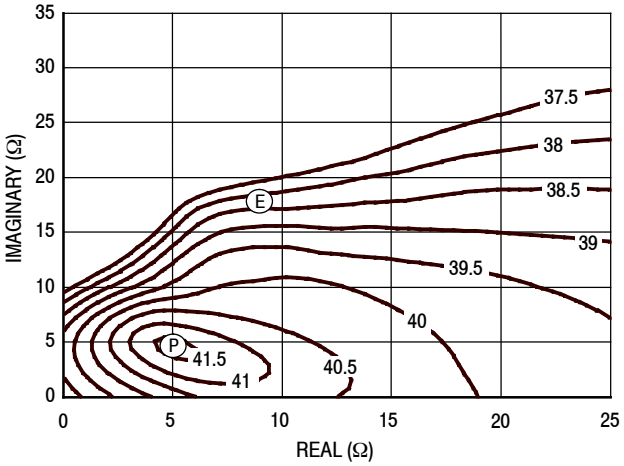


Figure 29. P1dB Load Pull Output Power Contours (dBm)

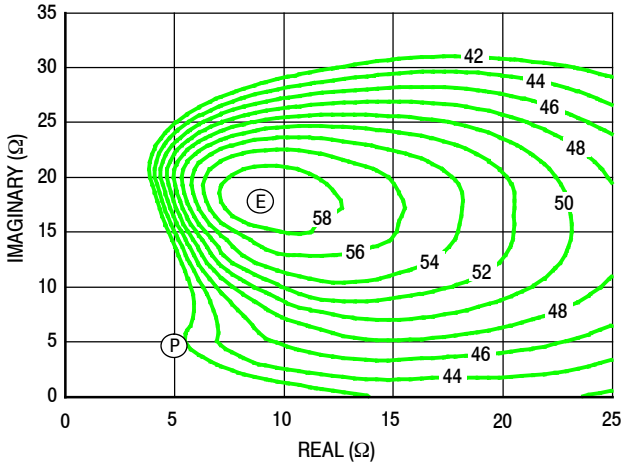


Figure 30. P1dB Load Pull Efficiency Contours (%)

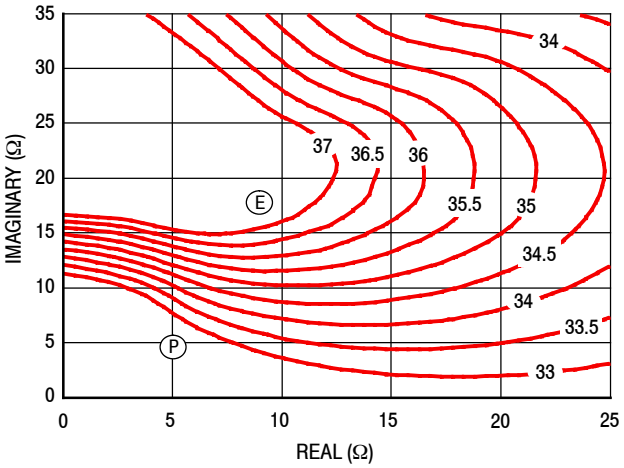


Figure 31. P1dB Load Pull Gain Contours (dB)

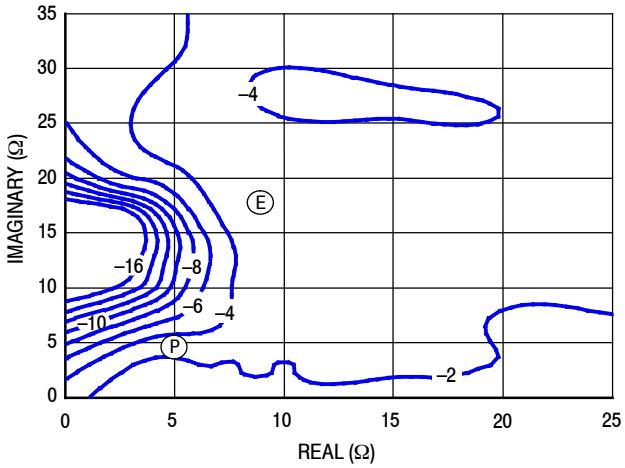


Figure 32. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER LOAD PULL CONTOURS — 748 MHz

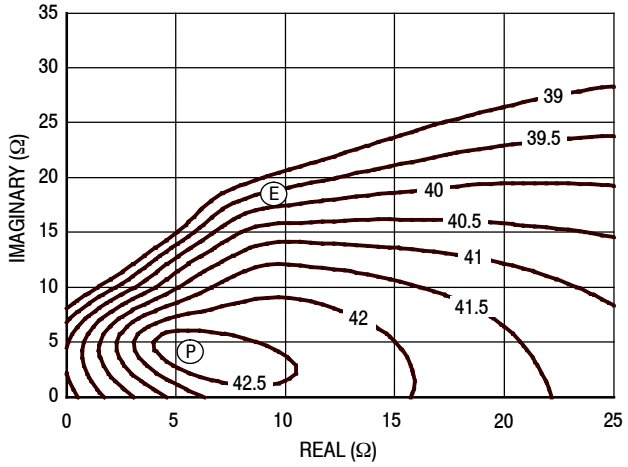


Figure 33. P3dB Load Pull Output Power Contours (dBm)

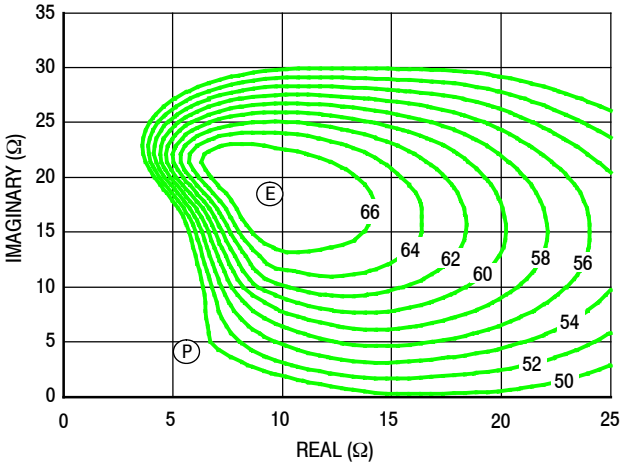


Figure 34. P3dB Load Pull Efficiency Contours (%)

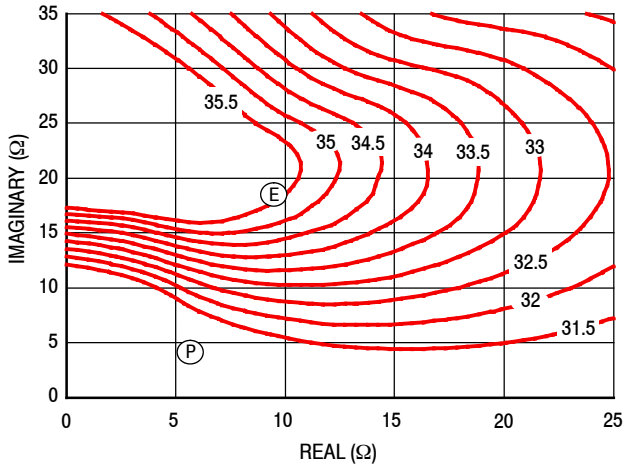


Figure 35. P3dB Load Pull Gain Contours (dB)

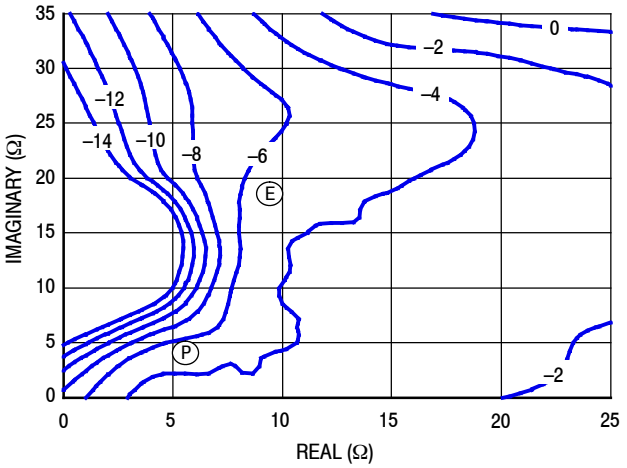


Figure 36. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB – TYPICAL PEAKING LOAD PULL CONTOURS — 748 MHz

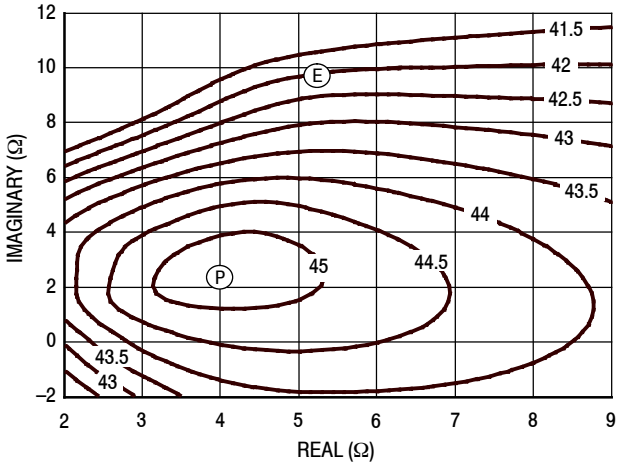


Figure 37. P1dB Load Pull Output Power Contours (dBm)

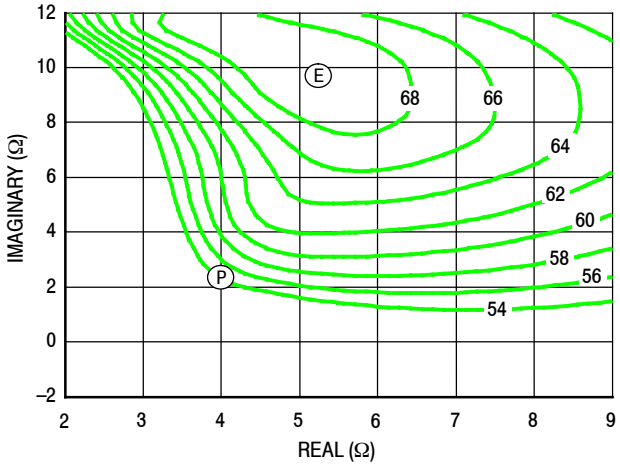


Figure 38. P1dB Load Pull Efficiency Contours (%)

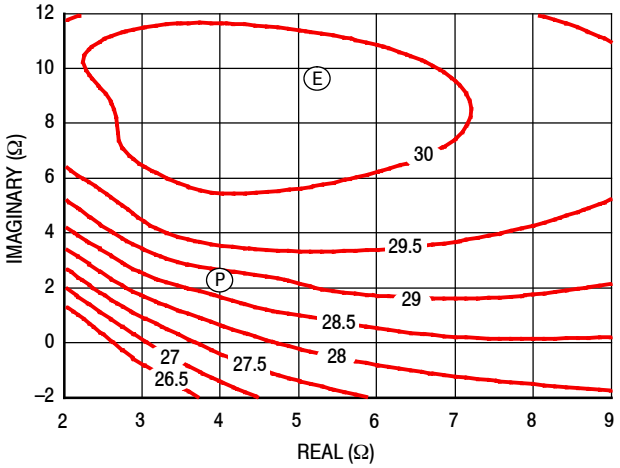


Figure 39. P1dB Load Pull Gain Contours (dB)

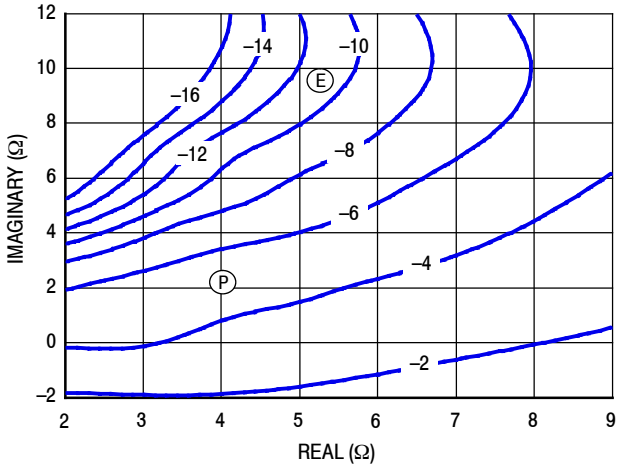


Figure 40. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL PEAKING LOAD PULL CONTOURS — 748 MHz

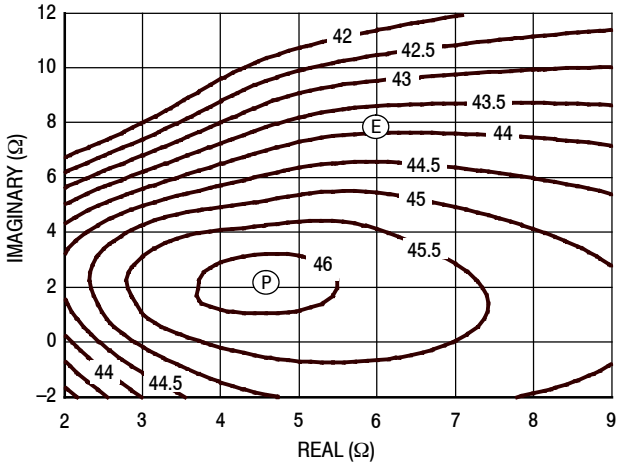


Figure 41. P3dB Load Pull Output Power Contours (dBm)

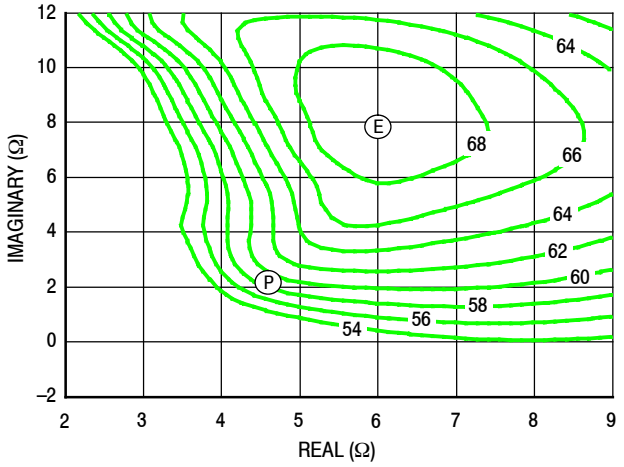


Figure 42. P3dB Load Pull Efficiency Contours (%)

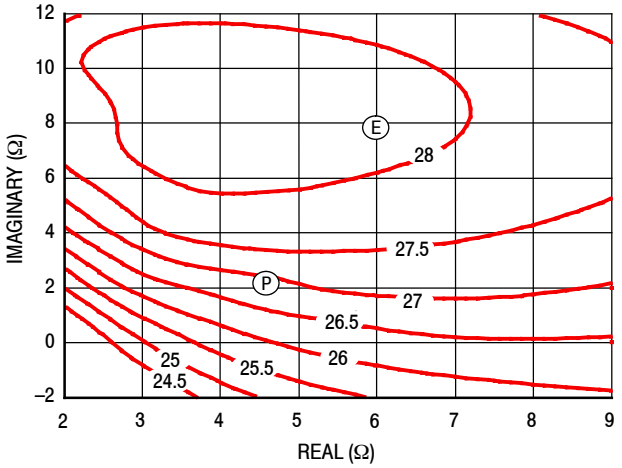


Figure 43. P3dB Load Pull Gain Contours (dB)

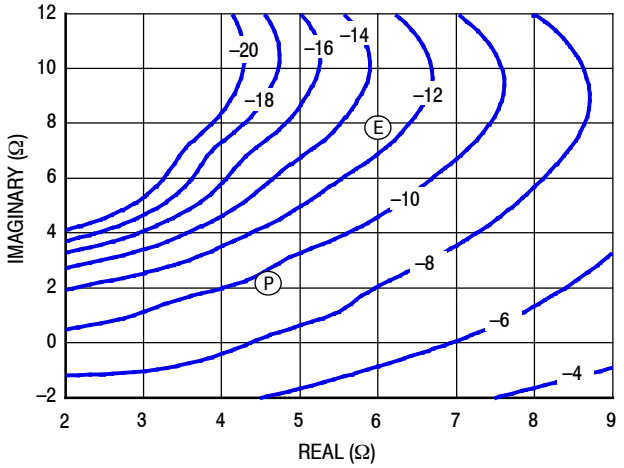


Figure 44. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

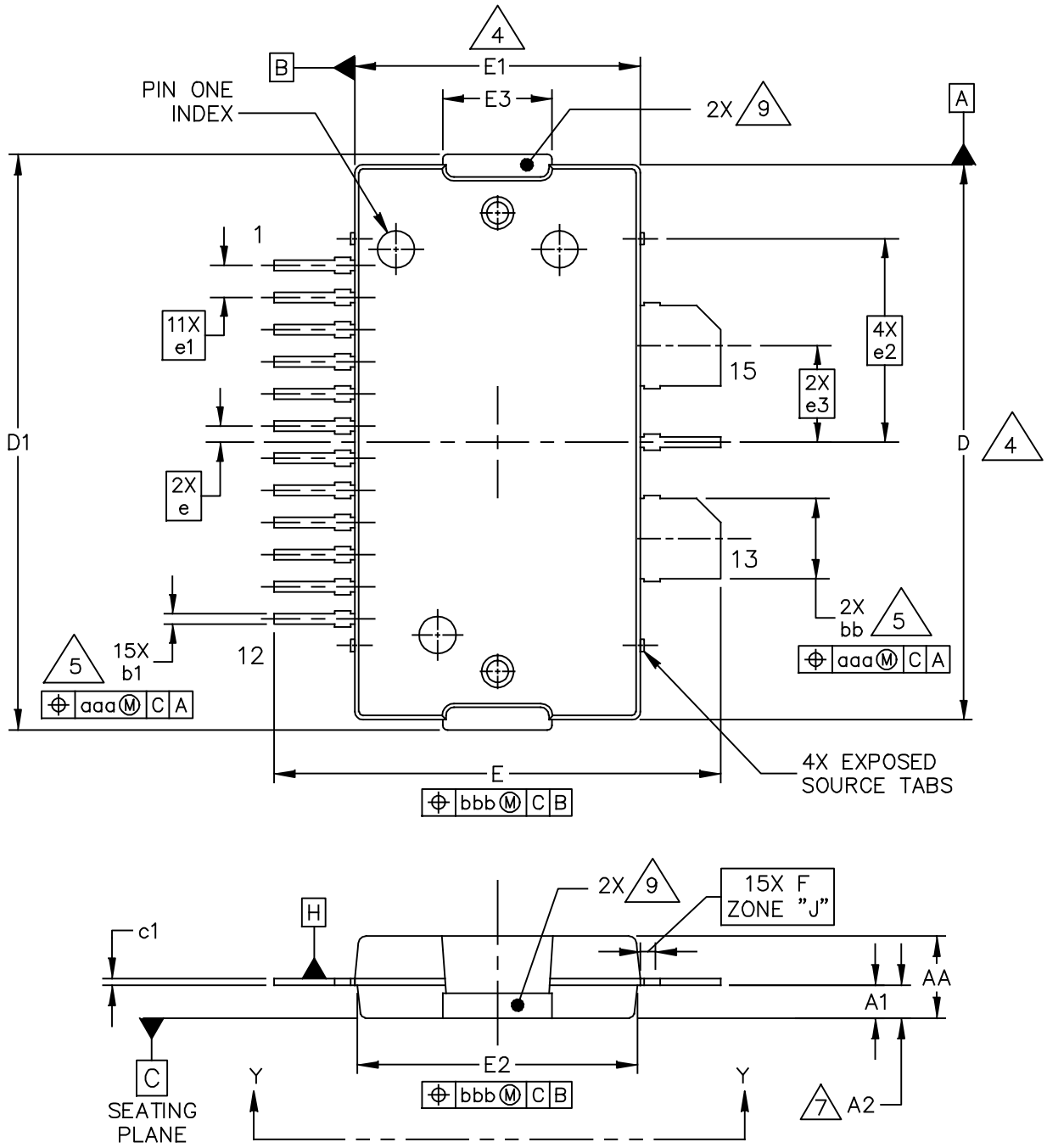
Gain

Drain Efficiency

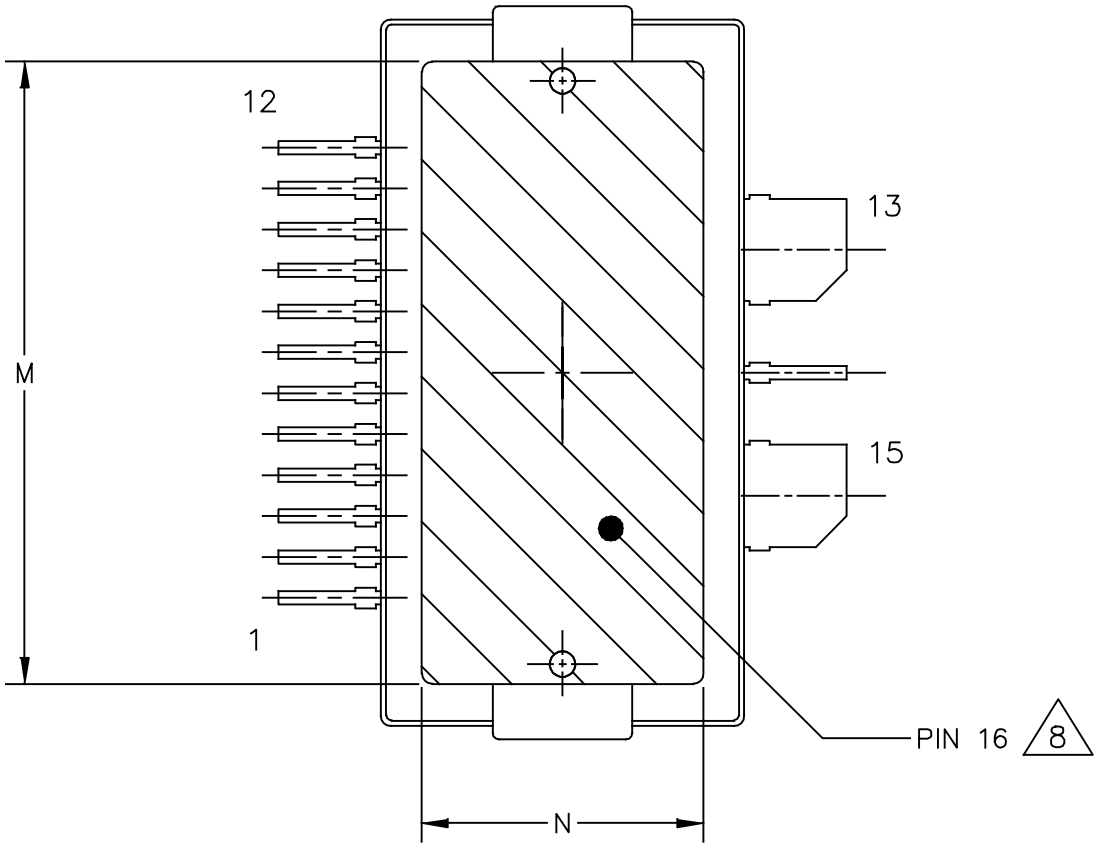
Linearity

Output Power

PACKAGE DIMENSIONS



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VIEW Y–Y

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NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	M	.600	----	15.24	----
A1	.039	.043	0.99	1.09	N	.270	----	6.86	----
A2	.040	.042	1.02	1.07	bb	.097	.103	2.46	2.62
D	.688	.692	17.48	17.58	b1	.010	.016	0.25	0.41
D1	.712	.720	18.08	18.29	c1	.007	.011	0.18	0.28
E	.551	.559	14.00	14.20	e	.020 BSC		0.51 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.253 INFO ONLY		6.43 INFO ONLY	
E3	.132	.140	3.35	3.56	e3	.120 BSC		3.05 BSC	
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
					bbb	.008		0.20	

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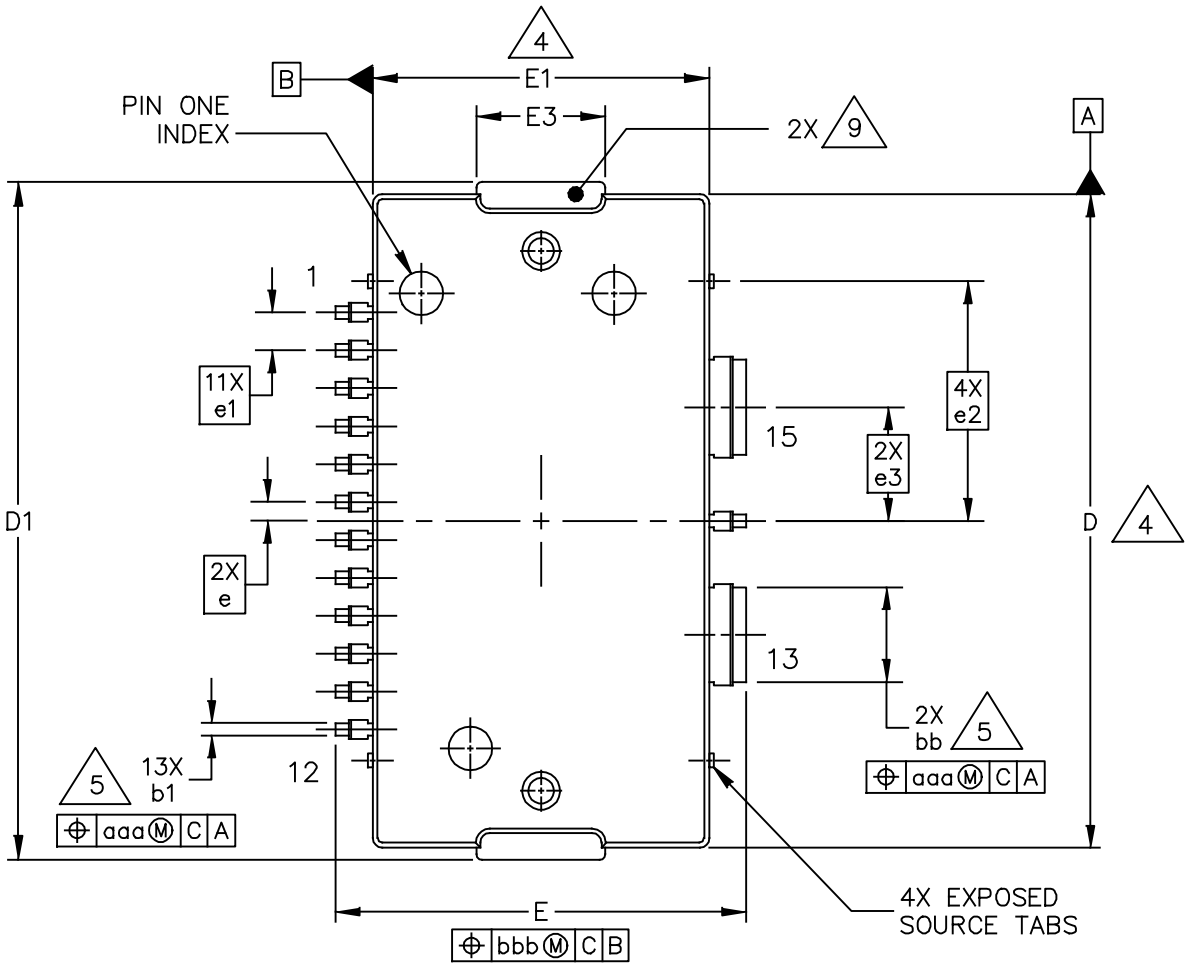
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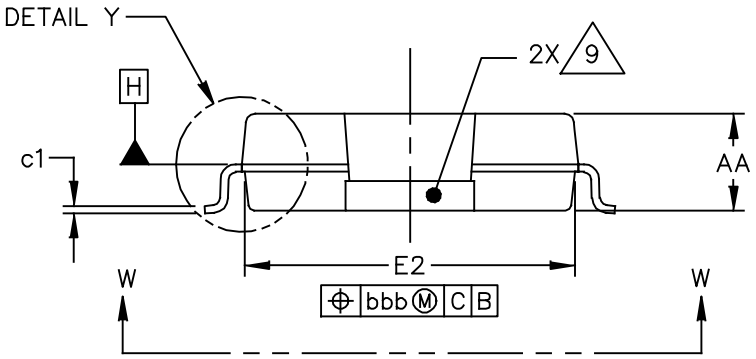
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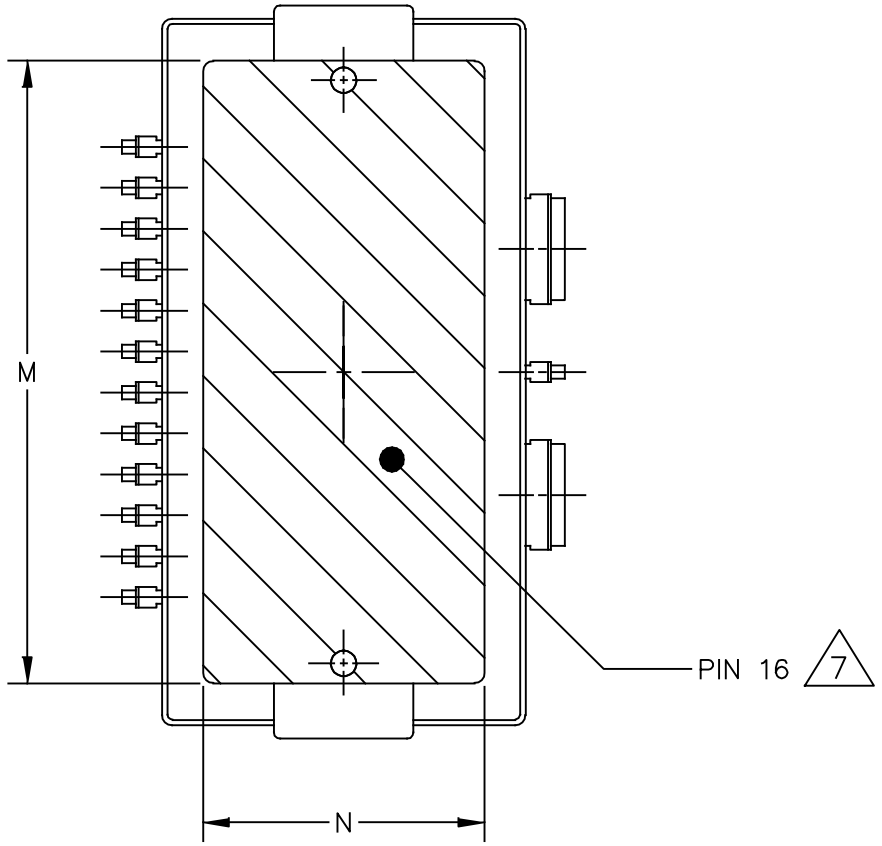
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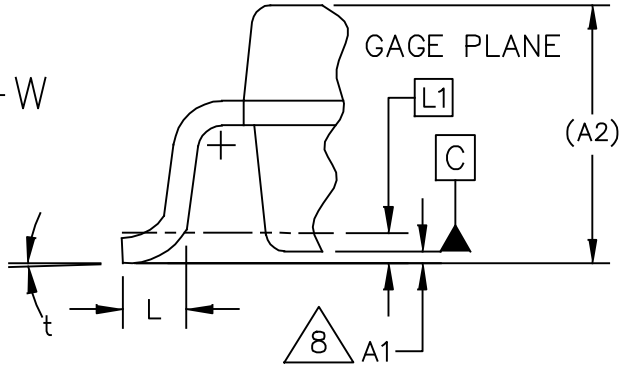




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VIEW W–W



DETAIL "Y"

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NOTES:

1. CONTROLLING DIMENSION: INCH

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3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

8. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM C. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF THE PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	M	.600	----	15.24	----
A1	.001	.004	0.03	0.10	N	.270	----	6.86	----
A2	(.105)		(2.67)		bb	.097	.103	2.46	2.62
D	.688	.692	17.48	17.58	b1	.010	.016	0.25	0.41
D1	.712	.720	18.08	18.29	c1	.007	.011	0.18	0.28
E	.429	.437	10.90	11.10	e	.020 BSC		0.51 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.253 INFO ONLY		6.43 INFO ONLY	
E3	.132	.140	3.35	3.56	e3	.120 BSC		3.05 BSC	
L	.018	.024	0.46	0.61	t	2°	8°	2°	8°
L1	.010 BSC		0.25 BSC		aaa	.004		0.10	
					bbb	.008		0.20	

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Jan. 2016	• Initial release of data sheet

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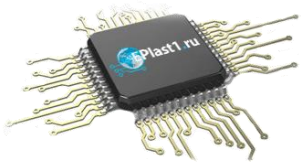
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- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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