2.5 V 1:4 AnyLevel™ Differential Input to LVDS Fanout Buffer/Translator

The NB6L14S is a differential 1:4 Clock or Data Receiver and will accept AnyLevel differential input signals: LVPECL, CML, LVDS, or HSCL. These signals will be translated to LVDS and four identical copies of Clock or Data will be distributed, operating up to 2.0 GHz or 2.5 Gb/s, respectively. As such, the NB6L14S is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock or Data distribution applications.

The NB6L14S has a wide input common mode range from GND + 50 mV to V_{CC} – 50 mV. Combined with the 50 Ω internal termination resistors at the inputs, the NB6L14S is ideal for translating a variety of differential or single–ended Clock or Data signals to 350 mV typical LVDS output levels.

The NB6L14S is the 2.5 V version of the NB6N14S and is offered in a small 3 mm x 3 mm 16–QFN package. Application notes, models, and support documentation are available at www.onsemi.com.

The NB6L14S is a member of the ECLinPS MAX[™] family of high performance products.

Features

- Maximum Input Clock Frequency > 2.0 GHz
- Maximum Input Data Rate > 2.5 Gb/s
- 1 ps Maximum of RMS Clock Jitter
- Typically 10 ps of Data Dependent Jitter
- 380 ps Typical Propagation Delay
- 120 ps Typical Rise and Fall Times
- Single Power Supply; $V_{CC} = 2.5 \pm 5\%$
- V_{REF AC} Reference Output
- These are Pb-Free Devices

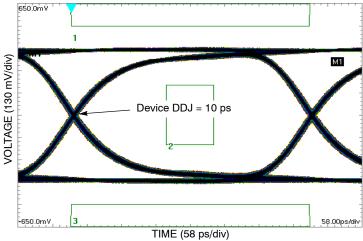


Figure 2. Typical Output Waveform at 2.488 Gb/s with PRBS 2^{23-1} (V_{INPP} = 400 mV; Input Signal DDJ = 14 ps)



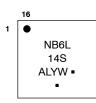
ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM*



QFN-16 MN SUFFIX CASE 485G



A = Assembly Location

= Wafer Lot

Y = Year

W = Work Week

= Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

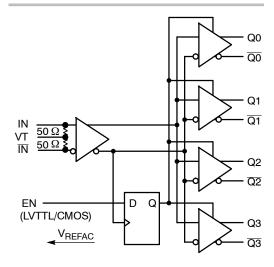


Figure 1. Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

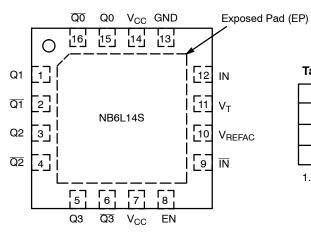


Table 1. TRUTH TABLE

IN	ĪN	EN	Q	Q
0	1	1	0	1
1	0	1	1	0
х	х	0	0 (Note 1)	1 (Note 1)

1. On next transition of the input signal (IN).

Figure 3. NB6L14S Pinout, 16-pin QFN (Top View)

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description	
1	Q1	LVDS Output	Non-inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.	
2	Q1	LVDS Output	Inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.	
3	Q2	LVDS Output	Non-inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.	
4	Q2	LVDS Output	Inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.	
5	Q3	LVDS Output	Non-inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.	
6	Q3	LVDS Output	Inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.	
7	V_{CC}	-	Positive Supply Voltage.	
8	EN	LVTTL / LVCMOS Input	Synchronous Output Enable. When LOW, Q outputs will go LOW and Qb outputs will go HIGH on the next negative transition of IN input. The internal DFF register is clocked on the falling edge of IN input; see Figure 26. The EN pin has an internal pullup resistor and defaults HIGH when left open.	
9	ĪN	LVPECL, CML, LVDS	Inverted Differential Input	
10	V _{REFAC}	LVPECL Output	The V _{REFAC} reference output can only be used to rebias capacitor–coupled differential or single–ended input signals. For the capacitor–coupled IN and/or INb inputs, V _{REFAC} should be connected to the VT pin and bypassed to ground with a 0.01 µF capacitor.	
11	V _T	LVPECL Output	Internal 100 Ω Center–tapped Termination Pin for IN and $\overline{\text{IN}}$	
12	IN	LVPECL, CML, LVDS	Non-inverted Differential Input. (Note 2)	
13	GND	-	Negative Supply Voltage.	
14	V _{CC}	-	Positive Supply Voltage.	
15	Q0	LVDS Output	Non–inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.	
16	Q0	LVDS Output	Inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.	
-	EP	-	The Exposed Pad (EP) on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to GND on the PC board.	

^{2.} In the differential configuration, when the input termination pin (VT) is connected to a termination voltage or left open, and if no signal is applied on IN/IN inputs, then the device will be susceptible to self–oscillation.

Table 3. ATTRIBUTES

Charac	Value	
Moisture Sensitivity (Note 3)	Level 1	
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V
Transistor Count	745	
Meets or exceeds JEDEC Spe		

^{3.} For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Positive Power Supply	GND = 0 V		3.8	V
V _{IN}	Positive Input	GND = 0 V	$V_{IN} \leq V_{CC}$	3.8	V
I _{IN}	Input Current Through R _T (50 Ω Resistor)	Static Surge		35 70	mA mA
I _{OSC}	Output Short Circuit Current Line-to-Line (Q to $\overline{\mathbf{Q}}$) Line-to-End (Q or $\overline{\mathbf{Q}}$ to GND)	Q or $\overline{\mathbb{Q}}$ Q to $\overline{\mathbb{Q}}$ to GND	Continuous Continuous	12 24	mA
I _{REF_AC}	V _{REF_AC} Sink/Source Current			± 0.5	mA
T _A	Operating Temperature Range	QFN-16		-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 4)	0 lfpm 500 lfpm	QFN-16 QFN-16	41.6 35.2	°C/W
θJC	Thermal Resistance (Junction-to-Case)	1S2P (Note 4)	QFN-16	4.0	°C/W
T _{sol}	Wave Solder Pb-Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

^{4.} JEDEC standard multilayer board – 1S2P (1 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS V_{CC} = 2.375 V to 2.625 V, GND = 0 V, T_A = -40°C to +85°C

Symbol	Characteristic	Min	Тур	Max	Unit
I _{CC}	Power Supply Current (Note 9)		65	100	mA
DIFFERE	NTIAL INPUTS DRIVEN SINGLE-ENDED (Figures 17, 18, 22, and 24)	•		•	
V _{th}	Input Threshold Reference Voltage Range (Note 8)	GND +100		V _{CC} - 100	mV
V _{IH}	Single-ended Input HIGH Voltage	V _{th} + 100		V _{CC}	mV
V _{IL}	Single-ended Input LOW Voltage	GND		V _{th} – 100	mV
V _{REFAC}	Reference Output Voltage (Note 11)	V _{CC} - 1.600	V _{CC} – 1.425	V _{CC} - 1.300	V
DIFFERE	NTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 10, 12, NO TAG, 1	NO TAG, 23, and 2	5)		
V_{IHD}	Differential Input HIGH Voltage	100		V _{CC}	mV
V_{ILD}	Differential Input LOW Voltage	GND		V _{IHD} – 100	mV
V_{CMR}	Input Common Mode Range (Differential Configuration)	GND + 50		V _{CC} – 50	mV
V_{ID}	Differential Input Voltage (V _{IHD} - V _{ILD})	100		V _{CC}	mV
R _{TIN}	Internal Input Termination Resistor	40	50	60	Ω
LVDS OU	TPUTS (Note 5)				
V _{OD}	Differential Output Voltage	250		450	mV
ΔV_{OD}	Change in Magnitude of V _{OD} for Complementary Output States (Note 10)	0	1	25	mV
V _{OS}	Offset Voltage (Figure 21)	1125		1375	mV
ΔV_{OS}	Change in Magnitude of V _{OS} for Complementary Output States (Note 10)	0	1	25	mV
V _{OH}	Output HIGH Voltage (Note 6)		1425	1600	mV
V _{OL}	Output LOW Voltage (Note 7)	900	1075		mV
LVTTL/LV	CMOS INPUT, EN				-
V _{IH}	Input HIGH Voltage	2.0		V _{CC}	V
V _{IL}	Input LOW Voltage	GND		0.8	V
I _{IH}	Input HIGH Current	-150		150	μΑ
I _{IL}	Input LOW Current	-150		150	μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 5. LVDS outputs require 100 Ω receiver termination resistor between differential pair. See Figure 20.
- 6. V_{OH} max = V_{OS} max + $\frac{1}{2}$ V_{OD} max. 7. V_{OL} max = V_{OS} min $\frac{1}{2}$ V_{OD} max.
- 8. V_{th} is applied to the complementary input when operating in single-ended mode.
- 9. Input termination pins open at the DC level within V_{CMR} and output pins loaded with R_L = 100 Ω across differential.
- 10. Parameter guaranteed by design verification not tested in production.
- 11. V_{REFAC} used to rebias capacitor-coupled inputs only (see Figures 17 and 18).

Table 6. AC CHARACTERISTICS V_{CC} = 2.375 V to 2.625 V, GND = 0 V; (Note 12)

			-40°C to +85°C			
Symbol	Characteristic		Min	Тур	Max	Unit
f _{inMax}	Maximum Input Clock Frequency		2.0			GHz
V _{OUTPP}	Output Voltage Amplitude (@ V _{INPPmin}) (Figure 4)	$f_{in} \le 1.0 \text{ GHz}$ $f_{in} = 1.5 \text{ GHz}$ $f_{in} = 2.0 \text{ GHz}$	220 200 170	350 300 270		mV
f _{DATA}	Maximum Operating Data Rate		2.5			Gb/s
t _{PLH} , t _{PHL}	Differential Input to Differential Output, IN to Q Propagation Delay @ 100 MHz		300	450	600	ps
t _s t _h	Setup Time Hold Time	EN to IN/ĪN	300 500	20 20		
tskew	Within Device Skew (Note 17) Device-to-Device Skew (Note 16)			5 30	20 200	ps
t _{JITTER}	RMS Random Clock Jitter (Note 14) Deterministic Jitter (Note 15)	$f_{in} = 2.0 \text{ GHz}$ $f_{DATA} \le 2.488 \text{ Gb/s}$		0.5 5.0	0.8 20	ps
V _{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 13)		100		V _{CC} -GND	mV
t _r t _f	Output Rise/Fall Times @ 250 MHz (20% – 80%)	Q, Q	70	150	225	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 13. Input voltage swing is a single-ended measurement operating in differential mode.
- 14. RMS jitter with 50% Duty Cycle clock signal at 750 MHz.
- 15. Deterministic jitter with input NRZ data at PRBS 223-1 and K28.5.
- 16. Skew is measured between outputs under identical transition @ 250 MHz.
- 17. The worst case condition between $Q0/\overline{Q0}$ and $Q1/\overline{Q1}$ from either $D0/\overline{D0}$ or $D1/\overline{D1}$, when both outputs have the same transition.

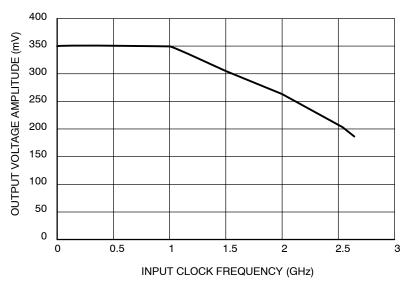


Figure 4. Output Voltage Amplitude (V_{OUTPP}) versus Input Clock Frequency (f_{in}) and Temperature (@ V_{CC} = 2.5 V)

^{12.} Measured by forcing $V_{INPPmin}$ with 50% duty cycle clock source and V_{CC} – 1400 mV offset. All loading with an external R_L = 100 Ω . Input edge rates 150 ps (20%–80%). See Figure 20.

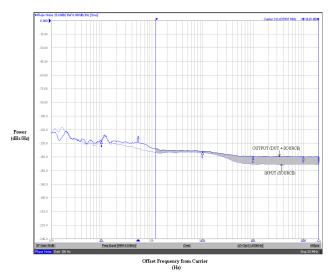


Figure 5. Typical Phase Noise Plot at $f_{carrier} = 311.04 \text{ MHz}$

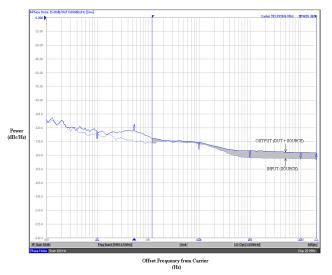


Figure 7. Typical Phase Noise Plot at $f_{carrier} = 1 \text{ GHz}$

The above phase noise plots captured using Agilent E5052A show additive phase noise of the NB6L14S device at frequencies 311.04 MHz, 622.08 MHz, 1 GHz and 1.5 GHz respectively at an operating voltage of 2.5 V in room temperature. The RMS Phase Jitter contributed by the

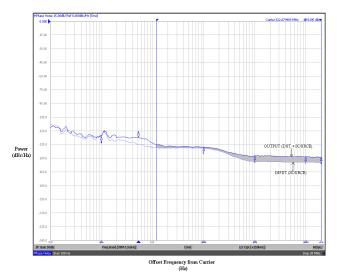


Figure 6. Typical Phase Noise Plot at f_{carrier} = 622.08 MHz

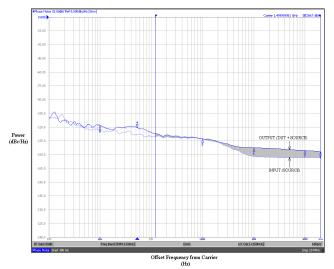


Figure 8. Typical Phase Noise Plot at $f_{carrier} = 1.5 \text{ GHz}$

device (integrated between 12 kHz and 20 MHz; as shown in the shaded region of the plot) at each of the frequencies is 65 fs, 29 fs, 24 fs and 20 fs respectively. The input source used for the phase noise measurements is Agilent E8663B.

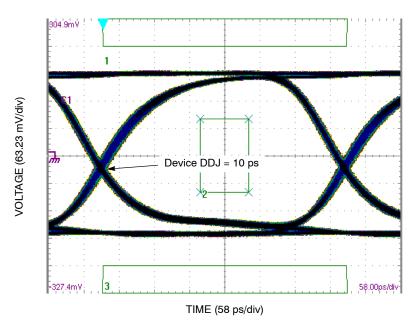


Figure 9. Typical Output Waveform at 2.488 Gb/s with PRBS 2^{23-1} and OC48 mask ($V_{INPP}=100$ mV; Input Signal DDJ = 14 ps)

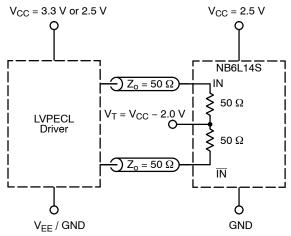


Figure 10. LVPECL Interface

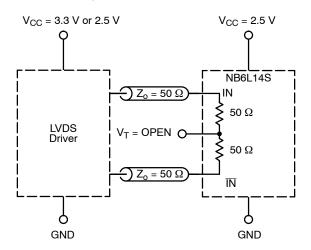


Figure 12. LVDS Interface

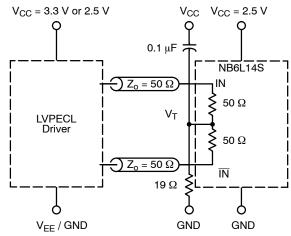


Figure 11. LVPECL Y-Termination Interface

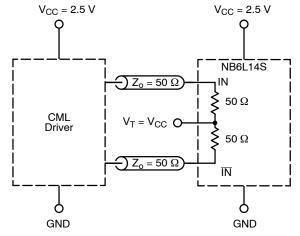
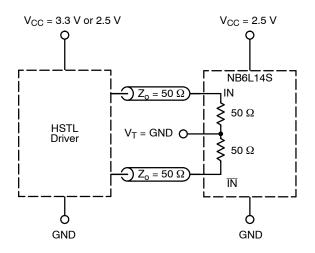


Figure 13. CML Interface



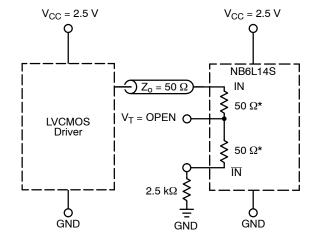
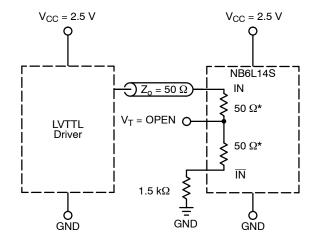


Figure 14. HSTL Interface

Figure 15. LVCMOS Interface



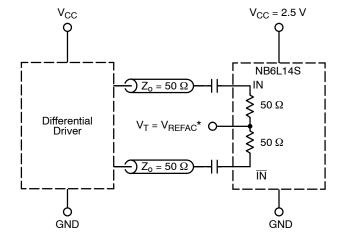


Figure 16. LVTTL Interface

Figure 17. Capacitor–Coupled Differential Interface (V_T Connected to V_{REF_AC})

* V_{REFAC} bypassed to ground with a 0.1 μF capacitor.

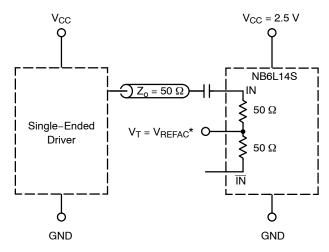


Figure 18. Capacitor-Coupled Single-Ended Interface (V_T Connected to V_{REFAC})

*V_REFAC bypassed to ground with a 0.1 μF capacitor.

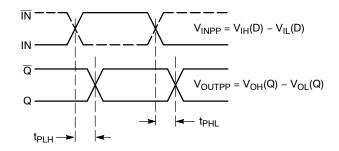


Figure 19. AC Reference Measurement

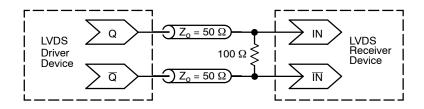


Figure 20. Typical LVDS Termination for Output Driver and Device Evaluation

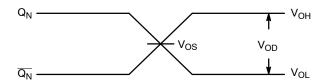


Figure 21. LVDS Output

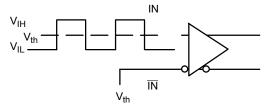


Figure 22. Differential Input Driven Single-Ended

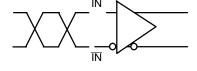


Figure 23. Differential Inputs Driven Differentially

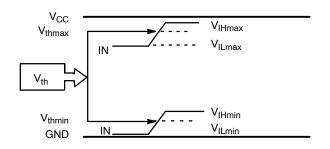


Figure 24. V_{th} Diagram

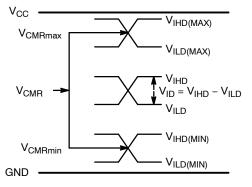


Figure 25. V_{CMR} Diagram

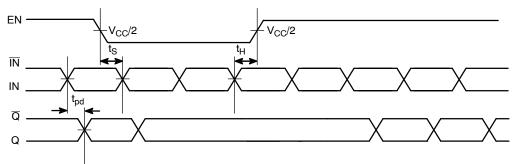


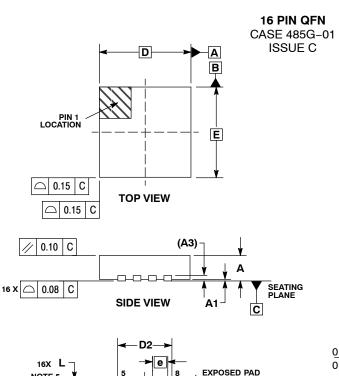
Figure 26. EN Timing Diagram

ORDERING INFORMATION

Device	Package	Shipping [†]
NB6L14SMNG	QFN-16, 3 X 3 mm (Pb-Free)	123 Units / Rail
NB6L14SMNTXG	QFN-16, 3 X 3 mm (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS



- NOTES:

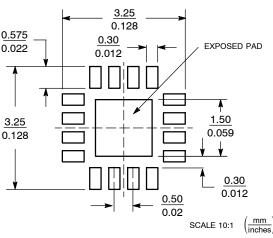
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

 2. CONTROLLING DIMENSION: MILLIMETERS.

 3. DIMENSION 6 APPLIES TO PLATED
- TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
- COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
- L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP

	MILLIMETERS			
DIM	MIN	MAX		
Α	0.80	1.00		
A1	0.00	0.05		
А3	0.20 REF			
b	0.18	0.30		
D	3.00 BSC			
D2	1.65	1.85		
Е	3.00	BSC		
E2	1.65	1.85		
е	0.50 BSC 0.18 TYP			
K				
L	0.30	0.50		

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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13

BOTTOM VIEW

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PUBLICATION ORDERING INFORMATION

NOTE 5

16X K

0.10 С A B

0.05 С NOTE 3 16

16X b

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Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов:
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
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- Экспресс доставка в любую точку России;
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- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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