Single-Channel, 128-/64-/32-Position, I²C, ±8% Resistor Tolerance, Nonvolatile Digital Potentiometer

Data Sheet

AD5110/AD5112/AD5114

FEATURES

- Nominal resistor tolerance error: ±8% maximum
- Wiper current: ±6 mA
- Rheostat mode temperature coefficient: 35 ppm/°C
- Low power consumption: 2.5 µA max @ 2.7 V and 125°C
- Wide bandwidth: 4 MHz (5 kΩ option)
- Power-on EEPROM refresh time < 50 µs
- 50-year typical data retention at 125°C
- 1 million write cycles
- 2.3 V to 5.5 V analog supply operation
- 1.8 V to 5.5 V logic supply operation
- Wide operating temperature: −40°C to +125°C
- Thin, 2 mm × 2 mm × 0.55 mm 8-lead LFCSP package

APPLICATIONS

- Mechanical potentiometer replacement
- Portable electronics level adjustment
- Audio volume control
- Low resolution DAC
- LCD panel brightness and contrast control
- Programmable voltage to current conversion
- Programmable filters, delays, time constants
- Feedback resistor programmable power supply
- Sensor calibration

FUNCTIONAL BLOCK DIAGRAM

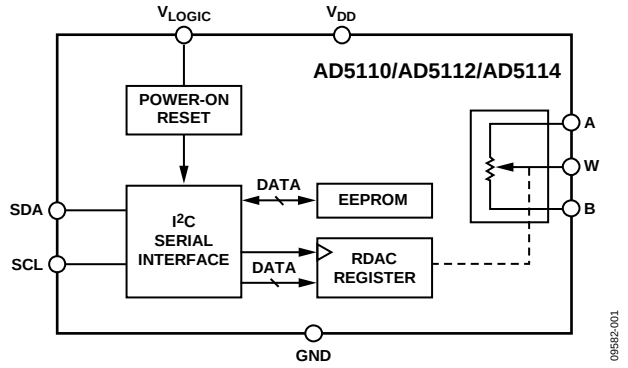


Figure 1.

Table 1. ±8% Resistance Tolerance Family

Model	Resistance (kΩ)	Position	Interface
AD5110	10, 80	128	I²C
AD5111	10, 80	128	Up/down
AD5112	5, 10, 80	64	I²C
AD5113	5, 10, 80	64	Up/down
AD5116	5, 10, 80	64	Push-button
AD5114	10, 80	32	I²C
AD5115	10, 80	32	Up/down

GENERAL DESCRIPTION

The AD5110/AD5112/AD5114 provide a nonvolatile solution for 128-/64-/32-position adjustment applications, offering guaranteed low resistor tolerance errors of ±8% and up to ±6 mA current density in the A, B, and W pins. The low resistor tolerance, low nominal temperature coefficient and high bandwidth simplify open-loop applications, as well as tolerance matching applications.

The new low wiper resistance feature minimizes the wiper resistance in the extremes of the resistor array to only 45 Ω, typical.

The wiper settings are controllable through an I²C-compatible digital interface that is also used to readback the wiper register and EEPROM content. Resistor tolerance is stored within EEPROM, providing an end-to-end tolerance accuracy of 0.1%.

The AD5110/AD5112/AD5114 are available in a 2 mm × 2 mm LFCSP package. The parts are guaranteed to operate over the extended industrial temperature range of −40°C to +125°C.

Rev. B
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REVISION HISTORY

11/12—Rev. A to Rev. B

Changed Low Power Consumption from 2.5 mA to 2.5 µA ... 1
Changed I_{DD} Unit from mA to µA, Table 2 ... 4
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4/12—Rev. 0 to Rev. A

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10/11—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—AD5110

10 kΩ and 80 kΩ versions: V_{DD} = 2.3 V to 5.5 V, V_{LOGIC} = 1.8 V to V_{DD}, $V_A = V_{DD}$, V_B = 0 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resolution	N		7			Bits
Resistor Integral Nonlinearity[2]	R-INL	R_{AB} = 10 kΩ, V_{DD} = 2.3 V to 2.7 V	−2.5	±0.5	+2.5	LSB
		R_{AB} = 10 kΩ, V_{DD} = 2.7 V to 5.5 V	−1	±0.25	+1	LSB
		R_{AB} = 80 kΩ	−0.5	±0.1	+0.5	LSB
Resistor Differential Nonlinearity[2]	R-DNL		−1	±0.25	+1	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		−8		+8	%
Resistance Temperature Coefficient[3]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full scale		35		ppm/°C
Wiper Resistance	R_W	Code = zero scale		70	140	Ω
	R_{BS}	Code = bottom scale		45	80	Ω
	R_{TS}	Code = top scale		70	140	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Integral Nonlinearity[4]	INL		−0.5	±0.15	+0.5	LSB
Differential Nonlinearity[4]	DNL		−0.5	±0.15	+0.5	LSB
Full-Scale Error	V_{WFSE}	R_{AB} = 10 kΩ	−2.5			LSB
		R_{AB} = 80 kΩ	−1.5			LSB
Zero-Scale Error	V_{WZSE}	R_{AB} = 10 kΩ			1.5	LSB
		R_{AB} = 80 kΩ			0.5	LSB
Voltage Divider Temperature Coefficient[3]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		±10		ppm/°C
RESISTOR TERMINALS						
Maximum Continuous I_A, I_B, and I_W Current[3]		R_{AB} = 10 kΩ	−6		+6	mA
		R_{AB} = 80 kΩ	−1.5		+1.5	mA
Terminal Voltage Range[5]			GND		V_{DD}	V
Capacitance A, Capacitance B[3]	C_A, C_B	f = 1 MHz, measured to GND, code = half scale, $V_W = V_A$ = 2.5 V or $V_W = V_B$ = 2.5 V		20		pF
Capacitance W[3]	C_W	f = 1 MHz, measured to GND, code = half scale, $V_A = V_B$ = 2.5 V		35		pF
Common-Mode Leakage Current[3]		$V_A = V_W = V_B$	−500	±15	+500	nA
DIGITAL INPUTS						
Input Logic[3]						
High	V_{INH}	V_{LOGIC} = 1.8 V to 2.3 V	0.8 × V_{LOGIC}			V
		V_{LOGIC} = 2.3 V to 5.5 V	0.7 × V_{LOGIC}			V
Low	V_{INL}	V_{LOGIC} = 1.8 V to 2.3 V			0.2 × V_{LOGIC}	V
		V_{LOGIC} = 2.3 V to 5.5 V			0.3 × V_{LOGIC}	V
Input Hysteresis[3]	V_{HYST}		0.1 × V_{LOGIC}			V
Input Current[3]	I_N				±1	µA
Input Capacitance[3]	C_{IN}			5		pF
DIGITAL OUTPUT (SDA)						
Output Low Voltage[3]	V_{OL}	I_{SINK} = 3 mA			0.2	V
		I_{SINK} = 6 mA			0.4	V
Three-State Leakage Current			−1		+1	µA
Three-State Output Capacitance[3]				2		pF

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
POWER SUPPLIES						
Single-Supply Power Range			2.3		5.5	V
Logic Supply Range			1.8		V_{DD}	V
Positive Supply Current	I_{DD}	V_{DD} = 5 V		0.75	3.5	μA
		V_{DD} = 2.7 V			2.5	μA
		V_{DD} = 2.3 V			2.4	μA
EEMEM Store Current[3, 6]	$I_{DD_NVM_STORE}$			2		mA
EEMEM Read Current[3, 7]	$I_{DD_NVM_READ}$			320		μA
Logic Supply Current	I_{LOGIC}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		30		nA
Power Dissipation[8]	P_{DISS}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		5		μW
Power Supply Rejection[3]	PSR	$\Delta V_{DD}/\Delta V_{SS}$ = 5 V ± 10%				
		R_{AB} = 10 kΩ		−50		dB
		R_{AB} = 80 kΩ		−64		dB
DYNAMIC CHARACTERISTICS[3, 9]						
Bandwidth	BW	Code = half scale, −3 dB				
		R_{AB} = 10 kΩ		2		MHz
		R_{AB} = 80 kΩ		200		kHz
Total Harmonic Distortion	THD	$V_A = V_{DD}/2$ +1 V rms, $V_B = V_{DD}/2$, f = 1 kHz, code = half scale				
		R_{AB} = 10 kΩ		−80		dB
		R_{AB} = 80 kΩ		−85		dB
V_W Settling Time	t_s	V_A = 5 V, V_B = 0 V, ±0.5 LSB error band				
		R_{AB} = 10 kΩ		3		μs
		R_{AB} = 80 kΩ		12		μs
Resistor Noise Density	e_{N_WB}	Code = half scale, T_A = 25°C, f = 100 kHz				
		R_{AB} = 10 kΩ		9		nV/√Hz
		R_{AB} = 80 kΩ		20		nV/√Hz
FLASH/EE MEMORY RELIABILITY[3]						
Endurance[10]		T_A = 25°C		1		MCycles
			100			kCycles
Data Retention[11]				50		Years

[1] Typical values represent average readings at 25°C, V_{DD} = 5 V, V_{SS} = 0 V, and V_{LOGIC} = 5 V.
[2] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. The maximum wiper current is limited to 0.75 × V_{DD}/R_{AB}.
[3] Guaranteed by design and characterization, not subject to production test.
[4] INL and DNL are measured at V_{WB} with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other.
[6] Different from operating current; supply current for NVM program lasts approximately 30 ms.
[7] Different from operating current; supply current for NVM read lasts approximately 20 μs.
[8] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$) + ($I_{LOGIC} \times V_{LOGIC}$).
[9] All dynamic characteristics use V_{DD} = 5.5 V, and V_{LOGIC} = 5 V.
[10] Endurance is qualified at 100,000 cycles per JEDEC Standard 22, Method A117 and measured at 150°C.
[11] Retention lifetime equivalent at junction temperature (T_J) = 125°C per JEDEC Standard 22, Method A117. Retention lifetime based on an activation energy of 1 eV derates with junction temperature in the Flash/EE memory.

ELECTRICAL CHARACTERISTICS—AD5112

5 kΩ, 10 kΩ, and 80 kΩ versions: V_{DD} = 2.3 V to 5.5 V, V_{LOGIC} = 1.8 V to V_{DD}, $V_A = V_{DD}$, V_B = 0 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resolution	N		6			Bits
Resistor Integral Nonlinearity[2]	R-INL	R_{AB} = 5 kΩ, V_{DD} = 2.3 V to 2.7 V	−2.5	±0.5	+2.5	LSB
		R_{AB} = 5 kΩ, V_{DD} = 2.7 V to 5.5 V	−1	±0.25	+1	LSB
		R_{AB} = 10 kΩ	−1	±0.25	+1	LSB
		R_{AB} = 80 kΩ	−0.25	±0.1	+0.25	LSB
Resistor Differential Nonlinearity[2]	R-DNL		+1	±0.25	+1	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		−8		+8	%
Resistance Temperature Coefficient[3]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full scale		35		ppm/°C
Wiper Resistance	R_W	Code = zero scale		70	140	Ω
	R_{BS}	Code = bottom scale		45	80	Ω
	R_{TS}	Code = top scale		70	140	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Integral Nonlinearity[4]	INL		−0.5	±0.15	+0.5	LSB
Differential Nonlinearity[4]	DNL		−0.5	±0.15	+0.5	LSB
Full-Scale Error	V_{WFSE}	R_{AB} = 5 kΩ	−2.5			LSB
		R_{AB} =10 kΩ	−1.5			LSB
		R_{AB} = 80 kΩ	−1			LSB
Zero-Scale Error	V_{WZSE}	R_{AB} = 5 kΩ			1.5	LSB
		R_{AB} =10 kΩ			1	LSB
		R_{AB} = 80 kΩ			0.25	LSB
Voltage Divider Temperature Coefficient[3]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		±10		ppm/°C
RESISTOR TERMINALS						
Maximum Continuous I_A, I_B, and I_W Current[3]		R_{AB} = 5 kΩ, 10 kΩ	−6		+6	mA
		R_{AB} = 80 kΩ	−1.5		+1.5	mA
Terminal Voltage Range[5]			GND		V_{DD}	V
Capacitance A, Capacitance B[3]	C_A, C_B	f = 1 MHz, measured to GND, code = half scale, $V_W = V_A$ = 2.5 V or $V_W = V_B$ = 2.5 V		20		pF
Capacitance W[3]	C_W	f = 1 MHz, measured to GND, code = half scale, $V_A = V_B$ = 2.5 V		35		pF
Common-Mode Leakage Current[3]		$V_A = V_W = V_B$	−500	±15	+500	nA
DIGITAL INPUTS						
Input Logic[3]						
High	V_{INH}	V_{LOGIC} = 1.8 V to 2.3 V	0.8 × V_{LOGIC}			V
		V_{LOGIC} = 2.3 V to 5.5 V	0.7 × V_{LOGIC}			V
Low	V_{INL}	V_{LOGIC} = 1.8 V to 2.3 V			0.2 × V_{LOGIC}	V
		V_{LOGIC} = 2.3 V to 5.5 V			0.3 × V_{LOGIC}	V
Input Hysteresis[3]	V_{HYST}		0.1 × V_{LOGIC}			V
Input Current[3]	I_N				±1	µA
Input Capacitance[3]	C_{IN}			5		pF
DIGITAL OUTPUT (SDA)						
Output Low Voltage[3]	V_{OL}	I_{SINK} = 3 mA			0.2	V
		I_{SINK} = 6 mA			0.4	V
Three-State Leakage Current			−1		+1	µA
Three-State Output Capacitance[3]				2		pF

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
POWER SUPPLIES						
Single-Supply Power Range			2.3		5.5	V
Logic Supply Range			1.8		V_{DD}	V
Positive Supply Current	I_{DD}	V_{DD} = 5 V		0.75	3.5	μA
		V_{DD} = 2.7 V			2.5	μA
		V_{DD} = 2.3 V			2.4	μA
EEMEM Store Current[3, 6]	$I_{DD_NVM_STORE}$			2		mA
EEMEM Read Current[3, 7]	$I_{DD_NVM_READ}$			320		μA
Logic Supply Current	I_{LOGIC}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		30		nA
Power Dissipation[8]	P_{DISS}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		5		μW
Power Supply Rejection[3]	PSR	$\Delta V_{DD}/\Delta V_{SS}$ = 5 V ± 10%				
		R_{AB} = 5 kΩ		−43		dB
		R_{AB} =10 kΩ		−50		dB
		R_{AB} = 80 kΩ		−64		dB
DYNAMIC CHARACTERISTICS[3, 9]						
Bandwidth	BW	Code = half scale − 3 dB				
		R_{AB} = 5 kΩ		4		MHz
		R_{AB} = 10 kΩ		2		MHz
		R_{AB} = 80 kΩ		200		kHz
Total Harmonic Distortion	THD	$V_A = V_{DD}/2$ + 1 V rms, $V_B = V_{DD}/2$, f = 1 kHz, code = half scale				
		R_{AB} = 5 kΩ		−75		dB
		R_{AB} = 10 kΩ		−80		dB
		R_{AB} = 80 kΩ		−85		dB
V_W Settling Time	t_s	V_A = 5 V, V_B = 0 V, ±0.5 LSB error band				μs
		R_{AB} = 5 kΩ		2.5		μs
		R_{AB} = 10 kΩ		3		μs
		R_{AB} = 80 kΩ		10		μs
Resistor Noise Density	e_{N_WB}	Code = half scale, T_A = 25°C, f = 100 kHz				
		R_{AB} = 5 kΩ		7		nV/√Hz
		R_{AB} = 10 kΩ		9		nV/√Hz
		R_{AB} = 80 kΩ		20		nV/√Hz
FLASH/EE MEMORY RELIABILITY[3]						
Endurance[10]		T_A = 25°C		1		MCycles
			100			kCycles
Data Retention[11]				50		Years

[1] Typical values represent average readings at 25°C, V_{DD} = 5 V, V_{SS} = 0 V, and V_{LOGIC} = 5 V.
[2] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. The maximum wiper current is limited to 0.75 × V_{DD}/R_{AB}.
[3] Guaranteed by design and characterization, not subject to production test.
[4] INL and DNL are measured at V_{WB} with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other.
[6] Different from operating current; supply current for NVM program lasts approximately 30 ms.
[7] Different from operating current; supply current for NVM read lasts approximately 20 μs.
[8] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$) + ($I_{LOGIC} \times V_{LOGIC}$).
[9] All dynamic characteristics use V_{DD} = 5.5 V, and V_{LOGIC} = 5 V.
[10] Endurance is qualified at 100,000 cycles per JEDEC Standard 22, Method A117 and measured at 150°C.
[11] Retention lifetime equivalent at junction temperature (T_J) = 125°C per JEDEC Standard 22, Method A117. Retention lifetime based on an activation energy of 1 eV derates with junction temperature in the Flash/EE memory.

ELECTRICAL CHARACTERISTICS—AD5114

10 kΩ and 80 kΩ versions: V_{DD} = 2.3 V to 5.5 V, V_{LOGIC} = 1.8 V to V_{DD}, $V_A = V_{DD}$, V_B = 0 V, −40°C < T_A < +125°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resolution	N		5			Bits
Resistor Integral Nonlinearity[2]	R-INL		−0.5		+0.5	LSB
Resistor Differential Nonlinearity[2]	R-DNL		−0.25		+0.25	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		−8		+8	%
Resistance Temperature Coefficient[3]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full scale		35		ppm/°C
Wiper Resistance	R_W	Code = zero scale		70	140	Ω
	R_{BS}	Code = bottom scale		45	80	Ω
	R_{TS}	Code = top scale		70	140	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Integral Nonlinearity[4]	INL		−0.25		+0.25	LSB
Differential Nonlinearity[4]	DNL		−0.25		+0.25	LSB
Full-Scale Error	V_{WFSE}	R_{AB} = 10 kΩ	−1			LSB
		R_{AB} = 80 kΩ	−0.5			LSB
Zero-Scale Error	V_{WZSE}	R_{AB} = 10 kΩ			1	LSB
		R_{AB} = 80 kΩ			0.25	LSB
Voltage Divider Temperature Coefficient[3]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		±10		ppm/°C
RESISTOR TERMINALS						
Maximum Continuous I_A, I_B, and I_W Current[3]		R_{AB} = 10 kΩ	−6		+6	mA
		R_{AB} = 80 kΩ	−1.5		+1.5	mA
Terminal Voltage Range[5]			GND		V_{DD}	V
Capacitance A, Capacitance B[3]	C_A, C_B	f = 1 MHz, measured to GND, code = half scale, $V_W = V_A$ = 2.5 V or $V_W = V_B$ = 2.5 V		20		pF
Capacitance W[3]	C_W	f = 1 MHz, measured to GND, code = half scale, $V_A = V_B$ = 2.5 V		35		pF
Common-Mode Leakage Current[3]		$V_A = V_W = V_B$	−500	±15	+500	nA
DIGITAL INPUTS						
Input Logic[3]						
High	V_{INH}	V_{LOGIC} = 1.8 V to 2.3 V	0.8 × V_{LOGIC}			V
		V_{LOGIC} = 2.3 V to 5.5 V	0.7 × V_{LOGIC}			V
Low	V_{INL}	V_{LOGIC} = 1.8 V to 2.3 V			0.2 × V_{LOGIC}	V
		V_{LOGIC} = 2.3 V to 5.5 V			0.3 × V_{LOGIC}	V
Input Hysteresis[3]	V_{HYST}		0.1 × V_{LOGIC}			V
Input Current[3]	I_N				±1	µA
Input Capacitance[3]	C_{IN}			5		pF
DIGITAL OUTPUT (SDA)						
Output Low Voltage[3]	V_{OL}	I_{SINK} = 3 mA			0.2	V
		I_{SINK} = 6 mA			0.4	V
Three-State Leakage Current			−1		+1	µA
Three-State Output Capacitance[3]				2		pF

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
POWER SUPPLIES						
Single-Supply Power Range			2.3		5.5	V
Logic Supply Range			1.8		V_{DD}	V
Positive Supply Current	I_{DD}	V_{DD} = 5 V		0.75	3.5	μA
		V_{DD} = 2.7 V			2.5	μA
		V_{DD} = 2.3 V			2.4	μA
EEMEM Store Current[3, 6]	$I_{DD_NVM_STORE}$			2		mA
EEMEM Read Current[3, 7]	$I_{DD_NVM_READ}$			320		μA
Logic Supply Current	I_{LOGIC}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		30		nA
Power Dissipation[8]	P_{DISS}	$V_{IH} = V_{LOGIC}$ or V_{IL} = GND		5		μW
Power Supply Rejection[3]	PSR	$\Delta V_{DD}/\Delta V_{SS}$ = 5 V ± 10%				
		R_{AB} = 10 kΩ		−50		dB
		R_{AB} = 80 kΩ		−64		dB
DYNAMIC CHARACTERISTICS[3, 9]						
Bandwidth	BW	Code = half scale, −3 dB				
		R_{AB} = 10 kΩ		2		MHz
		R_{AB} = 80 kΩ		200		kHz
Total Harmonic Distortion	THD	$V_A = V_{DD}/2$ + 1 V rms, $V_B = V_{DD}/2$, f = 1 kHz, code = half scale				
		R_{AB} = 10 kΩ		−80		dB
		R_{AB} = 80 kΩ		−85		dB
V_W Settling Time	t_s	V_A = 5 V, V_B = 0 V, ±0.5 LSB error band				
		R_{AB} = 10 kΩ		2.7		μs
		R_{AB} = 80 kΩ		9.5		μs
Resistor Noise Density	e_{N_WB}	Code = half scale, T_A = 25°C, f = 100 kHz				
		R_{AB} = 10 kΩ		9		nV/√Hz
		R_{AB} = 80 kΩ		20		nV/√Hz
FLASH/EE MEMORY RELIABILITY[3]						
Endurance[10]		T_A = 25°C		1		MCycles
			100			kCycles
Data Retention[11]				50		Years

[1] Typical values represent average readings at 25°C, V_{DD} = 5 V, V_{SS} = 0 V, and V_{LOGIC} = 5 V.
[2] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. The maximum wiper current is limited to 0.75 × V_{DD}/R_{AB}.
[3] Guaranteed by design and characterization, not subject to production test.
[4] INL and DNL are measured at V_{WB} with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other.
[6] Different from operating current; supply current for NVM program lasts approximately 30 ms.
[7] Different from operating current; supply current for NVM read lasts approximately 20 μs.
[8] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$) + ($I_{LOGIC} \times V_{LOGIC}$).
[9] All dynamic characteristics use V_{DD} = 5.5 V, and V_{LOGIC} = 5 V.
[10] Endurance is qualified at 100,000 cycles per JEDEC Standard 22, Method A117 and measured at 150°C.
[11] Retention lifetime equivalent at junction temperature (T_J) = 125°C per JEDEC Standard 22, Method A117. Retention lifetime based on an activation energy of 1 eV derates with junction temperature in the Flash/EE memory.

INTERFACE TIMING SPECIFICATIONS

V_{LOGIC} = 1.8 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5.

Parameter[1]	Test Conditions/ Comments	Min	Typ	Max	Unit	Description
f_{SCL}[2]	Standard mode			100	kHz	Serial clock frequency
	Fast mode			400	kHz	
t_1	Standard mode	4.0			µs	t_{HIGH}, SCL high time
	Fast mode	0.6			µs	
t_2	Standard mode	4.7			µs	t_{LOW}, SCL low time
	Fast mode	1.3			µs	
t_3	Standard mode	250			ns	$t_{SU;DAT}$, data setup time
	Fast mode	100			ns	
t_4	Standard mode	0		3.45	µs	$t_{HD;DAT}$, data hold time
	Fast mode	0		0.9	µs	
t_5	Standard mode	4.7			µs	$t_{SU;STA}$, setup time for a repeated start condition
	Fast mode	0.6			µs	
t_6	Standard mode	4			µs	$t_{HD;STA}$, hold time (repeated) start condition
	Fast mode	0.6			µs	
t_7	Standard mode	4.7			µs	t_{BUF}, bus free time between a stop and a start condition
	Fast mode	1.3			µs	
t_8	Standard mode	4			µs	$t_{SU;STO}$, setup time for stop condition
	Fast mode	0.6			µs	
t_9	Standard mode			1000	ns	t_{RDA}, rise time of SDA signal
	Fast mode	20 + 0.1 C_L		300	ns	
t_{10}	Standard mode			300	ns	t_{FDA}, fall time of SDA signal
	Fast mode	20 + 0.1 C_L		300	ns	
t_{11}	Standard mode			1000	ns	t_{RCL}, rise time of SCL signal
	Fast mode	20 + 0.1 C_L		300	ns	
t_{11A}	Standard mode			1000	ns	t_{RCL1}, rise time of SCL signal after a repeated start condition and after an acknowledge bit.
	Fast mode	20 + 0.1 C_L		300	ns	
t_{12}	Standard mode			300	ns	t_{FCL}, fall time of SCL signal
	Fast mode	20 + 0.1 C_L		300	ns	
t_{SP}[3]	Fast mode	0		50	ns	Pulse width of suppressed spike
$t_{EEPROM_PROGRAM}$[4]			15	50	ms	Memory program time
t_{POWER_UP}[5]				50	µs	Power-on EEPROM restore time
t_{RESET}				25	µs	Reset EEPROM restore time

[1] Maximum bus capacitance is limited to 400 pF.
[2] The SDA and SCL timing is measured with the input filters enabled. Switching off the input filters improves the transfer rate but has a negative effect on EMC behavior of the part.
[3] Input filtering on the SCL and SDA inputs suppress noise spikes that are less than 50 ns for fast mode.
[4] EEPROM program time depends on the temperature and EEPROM write cycles. Higher timing is expected at a lower temperature and higher write cycles.
[5] Maximum time after V_{DD} is equal to 2.3 V.

SHIFT REGISTER AND TIMING DIAGRAM

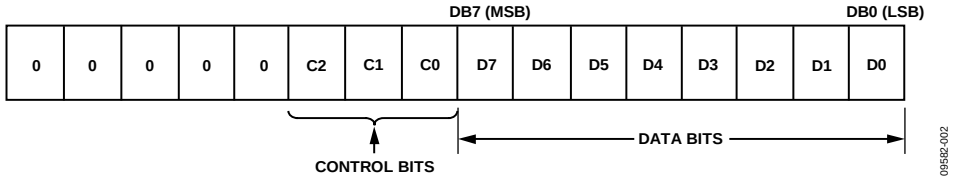


Figure 2. Input Register Content

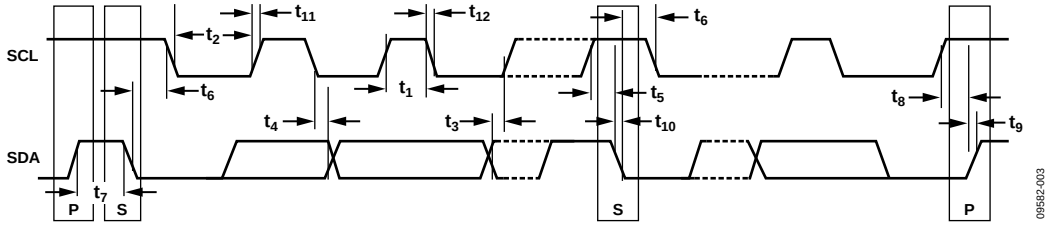


Figure 3. 2-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7.0 V
VLOGIC to GND	−0.3 V to +7.0 V
V_A, V_W, V_B to GND	GND − 0.3 V to V_{DD} + 0.3 V
I_A, I_W, I_B	
Pulsed[1]	
Frequency > 10 kHz	
R_{AW} = 5 kΩ and 10 kΩ	±6 mA/d[2]
R_{AW} = 80 kΩ	±1.5 mA/d[2]
Frequency ≤ 10 kHz	
R_{AW} = 5 kΩ and 10 kΩ	±6 mA/√d[2]
R_{AW} = 80 kΩ	±1.5 mA/√d[2]
Continuous	
R_{AW} = 5 kΩ and 10 kΩ	±6 mA
R_{AW} = 80 kΩ	±1.5 mA
Digital Inputs SDA and SCL	−0.3 V to +7 V or V_{LOGIC} + 0.3 V (whichever is less)
Operating Temperature Range[3]	−40°C to +125°C
Maximum Junction Temperature (T_J Max)	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Package Power Dissipation	(T_J max − T_A)/θ_{JA}

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] Pulse duty factor.
[3] Includes programming of EEPROM memory.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is defined by JEDEC specification JESD-51, and the value is dependent on the test board and test environment.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead LFCSP	90[1]	25	°C/W

[1] JEDEC 2S2P test board, still air (0 m/sec air flow).

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

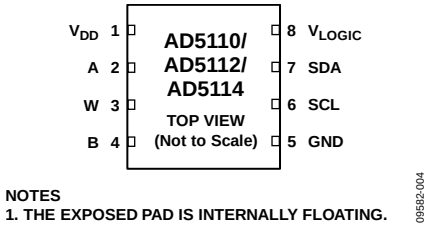


Figure 4. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Positive Power Supply; 2.3 V to 5.5 V. This pin should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
2	A	Terminal A of RDAC. GND ≤ V_A ≤ V_{DD}.
3	W	Wiper Terminal of RDAC. GND ≤ V_W ≤ V_{DD}.
4	B	Terminal B of RDAC. GND ≤ V_B ≤ V_{DD}.
5	GND	Ground Pin, Logic Ground Reference.
6	SCL	Serial Clock Line. This pin is used in conjunction with the SDA line to clock data into or out of the 16-bit input registers.
7	SDA	Serial Data Line. This pin is used in conjunction with the SCL line to clock data into or out of the 16-bit input registers. It is a bidirectional, open-drain data line that should be pulled to the supply with an external pull-up resistor.
8	V_{LOGIC}	Logic Power Supply; 1.8 V to V_{DD}. This pin should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
	EPAD	Exposed Pad. The exposed pad is internally floating.

TYPICAL PERFORMANCE CHARACTERISTICS

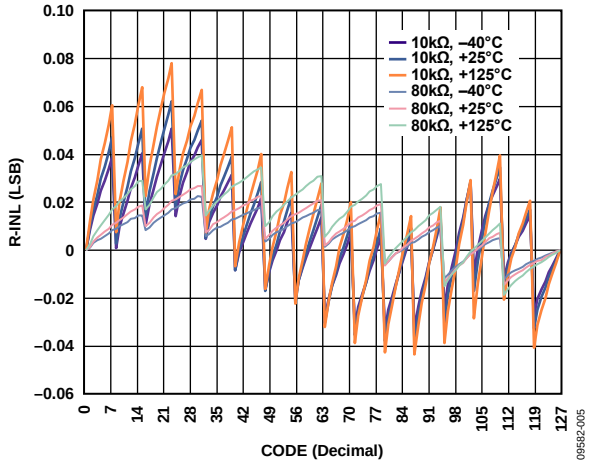


Figure 5. R-INL vs. Code (AD5110)

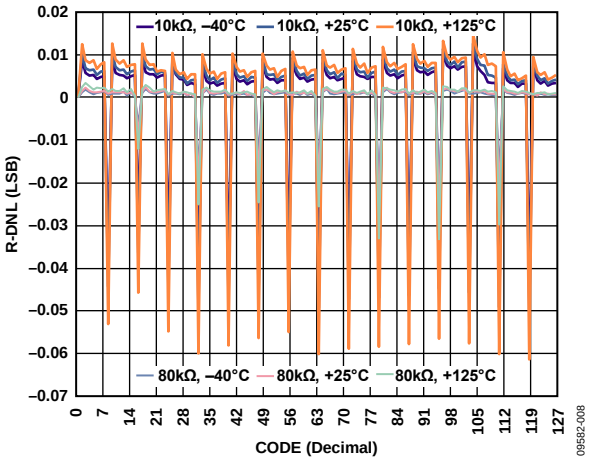


Figure 8. R-DNL vs. Code (AD5110)

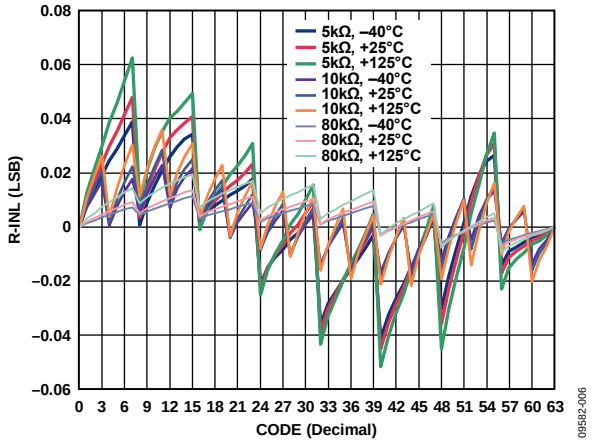


Figure 6. R-INL vs. Code (AD5112)

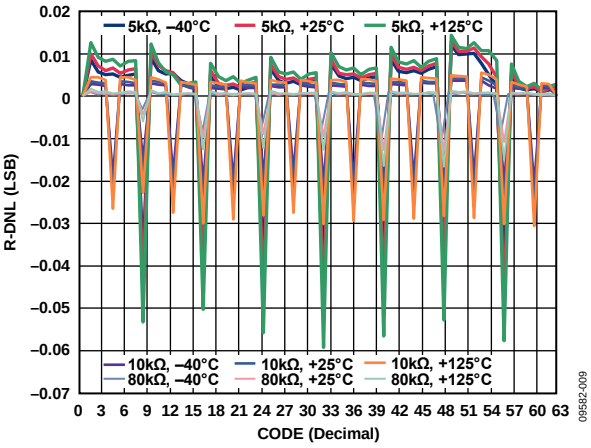


Figure 9. R-DNL vs. Code (AD5112)

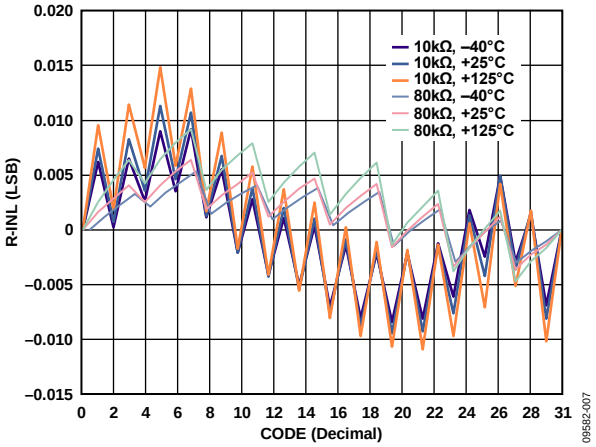


Figure 7. R-INL vs. Code (AD5114)

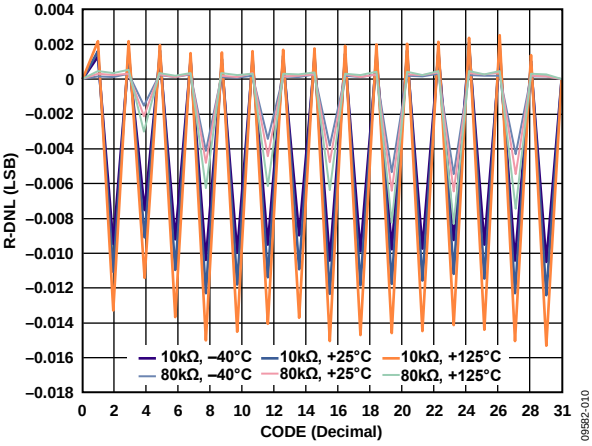


Figure 10. R-DNL vs. Code (AD5114)

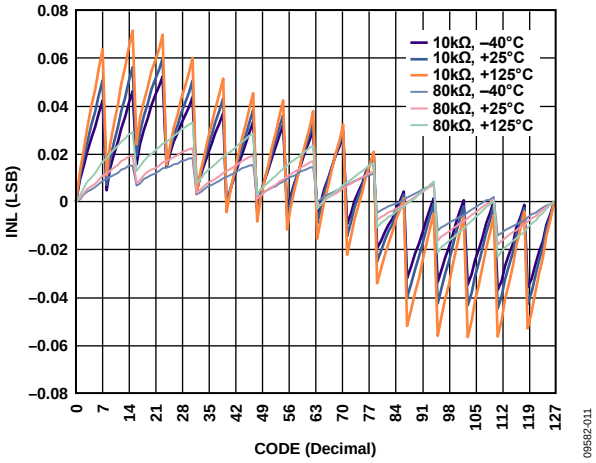


Figure 11. INL vs. Code (AD5110)

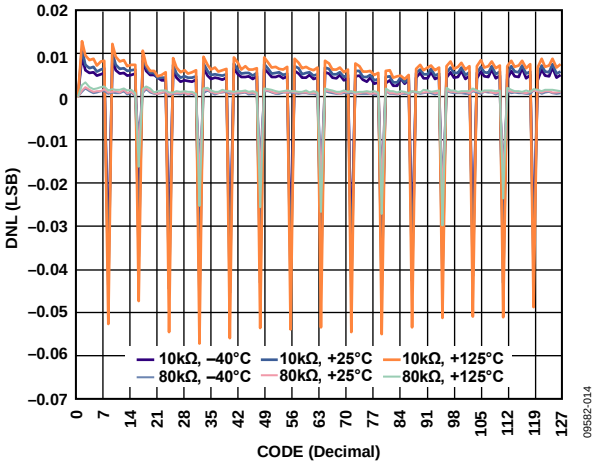


Figure 14. DNL vs. Code (AD5110)

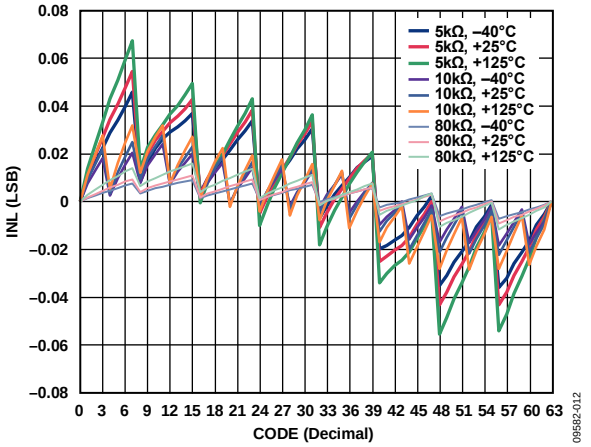


Figure 12. INL vs. Code (AD5112)

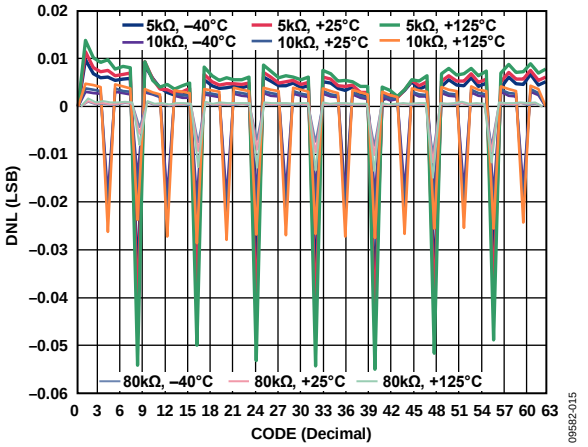


Figure 15. DNL vs. Code (AD5112)

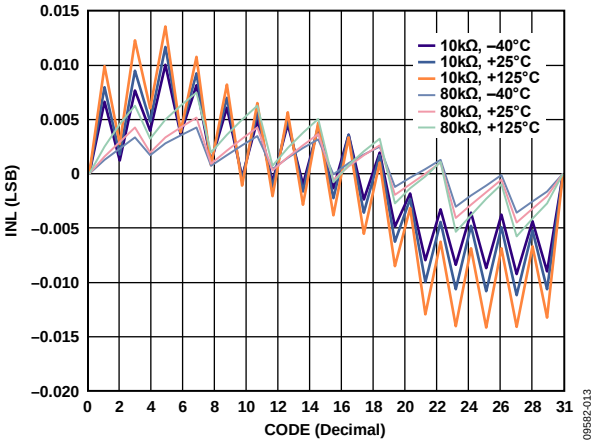


Figure 13. INL vs. Code (AD5114)

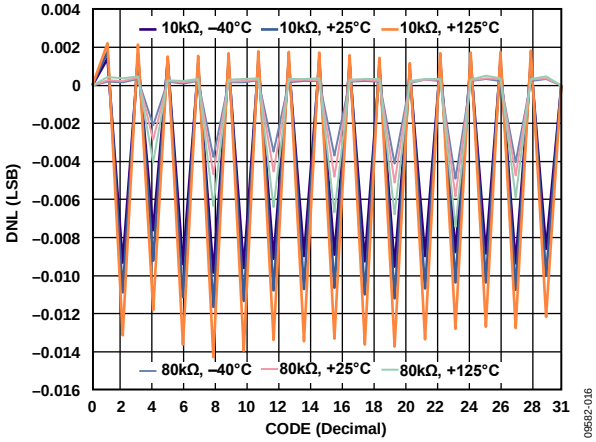


Figure 16. DNL vs. Code (AD5114)

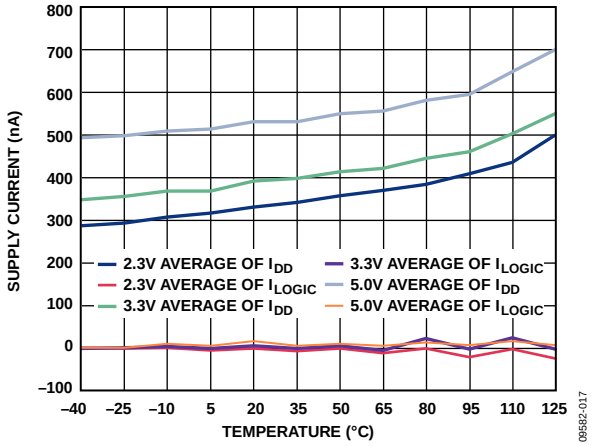


Figure 17. Supply Current vs. Temperature

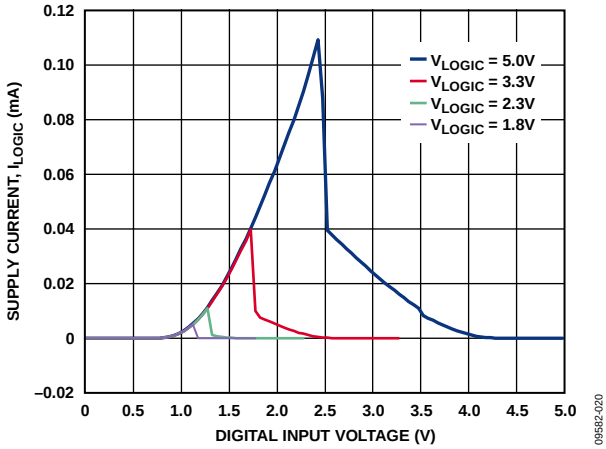


Figure 20. Supply Current (I_{LOGIC}) vs. Digital Input Voltage

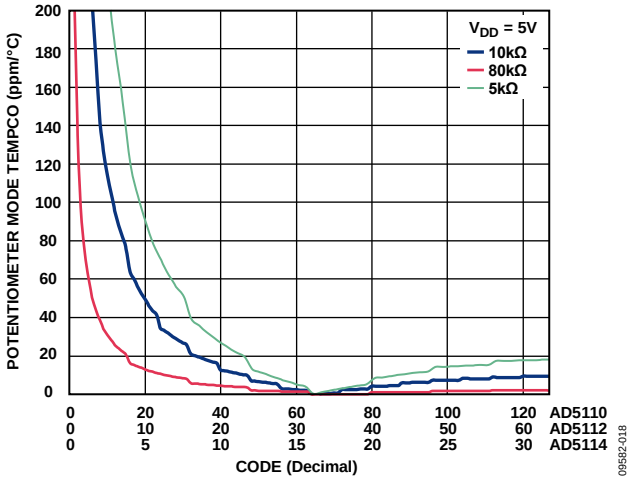


Figure 18. Potentiometer Mode Tempco ($(\Delta V_W/V_W)/\Delta T \times 10^6$) vs. Code

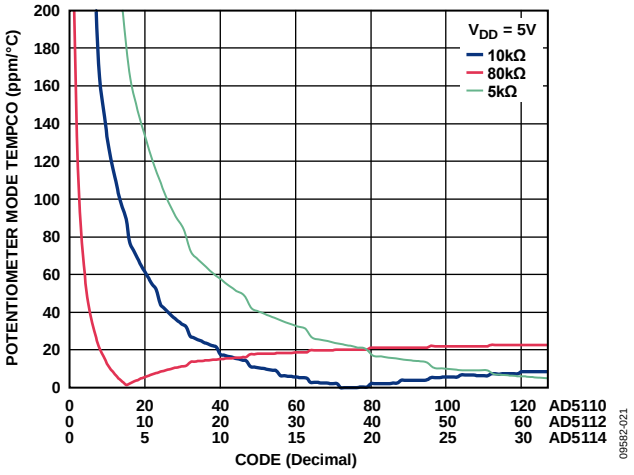


Figure 21. Rheostat Mode Tempco ($(\Delta R_{WB}/R_{WB})/\Delta T \times 10^6$) vs. Code

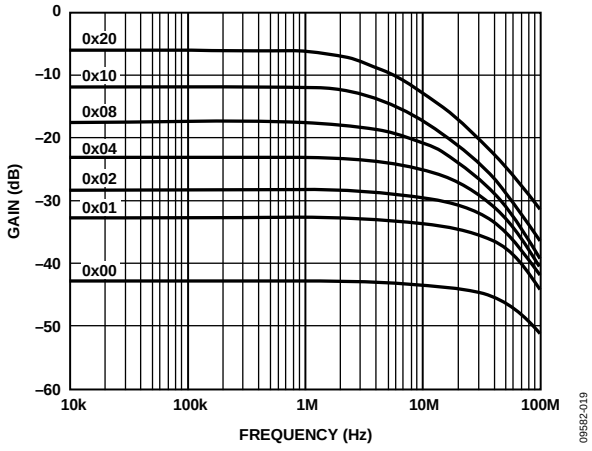


Figure 19. 5 kΩ Gain vs. Frequency vs. Code

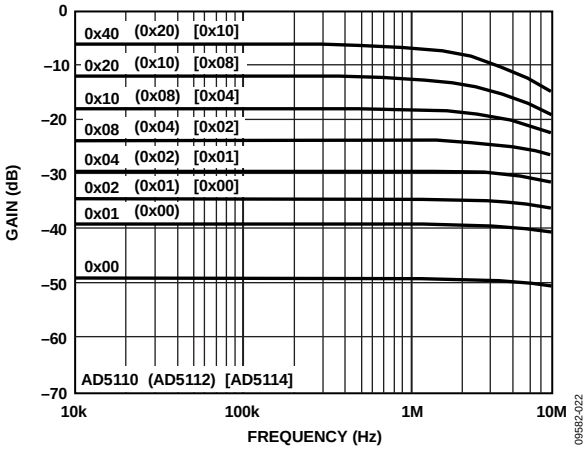


Figure 22. 10 kΩ Gain vs. Frequency vs. Code

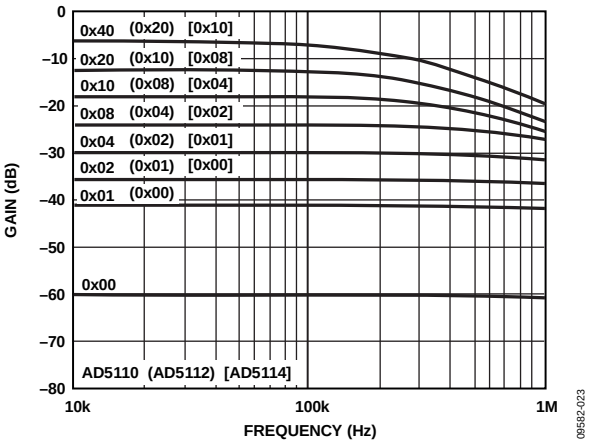


Figure 23. 80 kΩ Gain vs. Frequency vs. Code

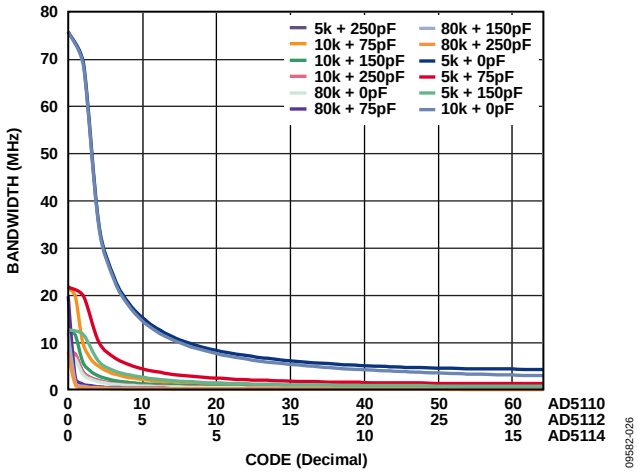


Figure 26. Maximum Bandwidth vs. Code vs. Net Capacitance

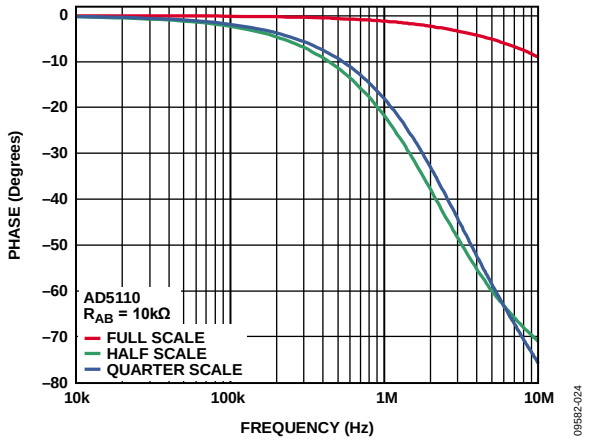


Figure 24. Normalized Phase Flatness vs. Frequency

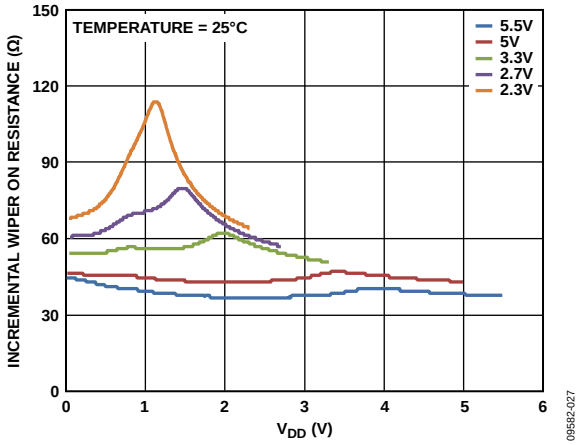


Figure 27. Incremental Wiper On Resistance vs. V_{DD}

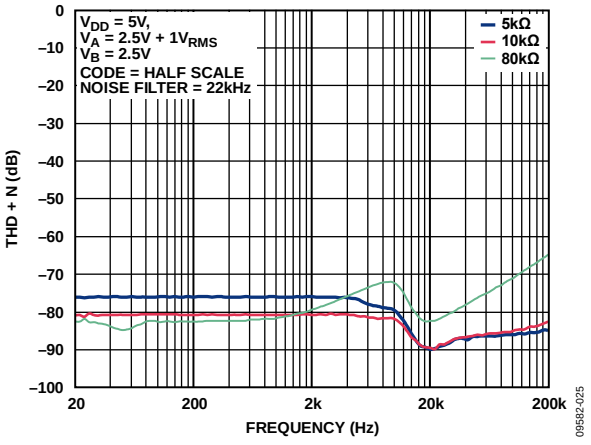


Figure 25. Total Harmonic Distortion + Noise (THD + N) vs. Frequency

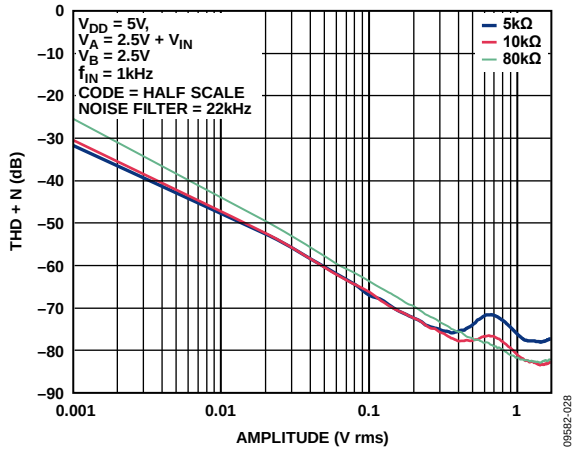


Figure 28. Total Harmonic Distortion + Noise (THD + N) vs. Amplitude

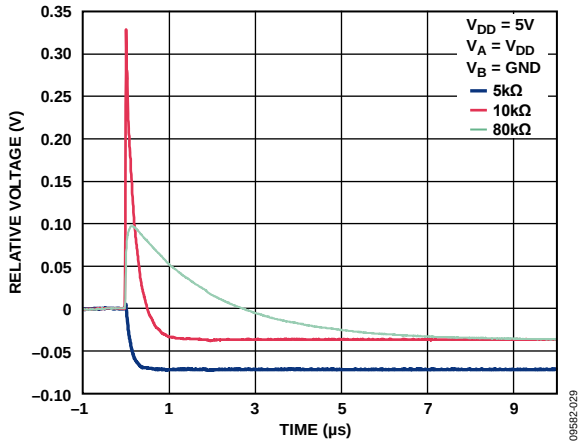


Figure 29. Maximum Transition Glitch

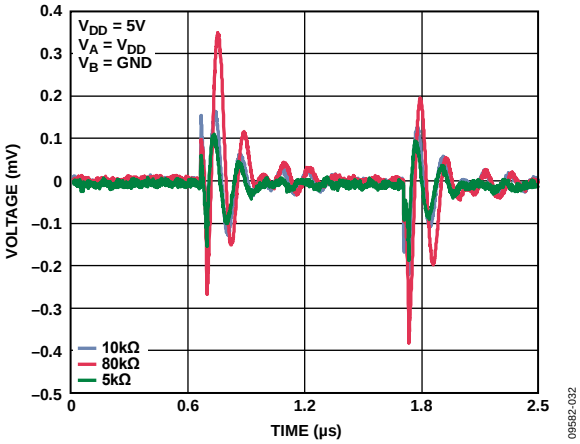


Figure 32. Digital Feedthrough

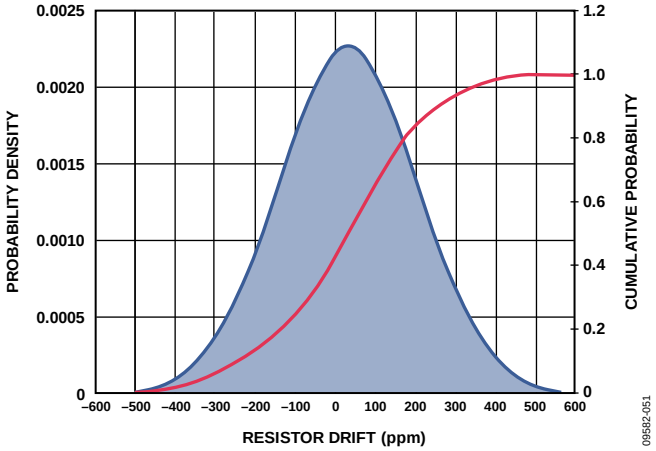


Figure 30. Resistor Lifetime Drift

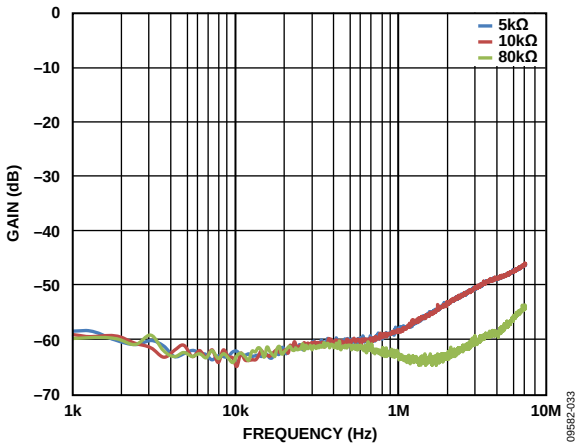


Figure 33. Shutdown Isolation vs. Frequency

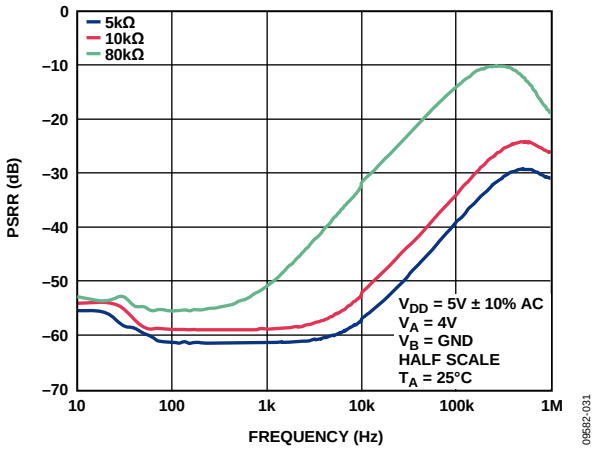


Figure 31. Power Supply Rejection Ratio (PSRR) vs. Frequency

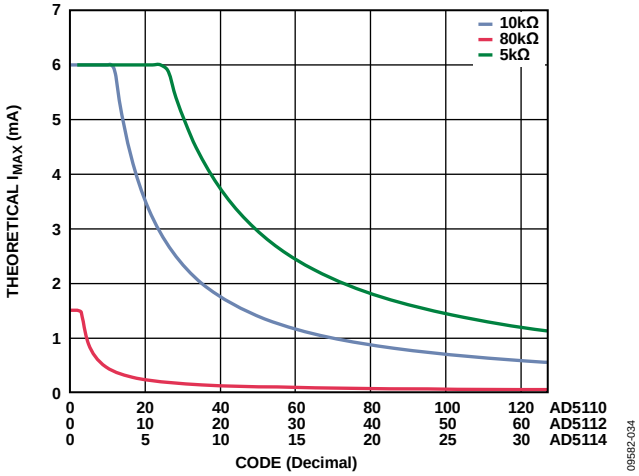


Figure 34. Theoretical Maximum Current vs. Code

TEST CIRCUITS

Figure 35 to Figure 40 define the test conditions used in the Specifications section.

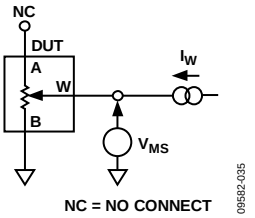


Figure 35. Resistor Position Nonlinearity Error (Rheostat Operation: R-INL, R-DNL)

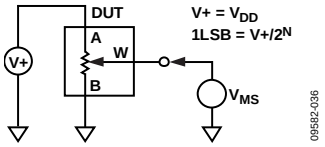


Figure 36. Potentiometer Divider Nonlinearity Error (INL, DNL)

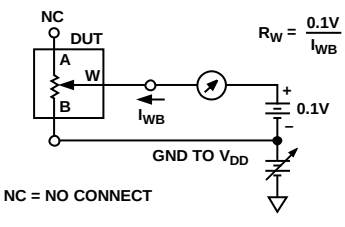


Figure 37. Wiper Resistance

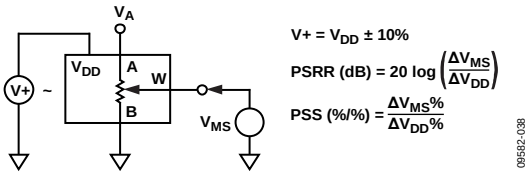


Figure 38. Power Supply Sensitivity (PSS, PSRR)

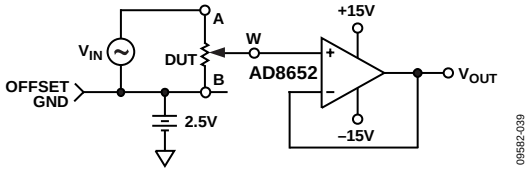


Figure 39. Gain and Phase vs. Frequency

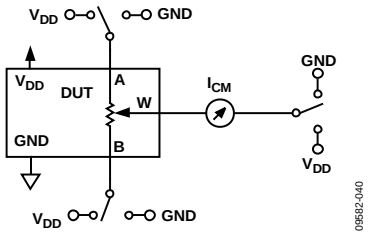


Figure 40. Common-Mode Leakage Current

THEORY OF OPERATION

The AD5110/AD5112/AD5114 digital programmable resistors are designed to operate as true variable resistors for analog signals within the terminal voltage range of GND < V_{TERM} < V_{DD}. The resistor wiper position is determined by the RDAC register contents. The RDAC register acts as a scratchpad register that allows unlimited changes of resistance settings.

The RDAC register can be programmed with any position setting using the I²C interface. Once a desirable wiper position is found, this value can be stored in the EEPROM memory. Thereafter, the wiper position is always restored to that position for subsequent power-up. The storing of EEPROM data takes approximately 18 ms; during this time, the device is locked and does not acknowledge any new command, thus preventing any changes from taking place.

RDAC REGISTER AND EEPROM

The RDAC register directly controls the position of the digital potentiometer wiper. For example, when the RDAC register is loaded with 0x3F (128-taps), the wiper is connected to full scale of the variable resistor. The RDAC register is a standard logic register; there is no restriction on the number of changes allowed.

It is possible to both write to and read from the RDAC register using the I²C interface (see Table 10).

The contents of the RDAC register can be stored to the EEPROM using Command 1 (Table 10). Thereafter, the RDAC register is always set at that position for any future on-off-on power supply sequence. It is possible to read back the data saved into the EEPROM with Command 6 in Table 10. In addition, the resistor tolerance error is saved within the EEPROM; this can be read back and used to calculate the end-to-end tolerance, providing an accuracy of 0.1%.

Low Wiper Resistance Feature

The AD5110/AD5112/AD5114 include extra steps to achieve a minimum resistance between Terminal W and Terminal A or Terminal B. These extra steps are called bottom scale and top scale. At bottom scale, the typical wiper resistance decreases from 70 Ω to 45 Ω. At top scale, the resistance between Terminal A and Terminal W is decreased by 1 LSB, and the total resistance is reduced to 70 Ω. The extra steps are not equal to 1 LSB and are not included in the INL, DNL, R-INL, and R-DNL specifications.

I²C SERIAL DATA INTERFACE

The AD5110/AD5112/AD5114 have 2-wire I²C-compatible serial interfaces. These devices can be connected to an I²C bus as a slave device under the control of a master device. See Figure 3 for a timing diagram of a typical write sequence.

The AD5110/AD5112/AD5114 support standard (100 kHz) and fast (400 kHz) data transfer modes. Support is not provided for 10-bit addressing and general call addressing.

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address and an R/W bit. The slave device corresponding to the transmitted address responds by pulling SDA low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its shift register.
2. If the R/$\overline{W}$ bit is set high, the master reads from the slave device. However, if the R/$\overline{W}$ bit is set low, the master writes to the slave device.
3. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.
4. When all data bits have been read or written, a stop condition is established. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master brings the SDA line low before the 10th clock pulse, and high during the 10th clock pulse to establish a stop condition.

I²C Address

The AD5110/AD5112/AD5114 each have two different slave address options available. See Table 9 for a list of slave addresses.

Table 9. Device Address Selection

Model	7-Bit I²C Device Address
AD511X[1] BCPZ Y[2]	0101111
AD511X[1] BCPZ Y[2]-1	0101100

[1] Model.
[2] Resistance.

INPUT SHIFT REGISTER

For the AD5110/AD5112/AD5114, the input shift register is 16 bits wide (see Figure 2). The 16-bit word consists of five unused bits (should be set to zero), followed by three control bits, and eight RDAC data bits. If the RDAC register is read from or written to in the AD5112, Bit DB0 is a don't care. The RDAC register is read from or written to in the AD5114, Bit DB0 and DB1 are don't cares. Data is loaded MSB first (Bit DB15).

The three control bits determine the function of the software command (Table 10). Figure 3 shows a timing diagram of a typical AD5110/AD5112/AD5114 write sequence.

The command bits (Cx) control the operation of the digital potentiometer and the internal EEPROM. The data bits (Dx) are the values that are loaded into the decoded register.

Table 10. Command Operation Truth Table

Command Number	Command			Data[1]								Operation
	DB10		DB8	DB7							DB0	
	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	X	X	X	X	X	X	X	X	No operation
1	0	0	1	X	X	X	X	X	X	X	X	Write contents of RDAC register to EEPROM
2	0	1	0	7 MSB	6	5	4	3	2	1[2]	0[2, 3] LSB	Write contents of serial register data to RDAC
				1	0	0	0	0	0	0	0	Top scale
				1	1	1	1	1	1	1	1	Bottom scale
3	0	1	1	X	X	X	X	X	X	X	A0	Software shutdown 0: shutdown off 1: shutdown on
4	1	0	0	X	X	X	X	X	X	X	X	Software reset: refresh RDAC register with EEPROM
5	1	0	1	X	X	X	X	X	X	X	X	Read contents of RDAC register
6	1	1	0	X	X	X	X	X	X	A1	A0	Read contents of EEPROM

A1	A0	Data
0	0	Wiper position saved
0	1	Resistor tolerance

[1] X is don't care.
[2] In the AD5114, this bit is a don't care.
[3] In the AD5112, this bit is a don't care.

WRITE OPERATION

When writing to the AD5110/AD5112/AD5114, the user must begin with a start command followed by an address byte (R/$\overline{W}$ = 0), after which the AD5110/AD5112/AD5114 acknowledge that it is prepared to receive data by pulling SDA low.

Two bytes of data are then written to the DAC, the most significant byte, followed by the least significant byte. Both of these data bytes are acknowledged by the AD5110/AD5112/AD5114. A stop condition follows. The write operations for the AD5110/AD5112/AD5114 are shown in Figure 41, Figure 42, and Figure 43.

A repeated write function gives the user flexibility to update the device a number of times after addressing the part only once, as shown in Figure 44.

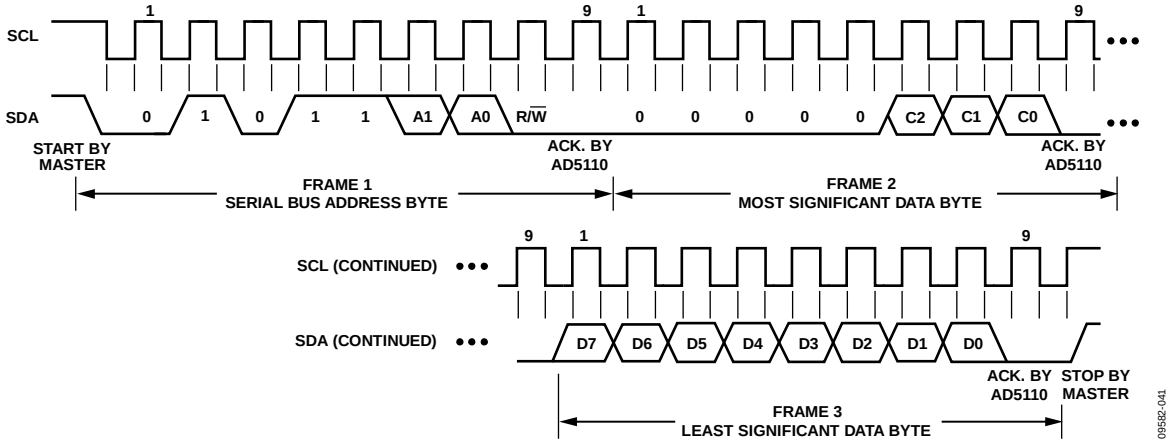


Figure 41. AD5110 Interface Write Command

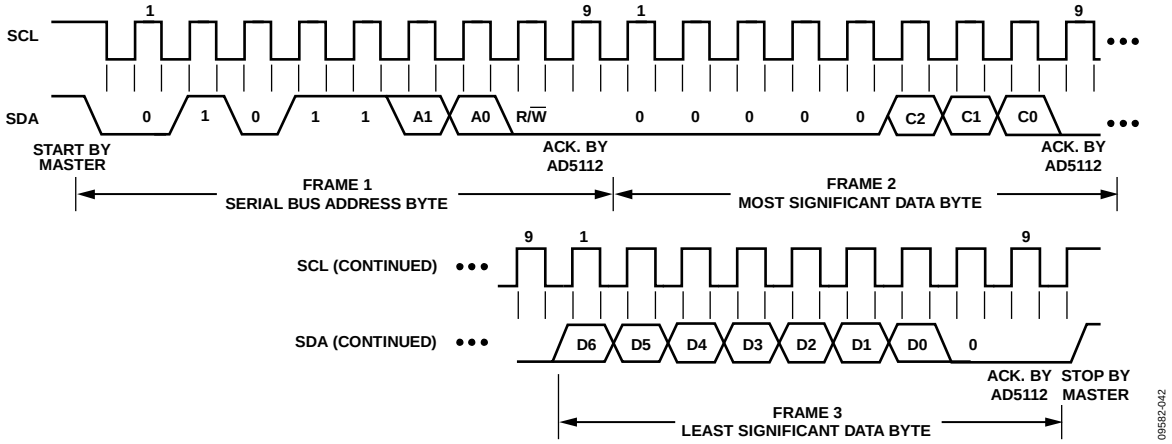


Figure 42. AD5112 Interface Write Command

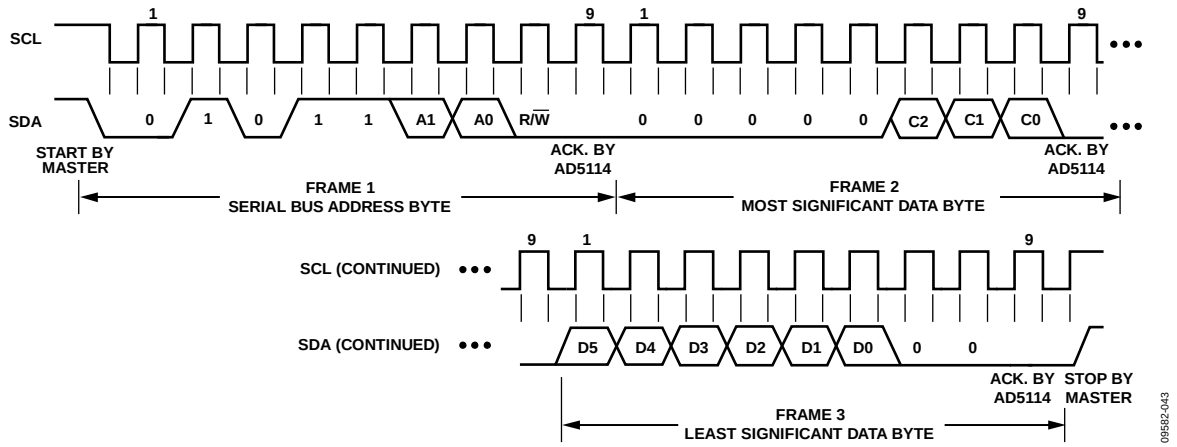


Figure 43. AD5114 Interface Write Command

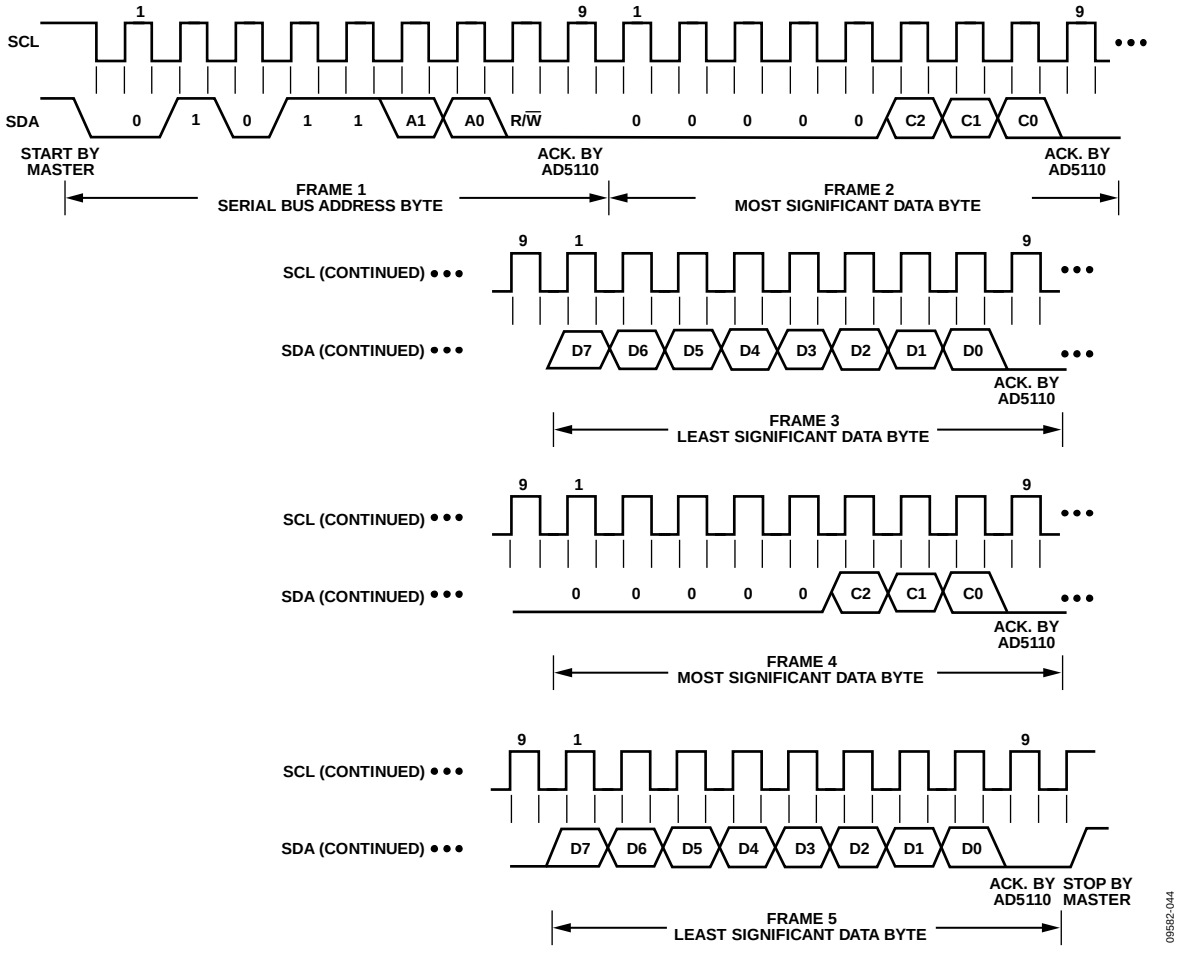


Figure 44. AD5110 Interface Multiple Write

EEPROM WRITE ACKNOWLEGDE POLLING

After each write operation to the EEPROM, an internal write cycle begins. The I²C interface of the device is disabled. To determine if the internal write cycle is complete and the I²C interface is enabled, interface polling can be executed. I²C interface polling can be conducted by sending a start condition, followed by the slave address and the write bit. If the I²C interface responds with an acknowledge, the write cycle is complete, and the interface is ready to proceed with further operations. Otherwise, I²C interface polling can be repeated until it succeeds.

READ OPERATION

The AD5110/AD5112/AD5114 allow read back of the contents of the RDAC register and EEPROM memory through the I²C interface by using Command 6 (see Table 10).

When reading data back from the AD5110/AD5112/AD5114, the user must first issue a readback command to the device. This begins with a start command, followed by an address byte (R/$\overline{W}$ = 0), after which the AD5110/AD5112/AD5114 acknowledges that it is prepared to receive data by pulling SDA low.

Two bytes of data are then written to the AD5110/AD5112/AD5114, the most significant byte followed by the least significant byte. Both of these data bytes are acknowledged by the AD5110/AD5112/AD5114. A stop condition follows. These bytes contain the read instruction, which enables readback of the RDAC register, EEPROM memory. The user can then read back the data. This begins with a start command followed by an address byte (R/$\overline{W}$ = 1), after which the device acknowledges that it is prepared to transmit data by pulling SDA low. Two bytes of data are then read from the device, which are both acknowledged by the master, as shown in Figure 45. A stop condition follows. If the master does not acknowledge the first byte, then the second byte is not transmitted by the AD5110/AD5112/AD5114.

The AD5110/AD5112/AD5114 does not support repeat readback.

RESET

The AD5110/AD5112/AD5114 can be reset by executing Command 4 (see Table 10). The reset command loads the RDAC register with the contents of the EEPROM and takes approximately 25 µs. EEPROM is pre-loaded to midscale at the factory, and initial power-up is, accordingly, at midscale.

SHUTDOWN MODE

The AD5110/AD5112/AD5114 can be shut down by executing the software shutdown command, Command 3 (see Table 10). This feature places the RDAC in a zero-power-consumption state where Terminal A is open-circuited and the wiper, Terminal W is connected to Terminal B but a finite wiper resistance of 45 Ω is present. The part can be taken out of shutdown mode by executing Command 3 (see Table 10) and setting Bit DB0 to 0.

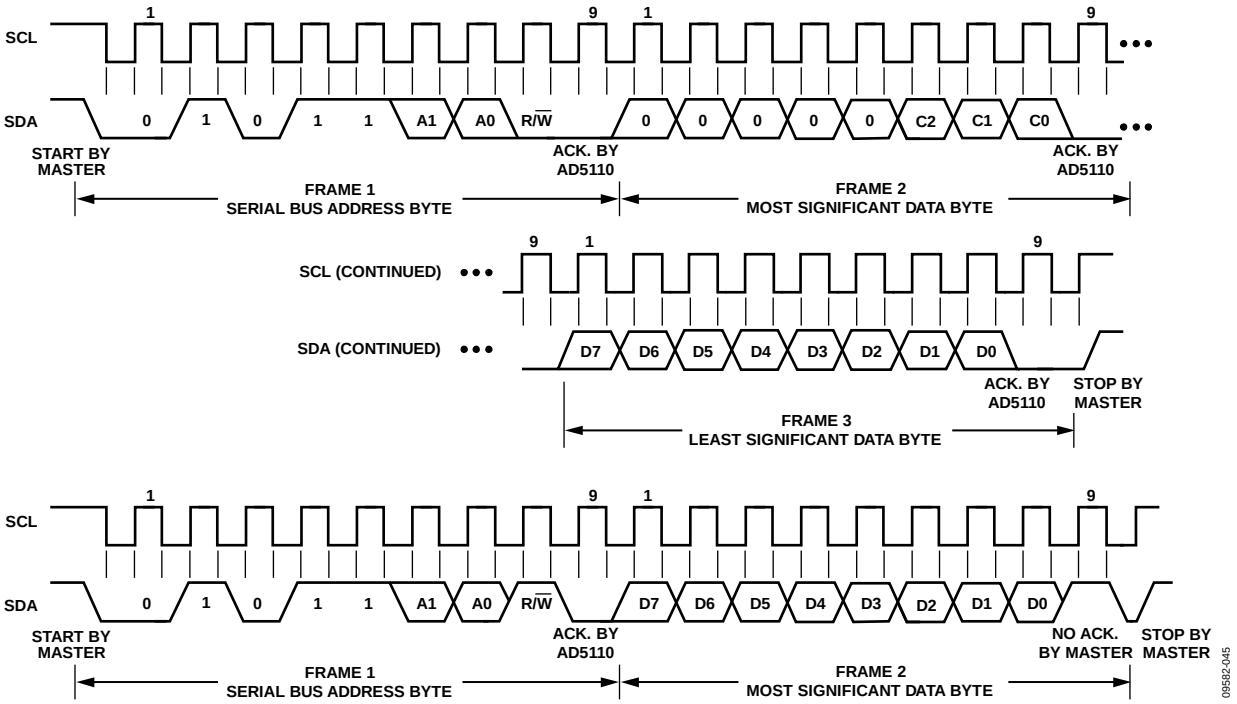


Figure 45. AD5110 Interface Read Command

RDAC ARCHITECTURE

To achieve optimum performance, Analog Devices, Inc., has patented the RDAC segmentation architecture for all the digital potentiometers. In particular, the AD5110/AD5112/AD5114 employ a two-stage segmentation approach as shown in Figure 46. The AD5110/AD5112/AD5114 wiper switch is designed with the transmission gate CMOS topology and with the gate voltage derived from V_{DD}.

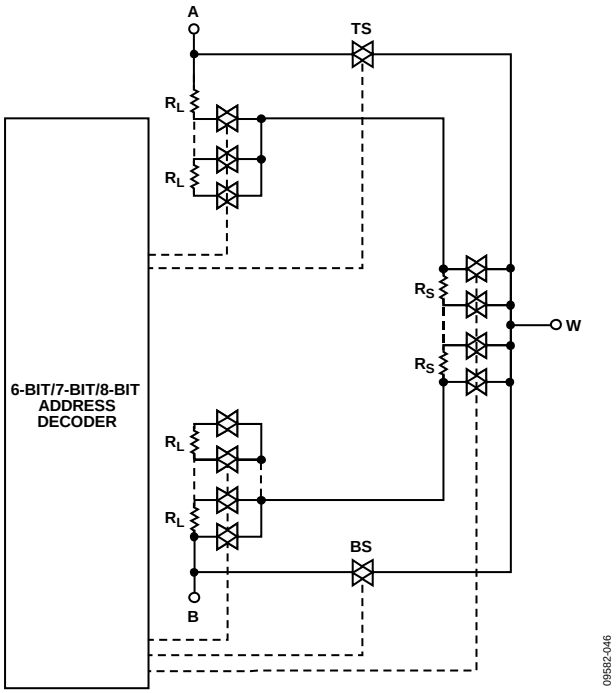


Figure 46. AD5110/AD5112/AD5114 Simplified RDAC Circuit

Top Scale/Bottom Scale Architecture

In addition, the AD5110/AD5112/AD5114 include a new feature to reduce the resistance between terminals. These extra steps are called bottom scale and top scale. At bottom scale, the typical wiper resistance decreases from 70 Ω to 45 Ω. At top scale, the resistance between Terminal A and Terminal W is decreased by 1 LSB, and the total resistance is reduced to 70 Ω. The extra steps are not equal to 1 LSB and are not included in the INL, DNL, R-INL, and R-DNL specifications.

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation—±8% Resistor Tolerance

The AD5110/AD5112/AD5114 operate in rheostat mode when only two terminals are used as a variable resistor. The unused terminal can be floating or tied to the Terminal W as shown in Figure 47.

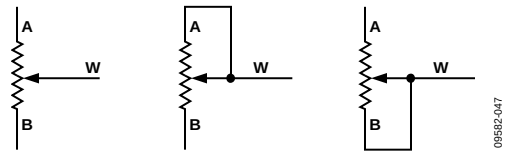


Figure 47. Rheostat Mode Configuration

The nominal resistance between Terminal A and Terminal B, R_{AB}, is available in 5 kΩ, 10 kΩ, and 80 kΩ and has 32/64/128 tap points accessed by the wiper terminal. The 5-/6-/7-bit data in the RDAC latch is decoded to select one of the 32/64/128 possible wiper settings. The general equations for determining the digitally programmed output resistance between the W terminal and B terminal are

AD5110:

$$R_{WB} = R_{BS} \quad \text{Bottom scale (0xFF)} \quad (1)$$

$$R_{WB}(D) = \frac{D}{128} \times R_{AB} + R_W \quad \text{From 0x00 to 0x80} \quad (2)$$

AD5112:

$$R_{WB} = R_{BS} \quad \text{Bottom scale (0xFF)} \quad (3)$$

$$R_{WB}(D) = \frac{D}{64} \times R_{AB} + R_W \quad \text{From 0x00 to 0x40} \quad (4)$$

AD5114:

$$R_{WB} = R_{BS} \quad \text{Bottom scale (0xFF)} \quad (5)$$

$$R_{WB}(D) = \frac{D}{32} \times R_{AB} + R_W \quad \text{From 0x00 to 0x20} \quad (6)$$

where:
D is the decimal equivalent of the binary code in the 5-/6-/7-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance.
R_{BS} is the wiper resistance at bottom scale

Similar to the mechanical potentiometer, the resistance of the RDAC between the W terminal and the A terminal also produces a digitally controlled complementary resistance, R_{WA}. R_{WA} also gives a maximum of 8% absolute resistance error. R_{WA} starts at the maximum resistance value and decreases as the data loaded into the latch increases. The general equations for this operation are

AD5110:

$$R_{AW} = R_{AB} + R_W \quad \text{Bottom scale (0xFF)} \quad (7)$$

$$R_{AW}(D) = \frac{128 - D}{128} \times R_{AB} + R_W \quad \text{From 0x00 to 0x7F} \quad (8)$$

$$R_{AW} = R_{TS} \quad \text{Top scale (0x80)} \quad (9)$$

AD5112:

$$R_{AW} = R_{AB} + R_W \quad \text{Bottom scale (0xFF)} \quad (10)$$

$$R_{AW}(D) = \frac{64 - D}{64} \times R_{AB} + R_W \quad \text{From 0x00 to 0x3F} \quad (11)$$

$$R_{AW} = R_{TS} \quad \text{Top scale (0x40)} \quad (12)$$

AD5114:

$$R_{AW} = R_{AB} + R_W \quad \text{Bottom scale (0xFF)} \quad (13)$$

$$R_{AW}(D) = \frac{32 - D}{32} \times R_{AB} + R_W \quad \text{From 0x00 to 0x1F} \quad (14)$$

$$R_{AW} = R_{TS} \quad \text{Top scale (0x20)} \quad (15)$$

where:
D is the decimal equivalent of the binary code in the 5-/6-/7-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance.
R_{TS} is the wiper resistance at top scale.

In the bottom-scale condition or top-scale condition, a finite total wiper resistance of 45 Ω is present. Regardless of which setting the part is operating in, take care to limit the current between Terminal A to Terminal B, Terminal W to Terminal A, and Terminal W to Terminal B, to the maximum continuous current of ±6 mA or to the pulse current specified in Table 6. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Calculating the Actual End-to-End Resistance

The resistance tolerance is stored in the internal memory during factory testing. The actual end-to-end resistance can, therefore, be calculated, which is valuable for calibration, tolerance matching, and precision applications.

The resistance tolerance in percentage is stored in fixed-point format, using an 8-bit sign magnitude binary. The data can be read back by executing Command 6 and setting Bit DB0 (A0). The MSB is the sign bit (0 = − and 1 = +) and the next four bits are the integer part, the fractional part is represented by the three LSBs, as shown in Table 11.

Table 11. Tolerance Format

Data Byte								
DB7	**DB6**	**DB5**	**DB4**	**DB3**		**DB2**	**DB1**	**DB0**
Sign	2^4	2^3	2^2	2^1	.	2^{-1}	2^{-2}	2^{-3}

For example, if R_{AB} = 10 kΩ and the data readback shows 01010010, the end-to-end resistance can be calculated as,

if,
DB[7] is 0 = negative
DB[6:3] is 1010 = 10
DB[2:0] is 010 = $2 \times 2^{-3} = 0.25$

then,
tolerance = −10.25% and, therefore, R_{AB} = 8.975 kΩ

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A that is proportional to the input voltage at A to B, as shown in Figure 48. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A-to-B, W-to-A, and W-to-B can be at either polarity.

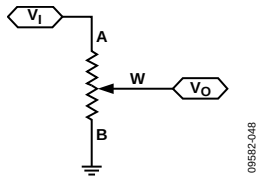


Figure 48. Potentiometer Mode Configuration

Connecting Terminal A to 5 V and Terminal B to ground produces an output voltage at the Wiper W to Terminal B ranging from 0 V to 5 V. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to Terminal A and Terminal B, is:

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} \times V_A + \frac{R_{AW}(D)}{R_{AB}} \times V_B \quad (16)$$

where:
$R_{WB}(D)$ can be obtained from Equation 1 to Equation 6.
$R_{AW}(D)$ can be obtained from Equation 7 to Equation 15.

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors, R_{AW} and R_{WB}, and not the absolute values. Therefore, the temperature drift reduces to 5 ppm/°C.

TERMINAL VOLTAGE OPERATING RANGE

The AD5110/AD5112/AD5114 are designed with internal ESD diodes for protection. These diodes also set the voltage boundary of the terminal operating voltages. Positive signals present on Terminal A, Terminal B, or Terminal W that exceed V_{DD} are clamped by the forward-biased diode. There is no polarity constraint between V_A, V_W, and V_B, but they cannot be higher than V_{DD} or lower than GND.

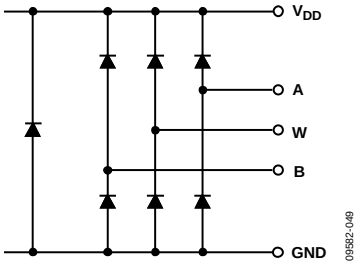


Figure 49. Maximum Terminal Voltages Set by V_{DD} and GND

POWER-UP SEQUENCE

Because there are diodes to limit the voltage compliance at Terminal A, Terminal B, and Terminal W (Figure 49), it is important to power V_{DD} first before applying any voltage to Terminal A, Terminal B, and Terminal W. Otherwise, the diode is forward-biased such that V_{DD} is powered unintentionally. The ideal power-up sequence is GND, V_{DD}, V_{LOGIC}, digital inputs, and V_A, V_B, and V_W. The order of powering V_A, V_B, V_W, and digital inputs is not important as long as they are powered after V_{DD} and V_{LOGIC}. Regardless of the power-up sequence and the ramp rates of the power supplies, once V_{LOGIC} is powered, the power-on preset activates, which restores EEPROM values to the RDAC registers.

LAYOUT AND POWER SUPPLY BIASING

It is always a good practice to use compact, minimum lead length layout design. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance. It is also good practice to bypass the power supplies with quality capacitors. Low equivalent series resistance (ESR) 1 µF to 10 µF tantalum or electrolytic capacitors should be applied at the supplies to minimize any transient disturbance and to filter low frequency ripple. Figure 50 illustrates the basic supply bypassing configuration for the AD5110/AD5112/AD5114.

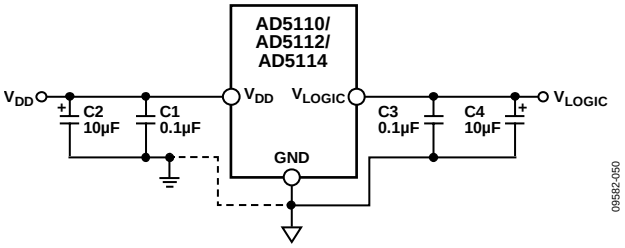


Figure 50. Power Supply Bypassing

OUTLINE DIMENSIONS

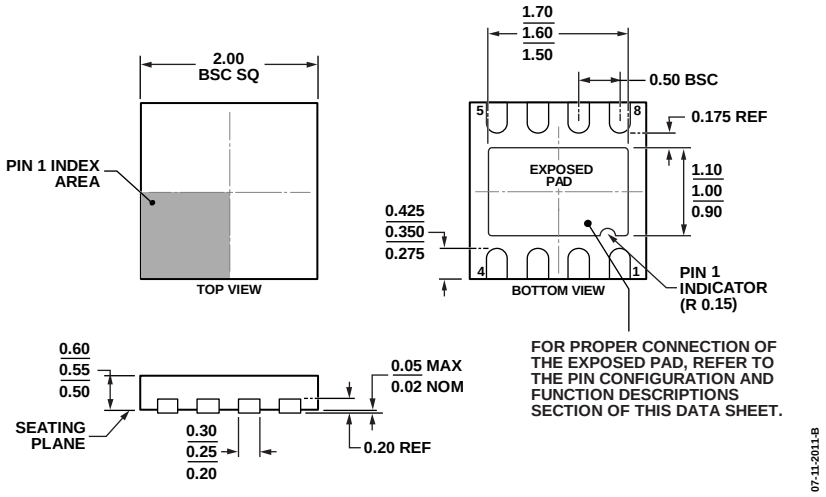


Figure 51. 8-Lead Frame Chip Scale Package[LFCSP_UD]
2.00 mm × 2.00 mm Body, Ultra Thin, Dual Lead
(CP-8-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	R_{AB} (kΩ)	Resolution	Temperature Range	Package Description	I^2C Address	Package Option	Branding
AD5110BCPZ10-RL7	10	128	−40°C to +125°C	8-Lead LFCSP_UD	0101111	CP-8-10	4J
AD5110BCPZ10-500R7	10	128	−40°C to +125°C	8-Lead LFCSP_UD	0101111	CP-8-10	4J
AD5110BCPZ10-1-RL7	10	128	−40°C to +125°C	8-Lead LFCSP_UD	0101100	CP-8-10	4H
AD5110BCPZ80-RL7	80	128	−40°C to +125°C	8-Lead LFCSP_UD	0101111	CP-8-10	4L
AD5110BCPZ80-500R7	80	128	−40°C to +125°C	8-Lead LFCSP_UD	0101111	CP-8-10	4L
AD5110BCPZ80-1-RL7	80	128	−40°C to +125°C	8-Lead LFCSP_UD	0101100	CP-8-10	4K
AD5112BCPZ5-RL7	5	64	−40°C to +125°C	8-Lead LFCSP_UD	0101111	CP-8-10	7P
AD5112BCPZ5-500R7	5	64	−40°C to +125°C	8-Lead LFCSP_UD	0101111	CP-8-10	7P
AD5112BCPZ5-1-RL7	5	64	−40°C to +125°C	8-Lead LFCSP_UD	0101100	CP-8-10	7N
AD5112BCPZ10-RL7	10	64	−40°C to +125°C	8-Lead LFCSP_UD	0101111	CP-8-10	7L
AD5112BCPZ10-500R7	10	64	−40°C to +125°C	8-Lead LFCSP_UD	0101111	CP-8-10	7L
AD5112BCPZ10-1-RL7	10	64	−40°C to +125°C	8-Lead LFCSP_UD	0101100	CP-8-10	7K
AD5112BCPZ80-RL7	80	64	−40°C to +125°C	8-Lead LFCSP_UD	0101111	CP-8-10	7R
AD5112BCPZ80-500R7	80	64	−40°C to +125°C	8-Lead LFCSP_UD	0101111	CP-8-10	7R
AD5112BCPZ80-1-RL7	80	64	−40°C to +125°C	8-Lead LFCSP_UD	0101100	CP-8-10	7Q
AD5114BCPZ10-RL7	10	32	−40°C to +125°C	8-Lead LFCSP_UD	0101111	CP-8-10	81
AD5114BCPZ10-500R7	10	32	−40°C to +125°C	8-Lead LFCSP_UD	0101111	CP-8-10	81
AD5114BCPZ10-1-RL7	10	32	−40°C to +125°C	8-Lead LFCSP_UD	0101100	CP-8-10	80
AD5114BCPZ80-RL7	80	32	−40°C to +125°C	8-Lead LFCSP_WD	0101111	CP-8-10	83
AD5114BCPZ80-500R7	80	32	−40°C to +125°C	8-Lead LFCSP_WD	0101111	CP-8-10	83
AD5114BCPZ80-1-RL7	80	32	−40°C to +125°C	8-Lead LFCSP_WD	0101100	CP-8-10	82
EVAL-AD5110SDZ				Evaluation Board			

[1] Z = RoHS Compliant Part.
[2] The EVAL-AD5110SDZ has an R_{AB} of 10 kΩ.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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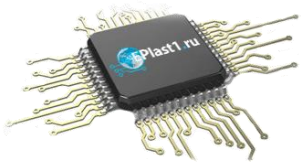
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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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