SN65HVD485E Half-Duplex RS-485 Transceiver

1 Features

- Bus-Pin ESD Protection up to 15 kV
- 1/2 Unit Load: up to 64 Nodes on a Bus
- Bus-Open-Failsafe Receiver
- Glitch-Free Power-Up and Power-Down Bus Inputs and Outputs
- Available in Small VSSOP-8 Package
- Meets or Exceeds the Requirements of the TIA/EIA-485A Standard
- Industry-Standard SN75176 Footprint

2 Applications

- Motor Control
- Power Inverters
- Industrial Automation
- Building Automation Networks
- Industrial Process Control
- Battery-Powered Applications
- Telecommunications Equipment

3 Description

The SN65HVD485E device is a half-duplex transceiver designed for RS-485 data bus networks. Powered by a 5-V supply, it is fully compliant with the TIA/EIA-485A standard. This device is suitable for data transmission up to 10 Mbps over long twisted-pair cables and is designed to operate with very low supply current, typically less than 2 mA, exclusive of the load. When the device is in the inactive shutdown mode, the supply current drops below 1 mA.

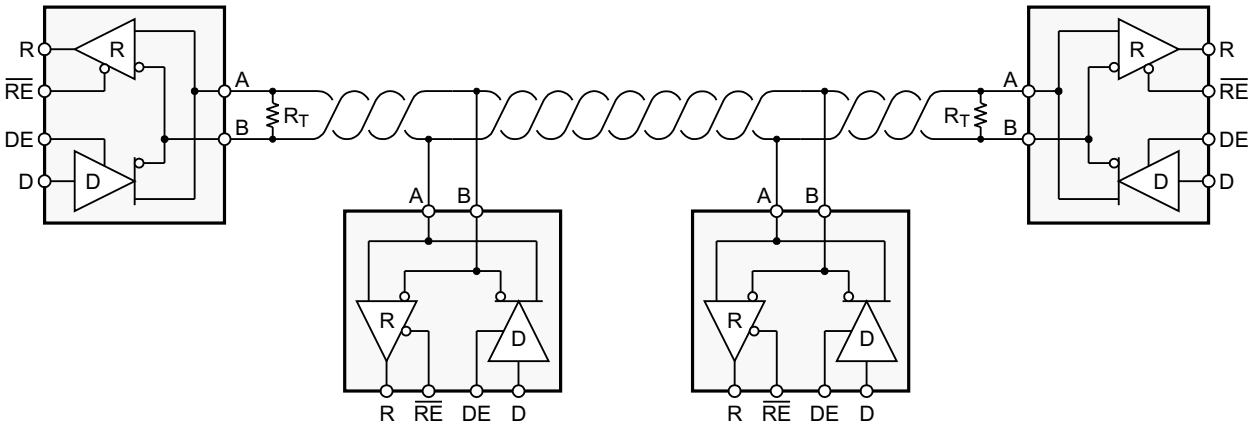
The wide common-mode range and high ESD protection levels of this device make it suitable for demanding applications such as: electrical inverters, status/command signals across telecom racks, cabled chassis interconnects, and industrial automation networks where noise tolerance is essential. The SN65HVD485E device matches the industry-standard footprint of the SN75176 device. Power-on reset circuits keep the outputs in a high-impedance state until the supply voltage has stabilized. A thermal-shutdown function protects the device from damage due to system-fault conditions. The SN65HVD485E device is characterized for operation from –40°C to 85°C air temperature.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVD485E	SOIC (8)	4.91 mm × 3.90 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (July 2015) to Revision E — **Page**

- Changed 3.3 V To: 5 V at pin V_{CC} in Figure 20 ... 16

Changes from Revision C (March 2007) to Revision D — **Page**

- Added *Pin Configuration and Functions* section, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table ... 1
- Changed *Thermal Information* table ... 5
- Added *Power Dissipation Characteristics* table ... 6

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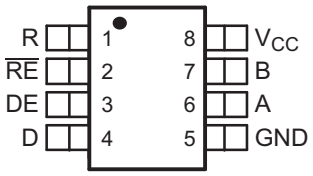
5 Device Comparison Table

Improved Replacement for Devices

PART NUMBER	REPLACE WITH	BENEFITS
ADM485	SN65HVD485E	Better ESD protection (±15 kV versus unspecified) Faster signaling rate (10 Mbps versus 5 Mbps) More nodes on a bus (64 versus 32) Wider power supply tolerance (10% vs 5%)
SP485E	SN65HVD485E	More nodes on a bus (64 versus 32) Wider power supply tolerance (10% versus 5%)
LMS485E	SN65HVD485E	Higher signaling rate (10 Mbps versus 2.5 Mbps) More nodes on a bus (64 versus 32) Wider power supply tolerance (10% versus 5%)
DS485	SN65HVD485E	Higher signaling rate (10 Mbps versus 2.5 Mbps) Better ESD (±15 kV versus ±2 kV) More nodes on a bus (64 versus 32) Wider power supply tolerance (10% versus 5%)
LTC485	SN65HVD485E	Better ESD (±15 kV versus ±2 kV) Wider power supply tolerance (10% versus 5%)
MAX485E	SN65HVD485E	Higher signaling rate (10 Mbps versus 2.5 Mbps) More nodes on a bus (64 versus 32) Wider power supply tolerance (10% versus 5%)
ST485E	SN65HVD485E	Higher signaling rate (10 Mbps versus 5 Mbps) Wider power supply tolerance (10% versus 5%)
ISL8485E	SN65HVD485E	More nodes on a bus (64 versus 32) Faster signaling rate (10 Mbps versus 5 Mbps)

6 Pin Configuration and Functions

D, DGK, P Packages
8-Pin SOIC, VSSOP, PDIP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital input	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low
V_{CC}	8	Supply	4.5-V to 5.5-V supply

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	7	V
	Voltage range at A or B	–9	14	V
	Voltage range at any logic pin	–0.3	V_{CC} + 0.3	V
	Receiver output current	–24	24	mA
	Voltage input range, transient pulse, A and B, through 100 Ω (see Figure 15)	–50	50	V
T_J	Junction temperature	170	170	°C
	Continuous total power dissipation	Refer to *Dissipation Ratings*		
T_{stg}	Storage temperature	–65	130	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	Bus pins and GND	±15000	V
			All pins	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)		–7		12	V
V_{IH}	High-level input voltage (D, DE, or RE inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (D, DE, or RE inputs)		0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_O	Output current	Driver	–60		60	mA
		Receiver	–8		8	
R_L	Differential load resistance		54	60		Ω
$1/t_{UI}$	Signaling rate		0		10	Mbps
T_A	Operating free-air temperature		–40		85	°C
T_J	Junction temperature (2)		–40		130	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.
(2) See *Thermal Information* for information on maintenance of this specification for the DGK package.

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7.4 Thermal Information

THERMAL METRIC[1]		SN65HVD485E			UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	127	180	153	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.4	66	40.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.6	108	28.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.9	4.6	17.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47	73.1	28.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) See the *Package Thermal Characterization Methodologies* application note (SZZA003) for an explanation of this parameter.

7.5 Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
$\lvert V_{OD}\rvert$	Differential output voltage	I_O = 0, No load	3	4.3		V
		R_L = 54 Ω (see Figure 3)	1.5	2.3		
		V_{TEST} = –7 V to 12 V (see Figure 4)	1.5			
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage	See Figure 3 and Figure 4	–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 5	1	2.6	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		–0.1	0	0.1	V
$V_{OC(PP)}$	Common-mode output voltage	See Figure 5		500		mV
I_{OZ}	High-impedance output current	See receiver input currents				μA
I_I	Input current	D, DE	–100		100	μA
I_{OS}	Short-circuit output current	–7 V ≤ V_O ≤ 12 V (see Figure 9)	–250		250	mA

(1) All typical values are at 25°C and with a 5-V supply.

7.6 Electrical Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = –8 mA		–85	–10	mV
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA	–200	–115		mV
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT-}$)			30		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –8 mA (see Figure 10)	4	4.6		V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OH} = 8 mA (see Figure 10)		0.15	0.4	V
I_{OZ}	High-impedance-state output current	V_O = 0 to V_{CC}, $\overline{RE}$ = V_{CC}	–1		1	μA
I_I	Bus input current	V_{IH} = 12 V, V_{CC} = 5 V			0.5	mA
		V_{IH} = 12 V, V_{CC} = 0			0.5	
		V_{IH} = –7 V, V_{CC} = 5 V	–0.4			
		V_{IH} = –7 V, V_{CC} = 0	–0.4			
I_{IH}	High-level input current ($\overline{RE}$)	V_{IH} = 2 V	–60	–30		μA
I_{IL}	Low-level input current ($\overline{RE}$)	V_{IL} = 0.8 V	–60	–30		μA
C_{diff}	Differential input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V		7		pF

(1) All typical values are at 25°C and with a 5-V supply.

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7.7 Power Dissipation Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{(AVG)}$	Average power dissipation	R_L = 54 Ω, Input to D is a 10 Mbps 50% duty cycle square wave V_{CC} at 5.5 V, T_J = 130°C			219	mW
T_{SD}	Thermal shut-down junction temperature			165		°C

7.8 Supply Current

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{CC}	Driver and receiver enabled	D at V_{CC} or open or 0 V,	DE at V_{CC}, RE at 0 V, No load			2	mA
	Driver and receiver disabled	D at V_{CC} or open,	DE at 0 V, RE at V_{CC}			1	mA

(1) All typical values are at 25°C and with a 5-V supply.

7.9 Switching Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 54 Ω, C_L = 50 pF (see Figure 6)			30	ns
t_{PHL}	Propagation delay time, high-to-low-level output				30	ns
t_r	Differential output signal rise time				25	ns
t_f	Differential output signal fall time				25	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)				5	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	R_L = 110 Ω, $\overline{RE}$ at 0 V (see Figure 7)			150	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output				100	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	R_L = 110 Ω, $\overline{RE}$ at 0 V (see Figure 8)			150	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output				100	ns
$t_{PZH(SHN)}$	Propagation delay time, shutdown-to-high-level output	R_L = 110 Ω, $\overline{RE}$ at VCC (see Figure 7)			2600	ns
$t_{PZL(SHDN)}$	Propagation delay time, shutdown-to-low-level output	R_L = 110 Ω, $\overline{RE}$ at VCC (see Figure 8)			2600	ns

7.10 Switching Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF (see Figure 11)			200	ns
t_{PHL}	Propagation delay time, high-to-low-level output				200	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)			6		ns
t_r	Output signal rise time				3	ns
t_f	Output signal fall time				3	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, DE at 3 V, (see Figure 12 and Figure 13)			50	ns
t_{PZL}	Output enable time to low level				50	ns
t_{PHZ}	Output enable time from high level				50	ns
t_{PLZ}	Output enable time from low level				50	ns
$t_{PZH(SHDN)}$	Propagation delay time, shutdown-to-high-level output	C_L = 15 pF, DE at 0 V, (see Figure 14)			3500	ns
$t_{PZL(SHDN)}$	Propagation delay time, shutdown-to-low-level output				3500	ns

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7.11 Dissipation Ratings

PACKAGE(1)	JEDEC BOARD MODEL	T_A < 25°C POWER RATING	DERATING FACTOR(2) ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D (SIOC)	Low k(3)	507 mW	4.82 mW/°C	289 mW	217 mW
	High k(3)	824 mW	7.85 mW/°C	471 mW	353 mW
P (PDIP)	Low k(3)	686 mW	6.53 mW/°C	392 mW	294 mW
DGK (VSSOP)	Low k(3)	394 mW	3.76 mW/°C	255 mW	169 mW
	High k(4)	583 mW	5.55 mW/°C	333 mW	250 mW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(3) In accordance with the low-k thermal metric definitions of EIA/JESD51-3.
(4) In accordance with the high-k thermal metric definitions of EIA/JESDS1-7.

7.12 Typical Characteristics

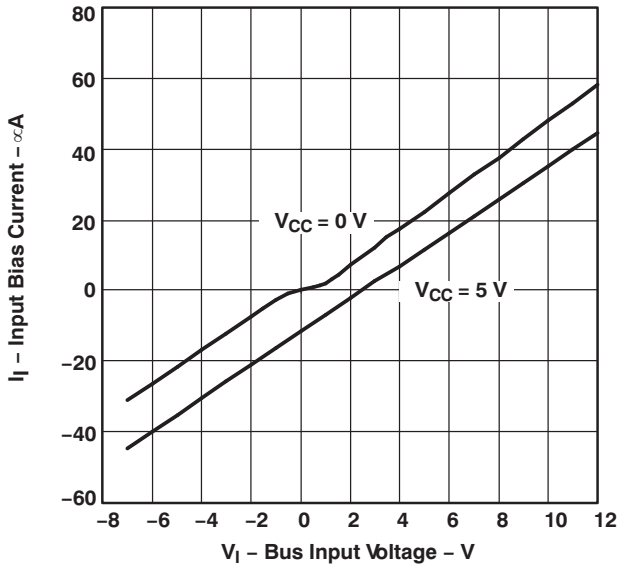


Figure 1. Bus Input Current vs Bus Input Voltage

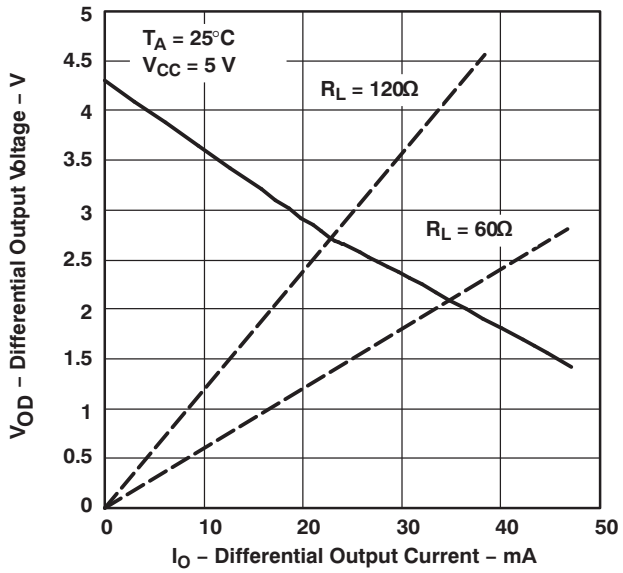


Figure 2. Driver Differential Output Voltage vs Differential Output Current

8 Parameter Measurement Information

Test load capacitance includes probe and jig capacitance (unless otherwise specified). Signal generator characteristics: rise time and fall time <6 ns, pulse rate 100 kHz, 50% duty cycle. Z_O = 50 Ω (unless otherwise specified).

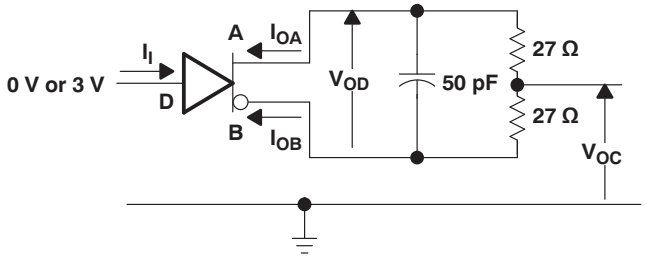


Figure 3. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

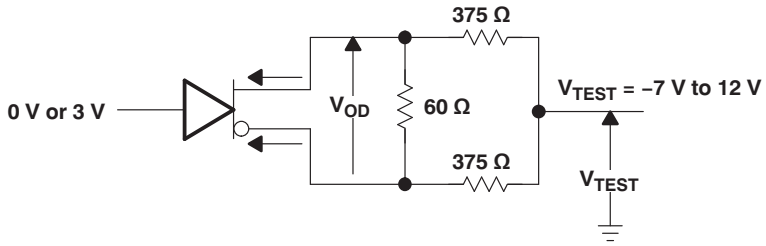


Figure 4. Driver Test Circuit, V_{OD} With Common-Mode Loading

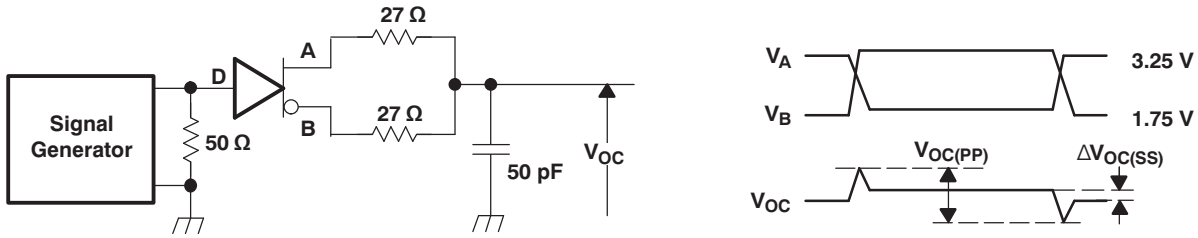


Figure 5. Driver V_{OC} Test Circuit and Waveforms

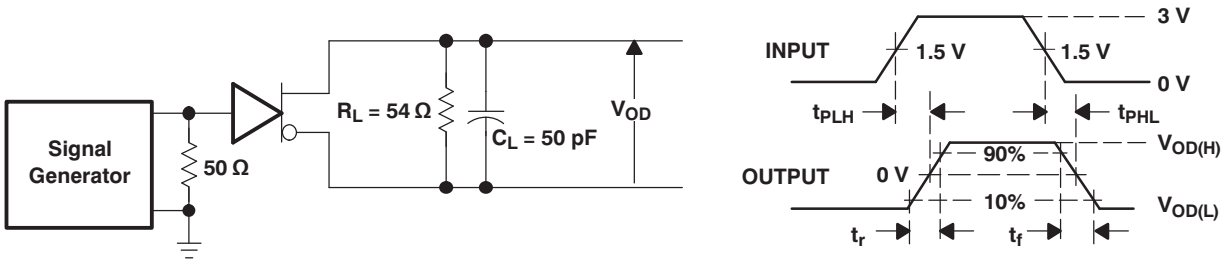


Figure 6. Driver Switching Test Circuit and Waveforms

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Parameter Measurement Information (continued)

Test load capacitance includes probe and jig capacitance (unless otherwise specified). Signal generator characteristics: rise time and fall time <6 ns, pulse rate 100 kHz, 50% duty cycle. Z_O = 50 Ω (unless otherwise specified).

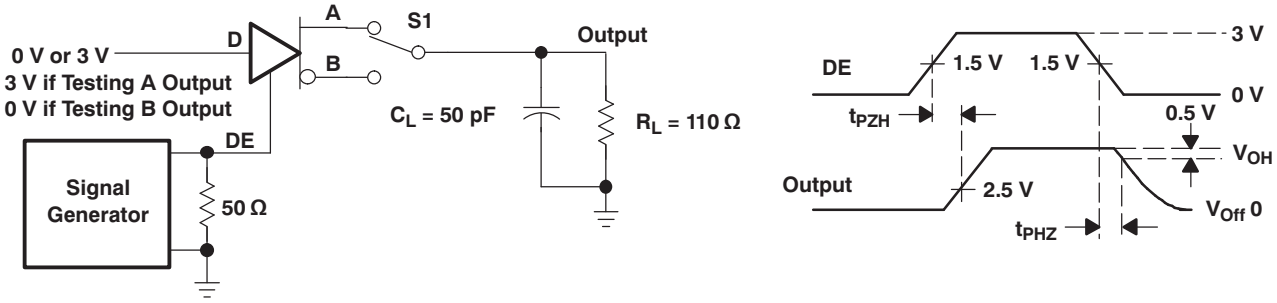


Figure 7. Driver Enable/Disable Test Circuit and Waveforms, High Output

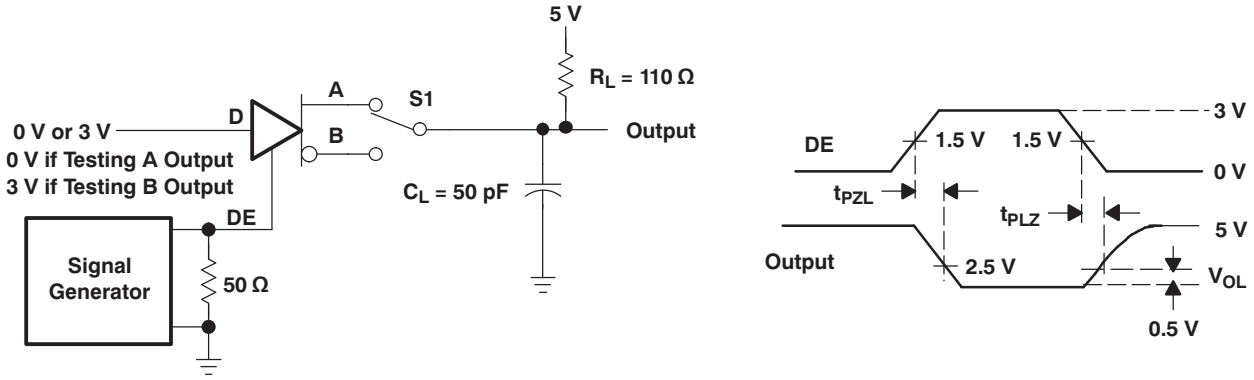


Figure 8. Driver Enable/Disable Test Circuit and Waveforms, Low Output

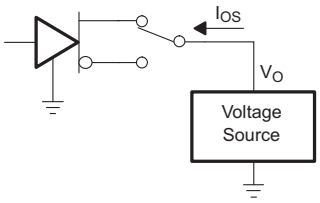


Figure 9. Driver Short-Circuit Test

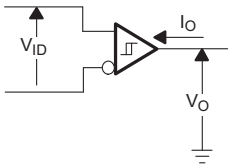


Figure 10. Receiver Parameter Definitions

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Parameter Measurement Information (continued)

Test load capacitance includes probe and jig capacitance (unless otherwise specified). Signal generator characteristics: rise time and fall time <6 ns, pulse rate 100 kHz, 50% duty cycle. Z_O = 50 Ω (unless otherwise specified).

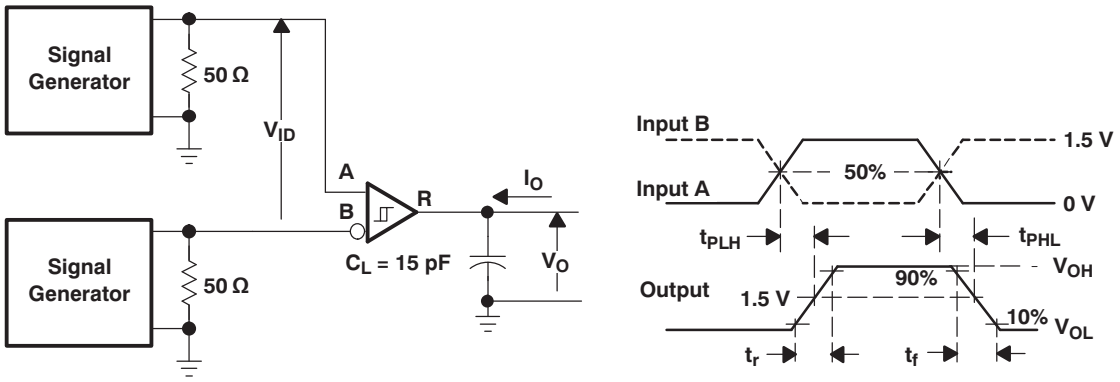


Figure 11. Receiver Switching Test Circuit and Waveforms

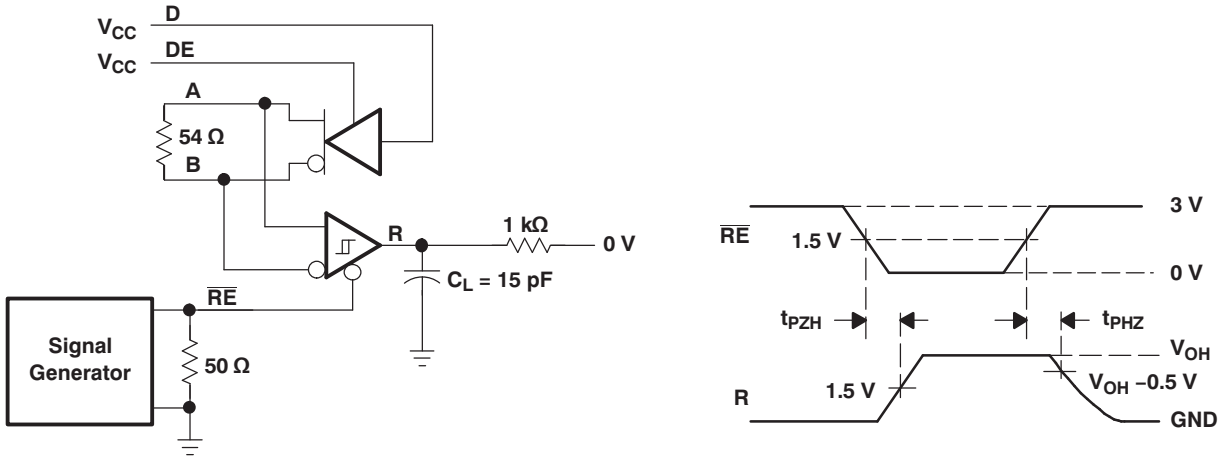


Figure 12. Receiver Enable/Disable Test Circuit and Waveforms, Data Output High

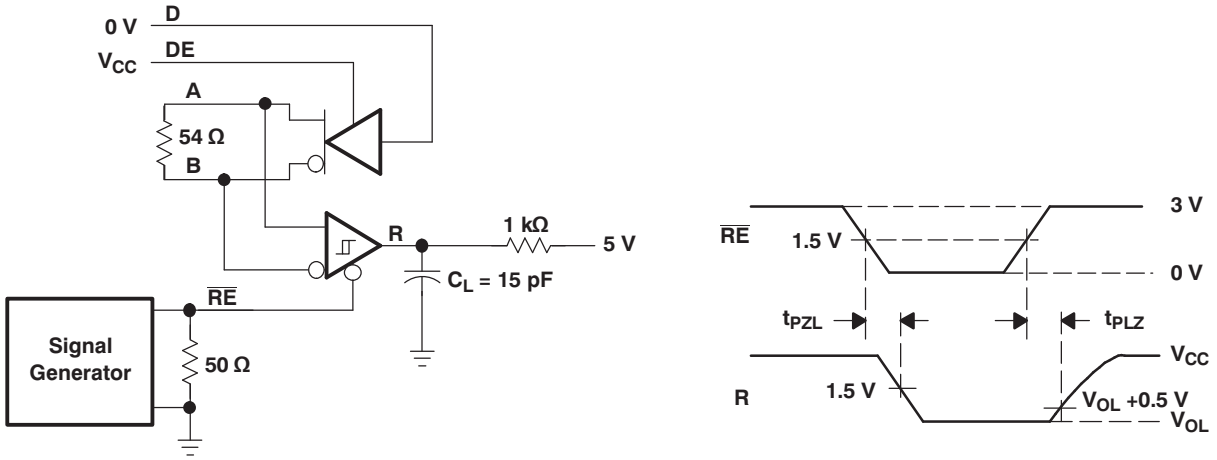


Figure 13. Receiver Enable/Disable Test Circuit and Waveforms, Data Output Low

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Parameter Measurement Information (continued)

Test load capacitance includes probe and jig capacitance (unless otherwise specified). Signal generator characteristics: rise time and fall time <6 ns, pulse rate 100 kHz, 50% duty cycle. Z_O = 50 Ω (unless otherwise specified).

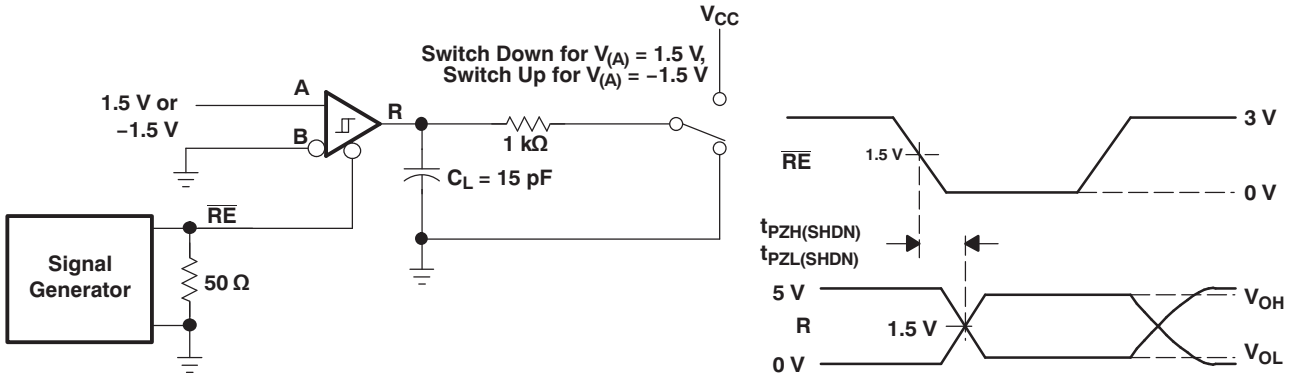


Figure 14. Receiver Enable From Shutdown Test Circuit and Waveforms

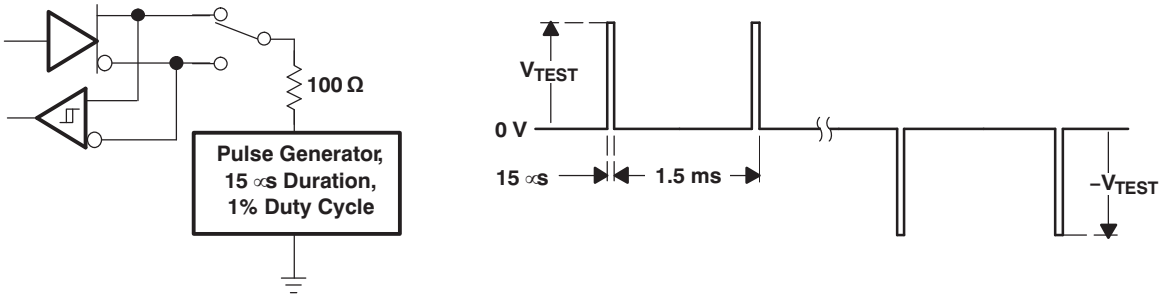


Figure 15. Test Circuit and Waveforms, Transient Over-Voltage Test

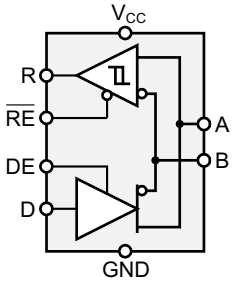
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9 Detailed Description

9.1 Overview

The SN65HVD485E device is a half-duplex RS-485 transceiver suitable for data transmission at rates up to 10 Mbps over controlled-impedance transmission media (such as twisted-pair cabling). Up to 64 units of the SN65HVD485E device can share a common RS-485 bus due to the low bus-input currents of the device. The device also features a high degree of ESD protection and low standby current consumption of 1 mA (maximum).

9.2 Functional Block Diagram



9.3 Feature Description

The SN65HVD485E device provides internal biasing of the receiver input thresholds for open-circuit, bus-idle, or short-circuit failsafe conditions. It features a typical hysteresis of 30 mV to improve noise immunity. Internal ESD protection circuits protect the transceiver bus terminals against ±15-kV Human Body Model (HBM) electrostatic discharges.

9.4 Device Functional Modes

When the driver enable pin (DE) is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse, B turns high, A is low, and V_{OD} is negative.

When DE is low, both outputs turn high impedance. In this condition, the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground; thus when left open, the driver is disabled (high impedance) by default. The D pin has an internal pullup resistor to VCC; thus when left open while the driver is enabled, output A turns high and B turns low.

Table 1. Driver Function Table

INPUT D	ENABLE DE	OUTPUTS		FUNCTION
		A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin ($\overline{RE}$) is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold (V_{IT+}) the receiver output (R) turns high. When V_{ID} is negative and lower than the negative input threshold (V_{IT-}), the receiver output (R) turns low. If V_{ID} is between V_{IT+} and V_{IT-}, the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

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Table 2. Receiver Function Table

DIFFERENTIAL INPUT $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R	FUNCTION
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

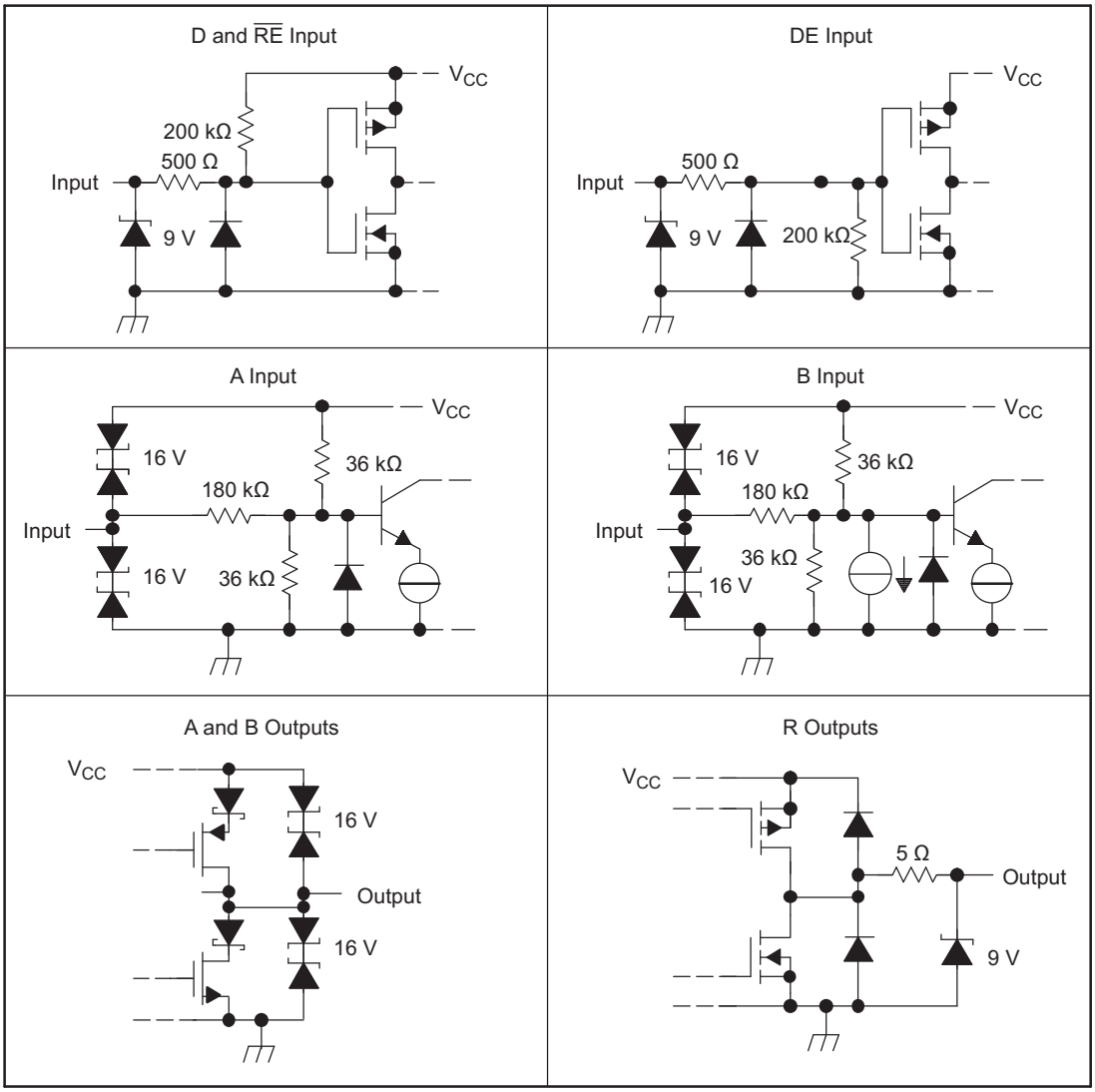


Figure 16. Equivalent Input and Output Schematic Diagrams

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN65HVD485E device is a half-duplex RS-485 transceiver commonly used for asynchronous data transmissions. The driver and receiver enable pins allow for configuration of different operating modes.

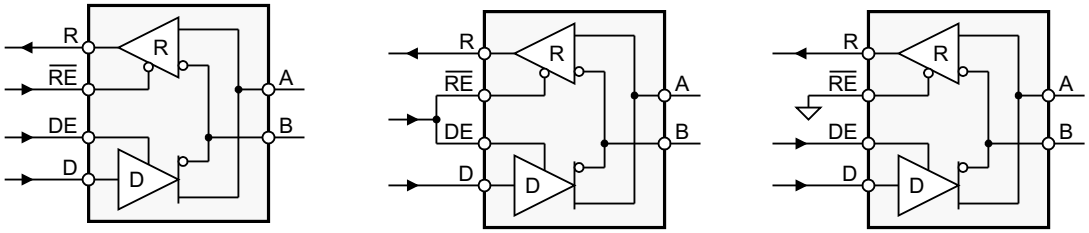


Figure 17. Half-Duplex Transceiver Configurations

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high and as a receiver when the direction-control line is low.

Additionally, only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node receives the data from the bus, receives the data it sends, and can verify that the correct data has been transmitted.

10.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor (R_T) whose value matches the characteristic impedance (Z_0) of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

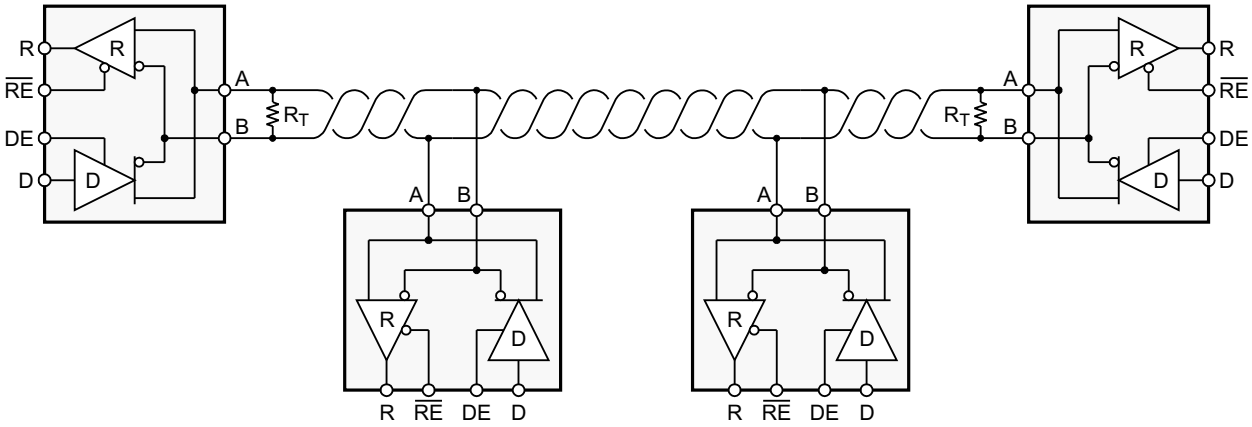


Figure 18. Typical RS-485 Network With Half-Duplex Transceivers

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Typical Application (continued)

10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that can be used in a wide range of applications with varying requirements such as distance, data rate, and number of nodes.

10.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length: the higher the data rate, the shorter the cable length, and conversely the lower the data rate, the longer the cable can be without introducing data errors. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

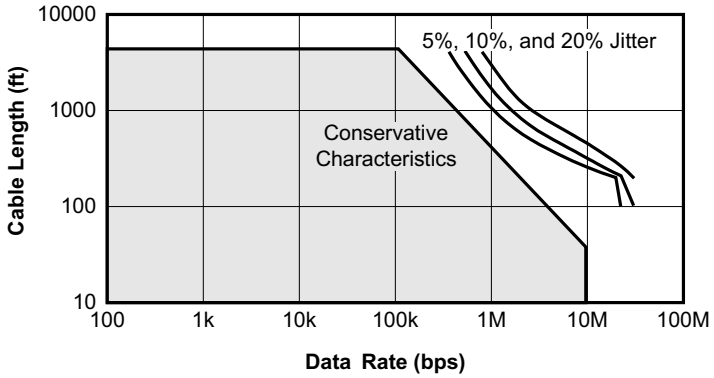


Figure 19. Cable Length vs Data Rate Characteristic

10.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, must be as short as possible. Stubs present a nonterminated piece of bus line that can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub must be less than one-tenth of the rise time of the driver; thus giving a maximum physical stub length as shown in Equation 1.

$$L_{stub} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

10.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32-unit loads (UL), where 1-unit load represents a load impedance of approximately 12 kΩ. Because the SN65HVD485E device is a ½ UL transceiver, it is possible to connect up to 64 receivers to the bus.

10.2.1.4 Receiver Failsafe

The differential receiver of the SN65HVD485E device is failsafe to invalid bus states caused by the following:

- Open bus conditions such as a disconnected connector
- Shorted bus conditions such as cable damage shorting the twisted pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic-high state so that the output of the receiver is not indeterminate.

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Typical Application (continued)

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and it must output a Low when V_{ID} is more negative than –200 mV. The receiver parameters that determine the failsafe performance are V_{IT+}, $V_{IT–}$, and V_{hys} (the separation between V_{IT+} and $V_{IT–}$). As shown in the *Electrical Characteristics: Receiver* table, differential signals more negative than –200 mV cause a low receiver output, and differential signals more positive than 200 mV cause a high receiver output.

When the differential input signal is close to zero, it is still above the V_{IT+} threshold, and the receiver output is High. Only when the differential input is more than V_{hys} below V_{IT+} does the receiver output transition to a Low state. Therefore, the noise immunity of the receiver inputs during bus fault conditions includes the receiver hysteresis value (V_{hys}) as well as the value of V_{IT+}.

10.2.2 Detailed Design Procedure

To protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary.

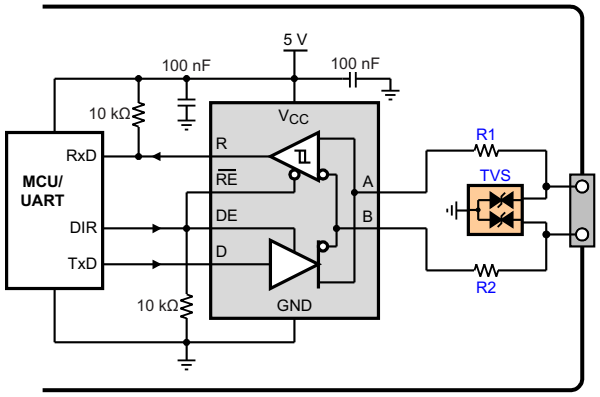


Figure 20. Transient Protection Against ESD, EFT, and Surge Transients

Figure 20 suggests a protection circuit against 10-kV ESD (IEC 61000-4-2), 4-kV EFT (IEC 61000-4-4), and 1-kV surge (IEC 61000-4-5) transients. Table 3 shows the associated bill of materials.

Table 3. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	5-V, 10-Mbps RS-485 transceiver	SN65HVD485E	TI
R1, R2	10-Ω, pulse-proof thick-film resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400-W transient suppressor	CDSOT23-SM712	Bourns

10.2.2.1 Power Usage in an RS-485 Transceiver

Power consumption is a concern in many applications. Power supply current is delivered to the bus load and to the transceiver circuitry. For a typical RS-485 bus configuration, the load that an active driver must drive consists of all of the receiving nodes plus the termination resistors at each end of the bus.

The load presented by the receiving nodes depends on the input impedance of the receiver. The TIA/EIA-485-A standard defines a unit load as allowing up to 1 mA. With up to 32 unit loads allowed on the bus, the total current supplied to all receivers can be as high as 32 mA. The SN65HVD485E device is rated as a ½ unit load device, so up to 64 can be connected on one bus.

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The current in the termination resistors depends on the differential bus voltage. The standard requires active drivers to produce at least 1.5 V of differential signal. For a bus terminated with one standard 120-Ω resistor at each end, this sums to 25-mA differential output current whenever the bus is active. Typically, the SN65HVD485E device can drive more than 25 mA to a 60-Ω load, which results in a differential output voltage higher than the minimum required by the standard (see Figure 2).

Supply current increases with signaling rate primarily because of the totem pole outputs of the driver. When these outputs change state, there is a moment when both the high-side and low-side output transistors are conducting, which creates a short spike in the supply current. As the frequency of state changes increases, more power is used.

10.2.3 Application Curve

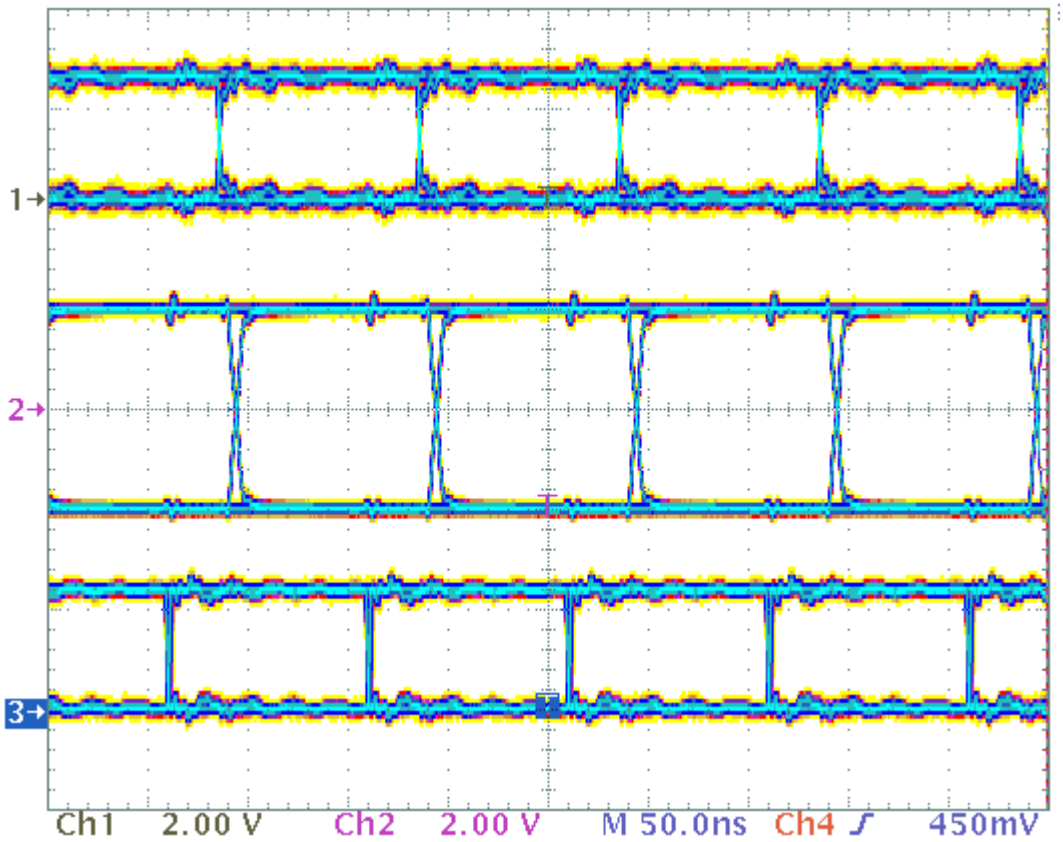


Figure 21. SN65HVD485E Single-Ended Input (Top), Differential Output (Middle), and Single-Ended Output (Bottom) at 10 MHz

11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply must be decoupled with a 100-nF ceramic capacitor located as close as possible to the supply pins. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

12 Layout

12.1 Layout Guidelines

Robust and reliable bus-node design often requires the use of external transient-protection devices to protect against EFT and surge transients that may occur in industrial environments. Because these transients have a wide frequency bandwidth (from approximately 3 MHz to 3 GHz), high-frequency layout techniques must be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
2. Use V_{CC} and ground planes to provide low-inductance power distribution. High-frequency currents tend to follow the path of least inductance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the V_{CC} pins of transceiver, UART, or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via inductance.
6. Use 1-kΩ to 10-kΩ pullup or pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert series pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs), which reduces the transients to a few hundred volts of clamping voltage and transient blocking units (TBUs) that limit transient current to less than 1 mA.

12.2 Layout Example

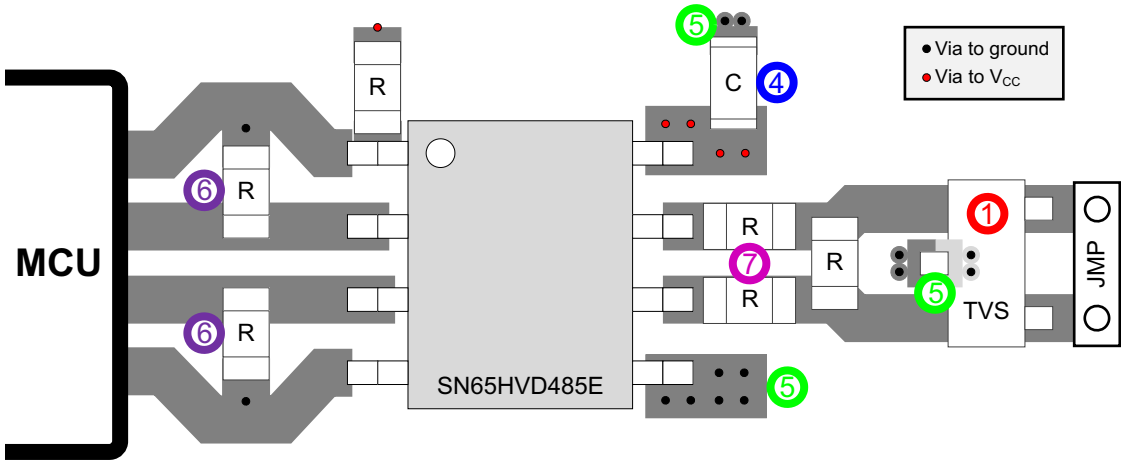


Figure 22. Layout Example

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13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.1.2 Device Nomenclature

13.1.2.1 Thermal Characteristics of IC Packages

θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power

θ_{JA} is NOT a constant and is a strong function of

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives average in-use condition thermal performance and consists of a single trace layer 25 mm long and 2-oz thick copper. The high-k board gives best case in-use condition and consists of two 1-oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in θ_{JA} can be measured between these two test cards

θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with θ_{JB} in 1-dimensional thermal simulation of a package system.

θ_{JB} (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. θ_{JB} is only defined for the high-k test card.

θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see Figure 23).

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Device Support (continued)

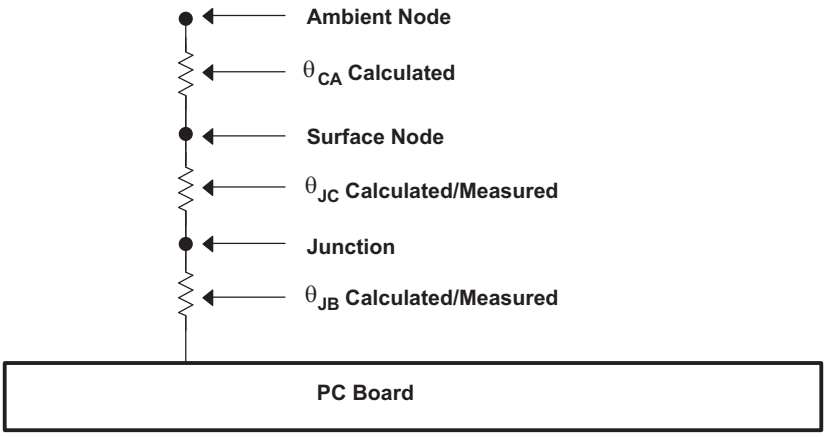


Figure 23. Thermal Resistance

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

SZZA003, *Package Thermal Characterization Methodologies*

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD485ED	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP485	Samples
SN65HVD485EDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP485	Samples
SN65HVD485EDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NWJ	Samples
SN65HVD485EDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NWJ	Samples
SN65HVD485EDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NWJ	Samples
SN65HVD485EDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NWJ	Samples
SN65HVD485EDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP485	Samples
SN65HVD485EDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP485	Samples
SN65HVD485EP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	65HVD485	Samples
SN65HVD485EPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	65HVD485	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

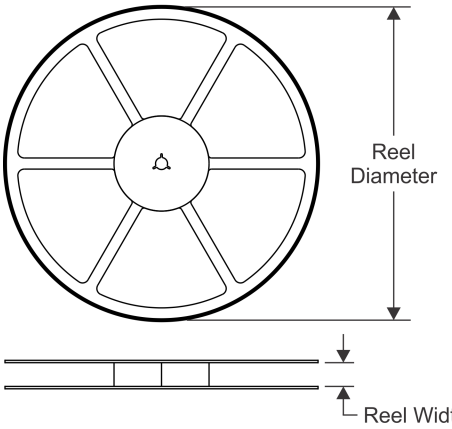
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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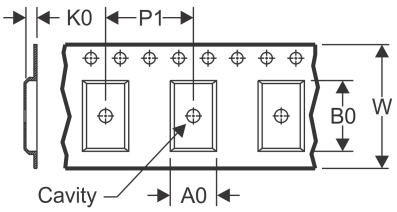
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

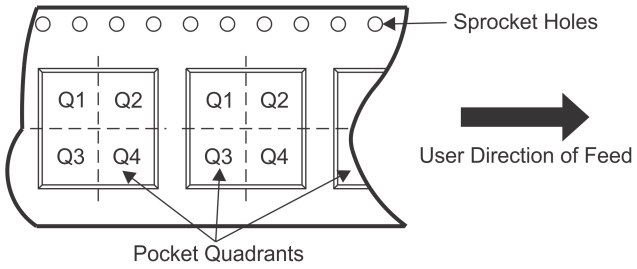


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

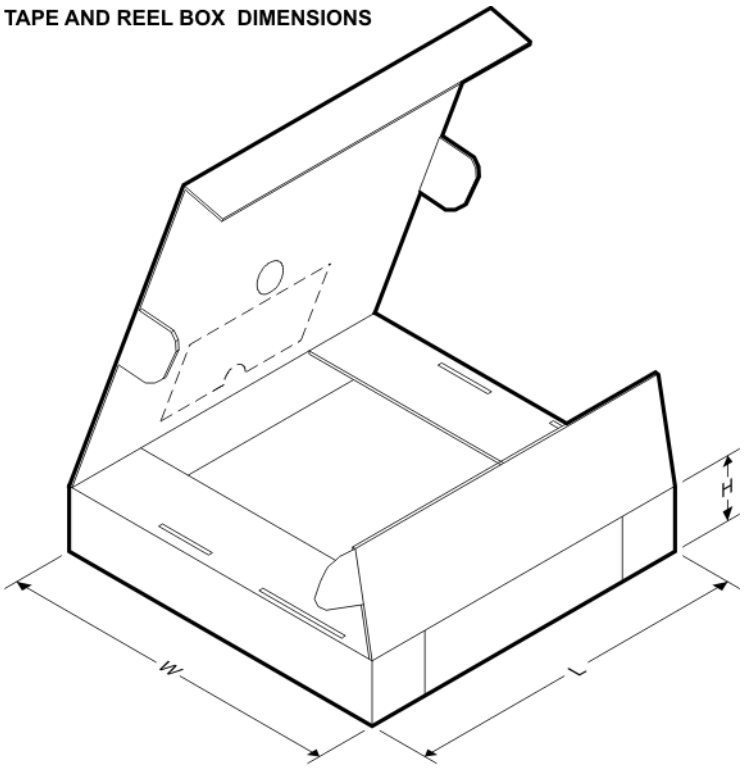
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD485EDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD485EDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

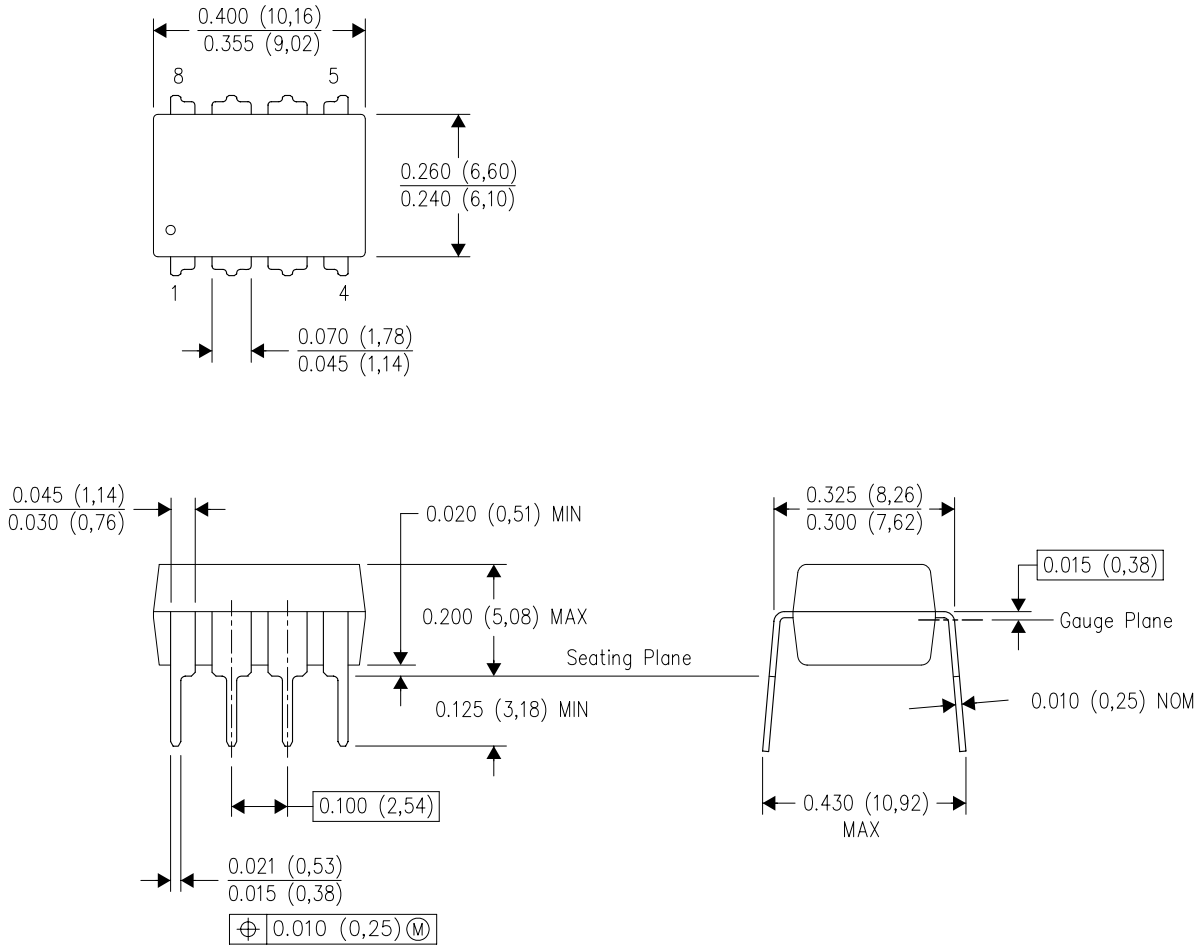
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

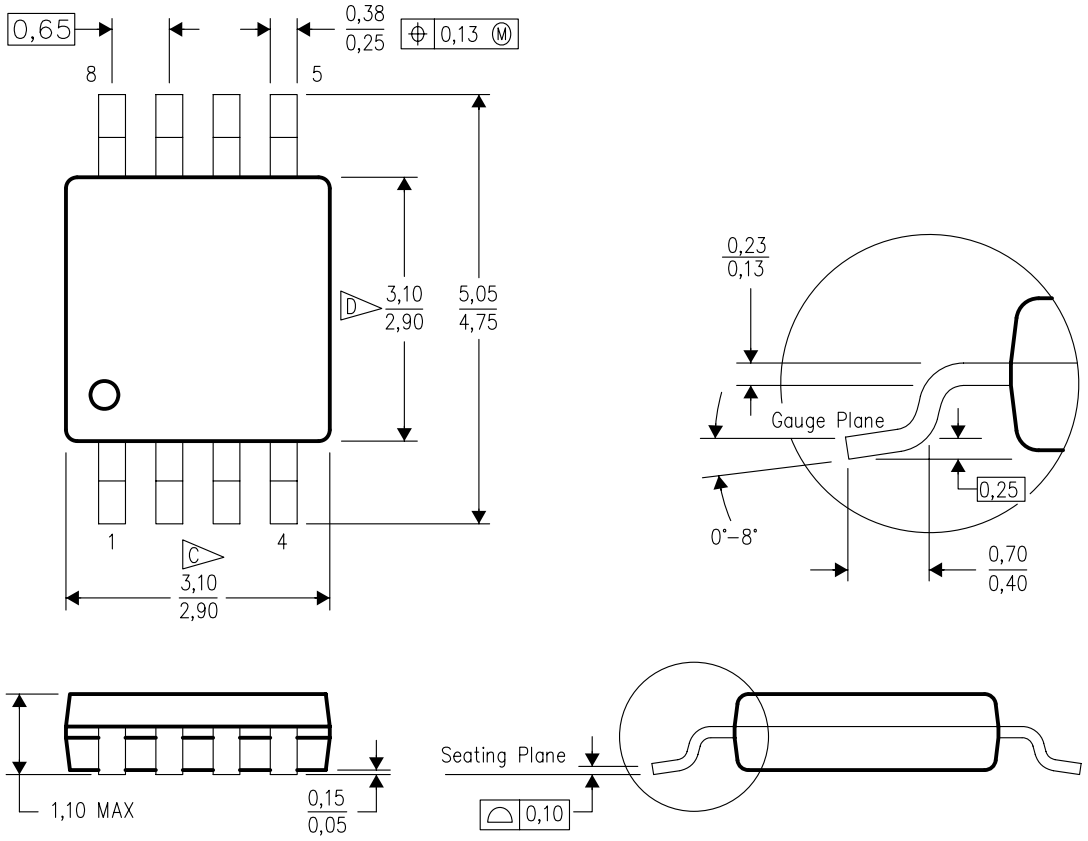
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD485EDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
SN65HVD485EDR	SOIC	D	8	2500	340.5	338.1	20.6

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

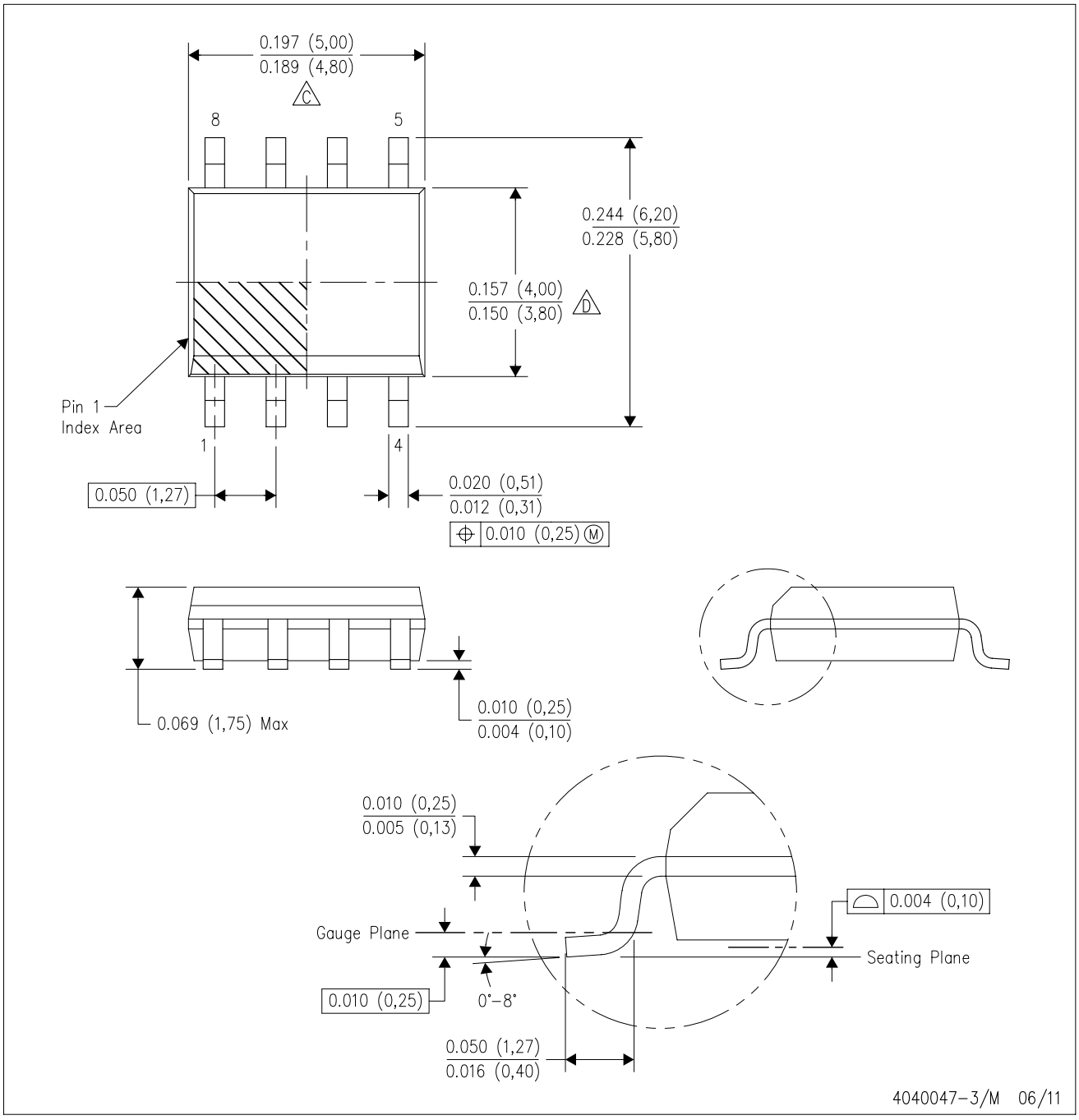
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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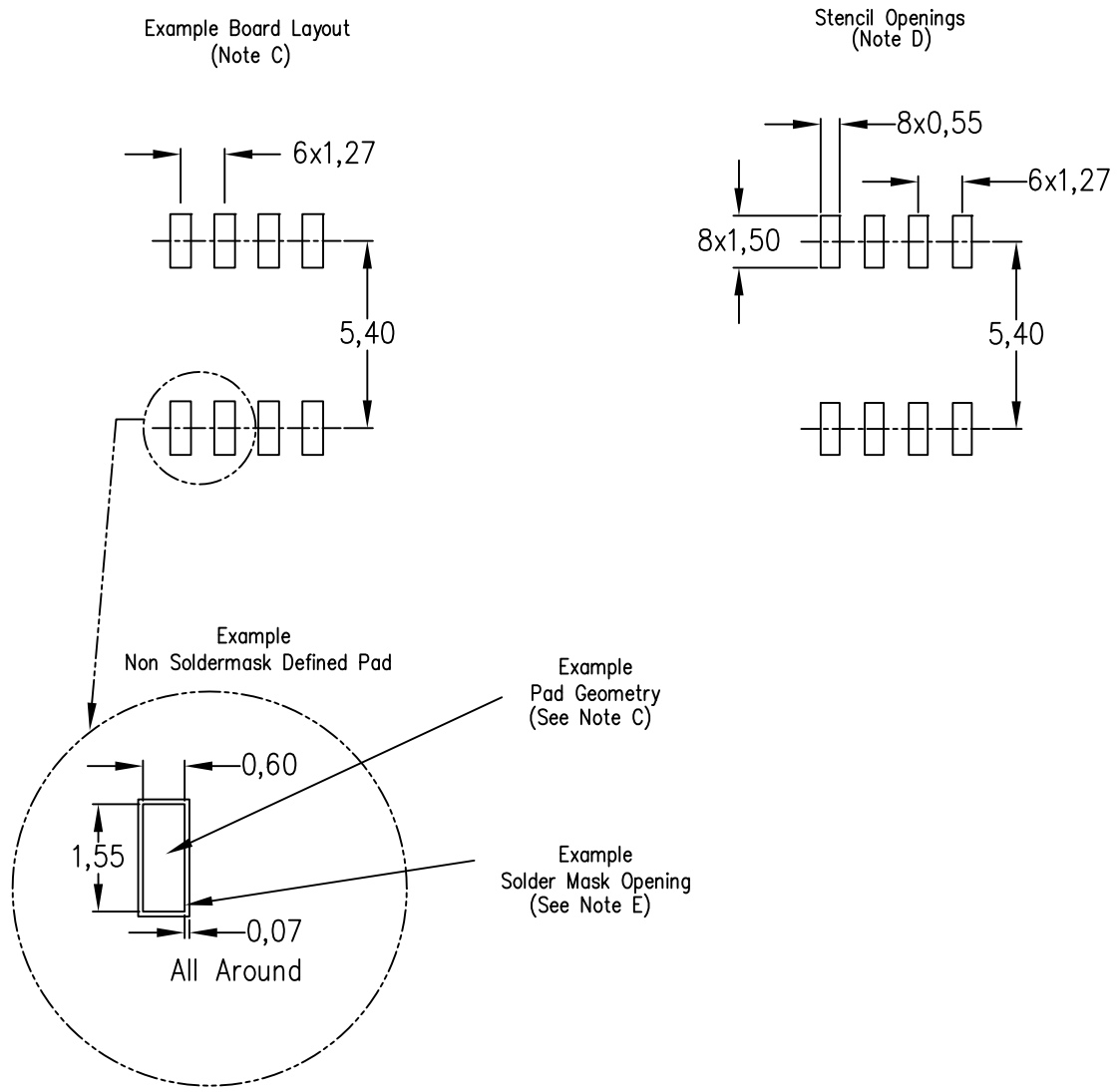
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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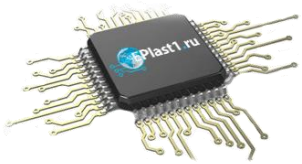
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