

# TLE4678-2

Low Drop Out Linear Voltage Regulator

5 V Fixed Output Voltage  
TLE4678-2LD

## Data Sheet

Rev. 1.0, 2014-03-03

Automotive Power

## Table of Contents

<b>1</b>	<b>Overview</b> .....	<b>3</b>
<b>2</b>	<b>Block Diagram</b> .....	<b>4</b>
<b>3</b>	<b>Pin Configuration</b> .....	<b>5</b>
3.1	Pin Configuration PG-TSON10 .....	5
<b>4</b>	<b>General Product Characteristics</b> .....	<b>7</b>
4.1	Absolute Maximum Ratings .....	7
4.2	Functional Range .....	8
4.3	Thermal Resistance .....	8
<b>5</b>	<b>Voltage Regulator</b> .....	<b>9</b>
5.1	Description Voltage Regulator .....	9
5.2	Electrical Characteristics Voltage Regulator .....	10
5.3	Typical Performance Characteristics Voltage Regulator .....	11
<b>6</b>	<b>Current Consumption</b> .....	<b>14</b>
6.1	Electrical Characteristics Current Consumption .....	14
6.2	Typical Performance Characteristics Current Consumption .....	15
<b>7</b>	<b>Reset Function</b> .....	<b>16</b>
7.1	Description Reset Function .....	16
7.2	Electrical Characteristics Reset Function .....	19
7.3	Typical Performance Characteristics Reset Function .....	21
<b>8</b>	<b>Watchdog Function</b> .....	<b>22</b>
8.1	Description .....	22
8.2	Electrical Characteristics Watchdog Function .....	25
8.3	Typical Performance Characteristics Standard Watchdog Function .....	27
<b>9</b>	<b>Application Information</b> .....	<b>28</b>
9.1	Application Diagram .....	28
9.2	Selection of External Components .....	28
9.3	Thermal Considerations .....	29
9.4	Reverse Polarity Protection .....	30
9.5	Further Application Information .....	30
<b>10</b>	<b>Package Outlines</b> .....	<b>31</b>
<b>11</b>	<b>Revision History</b> .....	<b>32</b>



## 1 Overview

### Features

- Output Voltage  $5\text{ V} \pm 2\%$
- Current Capability 200 mA
- Ultra Low Current Consumption
- Very Low Drop Out Voltage
- Watchdog Circuit for Monitoring a Microprocessor with Programmable Load-dependent Activating Threshold
- Reset Circuit Sensing the Output Voltage with Programmable Switching Threshold and Delay Time
- Reset Output Active Low Down to  $V_{\text{O}} = 1\text{ V}$
- Separated Reset and Watchdog Output
- Excellent Line Transient Robustness
- Maximum Input Voltage  $-14\text{ V} \leq V_{\text{I}} \leq +45\text{ V}$
- Reverse Polarity Protection
- Short Circuit Protected
- Overtemperature Shutdown
- Automotive Temperature Range  $-40\text{ }^{\circ}\text{C} \leq T_{\text{j}} \leq 150\text{ }^{\circ}\text{C}$
- Available in a small thermally enhanced PG-TSON10 package
- Green Product (RoHS Compliant)
- AEC Qualified



**PG-TSON10**

### Description

The TLE4678-2 is a monolithic integrated low drop out fixed output voltage regulator for loads up to 200 mA. An input voltage of up to 45 V is regulated to an output voltage of 5 V. The integrated reset and watchdog function, as well as several protection circuits, combined with a wide operating temperature range offered by the TLE4678-2 make it suitable for supplying microprocessor systems in automotive environments.

The watchdog circuitry will be disabled in case the output current drops below a programmable threshold, enabling a microcontroller to switch in stand-by mode. Modifying the reset threshold is possible by an optional resistor divider.

The TLE4678-2 is available in the tiny thermally enhanced PG-TSON10 exposed pad package.

Type	Package	Marking
TLE4678-2LD	PG-TSON10	46782LD

## 2 Block Diagram

For details on the circuit blocks see the respective section in this data sheet.

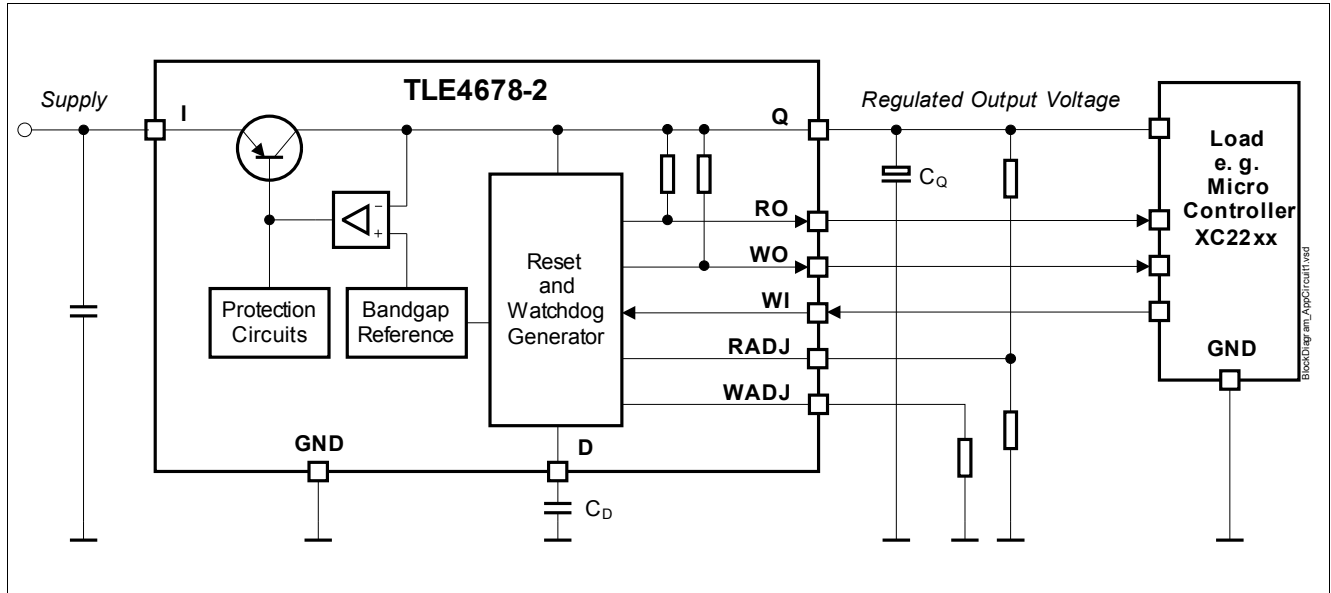


Figure 1 Block Diagram and Simplified Application Circuit

### 3 Pin Configuration

#### 3.1 Pin Configuration PG-TSON10

##### 3.1.1 Pin Assignment

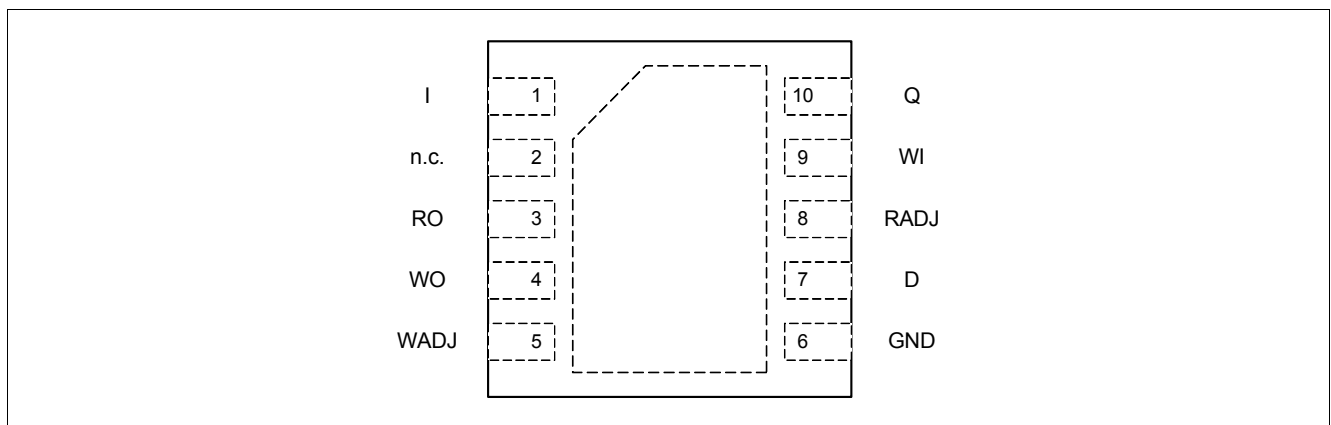


Figure 2 Pin Assignment Package

##### 3.1.2 Pin Definitions and Functions PG-TSON10

Pin	Symbol	Function
1	I	<b>Regulator Input and IC Supply</b> For compensating line influences, a capacitor to GND close to the IC pins is recommended.
3	RO	<b>Reset Output</b> Open collector output with an internal pull-up resistor to the output Q. An additional external pull-up resistor to the output Q is optional. Leave open if the reset function is not needed.
4	WO	<b>Watchdog Output</b> Open collector output with an internal pull-up resistor to the output Q. An additional external pull-up resistor to the output Q is optional. Leave open if the watchdog function is not needed.
5	WADJ	<b>Watchdog Activating Threshold Adjust</b> An external resistor to GND determines the watchdog activating threshold. Connect directly to GND for disabling the watchdog. Connect directly to GND if the watchdog function is not needed. Connect to output Q via 270 kΩ resistor for permanently activating the watchdog.
6	GND	<b>IC Ground</b> Interconnect with the exposed pad and heatsink area on PCB.

Pin Configuration

Pin	Symbol	Function
7	D	<p><b>Reset Delay and Watchdog Timing</b>            Connect a ceramic capacitor D (pin 6) to GND for reset delay and watchdog timing adjustment.            Leave only open if both, the reset and the watchdog function are not needed.</p>
8	RADJ	<p><b>Reset Switching Threshold Adjust</b>            For reset threshold adjustment connect to a voltage divider from output Q to GND.            For triggering the reset at the internally determined threshold, connect this pin directly to GND.            Connect directly to GND if the reset function is not needed.</p>
9	WI	<p><b>Watchdog Input</b>            Positive edge triggered input, usable for microcontroller monitoring.            Connect to GND if the watchdog function is not needed.</p>
10	Q	<p><b>5 V Regulator Output</b>            Block to GND with a capacitor close to the IC pins, respecting capacitance and ESR requirements given in the <a href="#">Chapter 4.2</a>.</p>
2	n. c.	<p><b>Internally not connected</b>            Connection to GND on PCB recommended.</p>
Exposed pad		<p>Connect to heat sink area on PCB. Interconnect with GND.</p>

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

**Table 1 Absolute Maximum Ratings<sup>1)</sup>**

$T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
<b>Voltage Rating</b>							
Regulator Input and IC Supply I	$V_I$	-14	–	45	V	–	P_4.1.1
Regulator Output Q	$V_Q$	-1	–	7	V	–	P_4.1.2
Reset Output RO	$V_{RO}$	-0.3	–	7	V	–	P_4.1.3
Reset Delay and Watchdog Timing D	$V_D$	-0.3	–	7	V	–	P_4.1.4
Reset Switching Threshold Adjust RADJ	$V_{RADJ}$	-0.3	–	7	V	–	P_4.1.5
Watchdog Input WI	$V_{WI}$	-0.3	–	7	V	–	P_4.1.6
Watchdog Output WO	$V_{WO}$	-0.3	–	7	V	–	P_4.1.7
Watchdog Activating Threshold Adjust WADJ	$V_{WADJ}$	-0.3	–	7	V	–	P_4.1.8
<b>Temperature</b>							
Junction Temperature	$T_j$	-40	–	150	$^\circ\text{C}$	–	P_4.1.9
Storage Temperature	$T_{stg}$	-55	–	150	$^\circ\text{C}$	–	P_4.1.10
<b>ESD Susceptibility</b>							
ESD Susceptibility	$V_{ESD,1}$	-3	–	3	kV	HBM <sup>2)</sup> ; Pin 1 (Input) only.	P_4.1.11
ESD Susceptibility	$V_{ESD}$	-2	–	2	kV	HBM <sup>2)</sup> All pins except pin 1 (Input)	P_4.1.12
ESD Susceptibility all pins	$V_{ESD}$	-1	–	1	kV	CDM <sup>3)</sup>	P_4.1.13

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5k  $\Omega$ , 100 pF)

3) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101.

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

## 4.2 Functional Range

**Table 2 Functional Range**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Voltage Range for Normal Operation	$V_{I(nor)}$	$V_Q + V_{dr}$	–	45	V	<sup>1)</sup>	P_4.2.1
Extended Input Voltage Range	$V_{I(ext)}$	3.3	–	45	V	<sup>2)</sup>	P_4.2.2
Input Voltage Transient Immunity	$dV_I/dt$	-10	–	20	V/ $\mu$ s	$dV_I \leq 10$ V; $V_I > 9$ V; No trigger of WO, RO. <sup>3)</sup>	P_4.2.3
Junction Temperature	$T_j$	-40	–	150	°C	–	P_4.2.4
Output Capacitor Requirements	$C_Q$	10	–	–	$\mu$ F	<sup>4)</sup>	P_4.2.5
Output Capacitor Requirements	$ESR_{CQ}$	–	–	3	$\Omega$	<sup>5)</sup>	P_4.2.6

1) For specification of the output voltage  $V_Q$  and the drop out voltage  $V_{dr}$ , see [Chapter 5](#).

2) The output voltage  $V_Q$  will follow the input voltage, but is outside the specified range. For details see [Chapter 5](#).

3) Transient measured directly at the input pin. Not subject to production test, specified by design.

4) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.

5) Relevant ESR value at  $f = 10$  kHz.

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).*

**Table 3 Thermal Resistance**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
<b>TLE4678-2LD (Package Versions PG-TSON10)</b>							
Junction to Case <sup>1)</sup>	$R_{thJC}$	–	16	–	K/W	–	P_4.3.1
Junction to Ambient	$R_{thJA}$	–	190	–	K/W	footprint only <sup>2)</sup>	P_4.3.2
Junction to Ambient	$R_{thJA}$	–	80	–	K/W	300 mm <sup>2</sup> heatsink area on PCB <sup>2)</sup>	P_4.3.3
Junction to Ambient	$R_{thJA}$	–	70	–	K/W	600 mm <sup>2</sup> heatsink area on PCB <sup>2)</sup>	P_4.3.4
Junction to Ambient	$R_{thJA}$	–	67	–	K/W	2s2p PCB <sup>2)</sup>	P_4.3.5

1) Not subject to production test, specified by design

2) Specified  $R_{thJA}$  value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 2 inner copper layers (2 x 70 $\mu$ m Cu, 2 x 35 $\mu$ m Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.



## 5 Voltage Regulator

### 5.1 Description Voltage Regulator

The output voltage  $V_Q$  is controlled by comparing a portion of it to an internal reference and driving a PNP pass transistor accordingly. Saturation control as a function of the load current prevents any oversaturation of the pass element. The control loop stability depends on the output capacitor  $C_Q$ , the load current, the chip temperature and the poles/zeros introduced by the integrated circuit. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the chapter [Chapter 4.2](#) have to be maintained. For details see also the typical performance graph "Output Capacitor Series Resistor  $ESR_{CQ}$  vs. Output Current  $I_Q$ ". Also, the output capacitor shall be sized to buffer load transients.

An input capacitor  $C_I$  is not needed for the control loop stability, but recommended to buffer line influences. Connect the capacitors close to the IC terminals.

Protection circuitry prevent the IC as well as the application from destruction in case of catastrophic events. These safeguards contain output current limitation, reverse polarity protection as well as thermal shutdown in case of overtemperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, the maximum output current is decreased at input voltages above  $V_I = 22\text{ V}$ .

The thermal shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, a junction temperature above  $150\text{ }^\circ\text{C}$  is outside the maximum rating and therefore reduces the IC lifetime.

The TLE4678-2 allows a negative supply voltage. However, several small currents are flowing into the IC increasing its junction temperature. This has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity condition.

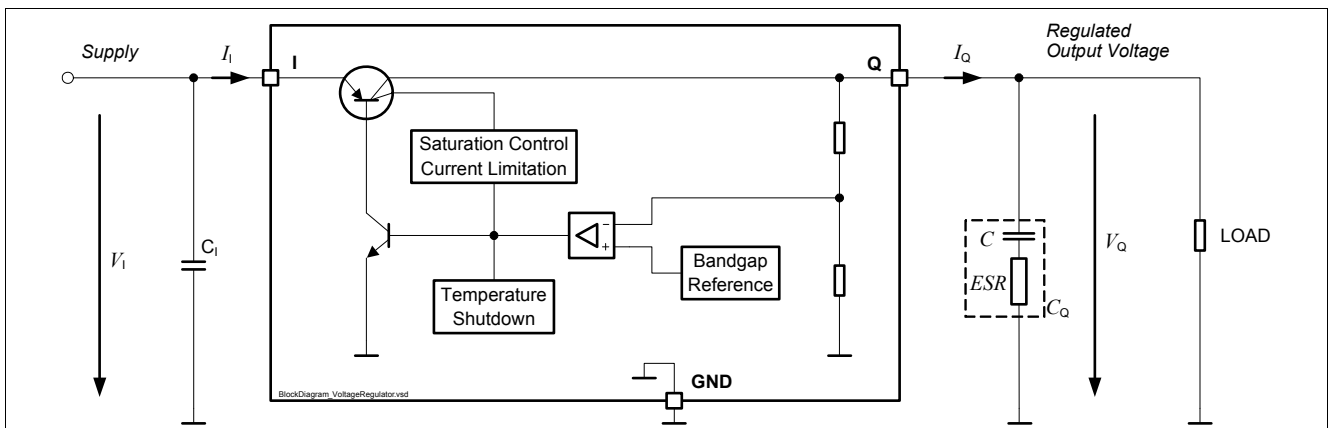


Figure 3 Block Diagram Voltage Regulator Circuit

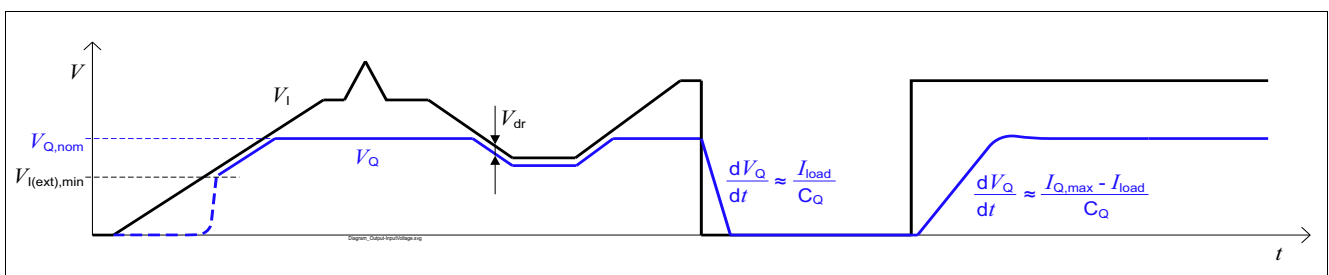


Figure 4 Output Voltage vs. Input Voltage

## 5.2 Electrical Characteristics Voltage Regulator

**Table 4 Electrical Characteristics: Voltage Regulator**
 $V_1 = 13.5 \text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,

 all voltages with respect to ground, direction of currents as shown in **Figure 3** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Voltage	$V_Q$	4.9	5.0	5.1	V	$0 \text{ mA} \leq I_Q \leq 200 \text{ mA}$ ; $8 \text{ V} \leq V_1 \leq 18 \text{ V}$	P_5.2.1
Output Voltage	$V_Q$	4.9	5.0	5.1	V	$0 \text{ mA} \leq I_Q \leq 150 \text{ mA}$ ; $6 \text{ V} \leq V_1 \leq 18 \text{ V}$	P_5.2.2
Output Voltage	$V_Q$	4.9	5.0	5.1	V	$0 \text{ mA} \leq I_Q \leq 100 \text{ mA}$ ; $18 \text{ V} \leq V_1 \leq 32 \text{ V}$ $T_j \leq 105^\circ\text{C}$ <sup>1) 2)</sup>	P_5.2.3
Output Voltage	$V_Q$	4.9	5.0	5.1	V	$0 \text{ mA} \leq I_Q \leq 10 \text{ mA}$ ; $32 \text{ V} \leq V_1 \leq 45 \text{ V}$ $T_j \leq 105^\circ\text{C}$ <sup>1) 2)</sup>	P_5.2.4
Output Voltage	$V_Q$	4.9	5.0	5.1	V	$0.3 \text{ mA} \leq I_Q \leq 100 \text{ mA}$ ; $18 \text{ V} \leq V_1 \leq 32 \text{ V}$ <sup>1)</sup>	P_5.2.5
Output Voltage	$V_Q$	4.9	5.0	5.1	V	$0.3 \text{ mA} \leq I_Q \leq 10 \text{ mA}$ ; $32 \text{ V} \leq V_1 \leq 45 \text{ V}$ <sup>1)</sup>	P_5.2.6
Load Regulation steady-state	$ dV_{Q,\text{load}} $	–	5	30	mV	$I_Q = 1 \text{ mA}$ to $150 \text{ mA}$ ; $V_1 = 6 \text{ V}$	P_5.2.7
Line Regulation steady-state	$ dV_{Q,\text{line}} $	–	5	20	mV	$V_1 = 6 \text{ V}$ to $32 \text{ V}$ ; $I_Q = 5 \text{ mA}$	P_5.2.8
Power Supply Ripple Rejection	$PSRR$	60	65	–	dB	$f_{\text{ripple}} = 100 \text{ Hz}$ ; $V_{\text{ripple}} = 1 \text{ Vpp}$ <sup>2)</sup>	P_5.2.9
Drop out Voltage $V_{\text{dr}} = V_1 - V_Q$	$V_{\text{dr}}$	–	80	170	mV	$I_Q = 50 \text{ mA}$ <sup>3)</sup>	P_5.2.10
Drop out Voltage $V_{\text{dr}} = V_1 - V_Q$	$V_{\text{dr}}$	–	120	300	mV	$I_Q = 150 \text{ mA}$ <sup>3)</sup>	P_5.2.11
Output Current Limitation	$I_{Q,\text{max}}$	201	350	500	mA	$0 \text{ V} \leq V_Q \leq 4.8 \text{ V}$	P_5.2.12
Reverse Current	$I_Q$	-1.5	-0.7	–	mA	$V_1 = 0 \text{ V}$ ; $V_Q = 5 \text{ V}$	P_5.2.13
Reverse Current at Negative Input Voltage	$I_1$	-2	-1	–	mA	$V_1 = -14 \text{ V}$ ; $V_Q = 0 \text{ V}$	P_5.2.14
Overtemperature Shutdown Threshold	$T_{j,\text{sd}}$	151	–	200	$^\circ\text{C}$	$T_j$ increasing <sup>2)</sup>	P_5.2.15
Overtemperature Shutdown Threshold Hysteresis	$T_{j,\text{hy}}$	–	20	–	K	$T_j$ decreasing <sup>2)</sup>	P_5.2.16

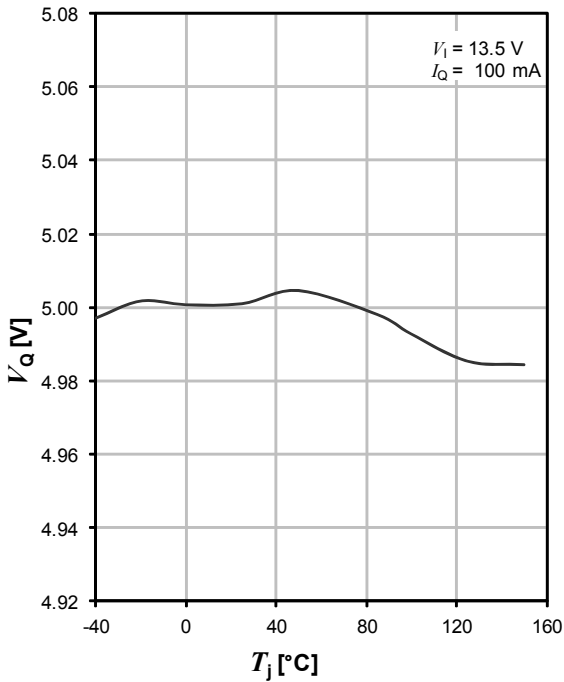
1) See typical performance graph for details.

2) Parameter not subject to production test; specified by design.

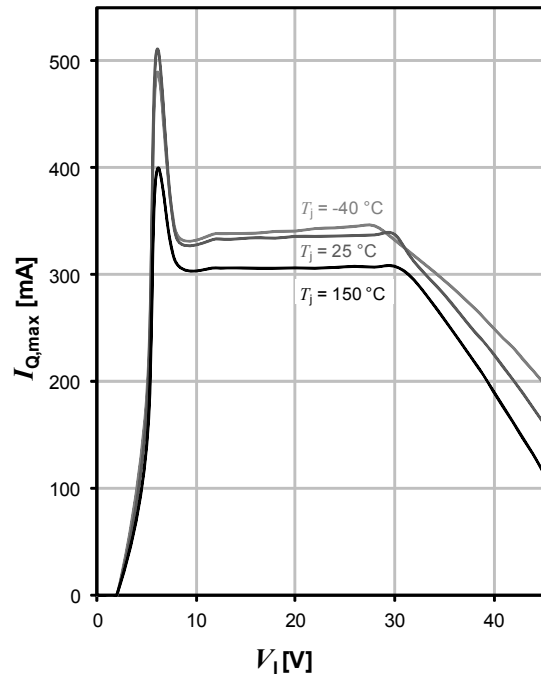
 3) Measured when the output voltage  $V_Q$  has dropped 100 mV from its nominal value.

### 5.3 Typical Performance Characteristics Voltage Regulator

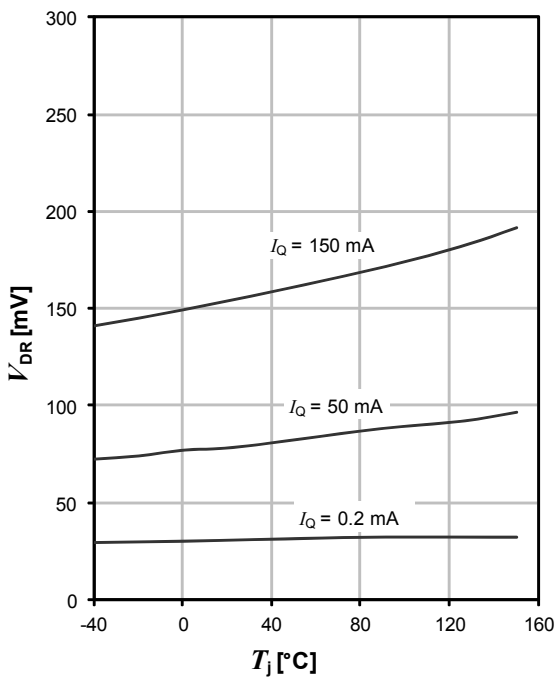
**Output Voltage  $V_Q$  versus Junction Temperature  $T_j$**



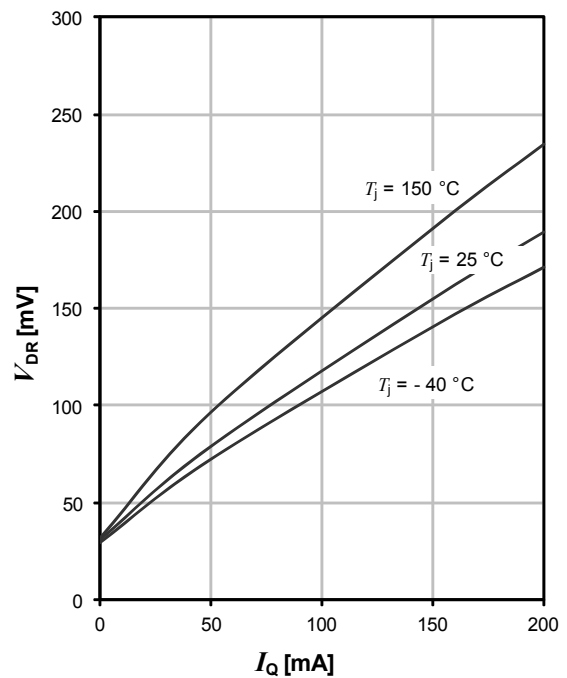
**Output Current Limitation  $I_{Q,max}$  versus Input Voltage  $V_I$**



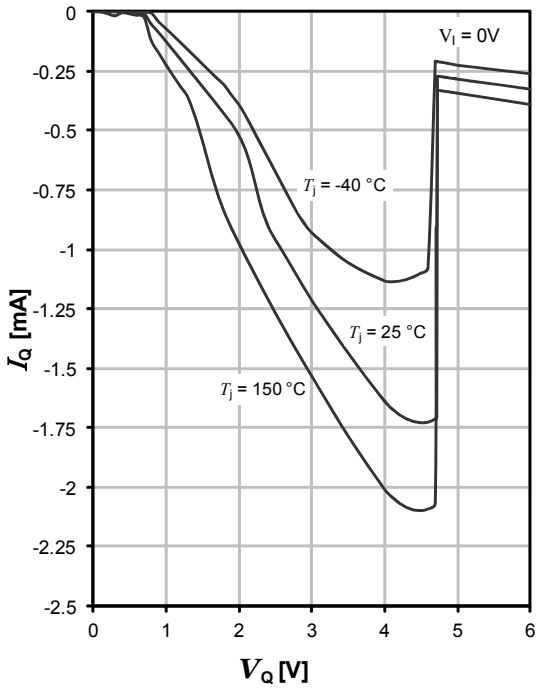
**Dropout Voltage  $V_{dr}$  versus Junction Temperature  $T_j$**



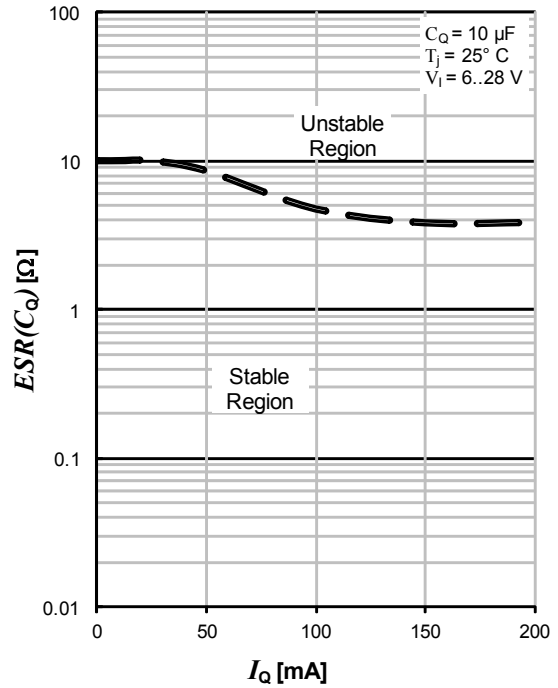
**Dropout Voltage  $V_{dr}$  versus Output Current  $I_Q$**



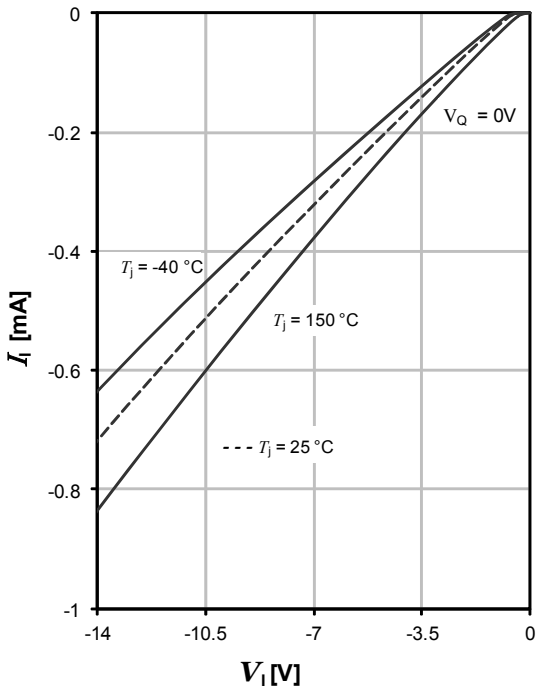
Reverse Output Current  $I_Q$  versus Output Voltage  $V_Q$



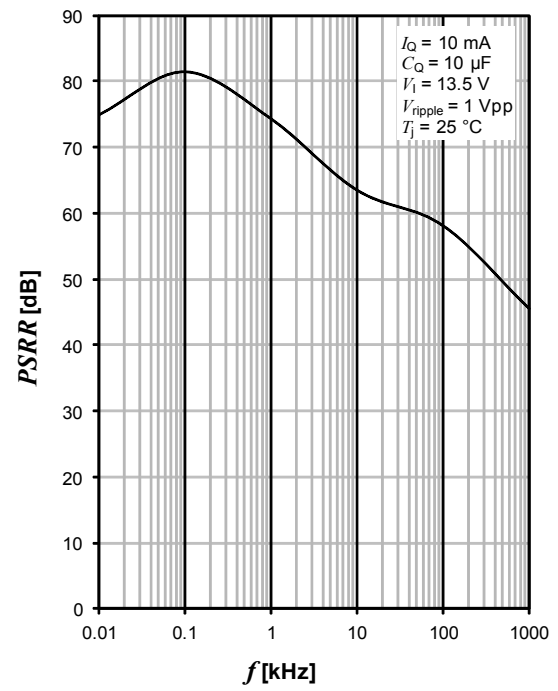
Output Capacitor Series Resistor  $ESR_{C_Q}$  versus Output Current  $I_Q$



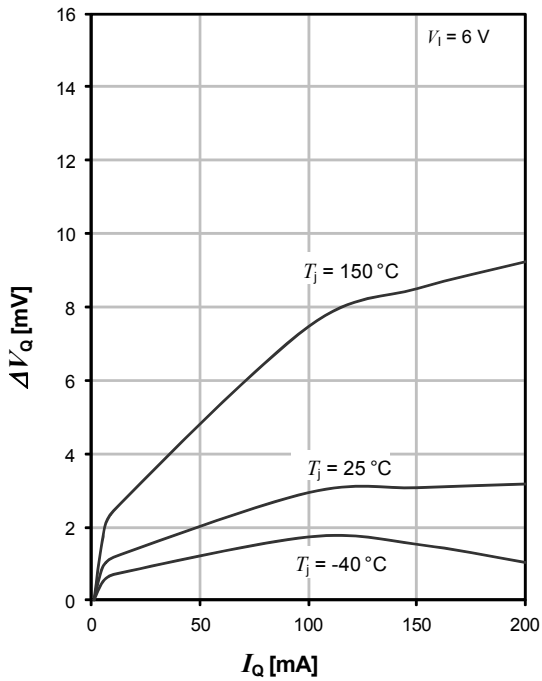
Reverse Current  $I_I$  versus Input Voltage  $V_I$



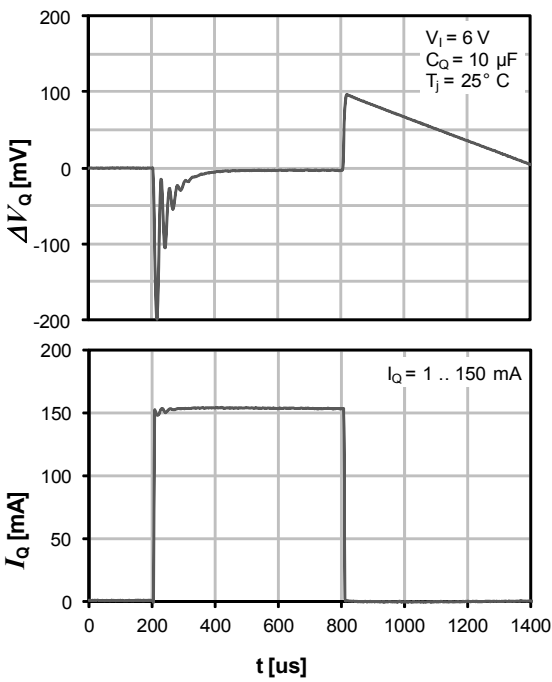
Power Supply Ripple Rejection  $PSRR$  versus Frequency  $f$



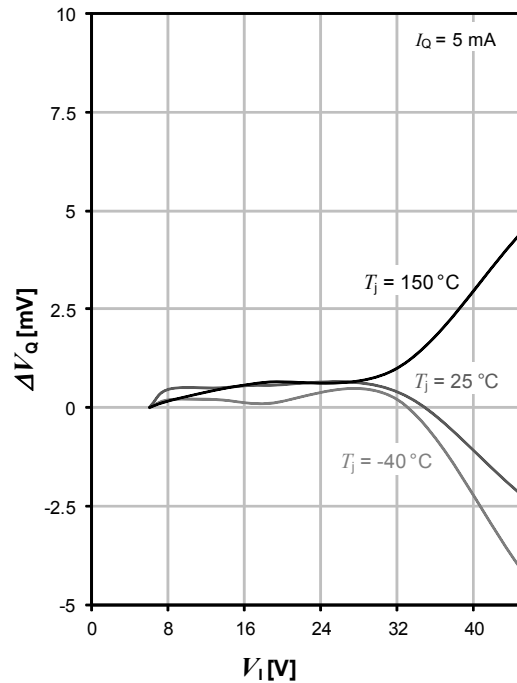
Output Voltage  $\Delta V_Q$  versus Output Current  $I_Q$



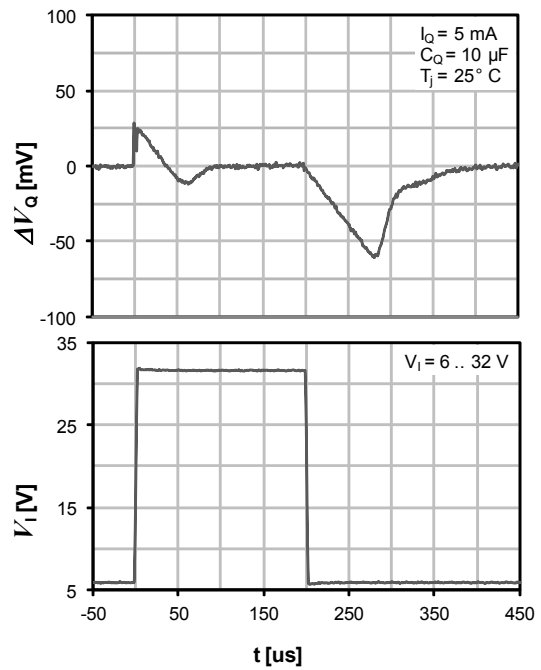
Load Transient Response



Output Voltage  $\Delta V_Q$  versus Input Voltage  $V_I$



Line Transient Response



## 6 Current Consumption

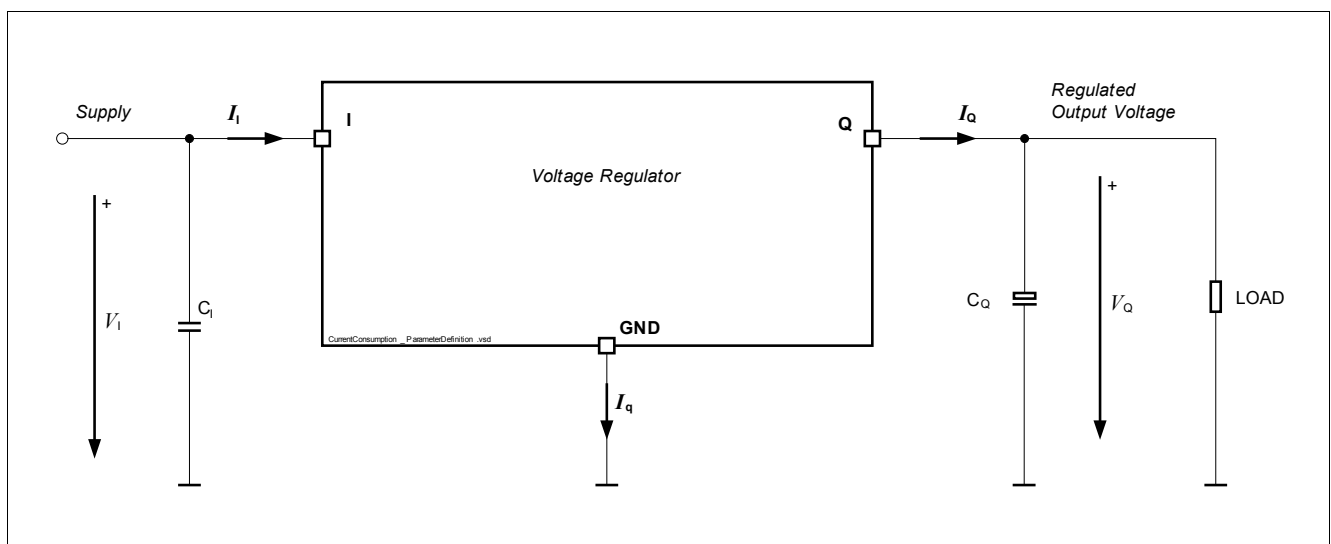
### 6.1 Electrical Characteristics Current Consumption

**Table 5 Electrical Characteristics: Current Consumption**

$V_1 = 13.5\text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,

all voltages with respect to ground, direction of currents as shown in **Figure 5** (unless otherwise specified).

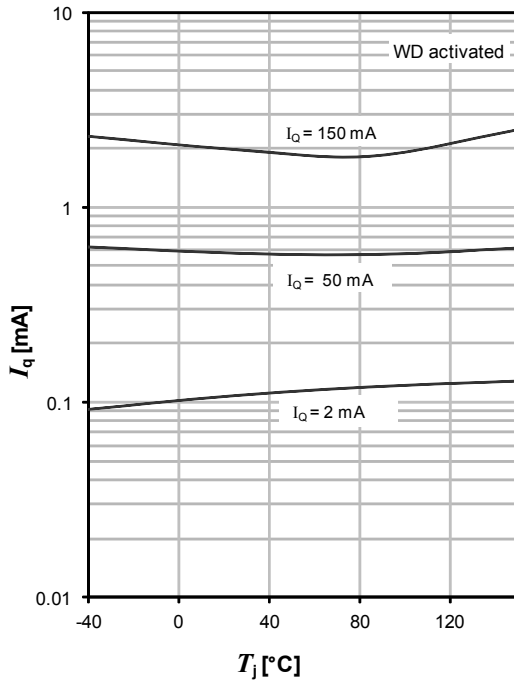
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption Watchdog Deactivated $I_q = I_1 - I_Q$	$I_{q1}$	–	60	80	$\mu\text{A}$	$I_Q \leq 200\ \mu\text{A}$ ; $T_j \leq 25^\circ\text{C}$ Watchdog deactivated	P_6.1.1
Current Consumption Watchdog Deactivated $I_q = I_1 - I_Q$	$I_{q1}$	–	70	85	$\mu\text{A}$	$I_Q \leq 200\ \mu\text{A}$ ; $T_j \leq 85^\circ\text{C}$ Watchdog deactivated	P_6.1.2
Current Consumption $I_q = I_1 - I_Q$	$I_{q2}$	–	110	140	$\mu\text{A}$	$I_Q \leq 2\ \text{mA}$ ; $T_j \leq 25^\circ\text{C}$ Watchdog activated	P_6.1.3
Current Consumption $I_q = I_1 - I_Q$	$I_{q2}$	–	120	155	$\mu\text{A}$	$I_Q \leq 2\ \text{mA}$ ; $T_j \leq 85^\circ\text{C}$ Watchdog activated	P_6.1.4
Current Consumption $I_q = I_1 - I_Q$	$I_{q2}$	–	0.6	1.6	mA	$I_Q = 50\ \text{mA}$	P_6.1.5
Current Consumption $I_q = I_1 - I_Q$	$I_{q2}$	–	2	6	mA	$I_Q = 150\ \text{mA}$	P_6.1.6



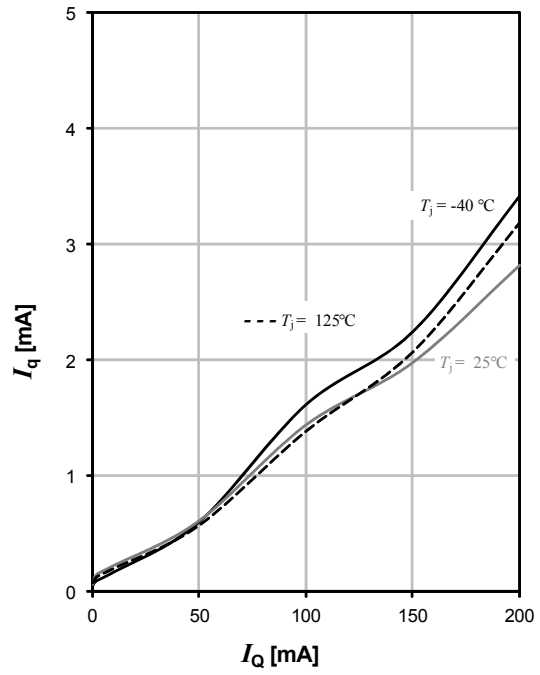
**Figure 5 Parameter Definition**

## 6.2 Typical Performance Characteristics Current Consumption

Current Consumption  $I_q$  versus Junction Temperature  $T_j$



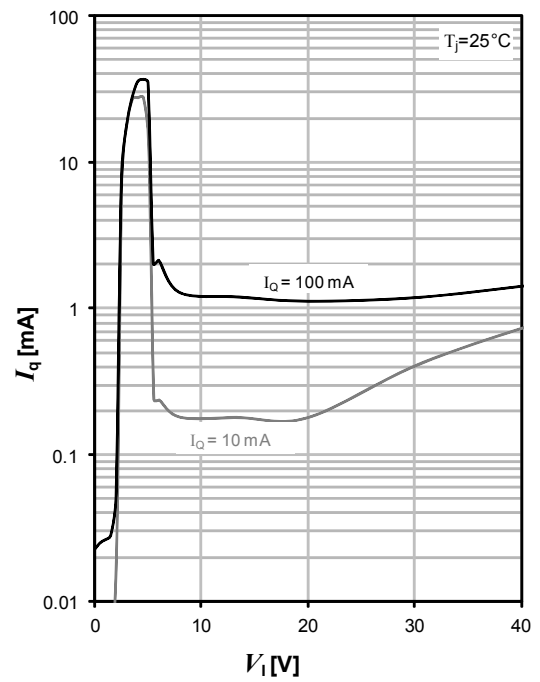
Current Consumption  $I_q$  versus Output Current  $I_Q$



Current Consumption  $I_q$  versus Junction Temperature  $T_j$



Current Consumption  $I_q$  versus Input Voltage  $V_I$



## 7 Reset Function

### 7.1 Description Reset Function

The reset function provides several features:

#### Output Undervoltage Reset:

An output undervoltage condition is indicated by setting the Reset Output "RO" to "low". This signal might be used to reset a microcontroller during low supply voltage.

#### Power-On Reset Delay Time

The power-on reset delay time  $t_{d,PWR-ON}$  allows a microcontroller and oscillator to start up. This delay time is the time period from exceeding the upper reset switching threshold  $V_{RT,hi}$  until the reset is released by switching the reset output "RO" from "low" to "high". The power-on reset delay time  $t_{d,PWR-ON}$  is defined by an external delay capacitor  $C_D$  connected to pin "D" which is charged up by the delay capacitor charge current  $I_{D,ch}$  starting from  $V_D = 0$  V.

In case a power-on reset delay time  $t_{d,PWR-ON}$  different from the value for  $C_D = 100$ nF is required, the delay capacitor's value can be derived from the specified value given in [Table "Power-on Reset Delay Time" on Page 20](#):

$$C_D = 100\text{nF} \times t_{d,PWR-ON} / t_{d,PWR-ON,100\text{nF}} \quad (1)$$

with

- $t_{d,PWR-ON}$ : Desired power-on reset delay time
- $t_{d,PWR-ON,100\text{nF}}$ : Power-on reset delay time specified in [Table "Power-on Reset Delay Time" on Page 20](#)
- $C_D$ : Delay capacitor required.

The formula is valid for  $C_D \geq 10$ nF. For precise timing calculations consider also the delay capacitor's tolerance.

#### Undervoltage Reset Delay Time

Unlike the power-on reset delay time, the undervoltage reset delay time  $t_d$  considers a short output undervoltage event where the delay capacitor  $C_D$  is assumed to be discharged to  $V_D = V_{DST,lo}$  only before the charging sequence starts. Therefore, the undervoltage reset delay time  $t_d$  is defined by the delay capacitor charge current  $I_{D,ch}$  starting from  $V_D = V_{DST,lo}$  and the external delay capacitor  $C_D$ .

A delay capacitor  $C_D$  for a different undervoltage reset delay time as specified in [Table "Undervoltage Reset Delay Time" on Page 19](#) can be calculated similar as above:

$$C_D = 100\text{nF} \times t_d / t_{d,100\text{nF}} \quad (2)$$

with:

- $t_d$ : Desired undervoltage reset delay time
- $t_{d,100\text{nF}}$ : Power-on reset delay time specified in [Table "Undervoltage Reset Delay Time" on Page 19](#)
- $C_D$ : Delay capacitor required

The formula is valid for  $C_D \geq 10$ nF. For precise timing calculations consider also the delay capacitor's tolerance.



### Reset Reaction Time

In case the output voltage of the regulator drops below the output undervoltage lower reset threshold  $V_{RT,lo}$ , the delay capacitor  $C_D$  is discharged rapidly. Once the delay capacitor's voltage has reached the lower delay switching threshold  $V_{DST,lo}$ , the reset output "RO" will be set to "low". In case of a very short drop of output voltage, may the delay capacitor voltage doesn't reach the lower delay switching threshold and therefore no "RO" = "low" will be set. This prevents a microcontroller reset because of a very short distortion on output voltage. Typically the time of this filter effect is about 550 ns ( $t_{rr,blank}$ ). See also timing diagram on [Page 18](#)

Additionally to the delay capacitor discharge time  $t_{rr,d}$ , an internal reaction time  $t_{rr,int}$  applies. Hence, the total reset reaction time  $t_{rr,total}$  becomes:

$$t_{rr,total} = t_{rr,int} + t_{rr,d} \quad (3)$$

with

- $t_{rr,total}$ : Total reset reaction time
- $t_{rr,int}$ : Internal reset reaction time; see [Table "Internal Reset Reaction Time" on Page 20](#).
- $t_{rr,d}$ : Delay capacitor discharge time. For a capacitor  $C_D$  different from the value specified in [Table "Delay Capacitor Discharge Time" on Page 20](#), see typical performance graphs.

### Reset Output "RO"

The reset output "RO" is an open collector output with an integrated pull-up resistor. In case a lower-ohmic "RO" signal is desired, an external pull-up resistor to the output "Q" can be connected. Since the maximum "RO" sink current is limited, the optional external resistor  $R_{RO,ext}$  must not be below as specified in [Table "Reset Output" on Page 19](#).

### Reset Output "RO" Low for $V_Q \geq 1$ V

In case of an undervoltage reset condition reset output "RO" is held "low" for  $V_Q \geq 1$  V, even if the input voltage  $V_I$  is 0 V. This is achieved by supplying the reset circuit from the output capacitor.

### Reset Adjust Function

The undervoltage reset switching threshold can be adjusted according to the application's needs by connecting an external voltage divider ( $R_{ADJ,1}$ ,  $R_{ADJ,2}$ ) at pin "RADJ". For selecting the default threshold connect pin "RADJ" to GND. The reset adjustment range is given in [Table "Reset Adjustment Range" on Page 19](#).

When dimensioning the voltage divider, take into consideration that there will be an additional current constantly flowing through the resistors.

With a voltage divider connected, the reset switching threshold  $V_{RT,new}$  is calculated as follows (neglecting the Reset Adjust Pin Current  $I_{RADJ}$ ):

$$V_{RT,new} = V_{RADJ,th} \times (R_{ADJ,1} + R_{ADJ,2}) / R_{ADJ,2} \quad (4)$$

with

- $V_{RT,new}$ : Desired reset switching threshold.
- $R_{ADJ,1}$ ,  $R_{ADJ,2}$ : Resistors of the external voltage divider, see [Figure 6](#).
- $V_{RADJ,th}$ : Reset adjust switching threshold given in [Table "Reset Adjust" on Page 19](#).

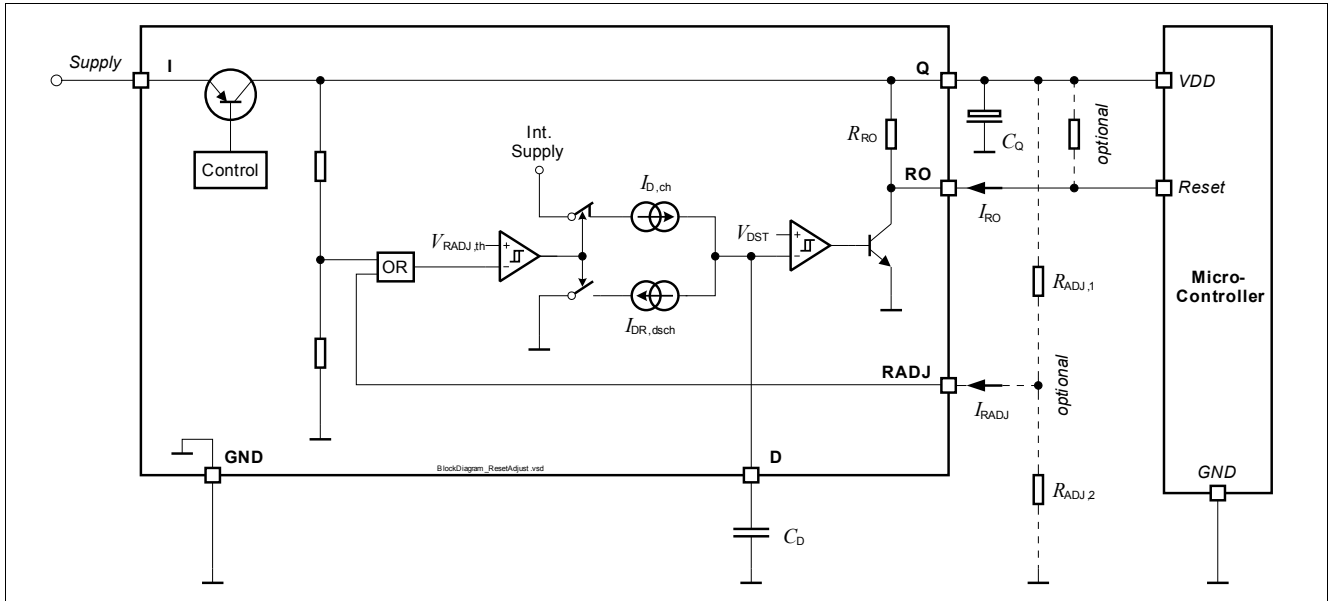


Figure 6 Block Diagram Reset Circuit

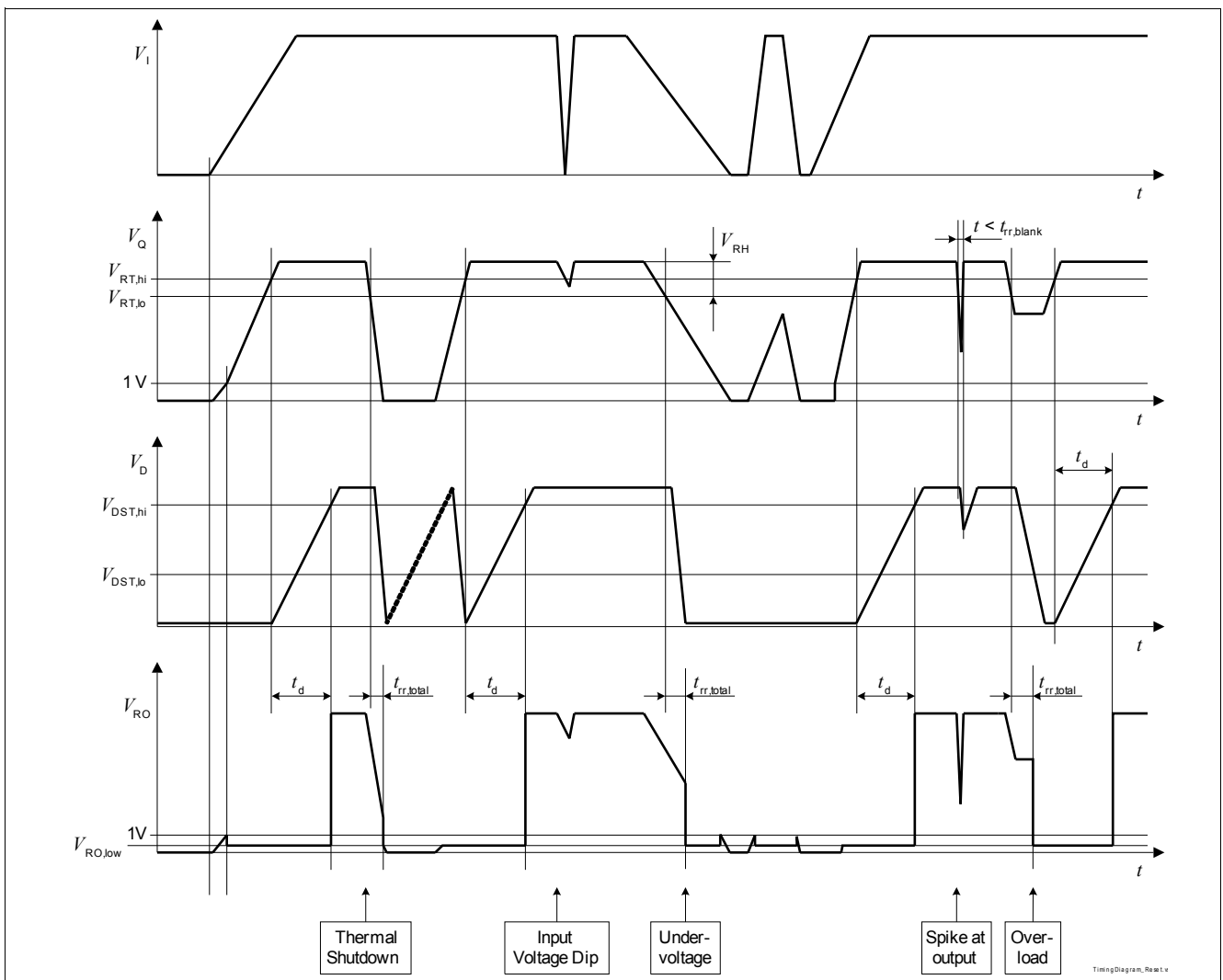


Figure 7 Timing Diagram Reset

## 7.2 Electrical Characteristics Reset Function

**Table 6 Electrical Characteristics: Reset Function**
 $V_I = 13.5\text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,

all voltages with respect to ground, direction of currents as shown in [Figure 6](#) (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
<b>Output Undervoltage Reset Comparator Default Values (Pin RADJ = GND)</b>							
Output Undervoltage Reset Lower Switching Threshold	$V_{RT,lo}$	4.6	4.7	4.8	V	$V_I = 0\text{ V}$ $V_Q$ decreasing RADJ = GND	P_7.2.1
Output Undervoltage Reset Upper Switching Threshold	$V_{RT,hi}$	4.7	4.8	4.9	V	$V_I$ within operating range $V_Q$ increasing RADJ = GND	P_7.2.2
Output Undervoltage Reset Switching Hysteresis	$V_{RT,hy}$	60	120	–	mV	$V_I$ within operating range RADJ = GND.	P_7.2.3
Output Undervoltage Reset Headroom	$V_{RH}$	250	300	–	mV	Calculated Value: $V_Q - V_{RT,lo}$ $V_I$ within operating range $I_Q = 50\text{ mA}$ RADJ = GND	P_7.2.4
<b>Reset Threshold Adjustment</b>							
Reset Adjust Lower Switching Threshold	$V_{RADJ,th}$	1.176	1.20	1.224	V	$V_I = 0\text{ V}$ $3.2\text{ V} \leq V_Q < 4.6\text{ V}$	P_7.2.5
Reset Adjustment Range <sup>1)</sup>	$V_{RT,range}$	3.20	–	4.60	V	–	P_7.2.6
<b>Reset Output RO</b>							
Reset Output Low Voltage	$V_{RO,low}$	–	0.2	0.4	V	$V_I = 0\text{ V}$ ; $1\text{ V} \leq V_Q \leq V_{RT,low}$ $R_{RO,ext} = 3.3\text{ k}\Omega$	P_7.2.8
Reset Output External Pull-up Resistor to Q	$R_{RO,ext}$	3	–	–	k $\Omega$	$V_I = 0\text{ V}$ ; $1\text{ V} \leq V_Q \leq V_{RT,low}$ $V_{RO} = 0.4\text{ V}$	P_7.2.9
Reset Output Internal Pull-up Resistor	$R_{RO}$	20	30	45	k $\Omega$	internally connected to Q	P_7.2.10
<b>Reset Delay Timing</b>							
Upper Delay Switching Threshold	$V_{DST,hi}$	–	1.21	–	V	–	P_7.2.11
Lower Delay Switching Threshold	$V_{DST,lo}$	–	0.30	–	V	–	P_7.2.12
Delay Capacitor Charge Current	$I_{D,ch}$	–	2.8	–	$\mu\text{A}$	$V_D = 1\text{ V}$	P_7.2.13
Delay Capacitor Reset Discharge Current	$I_{DR,dsch}$	–	80	–	mA	$V_D = 1\text{ V}$	P_7.2.14
Undervoltage Reset Delay Time	$t_{d,100nF}$	20	31	45	ms	Calculated value; $C_D = 100\text{ nF}$ <sup>2)</sup> ; $C_D$ discharged to $V_{DST,lo}$	P_7.2.15

**Table 6 Electrical Characteristics: Reset Function (cont'd)**

$V_1 = 13.5 \text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,

all voltages with respect to ground, direction of currents as shown in [Figure 6](#) (unless otherwise specified).

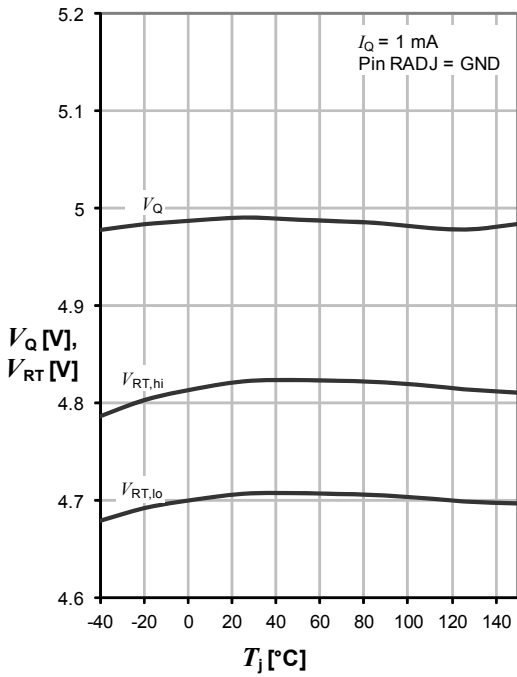
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Power-on Reset Delay Time	$t_{d,PWR-ON,100nF}$	28	43	64	ms	Calculated value; $C_D = 100 \text{ nF}^{2)}$ ; $C_D$ discharged to 0 V;	P_7.2.16
Internal Reset Reaction Time	$t_{rr,int}$	–	9	15	$\mu\text{s}$	$C_D = 0 \text{ nF}$	P_7.2.17
Delay Capacitor Discharge Time	$t_{rr,d,100nF}$	–	1.5	3	$\mu\text{s}$	$C_D = 100 \text{ nF}^{2)}$	P_7.2.18
Total Reset Reaction Time	$t_{rr,total,100nF}$	–	10.5	18	$\mu\text{s}$	Calculated Value: $t_{rr,d,100nF} + t_{rr,int}$ ; $C_D = 100 \text{ nF}^{2)}$	P_7.2.19

1) Related Parameters ( $V_{RT,hi}$ ,  $V_{RT,hy}$ ) are scaled linear when the Reset Switching Threshold is modified.

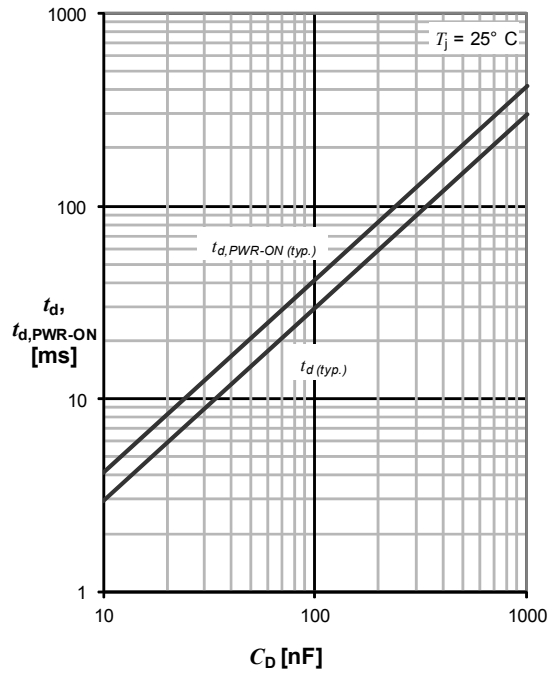
2) For programming a different delay and reset reaction time, see [Chapter 7.1](#).

### 7.3 Typical Performance Characteristics Reset Function

**Undervoltage Reset Switching Thresholds**  
 $V_{RT,LOW}$ ,  $V_{RT,HIGH}$  versus Junction Temperature  $T_j$



**Reset Delay Time  $t_d$ ,  $t_{d,PWR-ON}$  versus Delay Capacitor  $C_D$**



## 8 Watchdog Function

### 8.1 Description

The TLE4678-2 features a load dependent watchdog function with a programmable activating threshold as well as a programmable watchdog timing.

The watchdog function monitors a microcontroller, including time base failures. In case of a missing rising edge within a certain pulse repetition time, the watchdog output is set to 'low'. The programming of the expected watchdog pulse repetition time can be easily done by an external reset delay capacitor.

The watchdog output "WO" is separated from the reset output "RO". Hence, the watchdog output might be used as an interrupt signal for the microcontroller independent from the reset signal. It is possible to interconnect pin "WO" and pin "RO" in order to establish a wire-or function with a dominant low signal.

#### Programmable Watchdog Activation Threshold and Hysteresis

In case a microcontroller is set to sleep mode or to low power mode, its current consumption is very low and the controller might not be able to send any watchdog pulses to the regulators watchdog input "WI". In order to avoid unwanted wake-up signals due to missing edges at pin "WI", the TLE4678-2 watchdog function can be activated dependent on the regulator's output current. The TLE4678-2 comprises a default watchdog activating threshold  $I_{Q,WDact,th}$  with a small hysteresis  $I_{Q,WDact,hy}$  which is modifiable by an external resistor  $R_{WADJ,ext}$  connected to the pin "WADJ". For using the default watchdog activating threshold, leave pin "WADJ" open.

The following table shows the external resistor  $R_{WADJ,ext}$  that is needed at pin "WADJ" for activating/deactivating the watchdog at a desired output current  $I_{Q,WDact,th}$ ,  $I_{Q,WDdeact,th}$ .

**Table 7**

$R_{WADJ,ext}$ [kOhm]	$I_{Q,WDact,th}$ [mA]	$I_{Q,WDdeact,th}$ [mA]	$I_{Q,WDact,hy}$ [ $\mu$ A]
4000	1.015	0.987	28
470	1.339	1.310	29
220	1.761	1.700	61
100	2.728	2.612	116
50	4.435	4.217	219
33	6.333	6.016	318
20	9.792	9.310	482
10	18.523	17.838	685
7.5	24.198	23.472	725

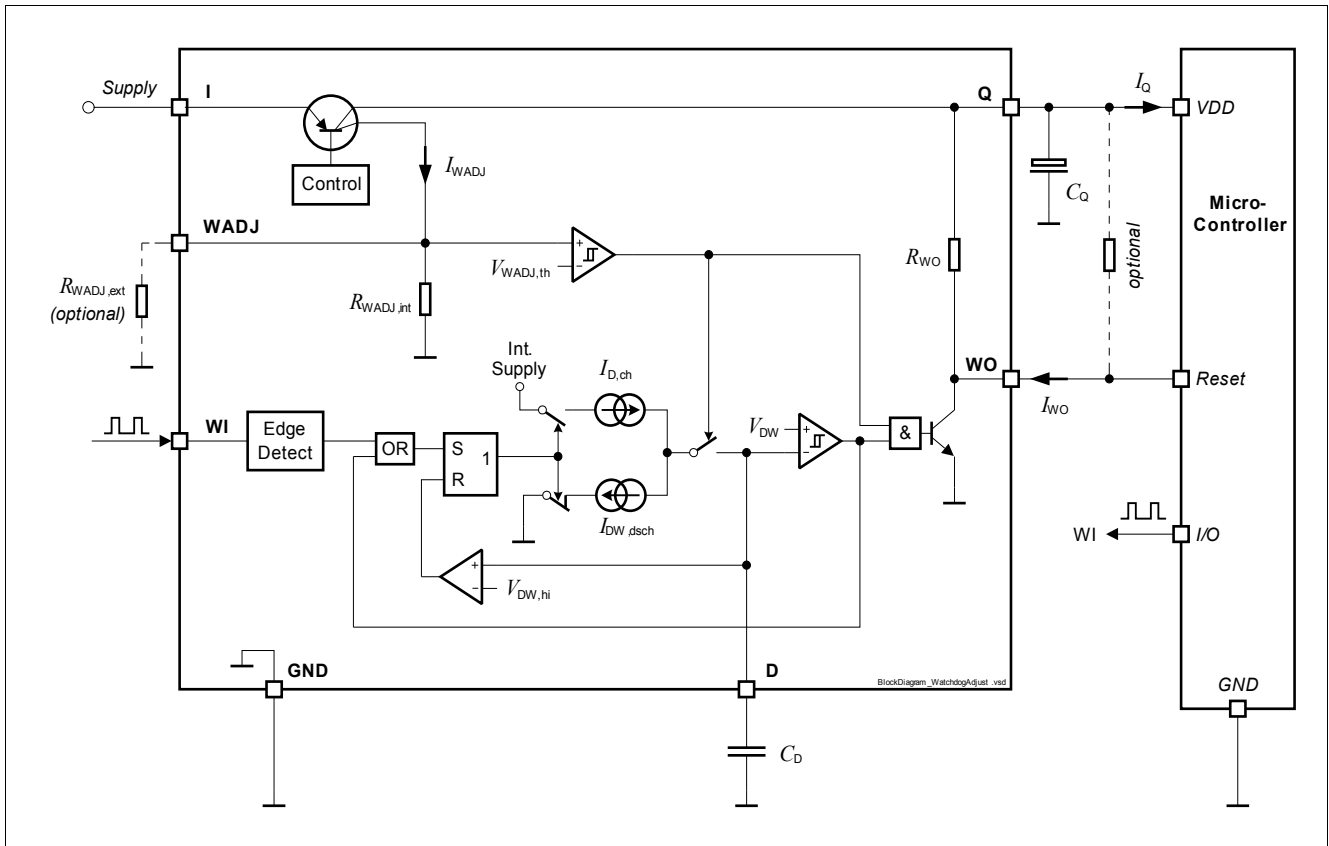


Figure 8 Block Diagram Watchdog Circuit

### Watchdog Output “WO”

The watchdog output “WO” is an open collector output with an integrated pull-up resistor. In case a lower-ohmic “WO” signal is desired, an external pull-up resistor to the output “Q” can be connected. Since the maximum “WO” sink current is limited, the optional external resistor  $R_{WO,ext}$  needs to be sized to comply with the watchdog output sink current (see [Table “Watchdog Output Low Voltage” on Page 25](#) and [Table “Watchdog Output Maximum Sink Current” on Page 25](#)).

### Watchdog Input “WI”

The watchdog is triggered by an positive edge at the watchdog input “WI”. The signal is filtered by a bandpass filter and therefore its amplitude and slope has to comply with the specification [Table “Watchdog Input” on Page 25](#) to [Table “Watchdog Input Signal Slew Rate” on Page 25](#). For details on the test pulse applied, see [Figure 9](#).

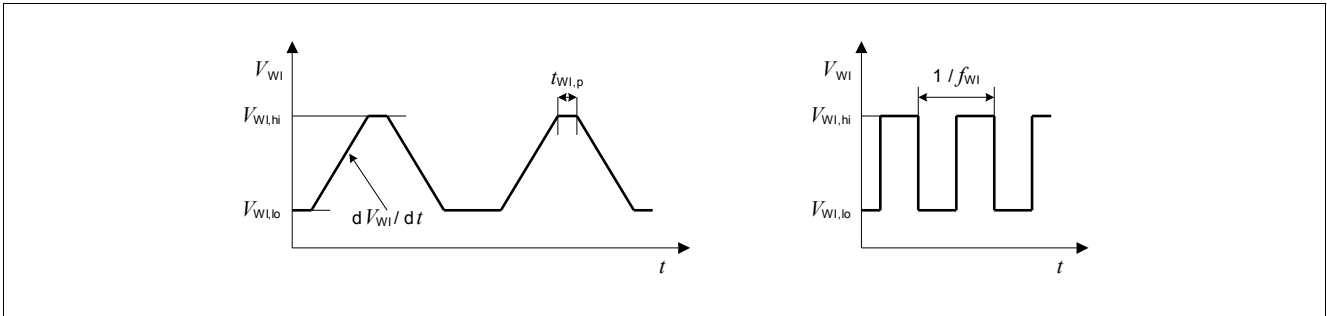


Figure 9 Test Pulses Watchdog Input WI

### Watchdog Timing

Positive edges at the watchdog input pin “WI” are expected within the watchdog trigger time frame  $t_{WI,tr}$ , otherwise a low signal at pin “WO” is generated. If a watchdog low signal at pin “WO” is generated, it remains low for  $t_{WD,lo}$ . All watchdog timings are defined by charging and discharging the capacitor  $C_D$  at pin “D”. Thus, the watchdog timing can be programmed by selecting  $C_D$ . For timing details see also [Figure 10](#).

In case a watchdog trigger time period  $t_{WI,tr}$  different from the value for  $C_D = 100\text{nF}$  is required, the delay capacitor’s value can be derived from the specified value given in [Table “Watchdog Trigger Time” on Page 26](#):

$$C_D = 100\text{nF} \times t_{WI,tr} / t_{WI,tr,100\text{nF}} \tag{5}$$

The watchdog output low time  $t_{WD,lo}$  and the watchdog period  $t_{WD,p}$  then becomes:

$$t_{WD,lo} = t_{WD,lo,100\text{nF}} \times C_D / 100\text{nF} \tag{6}$$

$$t_{WD,p} = t_{WI,tr} + t_{WD,lo} \tag{7}$$

The formula is valid for  $C_D \geq 10\text{nF}$ . For precise timing calculations consider also the delay capacitor’s tolerance.

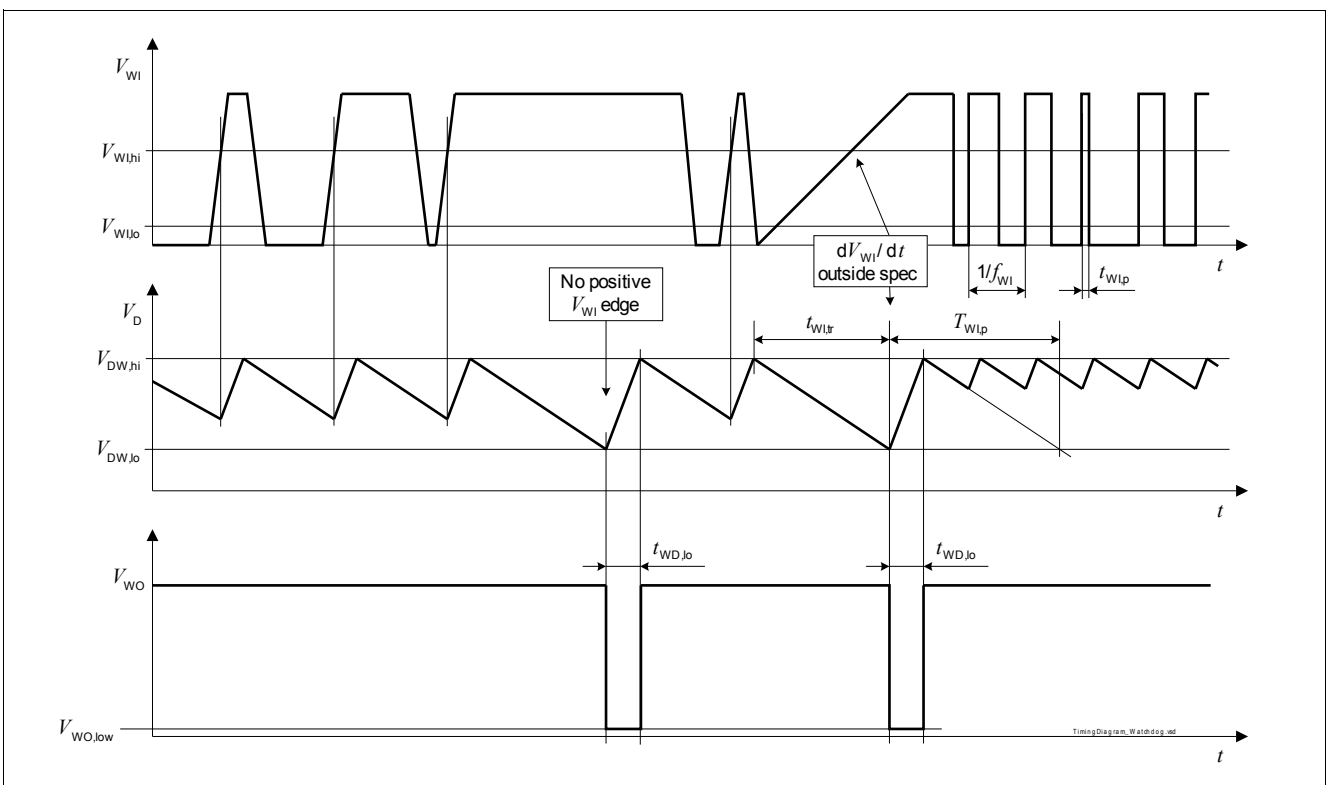


Figure 10 Timing Diagram Watchdog



## 8.2 Electrical Characteristics Watchdog Function

**Table 8 Electrical Characteristics: Watchdog Function**
 $V_1 = 13.5 \text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,

 all voltages with respect to ground, direction of currents as shown in [Table 8](#) (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
<b>Default Watchdog Activating Threshold (pin WADJ left open)</b>							
Watchdog Activating Threshold	$I_{Q,W\text{Dact,th}}$	0.65	1.1	1.65	mA	$I_Q$ increasing	P_8.2.1
Watchdog Deactivating Threshold	$I_{Q,W\text{Ddeact,th}}$	0.55	0.9	–	mA	$I_Q$ decreasing	P_8.2.2
Watchdog Activating Threshold Hysteresis	$I_{Q,W\text{Dact,hy}}$	–	26	–	$\mu\text{A}$	–	P_8.2.3
<b>Adjustable Watchdog Activating Threshold (external resistor connected to pin WADJ)</b>							
Watchdog Activating Threshold	$I_{Q,W\text{Dact,th}}$	–	1.76	–	mA	$I_Q$ increasing $R_{W\text{ADJ,ext}} = 220 \text{ k}\Omega^{1) 2)}$	P_8.2.4
Watchdog Deactivating Threshold	$I_{Q,W\text{Ddeact,th}}$	–	1.70	–	mA	$I_Q$ decreasing $R_{W\text{ADJ,ext}} = 220 \text{ k}\Omega^{1) 2)}$	P_8.2.5
Watchdog Activating Threshold Hysteresis	$I_{Q,W\text{Dact,hy}}$	–	60	–	$\mu\text{A}$	$R_{W\text{ADJ,ext}} = 220 \text{ k}\Omega^{1) 2)}$	P_8.2.6
<b>Watchdog Input WI</b>							
Watchdog Input Low Signal Valid	$V_{W\text{I,lo}}$	–	–	0.8	V	– <sup>3)</sup>	P_8.2.7
Watchdog Input High Signal Valid	$V_{W\text{I,hi}}$	2.6	–	–	V	– <sup>3)</sup>	P_8.2.8
Watchdog Input High Signal Pulse Length	$t_{W\text{I,p}}$	0.5	–	–	$\mu\text{s}$	$V_{W\text{I}} \geq V_{W\text{I,high}}^{3)}$	P_8.2.9
Watchdog Input Signal Slew Rate	$dV_{W\text{I}}/dt$	1	–	–	V/ $\mu\text{s}$	$V_{W\text{I,low}} \leq V_{W\text{I}} \leq V_{W\text{I,high}}^{3)}$	P_8.2.10
Watchdog Input Signal Frequency Capture Range	$f_{W\text{I}}$	–	–	1	MHz	Square Wave, 50% Duty Cycle <sup>3)</sup>	P_8.2.11
<b>Watchdog Output WO</b>							
Watchdog Output Low Voltage	$V_{W\text{O,low}}$	–	0.2	0.4	V	$I_{W\text{O}} = 1 \text{ mA}$ ; Watchdog active; $V_{W\text{I}} = 0 \text{ V}$	P_8.2.12
Watchdog Output Maximum Sink Current	$I_{W\text{O,max}}$	1.5	13	30	mA	$V_{W\text{O}} = 0.8 \text{ V}$ ; Watchdog active; $V_{W\text{I}} = 0 \text{ V}$	P_8.2.13
Watchdog Output Internal Pull-up Resistor	$R_{W\text{O}}$	20	30	45	k $\Omega$	–	P_8.2.14
<b>Watchdog Timing</b>							
Delay Capacitor Charge Current	$I_{D}$	–	2.78	–	$\mu\text{A}$	$V_{D} = 1 \text{ V}$	P_8.2.15
Delay capacitor watchdog discharge current	$I_{D\text{W,disch}}$	–	1.39	–	$\mu\text{A}$	$V_{D} = 1 \text{ V}$	P_8.2.16

**Table 8 Electrical Characteristics: Watchdog Function (cont'd)**

$V_1 = 13.5\text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,

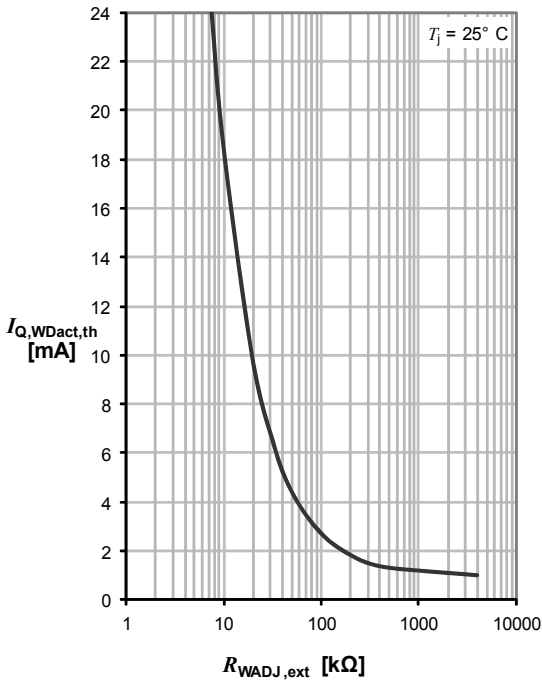
all voltages with respect to ground, direction of currents as shown in [Table 8](#) (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Upper watchdog timing threshold	$V_{DW,hi}$	–	1.2	–	V	–	P_8.2.17
Lower watchdog timing threshold	$V_{DW,lo}$	–	0.7	–	V	–	P_8.2.18
Watchdog Trigger Time	$t_{WI,tr,100nF}$	24	36	54	ms	Calculated value; $C_D = 100\text{ nF}$ <sup>4)</sup>	P_8.2.19
Watchdog Output Low Time	$t_{WD,lo,100nF}$	12	18	27	ms	Calculated value; $C_D = 100\text{ nF}$ <sup>4)</sup> $V_Q > V_{RT,lo}$	P_8.2.20
Watchdog Period	$t_{WD,p,100nF}$	36	54	81	ms	Calculated value; $t_{WI,tr,100nF} + t_{WD,lo,100nF}$ $C_D = 100\text{ nF}$ <sup>4)</sup>	P_8.2.21

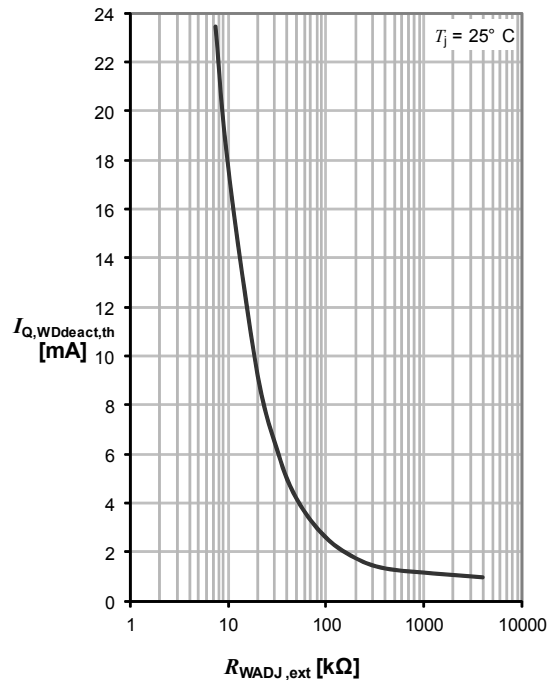
- 1) For details see Table 7.
- 2) Not subject to production test, specified by design.
- 3) For details on the test pulse applied, see [Figure 9](#).
- 4) For programming a different watchdog timing, see [Chapter 8.1](#)..

### 8.3 Typical Performance Characteristics Standard Watchdog Function

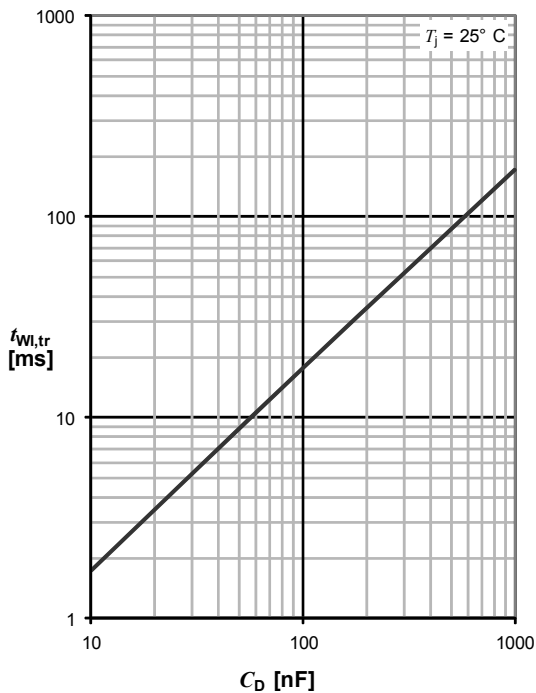
**Watchdog Activating Threshold  $I_{Q,WDact,th}$  versus External Resistor  $R_{WADJ,ext}$**



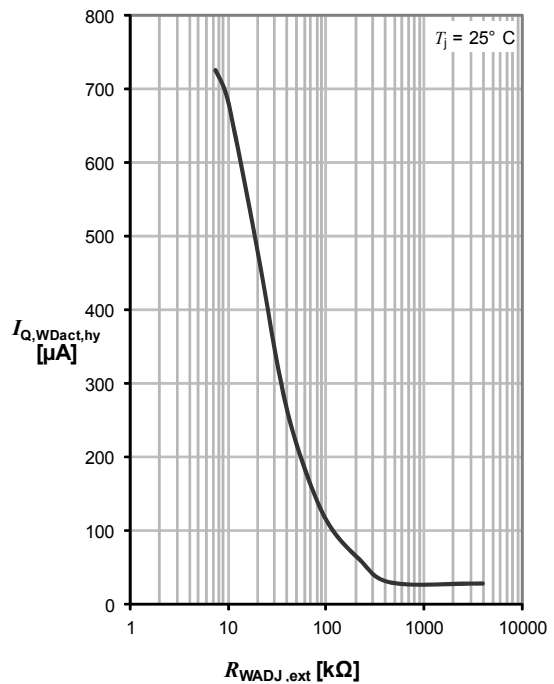
**Watchdog Deactivating Threshold  $I_{Q,WDdeact,th}$  versus External Resistor  $R_{WADJ,ext}$**



**Watchdog Trigger Time  $t_{WI,tr}$  versus Delay Capacitor  $C_D$**



**Watchdog Activation Threshold Hysteresis  $I_{Q,WDact,hy}$  versus External Resistor  $R_{WADJ,ext}$**



## 9 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

### 9.1 Application Diagram

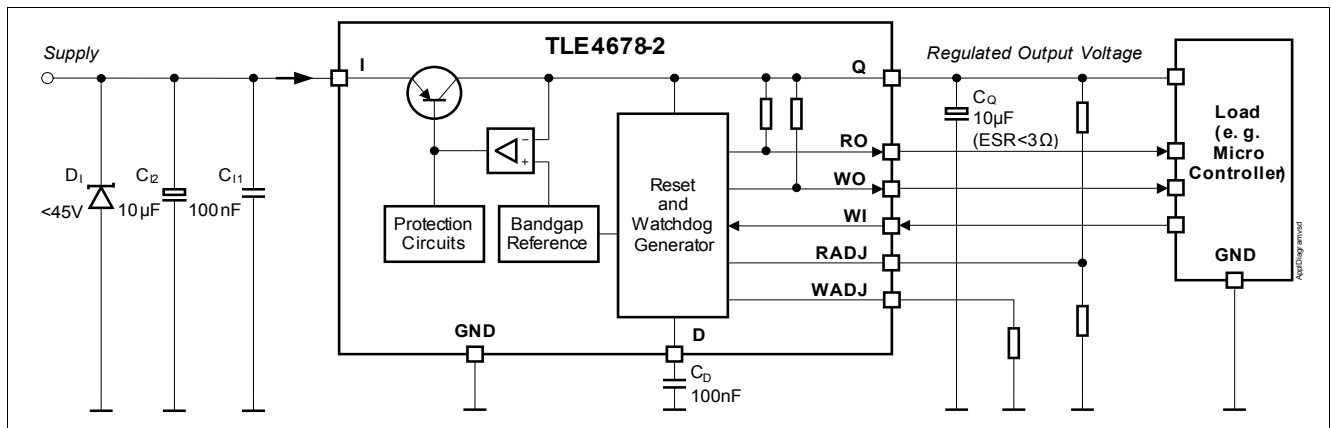


Figure 11 Application Diagram

### 9.2 Selection of External Components

#### 9.2.1 Input Pin

The typical input circuitry for a linear voltage regulator is shown in the application diagram above.

A ceramic capacitor at the input, in the range of 100nF to 470nF, is recommended to filter out the high frequency disturbances imposed by the line e.g. ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10µF to 470µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to over-voltage above 45 V.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in case of possible external disturbances.

#### 9.2.2 Output Pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in **“Functional Range” on Page 8**. The graph **“Output Capacitor Series Resistor ESR<sub>CQ</sub> versus Output Current I<sub>Q</sub>” on Page 12** shows the stable operation range of the device.

TLE4678-2 is designed to be stable with extremely low ESR capacitors. According to the automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator’s output and GND pins and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

### 9.3 Thermal Considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (8)$$

with

- $P_D$ : continuous power dissipation
- $V_I$ : input voltage
- $V_Q$ : output voltage
- $I_Q$ : output current
- $I_q$ : quiescent current

The maximum acceptable thermal resistance  $R_{thJA}$  can then be calculated:

$$R_{thJA,max} = (T_{j,max} - T_a) / P_D \quad (9)$$

with

- $T_{j,max}$ : maximum allowed junction temperature
- $T_a$ : ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in [“Thermal Resistance” on Page 8](#).

#### Example

Application conditions:

$$V_I = 13.5V$$

$$V_Q = 5V$$

$$I_Q = 50mA$$

$$T_a = 85^\circ C$$

Calculation of  $R_{thJA,max}$ :

$$\begin{aligned} P_D &= (V_I - V_Q) \times I_Q + V_I \times I_q \\ &= (13.5V - 5V) \times 50mA + 13.5V \times 1.6mA \\ &= 0.425W + 0.022W \\ &= 0.447W \end{aligned}$$

$$\begin{aligned} R_{thJA,max} &= (T_{j,max} - T_a) / P_D \\ &= (150^\circ C - 85^\circ C) / 0.447W = 145.41K/W \end{aligned}$$

As a result, the PCB design must ensure a thermal resistance  $R_{thJA}$  lower than 145.41 K/W. According to [“Thermal Resistance” on Page 8](#), at least 300 mm<sup>2</sup> heatsink area is needed on the FR4 1s0p PCB, or the FR4 2s2p board can be used.

## 9.4 Reverse Polarity Protection

TLE4678-2 is self protected against reverse polarity faults and allows negative supply voltage. External reverse polarity diode is not needed. However, the absolute maximum ratings of the device as specified in **“Absolute Maximum Ratings” on Page 7** must be kept.

The reverse voltage causes several small currents to flow into the IC hence increasing its junction temperature. As the thermal shut down circuitry does not work in the reverse polarity condition, designers have to consider this in their thermal design.

## 9.5 Further Application Information

- For further information you may contact <http://www.infineon.com/>

## 10 Package Outlines

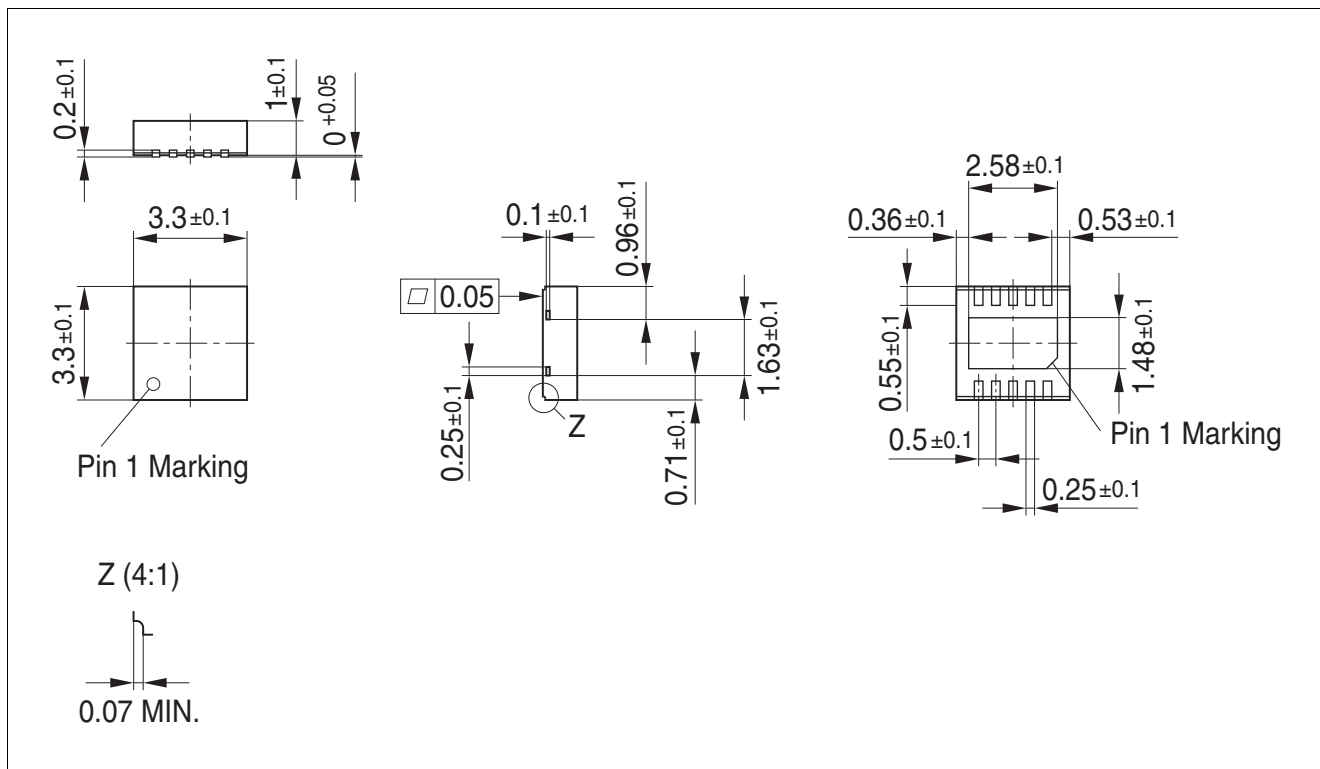


Figure 12 PG-TSON10

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

## 11 Revision History

Revision	Date	Changes
1.0	2014-03-03	Initial version



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#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.