General Description

The PV88080 power management integrated circuit (PMIC) provides one PWM buck controller and three adjustable synchronous buck regulators. The high voltage buck controller can optionally be used to generate the supply for the other three buck converters. Two pass devices (NMOS FET) for the high side and low side of the high voltage buck controller are external which allows the majority of the buck controller power dissipation to be outside the PV88080. This high voltage buck controller uses a constant on time (COT) control scheme with integrated bootstrap PMOS switch. In certain applications, multiple PV88080s can be used together to provide enough power rails to power the larger systems. There are three buck converters that can be used to generate the supplies for CPUs, DDR memory and other Auxiliary functions in a typical application. The pass devices of these buck converters are fully integrated, so no external FETs or Schottky diodes are needed. This results in optimized power efficiency and a reduced external component count. PV88080 provides Dynamic Voltage Control (DVC) via I2C command to support adaptive adjustment of the supply voltage based on the processor. All power blocks have over current circuit protection and the start-up timing can be controlled through the I^2C interface. Soft start-up limits the inrush current from the input node and secures a slope controlled activation of the rail. The PV88080 is available in a 32-pin QFN package and is specified from –40 °C to 85 °C ambient temperature.

Key Features

- One synchronous buck controller
  - V_{IN} input voltage range : 7 V to 26 V
  - Programmable output voltage : 0.8 V~5.25 V when V_{IN} <13.2 V or 1.8 V~5.25 V when V_{IN} >13.2 V
  - Supports all ceramic output capacitors
  - Switching frequency up to 1 Mhz
  - Reference voltage with ±1% tolerance
  - Provide OVP, OCP and OTP
- Three synchronous buck converters with integrated low R_{ON} FET
  - Buck1, programmable output voltage from 0.75 V to 3.3 V with 5-A continuous output current. Peak current 6 A if standalone.
  - Buck2, programmable output voltage from 0.9 V to 3.6 V with 2-A continuous output current. Peak current 3 A if standalone.
  - Buck3, programmable output voltage from 0.9 V to 3.6 V with 2-A continuous output current. Peak current 3 A if standalone.
  - Light load efficiency improved > 85%
  - Boot up selectable output voltage through GPIO
- Dynamic Voltage Control (DVC) on all buck converters
- Constant on time (COT) control with selectable frequencies
- Auto mode on all three buck converters
- Adjustable soft start
- Two GPIO, one nIRQ and I^2C compatible interface
- Mute function: eliminates audio popping noise in power plug OFF scenario.
- Power fail detect function to alert the application processor.
- External thermal sense function: establish the remote temperature sensing ability on the system.
- -40 to 85 ºC ambient temperature range
- Custom 32-pin QFN package with thermal pad, 0.5 mm pin pitch

Applications

- Supply for digital television processor
- Power supply for digital Set Top Box (STB)
- Networking home terminal

System Diagram

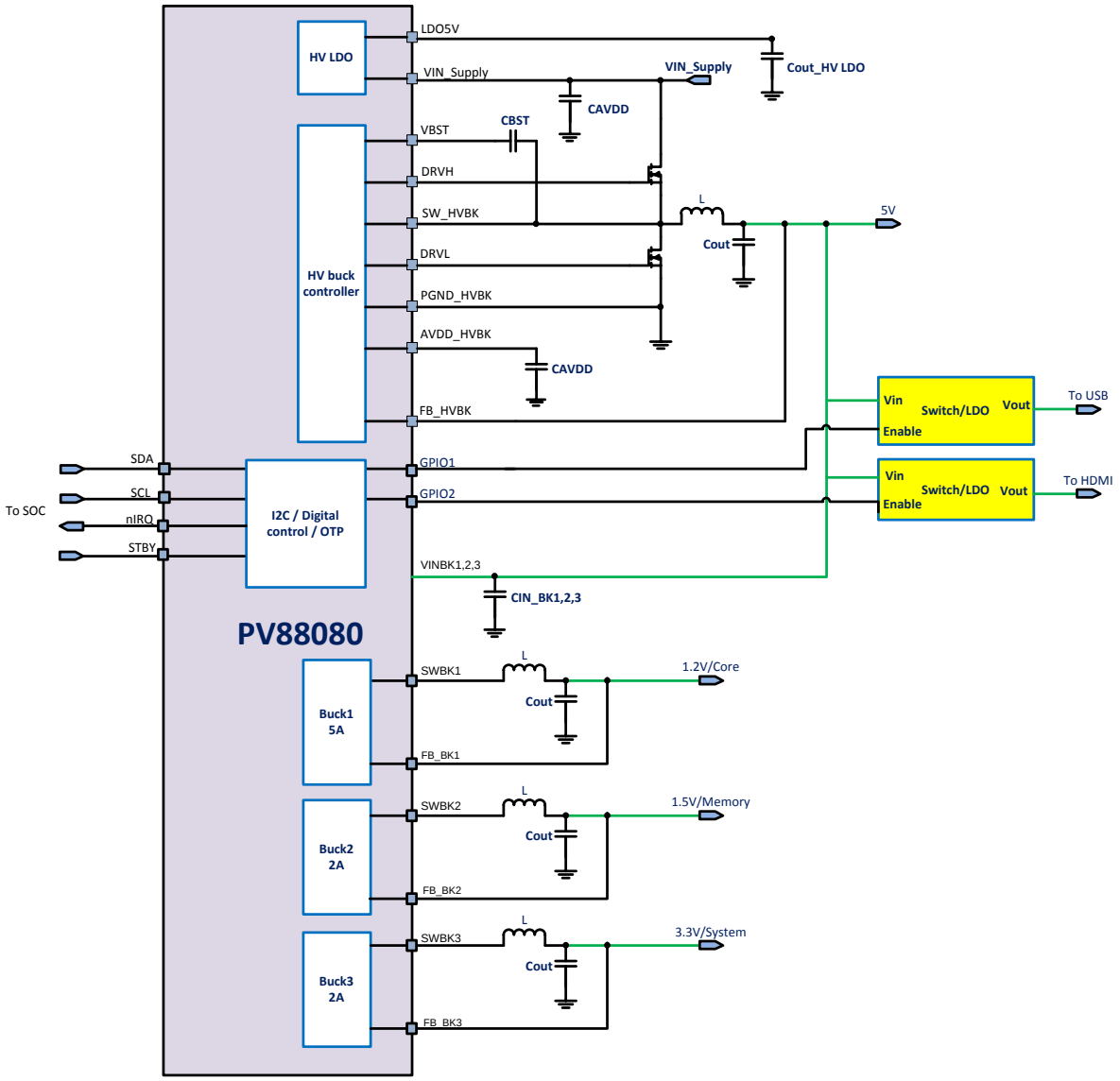

Figure 1: PV88080 Application Circuit

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1 Block Diagram

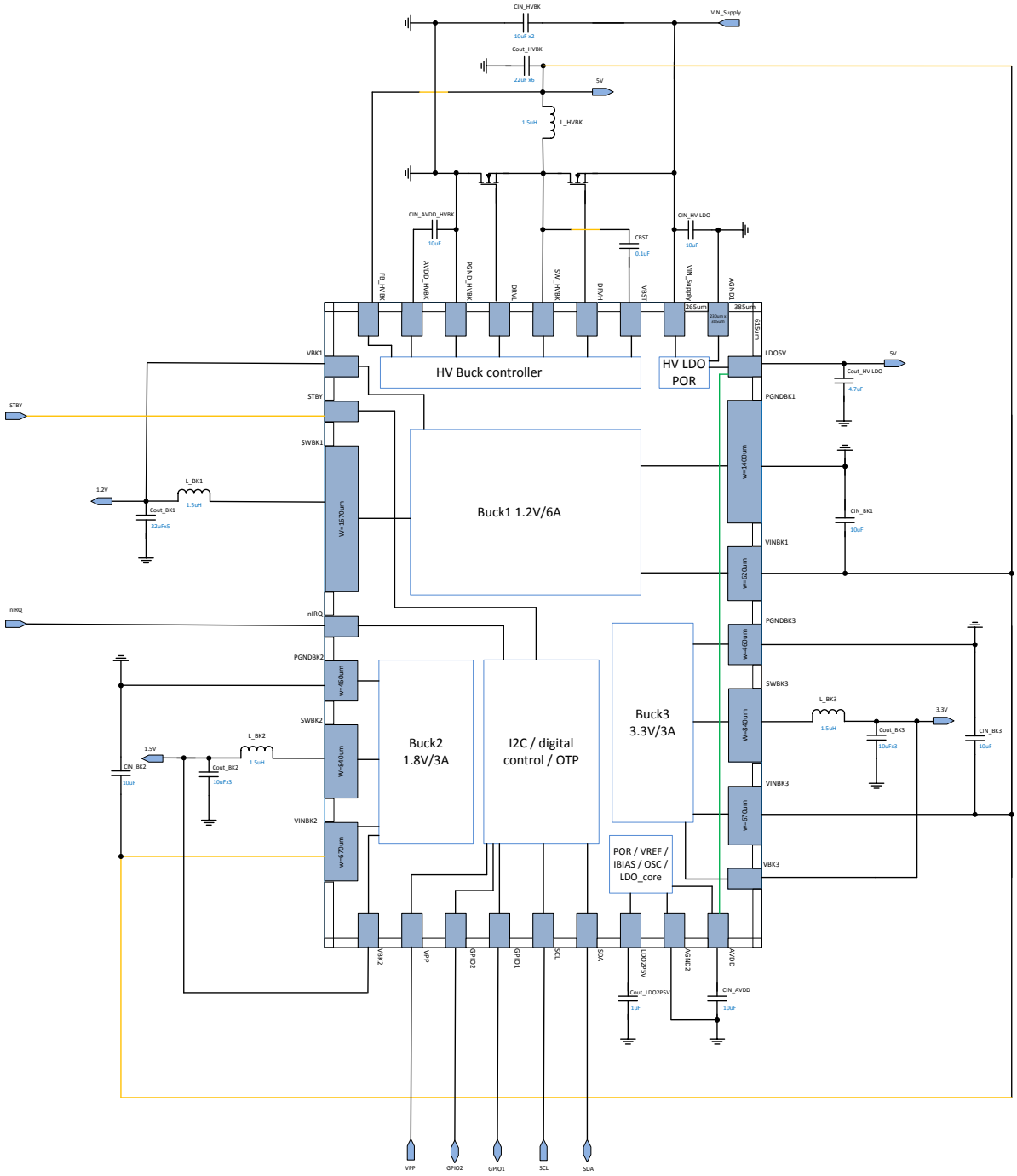


Figure 1: PV88080 Block Diagram

2 Pinout

The pin outs are subject to change during the detailed design and floor planning stages.

Table 1: PV88080 Pin Description

Pin No.	Pin Name	Type (Table 2)	Description
1	FB_BK1 (VBK1)	AI	Feedback node for Buck1
2	STBY	DI	System standby signal or acting as power enable
3	SWBK1	AO	Switching node for Buck1 To be connected to output inductor
4	nIRQ	DO	Interrupt line towards the host Option role can be set by OTP: Buck2 voltage selection; MUTE flag; Power fail detect function flag; GPO.
5	PGNDBK2	VSS	Power Ground for Buck2
6	SWBK2	AO	Switching node for Buck2 To be connected to output inductor
7	VINBK2	PS	Supply voltage for Buck2 To be connected to VDD after Input Capacitor
8	FB_BK2 (VBK2)	AI	Feedback node for Buck2
9	VPP	VSS	Connect to VSS in application
10	GPIO2	DIO	General Purpose I/O Option roles can be set by OTP: Buck2 voltage selection; MUTE flag; TS source current output.
11	GPIO1	DIO	General Purpose I/O Option roles can be set by OTP: Buck2 voltage selection; MUTE flag.
12	SCL	DI	2-WIRE clock
13	SDA	DIO	2-WIRE data Option role can be set by OTP: GPO
14	LDO2P5V	AO	Supply for internal digital circuit.
15	AGND2	VSS	Analog Ground. Connected directly to the PCB ground plane.
16	AVDD	PS	Analog Supply Voltage, internally short to LDO5V and externally shorted by PCB trace.
17	FB_BK3 (VBK3)	AI	Feedback node for Buck3
18	VINBK3	PS	Supply voltage for Buck3 To be connected to VDD after Input Capacitor
19	SWBK3	AO	Switching node for Buck3 To be connected to output inductor
20	PGNDBK3	VSS	Power Ground for Buck3

Pin No.	Pin Name	Type (Table 2)	Description
21	VINBK1	PS	Supply voltage for Buck1 To be connected to VDD after Input Capacitor
22	PGNDBK1	VSS	Power Ground for Buck1
23	LDO5V	AO	Analog Supply Voltage, internally short to AVDD
24	AGND1	VSS	Analog Ground. Connected directly to the PCB ground plane.
25	VIN_Supply	PS	High voltage supply for the HV buck controller
26	VBST	AO	Bootstrap node external cap
27	DRVH	AO	High side driver pin to drive external MOS
28	SW_HVBK	AO	Switching node for HV buck controller
29	DRVL	AO	Low side driver pin to drive external MOS
30	PGND_HVBK	VSS	Ground for HV buck controller
31	AVDD_HVBK	PS	Supply for HV buck controller driver block
32	FB_HVBK	AI	Feedback node for HV buck controller

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital Input	AI	Analog Input
DO	Digital Output	AO	Analog Output
DIO	Digital Input / Output	AIO	Analog Input / Output
PS	Power Supply	VSS	Ground

3 Characteristics

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Recommended Operating Conditions are conditions for which the device is intended to be functional, but parameter specifications may not be guaranteed. For guaranteed specifications and associated test conditions, see the Min and Max limits and Conditions in the Electrical Characteristics tables. Electrical Characteristics table limits are guaranteed by production testing, design or correlation using standard Statistical Quality Control methods. Typical (Typ) specifications are mean or average values from characterization at 25 °C and are not guaranteed.

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Max	Unit
T_{STG}	Storage temperature		-60	+165	°C
T_J	Junction temperature		-40	+125	°C
	Voltage at pins	Pins: FB_BK1, STBY, SWBK1, SWBK2, VINBK2, FB_BK2, SCL, AVDD, FB_BK3, VINBK3, SWBK3, VINBK1, LDO5V, DRVL, AVDD_HVBK, FB_HVBK	-0.3	5.5	V
		Pins: nIRQ, GPIO2, GPIO1, SDA, LDO2P5V,	-0.3	2.75	V
		Pins: VIN_Supply, SW_HVBK	-0.3	26	V
		Pins: VBST, DRVH	-0.3	31.5	V
		Pins: VBST-SW_HVBK, DRVH-SW_HVBK.	-0.3	5.5	V
	ESD compliance	Human body model		2	kV
		CDM		500	V

Note 1 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Max	Unit
T_A	Operating temperature		-40		+85

All voltages are referenced to VSS unless otherwise stated. Currents flowing into PV88080 are deemed positive, currents flowing out are deemed negative. Unless otherwise stated, all parameters are valid over the recommended temperature range and power supply range. Please note that the power dissipation must be limited to avoid overheating of PV88080. The maximum power dissipation should not be reached at maximum ambient temperature.

3.3 Electrical Characteristics

3.3.1 Power Dissipation

The power that can be dissipated by this circuit is limited by the package, PCB technology and ambient temperature. The load on the various outputs must be limited to stay below the power dissipation limit for the PCB/ambient conditions.

An integrated over temperature protection circuit is provided to prevent the chip exceeding the safe operating range. The over temperature protection threshold is guaranteed to be a maximum junction temperature of T_J=125 °C.

Use cases specified for the power dissipation are given in Table 5.

Table 5: Power Dissipation Use Cases

Use Case			High Power Dissipation 1	High Power Dissipation 2	Low Power Dissipation 1
Package			QFN	QFN	QFN
Board Technology			4 layer 100mm*100mm	4 layer 100mm*100mm	2 layer 100mm*100mm
Block	**Function**	**Voltage (V)**	**Current (mA)**	**Current (mA)**	**Current (mA)**
Buck 1	CORE	1.2	5000	6000	3000
Buck 2	MEMORY	1.8	2000	3000	3000
Buck 3	AUX	3.3	2000	1000	3000
HV Buck Controller	Supply Buck1-3	5.0	20000	20000	10000

3.3.2 Buck Converters / Controller

Buck1 to Buck3 are high efficiency synchronous step down regulators operating at 1 MHz frequency and providing individual output voltages with +/- 3% accuracy.

The default output voltages of these regulators are loaded from OTP and can be programmed in 5 mV steps. The switching frequency is chosen to be high enough to allow the use of a 1.5 uH inductor.

The buck converter has an automatic mode where it switches between synchronous mode (PWM) and sleep mode (PFM) depending on the load current. An internal zero crossing comparator is used to time the turn-off of the internal MOSFET, thereby removing the need for an external Schottky diode. The quiescent current for all these buck converters in PFM mode is 25 uA.

Each one of the three buck converters can be individually controlled (through I^2C) by dedicated registers. All buck converter pins deliver high currents except the feedback pin.

Each one of the three buck converters contains a P-MOSFET on the high side and N-MOSFET on the low side. These two MOSFET devices are integrated inside the PV88080.

All PV88080 buck converters feature a programmable pull down resistors, which can be either enabled or disabled when the buck converters is powered down.

Table 6: Bucks Summary

Block	V_{OUT}	I_{OUT}	External Components	Control
Buck1	0.75 V - 3.3 V	PWM: 5000 mA	L=1.5 uH / C_{OUT} > 60 uF	I^2C
Buck2	0.9 V – 3.6 V	PWM: 2000 mA	L=1.5 uH / C_{OUT} > 34 uF	I^2C
Buck3	0.9 V – 3.6 V	PWM: 2000 mA	L=1.5 uH / C_{OUT} > 34 uF	I^2C
HV Buck Controller	0.8 V – 5.25V (V_{IN} < 13.2 V) 1.8 V – 5.25 V (V_{IN} > 13.2 V)	>10 A	L=1.5 uH / C_{OUT} >130 uF	I^2C

3.3.3 Buck1 Core Voltage

Buck1 is a high efficiency synchronous step down regulators operating at 1 MHz frequency and providing individual output voltages with +/- 3% accuracy. The default output voltage of the regulator is loaded from OTP and can be programmed. The switching frequency is chosen to be high enough to allow the use of a 1.5 uH inductor. The standalone Buck1 can support the output load up to 6 A continuous current at nominal output voltage of 1.2 V. Maximum current depends on the system power dissipation calculation. Switch sizes are optimized for 1.2 V. The Buck1 converter supports dynamic voltage control (DVC) at the output voltage range of 0.75 V to 3.3 V.

The Buck1 converter has an automatic mode where it switches between synchronous mode (PWM) and sleep mode (PFM) depending on the load current. An internal zero crossing comparator is used to time the turn-off of the internal MOSFET, thereby removing the need for an external Schottky diode. The quiescent current for all these buck converters in PFM mode is 25 uA.

Table 7: Electrical Characteristics V_{DD} = 4.75 to 5.25 V

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage		4.75		5.25	V
C_{OUT}	Output capacitance	(including voltage and temperature coefficient)	60		200	µF
LBK1	Inductor value		-20 %	1.5	20 %	µH
VBUCK1	Output voltage	I_{OUT} = 5 A	0.75		3.3	V
	Output voltage accuracy	V_{DD} = 5 V V_{OUT}=1.01 V, I_{OUT}=0 A PWM operation	-3		3	%
	Load regulation	V_{DD} = 5 V, V_{OUT} = 1.2 V, I_{OUT} = 0 A~5 A PWM operation		1.67		%/A
	Line regulation	V_{DD} = 4.75 V ~ 5.25 V V_{OUT}=1.2 V, I_{OUT}=0 A PWM operation		0.33		%/V
	Output Current			5000	6000	mA
I_{Q_OFF}	Quiescent current in OFF mode				2	µA
Fsw	Switching frequency			1		MHz
	Switching duty cycle		10		95	%

3.3.4 Buck2 Memory

Buck2 is a high efficiency synchronous step down regulators operating at 1 MHz frequency and providing individual output voltages with +/- 3% accuracy. The default output voltage of the regulator is loaded from OTP and can be programmed. The switching frequency is chosen to be high enough to allow the use of a 1.5 uH inductor. The standalone Buck2 can support the output load up to 3 A continuous current at nominal output voltage of 1.8 V. Maximum current depends on the system power dissipation calculation.

The Buck2 converter supports dynamic voltage control (DVC) at the output voltage range of 0.9 V to 3.6 V. The Buck2 converter has an automatic mode where it switches between synchronous mode

(PWM) and sleep mode (PFM) depending on the load current. An internal zero crossing comparator is used to time the turn-off of the internal MOSFET, thereby removing the need for an external Schottky diode. The quiescent current for all these buck converters in PFM mode is 25 uA.

Table 8: Electrical Characteristics V_{DD} = 4.75 to 5.25 V

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage		4.75		5.25	V
C_{OUT}	Output capacitance	(including voltage and temperature coefficient)	34	60	200	µF
LBK2	Inductor value		-20 %	1.5	20 %	µH
VBUCK2	Output voltage		0.9		3.6	V
	Output voltage accuracy	V_{DD} = 5 V V_{OUT}=1.85 V, I_{OUT}=0 A PWM operation	-3		3	%
	Load regulation	V_{DD} = 5 V, V_{OUT} = 1.8 V, I_{OUT} = 0 A~2 A PWM operation		1.11		%/A
	Line regulation	V_{DD} = 4.75 V ~ 5.25 V V_{OUT}=1.8 V, I_{OUT}=0 A PWM operation		0.22		%/V
	Output Current			2000	3000	mA
I_{Q_OFF}	Quiescent current in OFF mode				2	µA
Fsw	Switching frequency			1		MHz
	Switching duty cycle		10		95	%

3.3.5 Buck3 Aux

Buck3 is a high efficiency synchronous step down regulators operating at 1 MHz frequency and providing individual output voltages with +/- 3% accuracy. The default output voltage of the regulator is loaded from OTP and can be programmed. The switching frequency is chosen to be high enough to allow the use of a 1.5 uH inductor. The standalone Buck3 can support the output load up to 3 A continuous current at nominal output voltage of 3.3 V. Maximum current depends on the system power dissipation calculation. The Buck3 converter supports dynamic voltage control (DVC) at the output voltage range of 0.9 V to 3.6 V. The Buck3 converter has an automatic mode where it switches between synchronous mode (PWM) and sleep mode (PFM) depending on the load current.

An internal zero crossing comparator is used to time the turn-off of the internal MOSFET, thereby removing the need for an external Schottky diode. The quiescent current for all these buck converters in PFM mode is 25 uA.

Table 9: Electrical Characteristics V_{DD} = 4.75 to 5.25 V

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage		4.75		5.25	V
C_{OUT}	Output capacitance	(including voltage and temperature coefficient)	34	60	200	µF
LBK3	Inductor value		-20 %	1.5	20 %	µH
VBUCK3	Output voltage		0.9		3.6	V
	Output voltage accuracy	V_{DD} = 5 V V_{OUT}=3.25 V, I_{OUT}=0 A PWM operation	-3		3	%
	Load regulation	V_{DD} = 5 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A~2 A PWM operation		1.21		%/A
	Line regulation	V_{DD} = 4.75 V ~ 5.25 V V_{OUT}=3.3 V, I_{OUT}=0 A PWM operation		0.6		%/V
	Output Current			2000	3000	mA
I_{QFF}	Quiescent current in OFF mode				2	µA
Fsw	Switching frequency			1		MHz
	Switching duty cycle		10		95	%

3.3.6 HV Buck Controller

The HV buck controller is a high efficiency synchronous step down controller. The Constant On Time (COT) control scheme enables the fast transient response with no external compensation components. The HV buck controller allows wide input voltage range (9 V to 26 V) and can support the output load up to 20 A. It operates at pseudo constant frequency at CCM and can support DCM operation. The default output voltage of the controller is loaded from OTP and can be programmed.

The switching frequency is chosen to be high enough to allow the use of a 1.5 uH inductor. The high side and low side drivers are integrated internally and designed to drive the gate of the external N-MOSFET. The HV buck controller requires a bootstrap capacitor from SW_HVBK to VBST to provide a floating voltage supply for the high side driver. The boot charging PMOS switch is integrated internally. There is an 8-bit internal DAC in HV buck controller.

The LSB of the DAC is 5 mV with output ranges from 0.8 V to 1.275 V. When the HV buck controller output voltage is set at 1.0 V, the controller regulates the VFB_HVBK pin to DAC, such that VFB_HVBK=V_{OUT}. When the HV buck controller output voltage is set at 5.0 V, the controller regulates the VFB_HVBK pin. The HV buck controller is designed to be very flexible to fit into various market applications. Therefore, several parameters are designed to be configurable including:

OV, UV, OC, negative OC, zero current detection threshold,

Soft-start / soft-stop slew rate,

External MOSFET driver dead time,

External MOSFET switching ringing suppression,

Constant-on time and ramp characteristics.

Table 10: Electrical Characteristics V_{DD} = 4.75 to 5.25 V

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage		4.75		5.25	V
V_{IN}	Input voltage		7		26	V
C_{OUT}	Output capacitance	(including voltage and temperature coefficient)	34	60	200	µF
LHVBK	Inductor value		-20 %	1.5	20 %	µH
L_{ESR}	Inductor resistance				10	mΩ
V_{OUT}	Output Voltage	DC V_{OUT} for the first PV88080, FB = V_{OUT}*(1/5)	4.75		5.25	V
V_{OUT}	Output Voltage	DC V_{OUT} for the other PV88080s with V_{IN}>13.2 V, FB is from divided V_{OUT}	1.8		5.25	V
V_{OUT}	Output Voltage	DC V_{OUT} for the other PV88080s with V_{IN}<13.2 V, FB is from divided V_{OUT}	0.8		5.25	V
	FB voltage step			5		mV
	Output voltage accuracy	V_{IN} =12 V V_{OUT} =FB=1 V T_A=25 ºC	-1		1	%

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{OUT\_TR\_LOAD}$	Load regulation transient	I_{OUT} = 25 %*Imax/Imax V_{IN}=12 V+/-10%, V_{OUT}=1 V. L=1.5 µH C=470 uF Tr=Tf=25 us			30	mV
$V_{OUT\_TR\_LOAD}$	Load regulation transient	I_{OUT} = 25 %*Imax/Imax V_{IN}=12 V+/-10 %, V_{OUT}=5 V. L=1.5 µH C=470 uF Tr=Tf=25 us			150	mV
F_{SW}	Switching frequency	V_{IN}=12 V, V_{OUT}=FB=1 V		500		kHz
T_{OFF}	Minimum off time			200		ns
	DRVH source resistance	T_A=25 ºC I(DRVH)=-50 mA		3		Ω
	DRVH sink resistance	T_A=25 ºC I(DRVH)=-50 mA		3		Ω
	DRVL source resistance	T_A=25 ºC I(DRVL)=-50 mA		1.5		Ω
	DRVL sink resistance	T_A=25 ºC I(DRVL)=-50 mA		1.5		Ω
	DRVH-low to DRVL-high dead time			20		ns
	DRVL-low to DRVH-high dead time			20		ns

NOTE:
A minimum RDS_on of 3 milli-ohms for the low side MOSFET is recommend when utilizing mode switching.

3.3.7 Core LDO

The core LDO generates the 2.5 V core supply for the digital.

Table 11: Electrical Characteristics V_{DD} = 4.75 to 5.25 V

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage		4.75		5.25	V
C_{IN}	Decoupling capacitor			1		uF
C_{OUT}	Stabilization capacitor	(including voltage and temperature coefficient at 2.5 V)	-55 %	1	+35 %	uF
	ESR resistance	F=1 MHz			0.1	Ω
I_{OUT_MAX}	Max output current				4	mA
I_Q	Quiescent current			7.5		uA
I_{OUT_SHDN}	Shutdown current				6	nA
V_{OUT_LDO}	Output voltage	I_{OUT} = Imax	2.48	2.50	2.52	V

3.3.8 HV LDO

The HV LDO generates the 5 V supply for the analog blocks, HV controller and partially the HV controller driver.

Table 12: Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage		7		26	V
C_{OUT}	Stabilization capacitor (minimum capacitance to ensure stability)	(including voltage and temperature coefficient at 5 V)	-55 %	4.7	+35 %	uF
	ESR of capacitor	F=1 MHz			0.1	Ω
V_{OUT}	Output Voltage	V_{IN}=9 V, 12 V, 26 V	4.98	5	5.1	V
I_Q	Quiescent current	V_{IN}=9 V, 12 V, 26 V Iload=0	7.2	7.5	8.3	µA
I_{MAX}	Maximum Output Current	V_{IN}=9 V to 26 V			100	mA
$V_{OUT\_TR\_LOAD}$	Load transient response	V_{IN} = 9 V, 12 V, 26 V I_{OUT} = 1 uA to I_{MAX} tr = tf = 0.1 µs			90	mV
$V_{OUT\_TR\_LINE}$	Line transient response	V_{IN} = 10.8 V to 13.2 V 21.6 to 26.4 V I_{OUT} = I_{MAX} tr = tf = 10 µs			13	mV
T_{ON}	Turn on time	V_{IN}=9 V, 12 V, 26 V V_{OUT}=10 % to 90 % I_{OUT}=0 A		150	435	µs

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{OFF}	Shut down current	V_{IN} = 9 V			2.2	µA
OVP	Over voltage protection			5.1		V
OCP	Over current protection			225		mA

3.3.9 Power on Reset

PV88080 POR is generated when the Vin_Supply pin voltage rises to 6.5 V. A POR event returns the chip to the NO POWER condition. All registers are cleared and the OTP is reloaded on the next start.

The hysteresis voltage of 500 mV maximum is implemented in PV88080.

Table 13: Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage		7		26	V
V_{DD}	Supply voltage		4.0		5.65	V
V_{REF}	Reference voltage		-1%	1.2	1%	V
	IBIAS current accuracy		-3		3	%
V_{POR_HI}	Upper POR threshold		6.5			V
V_{POR_HYS}	POR hysteresis voltage				500	mV

3.3.10 Supply Monitoring

The 5 V V_{DD} supply is monitored by the VDD fault comparator.

The circuits remain in the RESET state until 5 V has been established ($V_{DD\_FLT\_LO}$).

If the 5 V V_{DD} supply falls below $V_{DD\_FLT\_TR}$ the input supply is too low, and a fault condition is generated.

Table 14: Electrical Characteristics V_{DD} = 4.75 to 5.25 V

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{POR_HI}	Upper POR threshold	Digital core supply	2.25	2.375	2.5	V
V_{POR_LO}	Lower POR threshold	Digital core supply		2.0		V
V_{DD_FLT}	V_{DD} fault			4.5		V
$V_{DD\_FLT\_HYS}$	V_{DD} fault hysteresis			100		mV
OT	Critical temperature		125	140	155	°C

3.3.11 Fault Condition

A fault condition is generated by:

An over temperature event,

An under voltage of the 5 V supply

If a fault condition is detected the chip will signal an alert to the other chip, then follow its power down sequence without waiting for the other chip. At the end of the power down sequence the chip moves to the RESET state.

In the RESET state the registers, apart from the fault log, are reset and the OTP is reloaded at start-up.

Table 15: Electrical Characteristics V_{DD} = 4.75 to 5.25 V

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage		4.75		5.25	V
$V_{DD\_FLT\_UPPER}$	V_{DD} fault upper			4.5		V
$V_{DD\_FLT\_LWR}$	V_{DD} fault lower			4.4		V
$V_{DD\_FLT\_CRIT}$	V_{DD} fault critical			4.2		V

3.3.12 Digital I/O Signals

Standby Pin (STBY)

The STBY pin is an input which controls the power up sequence of a system containing PV88080. If STBY=0 the power up sequence is followed to ACTIVE mode. If STBY=1 the power down sequence is followed to STANDBY mode. STBY should be 0 at power up so that the system boots when power is applied.

Interrupt Request (nIRQ)

The nIRQ is an active low output signal which indicates that an interrupt causing event has occurred and status information is available in the related registers. Such information can be temperature, voltage and over current fault conditions.

When an event bit is set the nIRQ signal is asserted (unless masked by a bit in the IRQ mask register), the nIRQ is not released until the event registers have been cleared by writing to the related register with an assigned ‘1’ for the bit to be cleared. The event registers should be written in PAGE/REPEATED mode because the nIRQ is not cleared until all registers with an asserted event have been reset. New events that occur during writing to the registers are held until all the event registers have been written. Then they are passed to the event register, ensuring the SOC does not miss them.

There are also some reserved options for the digital pins function/definition which are programmable by the OTP memory. Table 16 shows the list of the options, and the functionality can be realized for different applications with proper role combinations of the pins.

Table 16: GPIO Functions Summary

	Sequencer Control GPO	Voltage Selection for Buck1/2/3 (digital in)	MUTE flag (digital out)	TS 10 uA source current (analog in/out)	TS flag (digital out)	Normal GPIO (digital in/out)
GPIO_1 (pin GPIO1)	v	v	v			v
GPIO_2 (pin GPIO2)	v	v	v	v		v
GPIO_3/nIRQ (pin nIRQ)	v	v	v		v	v
GPIO_4/SDA (pin SDA)	v					

Table 17: Electrical Characteristics V_{DD} = 4.75 to 5.25 V

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OH}	nIRQ Output high voltage	1 mA	0.8*LDO2P5V		LDO2P5V	V
V_{OL}	nIRQ Output low voltage	1 mA	0		0.3	V

4 Application Curves and Waveforms

TA = 25 °C, VIN_Supply = 12 V, VINBKx = 5 V, VOUT_HV = 5 V, VOUT_BK1=1.2 V, VOUT_BK2 =1.8 V, VOUT_BK3=3.3 V, FSW_LV = 500 KHz, FSW_LV = 1 MHz (unless otherwise noted)

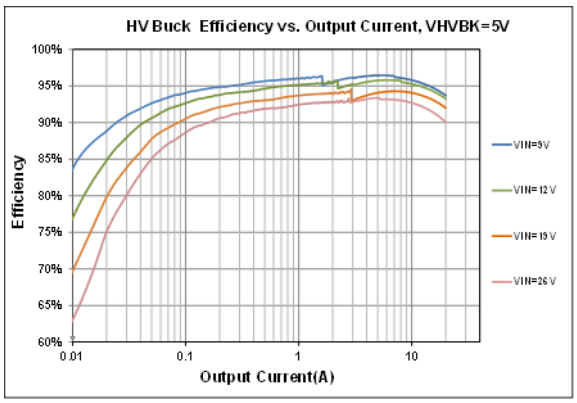


Figure 2: HV Buck Controller Efficiency

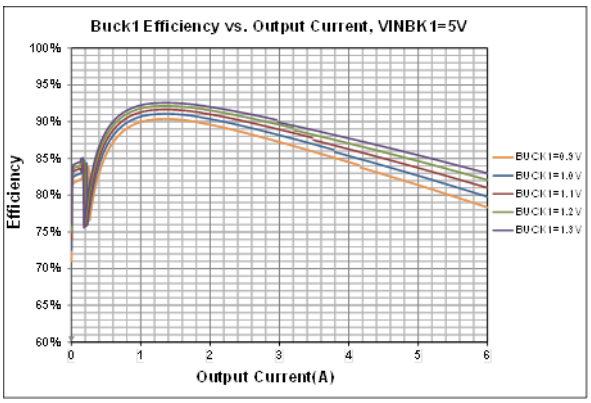


Figure 5: Buck1 Converter Efficiency

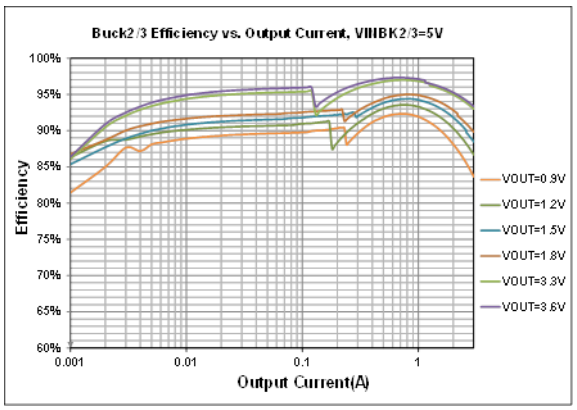


Figure 3: Buck2/3 Converter Efficiency

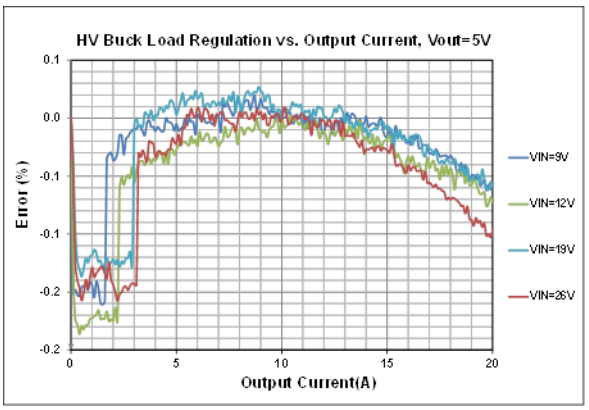


Figure 6: HV Buck Controller Load Regulation

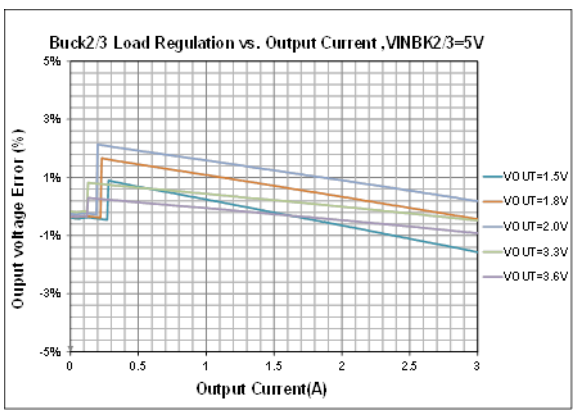


Figure 4: Buck1 Converter Load Regulation

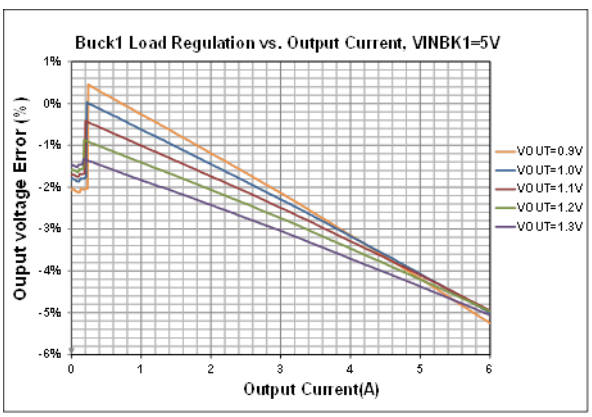


Figure 7: Buck2/3 Converter Load Regulation

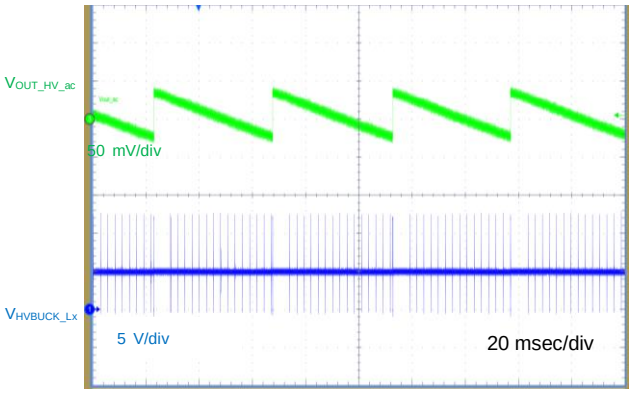


Figure 8: HVBuck Steady State Operation at No Load

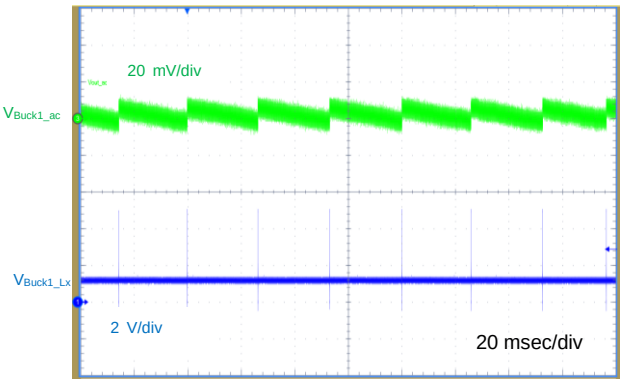


Figure 9: Buck1 Steady State Operation at No Load

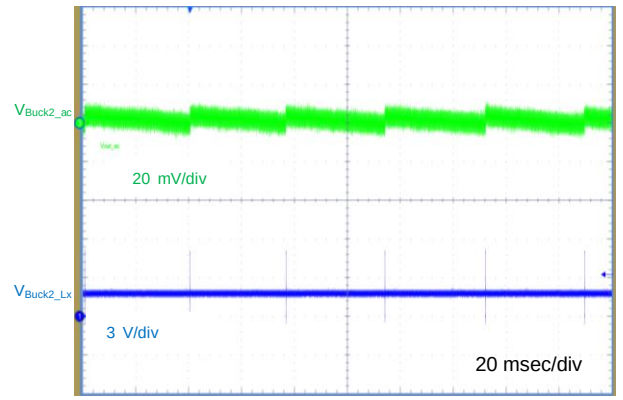


Figure 10: Buck2 Steady State Operation at No Load

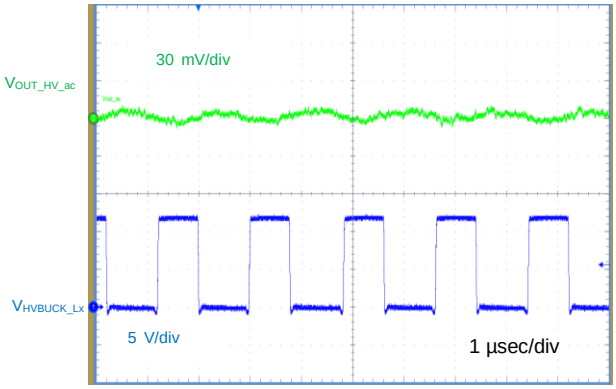


Figure 11: HVBuck Steady State Operation at 5 V, 20 A

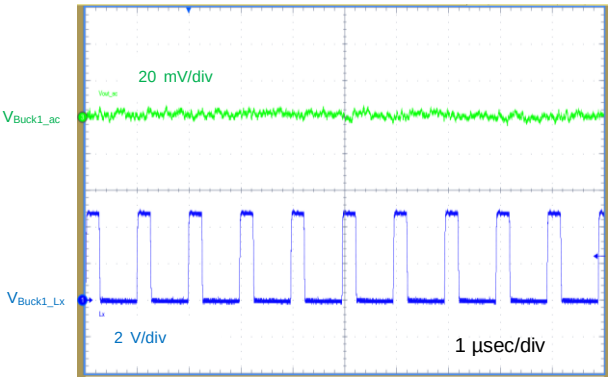


Figure 12: Buck1 Steady State Operation at 1.2 V, 5 A

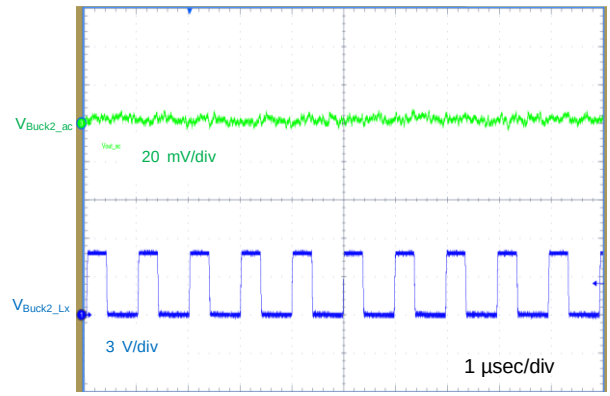


Figure 13: Buck2 Steady State Operation at 1.5 V, 2 A

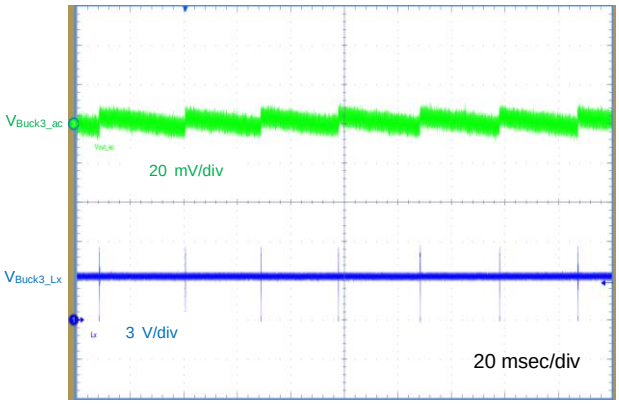


Figure 14: Buck3 Steady State Operation at No Load

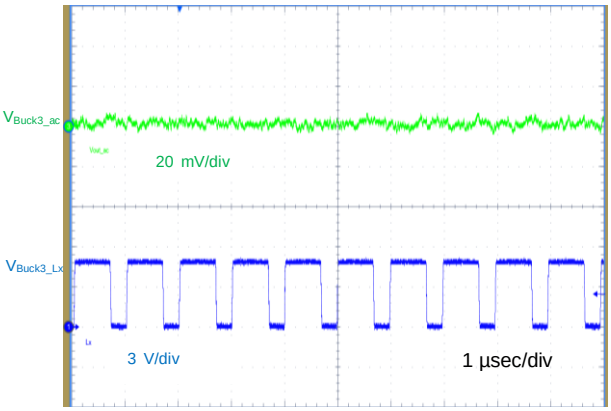


Figure 17: Buck3 Steady State Operation at 3.3 V, 2 A

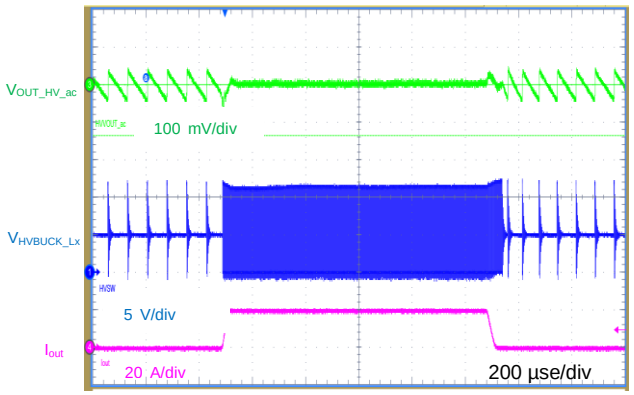


Figure 15: HVBUCK Load Transient when I_{OUT} = 1 mA to 20 A

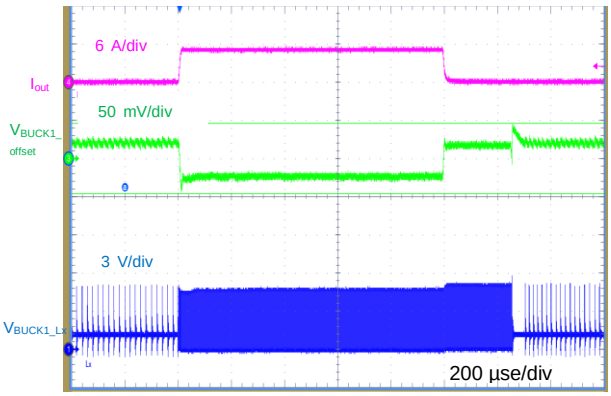


Figure 18: Buck1 Load Transient when I_{OUT} = 1 mA to 5 A

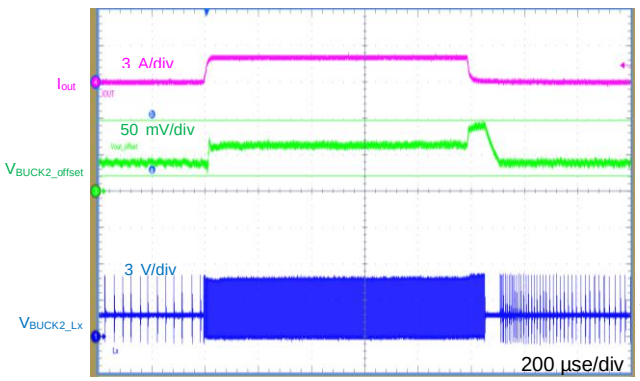


Figure 16: Buck2 Load Transient when I_{OUT} = 1 mA to 2 A

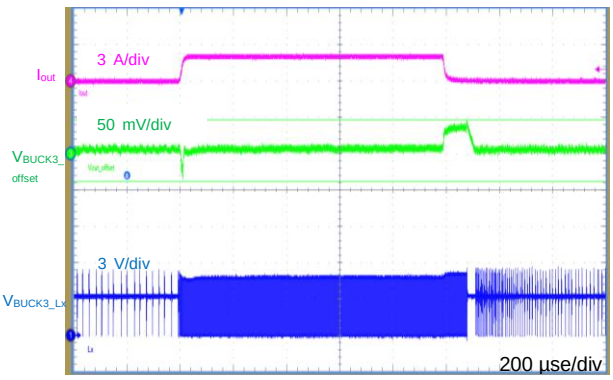


Figure 19: Buck3 Load Transient when I_{OUT} = 1 mA to 2 A

5 Functional Description

5.1 Operating Modes

5.1.1 NORMAL Mode - Default Power On Status

The default power up state is entered at start-up when VIN. Supply exceeds the POR threshold.

After start-up the SOC will either enable STANDBY mode, or configure the NORMAL operation mode via the I²C interface.

5.1.2 STANDBY Mode

STANDBY mode is entered when the STBY input pin is driven to 2.5 V.

In STANDBY mode the device enters a low power state.

The standby and I/O 5.0 V supplies are maintained by HVBUCK controller, HVLDO and LDO_Core.

The memory supplies from Buck 2, 3 are optionally maintained depending on OTP/I²C setting.

When the STBY pin is driven to 0 volts the system restarts NORMAL mode.

Table 18: Functional Block Mode of Operation

Block	Function	NORMAL Mode	STANDBY Mode
Buck 1	CORE	Enabled Voltage I²C Default 1.2 V	Off
Buck 2	MEMORY	Enabled Voltage I²C Default 1.8 V	I²C Default Off Voltage I²C Default 1.8 V
Buck 3	AUX	I²C Default Off Voltage I²C Default 3.3V	I²C Default Off Voltage I²C Default 3.3V
Serial Control	I²C	Enabled	Enabled
Enable Control	STBY PIN	Enabled	Enabled
Interrupt	nIRQ PIN	Enabled	Enabled
Reference		Enabled	Enabled
Trimmed OSC		Enabled	Enabled
Internal digital supply		Enabled	Enabled

5.1.3 Power Sequence

The start-up sequence for a single PV88080 is summarized in Table 19.

Table 19: PV88080 Start-Up Sequence

	Event	Action
1	VIN_Supply > 6.5 V	1. PV88080 POR, reset all register. 2. HVLDO generate 5 V supply.
2	HVLDO = 5.0 V	1. HVLDO = 5.0 V supplies bandgap reference voltage and bias current. 2. HVLDO = 5.0 V supply LDO_CORE to generate 2.5 V.
3	LDO_CORE = 2.5 V	LDO_CORE = 2.5 V supplies oscillator and entire digital IP
4	Digital circuitry is ready	1. Load OTP. 2. Enable / Disable block under I^2C control. 3. Digital circuitry turns on AVDD_HVBK pre-regulator and HV buck loop. 4. AVDD_HVBK pre-regulator POR triggered.
5	AVDD_HVBK pre-regulator POR triggered	Digital circuitry turns on HV buck driver -> generating 5 V supply
6	HV buck controller 5 V buck supply OK	Turn on the switch between VINBK1 and AVDD_HVBK -> Switch HV buck driver supply to controller 5 V supply
7	Digital turn on analog IP	After all LV buck V_{IN} UVLO, digital turns on the LV bucks sequentially determined by OTP or user application cases

The start-up sequence for multiple PV88080s are summarized in Table 20.

Table 20: Start-Up sequence for multiple PV88080s

	Event	Action
1	VIN_Supply > 6.5 V	1. All PV88080 POR. Reset all registers in all PV88080. 2. HVLDO in each PV88080 generate 5 V supply.
2	HVLDO = 5.0 V	1. HVLDO = 5.0 V supplies bandgap reference voltage and bias current. 2. HVLDO = 5.0 V supply LDO_CORE to generate 2.5 V.
3	LDO_CORE = 2.5 V	LDO_CORE = 2.5 V supplies oscillator and entire digital IP
4	Digital circuitry is ready	1. Load OTP individually for all PV88080. 2. Enable / Disable block under I^2C control.
5	PV88080-1 ONLY	1. Digital circuitry turns on AVDD_HVBK pre-regulator and HV buck loop. 2. AVDD_HVBK pre-regulator POR triggered. 3. Digital circuitry turns on HV buck driver -> generating 5 V supply. 4. HV buck controller 5 V buck supply OK -> Turn on the switch between VINBK1 and AVDD_HVBK -> Switch HV buck driver supply to controller 5 V supply.
6	Digital turn on analog IP in ALL PV88080	Digital circuitry turns on the LV bucks sequentially determined by OTP or user application cases in ALL PV88080

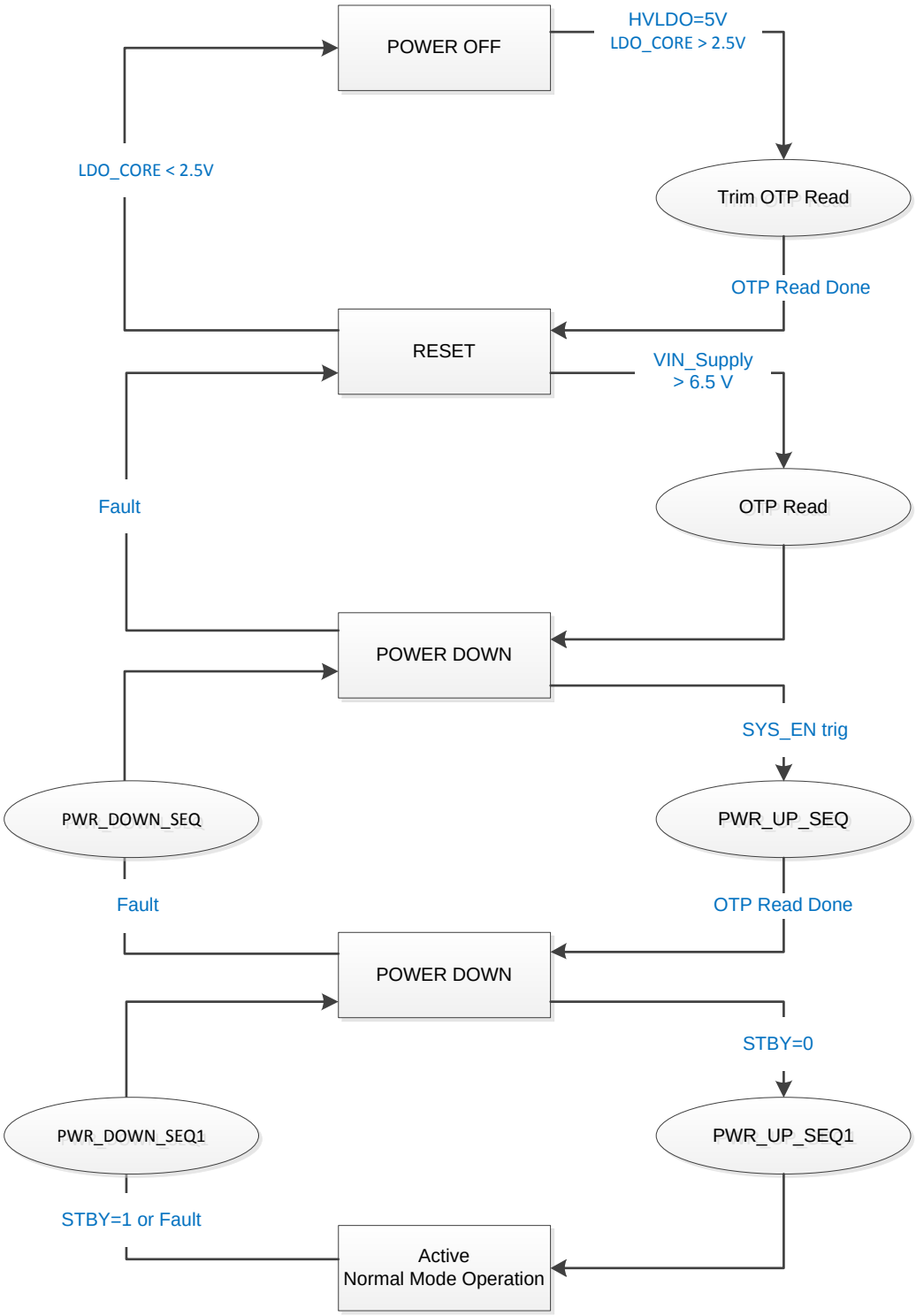


Figure 20: PV88080 Boot Sequence

5.2 Multiple PV88080 Power On/Off Behavior

For multiple PV88080 application, PV88080-1 acts as the master and the others act as the slaves.

The first PV88080 (PV88080-1) HV buck V_{OUT} range is 4.75 V to 5.25 V and supplies all the LV buck converters in all PV88080. The HVBUCK V_{OUT} from other PV88080 can be programmed to 0.9 V to 5.25 V. The PV88080-1 could configure one GPIO pin as the sequence control GPIO to connect the other PV88080's STDBY pin. Figure 20 shows the example of three PV88080 working together.

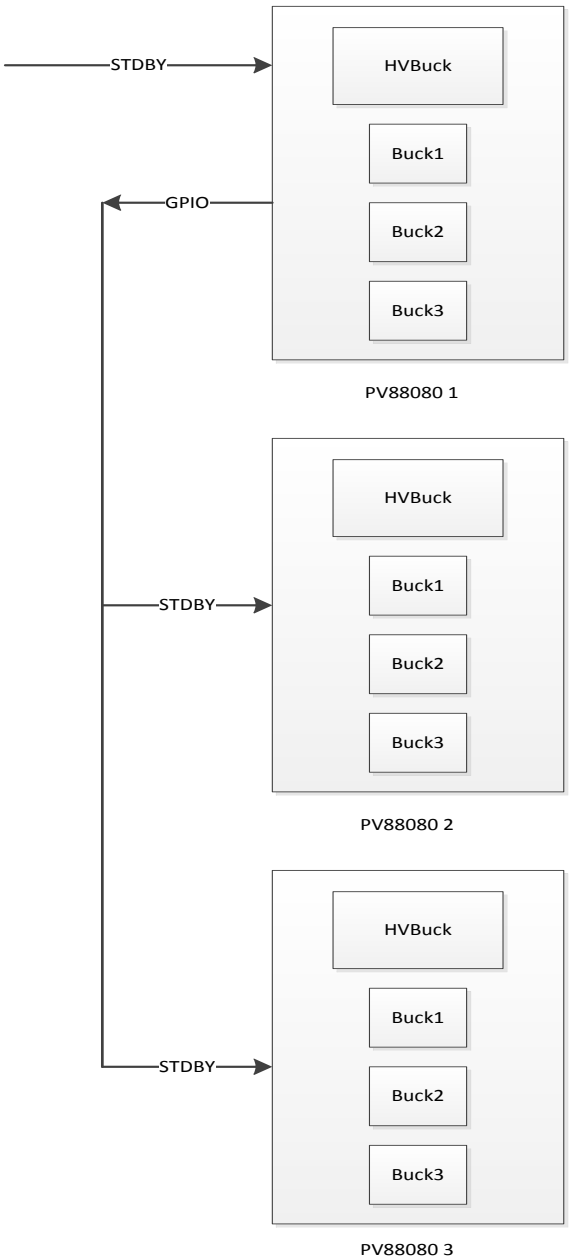


Figure 20: Proposal for mPV88080 Connection

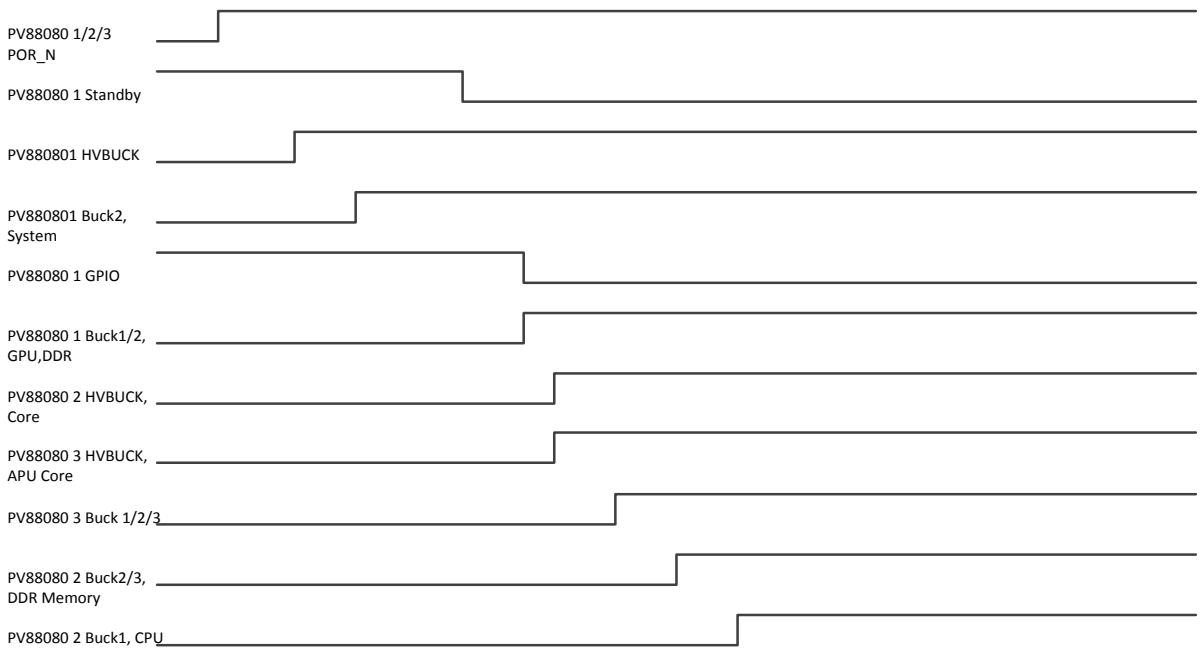


Figure 21: Multiple PV88080 Connection Power on Sequence

5.3 Multiple PV88080 Power On/Off Behavior

If a fault condition occurs when multiple PV88080 are connected, the behavior differs according to where the fault condition is. If a fault condition occurs in:

PV88080-1 (master), all PV88080 are powered down and re-booted,

other PV88080 (slaves), the power down and re-boot only happens in the PV88080 with the fault, the un-affected PV88080s stay powered up.

In the second example, however, the CPU or system can decide to power down and re-boot all PV88080s by asserting the PV88080-1 (master) standby pin.

5.4 HV Buck Controller Protection Behavior

5.4.1 Over-Voltage (OV) Protection

HVBUCK controller over-voltage protection is performed by comparing the VFB with internal DAC output.

Once the OV signal is triggered, the digital core sequentially soft stops all the rails and then the HVBUCK controller is also turned off.

After a short period of time (around ~10 ms), HVBUCK controller is automatically re-started and turns on all the rails. The OV detection / protection function is disabled during DVC stage.

For the OV register bit and threshold voltage, see Section 6.

5.4.2 Under-Voltage (UV) Protection

HVBUCK controller under-voltage protection is performed by comparing the VFB with internal DAC output.

Once the UV signal is triggered, the digital core sequentially soft stops all the rails and then the HVBUCK controller is also turned off.

After a short period of time (around ~10 ms), HVBUCK controller is automatically re-started and turns on all the rails.

The UV detection / protection function is disabled during DVC stage.

The UV filter time also applies to output Short Circuit Protection (SCP).

For the UV register bit and threshold voltage, see Section 6.

5.4.3 Positive Over-Current (P-OC) Protection

The positive over-current protection is achieved by detecting the voltage across the low side external NMOS Vsd (=-IL*RDS_on) and compares this voltage to a pre-defined threshold. The inductor valley current is limited to the positive over-current threshold.

The positive over-current enable and threshold are configurable.

For the P-OC register bit and threshold voltage, see Section 6.

5.4.4 Negative Over-Current (N-OC) Protection

The negative over-current protection is achieved by detecting the voltage across the low side external NMOS Vsd (=-IL*RDS_on) and compares this voltage to a pre-defined threshold. The inductor valley current is limited to the negative over-current threshold.

When the negative over-current is triggered, the buck controller IP turns off the low side external NMOS and turns on the high side external NMOS with normal on-time. This behavior is designed to avoid the inductor current flowing through the high side body diode.

The negative over-current enable and threshold are configurable.

For the N-OC register bit and threshold voltage, see Section 6.

5.4.5 Output Short Circuit Protection (SCP)

In the event of an output short, the PV88080 automatically enters SCP operation. There are several scenarios that can cause the device to enter SCP operation, which are shown in Figure 22 to Figure 27.

During normal start up, the output of the DAC ramps from 0V to 0.5V. Once the DAC output reaches 0.5 V, it stays at 0.5 V for 1 ms in order to check the SCP condition.

If VFB < 0.3 V => output short is valid => SCP=1, set DAC output to 0 V. Digital core to shut down and then power up the PV88080.

If VFB > 0.3 V, DAC continue to ramp up to target V_{OUT}. Once the target V_{OUT} is reached, PowerGood signal is enabled and the protection threshold is changed from 0.3 V to UV threshold.

For the SCP, DAC and UV threshold related register bit, see Section 6.

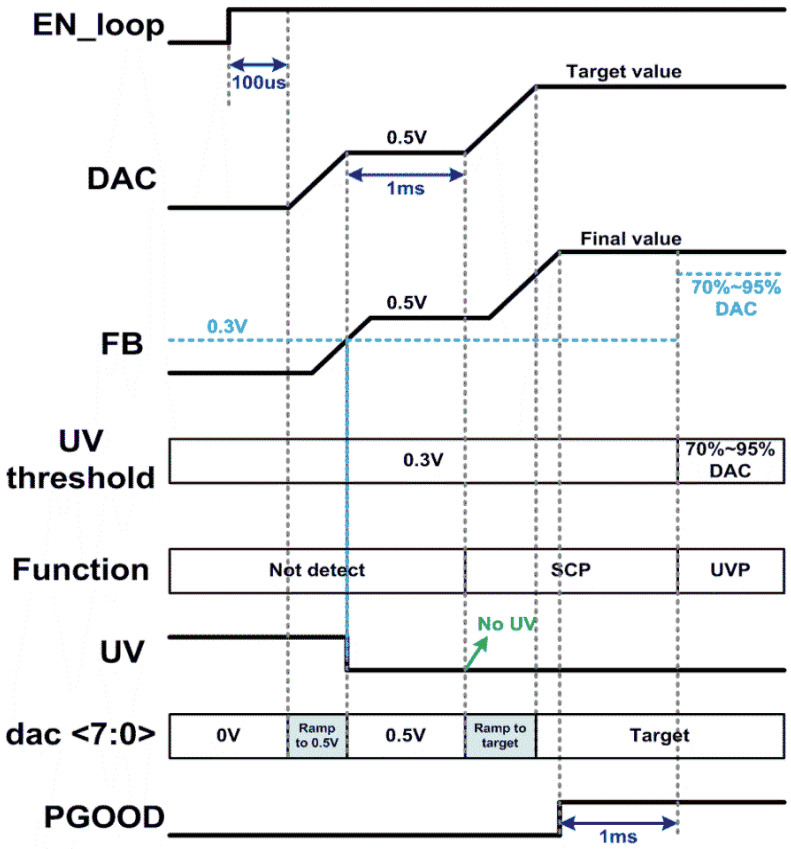


Figure 22: SCP - Normal Power On, no SCP/UVP is Triggered

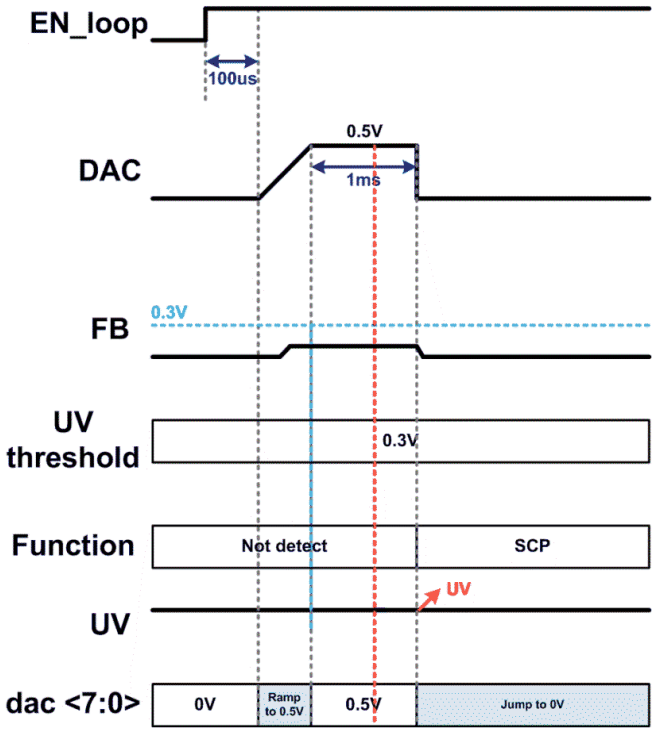


Figure 23: SCP - Short Circuit Occurs at the Beginning

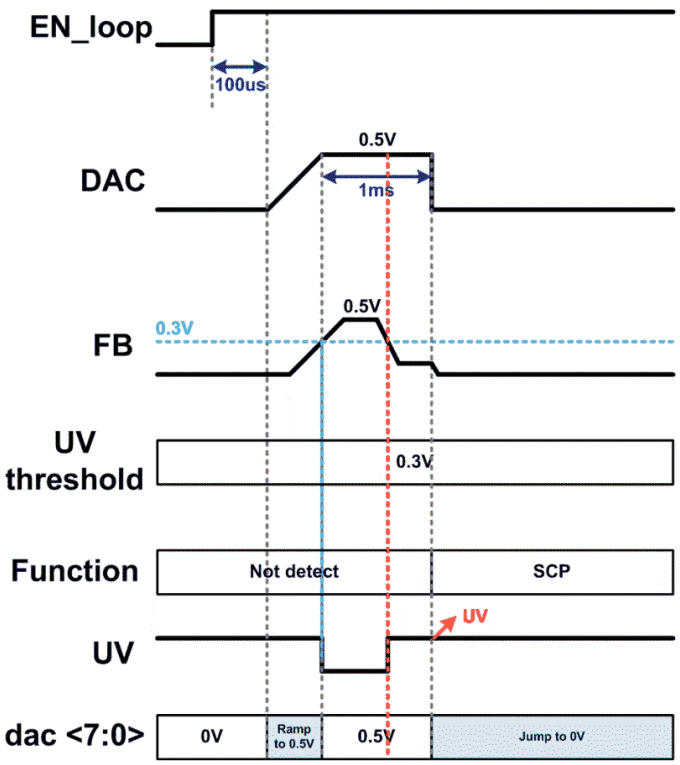


Figure 24: SCP - Short Circuit Occurs when V_DAC=0.5 V

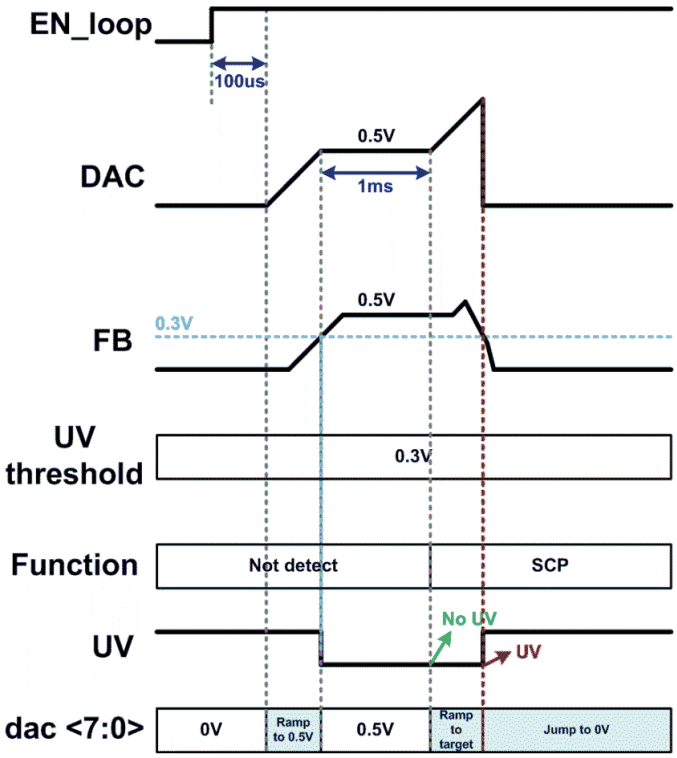


Figure 25: SCP - Short Circuit Occurs when V_DAC is Ramping Up

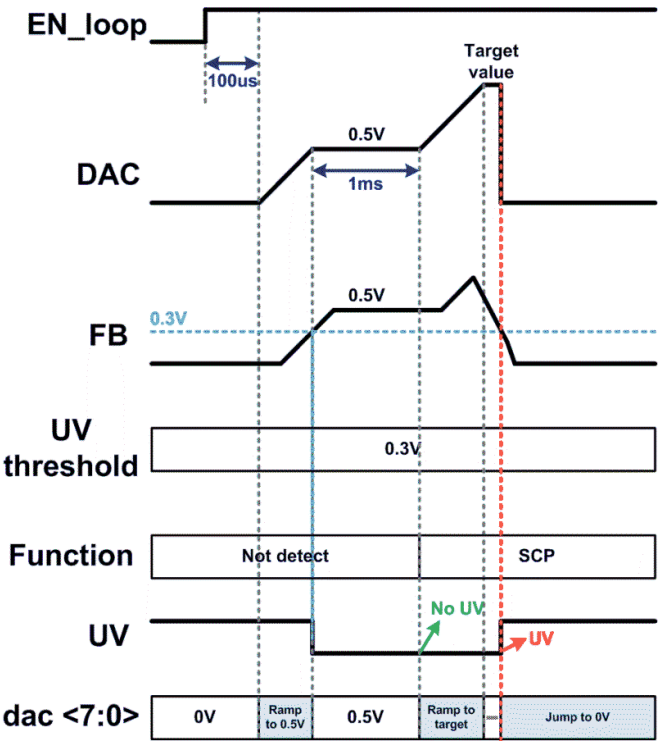


Figure 26: SCP - Short Circuit Occurs when V_DAC Ramps Up and Reaches the Target

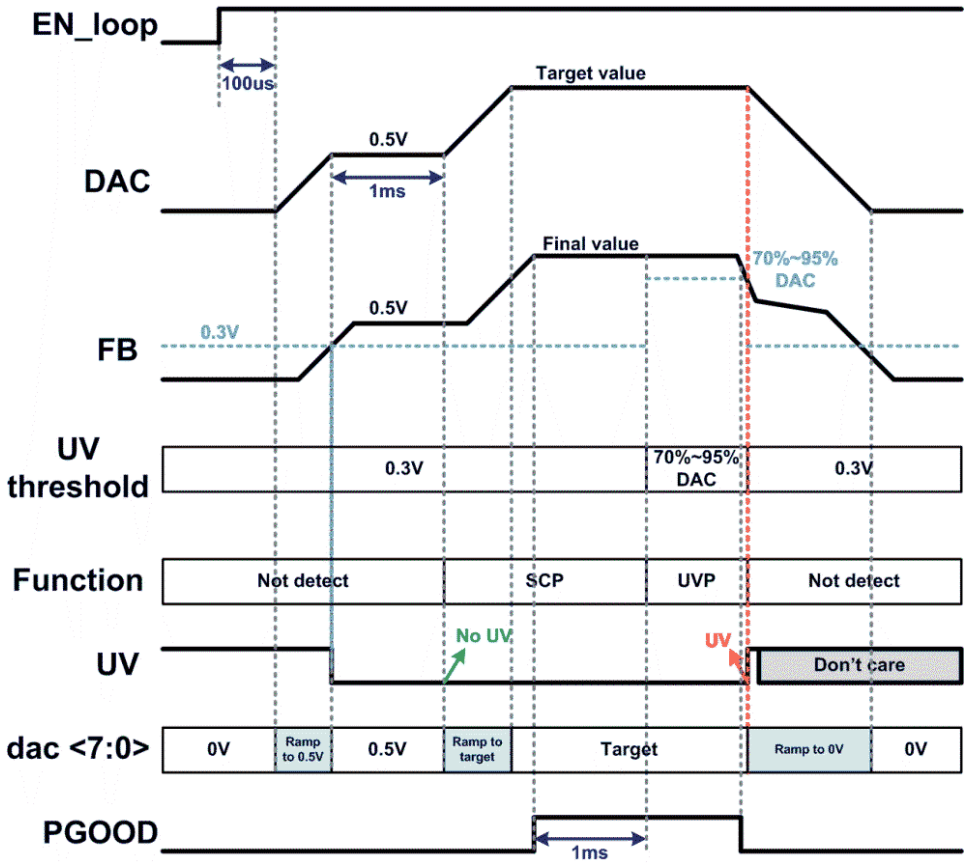


Figure 27: SCP - Under Voltage Protection (UVP)

5.5 Buck Converter Output Voltage Selection Function

This function allows the output voltage of the Buck converter to be changed through the digital pins GPIO1, GPIO2, or nIRQ without changing the OTP setting. Additionally the digital register GPIO_VBUCK_CONF can be used to determine which output voltage is applied to which GPIO pin.

For converter Buck2, there is another feature for voltage selection throughout the digital pins, see Table 21.

Table 21: Output Voltage Selection Function Summary of Buck2 Converter

Output Voltage Selection		
Buck2 Output Voltage	GPIO1 Pull Low	GPIO1 Pull High
GPIO2 Pull Low	VBuck2	VBuck2_ALT
GPIO2 Pull High	VBuck1_ALT	VBuck3_ALT

For the related register bits see Section 6.

5.6 MUTE Function

This feature provides detection of a low system supply voltage.. The PV88080 sends out a flag signal with programmable polarity through the digital pins GPIO1, GPIO2, or nIRQ according to the OTP settings. This flag signal can be used to control any audio related components as a shutdown signal to prevent any unwanted audio "popping" noise from occurring in the system.

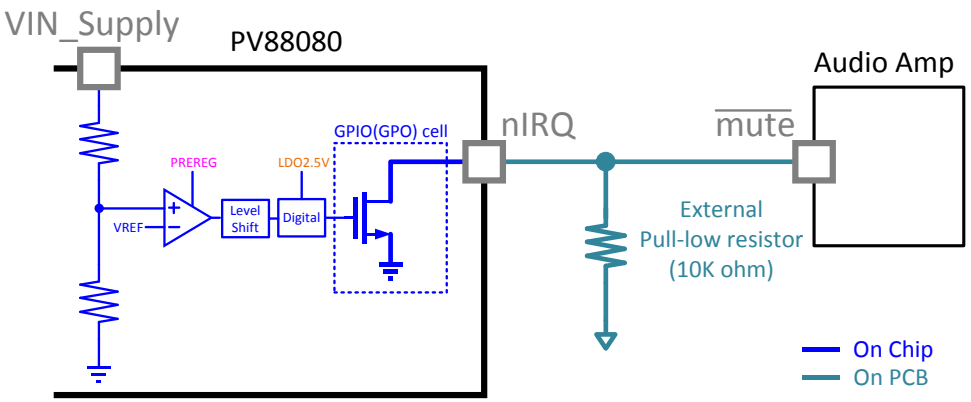


Figure 28: Typical Application of Mute Function

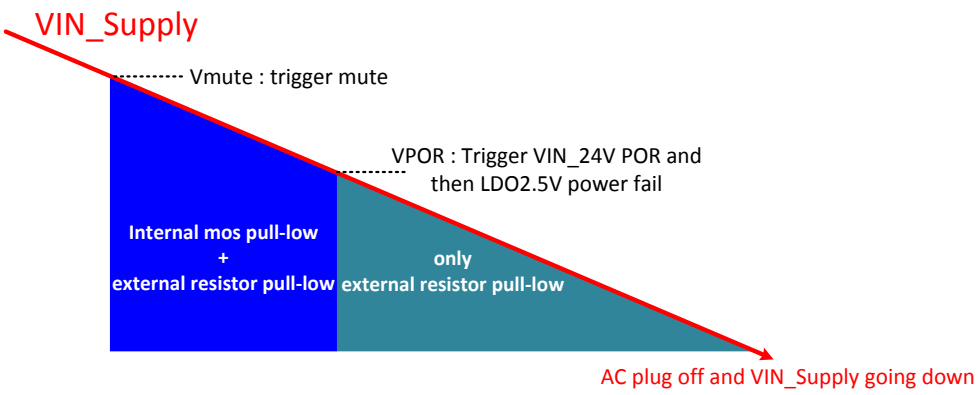


Figure 29: Mute Function Operation Level

5.6.1 MUTE Levels

Table 22: Electrical Characteristics V_{DD} = 4.75 to 5.25 V

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{MUTE}	MUTE detection level at VIN_Supply pin	mutelvl_sel = 00 mutelvl_sel = 01 mutelvl_sel = 10 mutelvl_sel = 11		8.5 8 7.5 7		V

5.6.2 Sequence of Power and Signals

For the typical application VIN_Supply and rise time, the PMIC keeps the MUTE flag for approximately 20 msec from digital reset/OT load start. This is to create a deglitch time period for the slow power ramp up. Then the MUTE level detection is enabled and the MUTE flag is set accordingly.

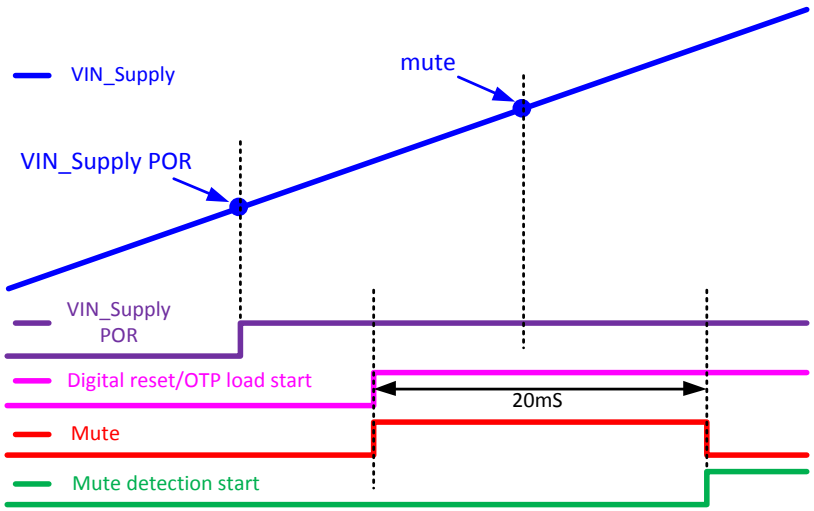


Figure 30: Sequence of Power and Signal - Condition I

Figure 32 depicts a condition where the input supply is not capable of reaching the desired voltage level and is held below the OTP programmed Mute level. In this situation, the Mute signal will be continuously asserted.

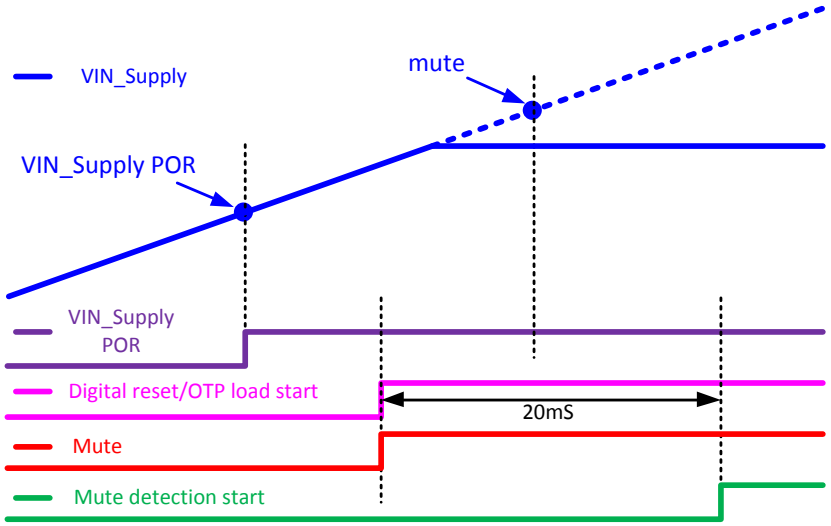


Figure 31: Sequence of Power and Signal - Condition II

The MUTE function has 200 us one-way deglitch time. Once the VIN_SUPPLY drops below MUTE level, the PMIC sends out the MUTE flag immediately. Only when VIN_SUPPLY returns higher than the MUTE level continuously over the 200 us deglitch time, will the PMIC release the MUTE flag signal.

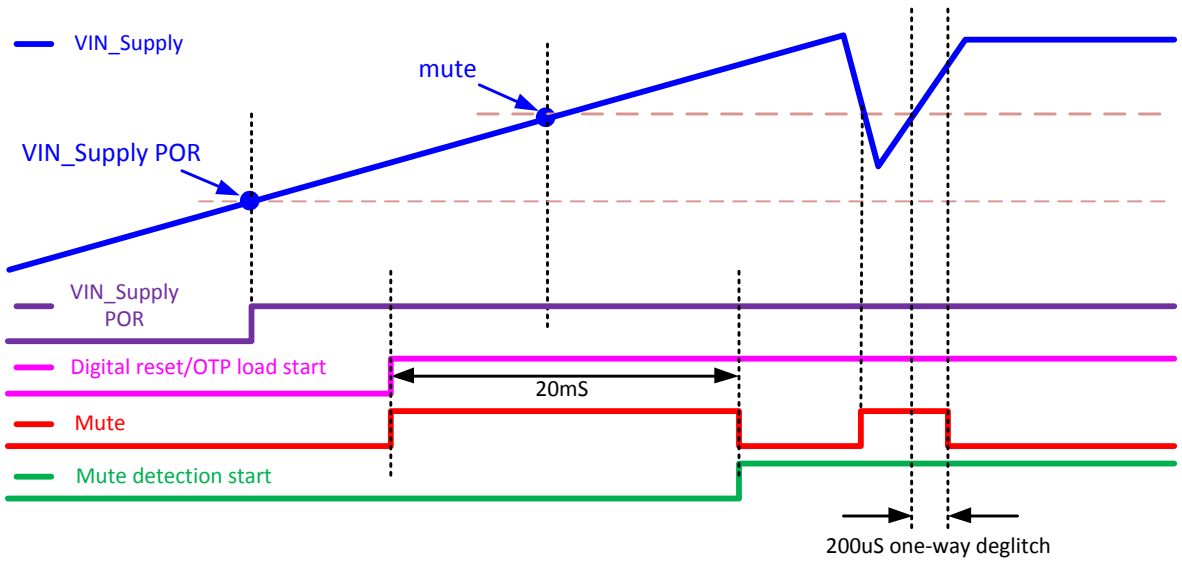


Figure 32: Sequence of Power and Signal - Condition III

The Mute function can also be used for power fail detection if the input supply voltage drops to levels programmed in Table 22.

5.7 Thermal Sensing and Power Fail Function

The internal comparator shown in Figure 33 and Figure 34 can be used to support multiple functions. Among these are power fail and thermal sensing. Figure 33 and Figure 34 illustrate how to connect GPIO2 pin to external passives to implement these two functions.

Figure 33 shows a typical NTC interface connected to the PV88080. This function provides thermal sensing for the system with an external NTC thermistor mounted on the system PCB where thermal conditions need to be sensed. With proper OTP setting, the PV88080 PMIC can source a 10 uA current through the GPIO2 pin. The voltage generated by the 10uA current source multiplied by the resistance (external resistor + external thermistor) at the pin GPIO2 is compared to the internal 1.2 V voltage reference. If GPIO2 voltage is smaller than the internal 1.2 V VREF, the PMIC will assert the nIRQ pin to the SOC system as an alert signal. The GPIO2 pin can also support power fail detection when configured as shown in Figure 34.

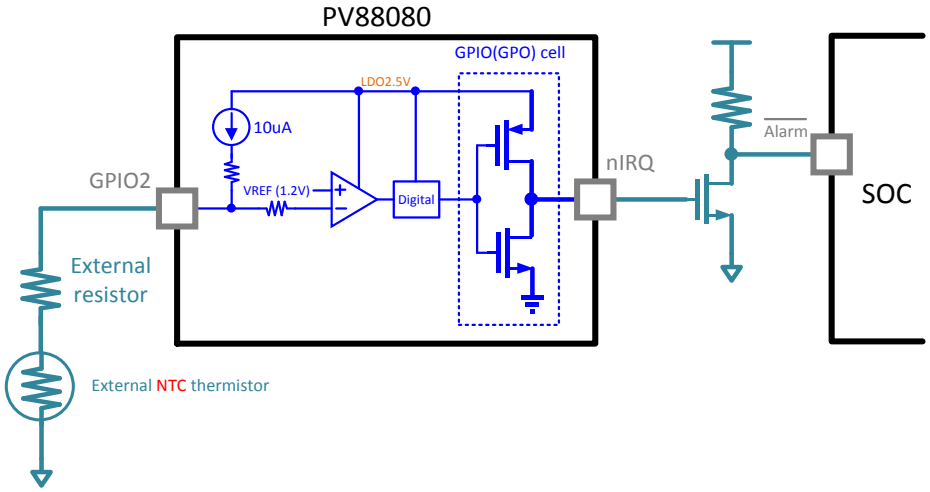


Figure 33: Typical application schematic of Thermal Sense Function

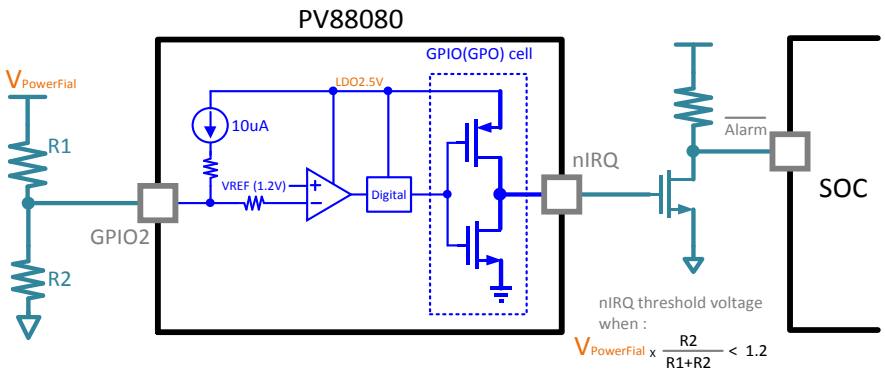


Figure 34: Typical application schematic of Power fail function

5.7.1 Function Description with Related Signals

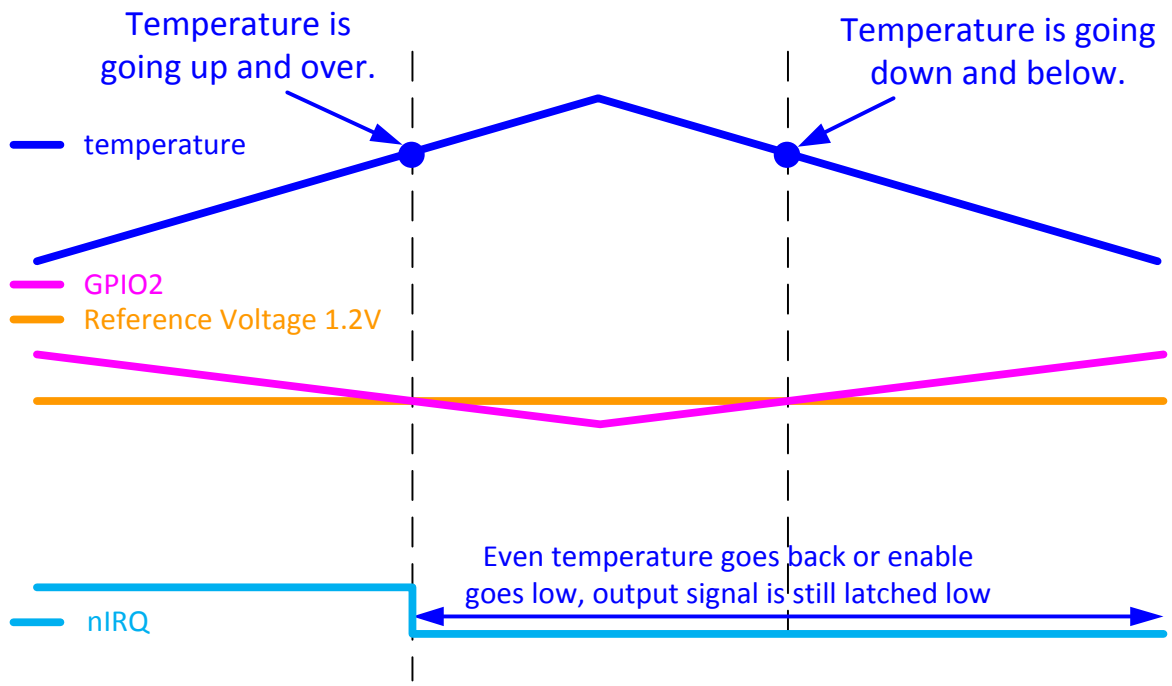


Figure 35: Thermal Sense Function Waveform

Table 23: Electrical Characteristics V_{DD} = 4.75 to 5.25 V

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{SRC}	Source current for the external thermal sensing function		9.7	10	10.3	uA
V_{OT_THR}	Over temperature threshold		1.164	1.2	1.236	V

5.8 2-Wire Interface

The 2-wire interface provides access to control and status registers. The interface supports operations compatible to standard, fast, fast-plus and high-speed mode of the I²C bus specification.

Communication on the 2-wire bus always takes place between two devices, one acting as the master and the other as the slave. The PV88080 will only operate as a slave. The 2-wire interface has direct access to two pages of the PV88080 register map (up to 256 addresses).

SCL carries the 2-wire clock and SDA carries the bi-directional data. The 2-wire interface is open-drain supporting multiple devices on a single line. The bus lines have to be pulled high by external pull-up resistors (2 kΩ to 20 kΩ). The attached devices only drive the bus lines low by connecting them to ground. As a result, two devices cannot conflict if they drive the bus simultaneously. In standard/fast mode the highest frequency of the bus is 400 kHz. The exact frequency can be determined by the application and it does not have any relation to the PV88080 internal clock signals. PV88080 follows the host clock speed within the described limitations and does not initiate any clock arbitration or slow down.

5.8.1 Details of the 2-Wire Protocol

All data is transmitted across the 2-wire bus in groups of 8 bits. To send a bit the SDA line is driven at the intended state while the SCL is low. Once the SDA has settled, the SCL line is brought high and then low. This pulse on SCL clocks the SDA bit into the receivers shift register.

A two-byte serial protocol is used containing one byte for address and one byte data. Data and address transfer is transmitted MSB first for both read and write operations. All transmission begins with the START condition from the master during which the bus is in IDLE state (the bus is free). It is initiated by a high-to-low transition on the SDA line while the SCL is in the high state. A STOP condition is indicated by a low-to-high transition on the SDA line while the SCL is in the high state. The START and STOP conditions are illustrated in Figure 36.

Figure 36: Timing of the START and STOP Conditions

The 2-wire bus will be monitored by PV88080 for a valid slave address whenever the interface is enabled. It responds immediately when it receives its own slave address. These acknowledge is done by pulling the SDA line low during the following clock cycle (white blocks marked with 'A' in the following figures).

The protocol for a register write from master to slave consists of a START condition, a slave address, a read/write-bit, 8-bit address, 8-bit data, and a STOP condition. All bytes are responded by PV88080 with an ACK. A register write operation is illustrated in Figure 37.

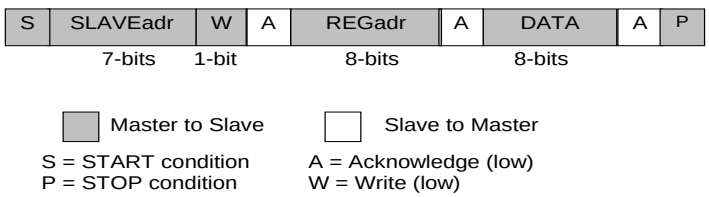


Figure 37: Byte Write Operation

When the host reads data from a register it first has to write access PV88080 with the target register address and then read access PV88080 with a repeated START or alternatively a second START condition. After receiving the data the host sends NACK and terminates the transmission with a STOP condition. This is illustrated in Figure 38.

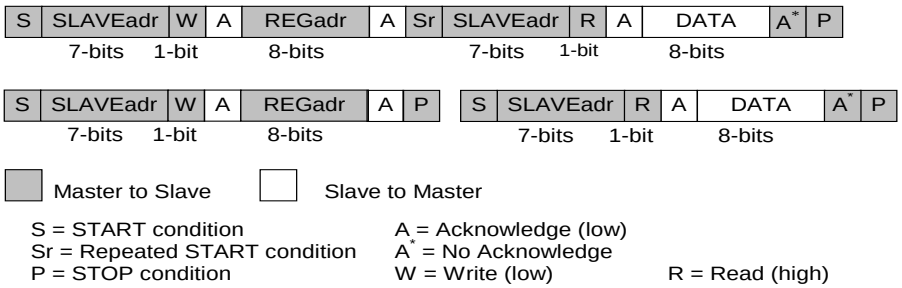


Figure 38: Examples of Byte Read Operations

Consecutive (page) read out mode is initiated from the master by sending an ACK instead of NACK after receiving a byte. This is illustrated in Figure 39. The 2-wire control block then increments the address pointer to the next register address and sends the data to the master. This enables an unlimited read of data bytes until the master sends a NACK directly after receiving the data, followed by a subsequent STOP condition. If a non-existent 2-wire address is read out then the PV88080 will return code zero.

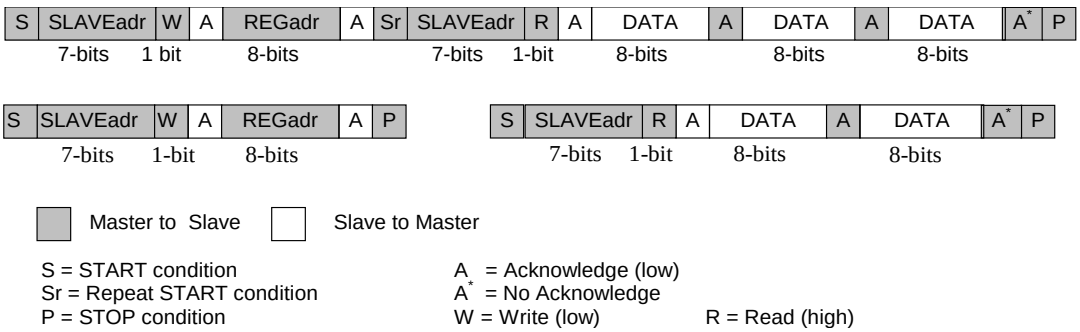


Figure 39: 2-Wire Page Read

The slave address after the Repeated START condition must be the same as the previous slave address.

Consecutive (page) write mode is supported if the master sends several data bytes following a slave register address. The 2-wire control block then increments the address pointer to the next 2-wire address, stores the received data and sends an ACK until the master sends a STOP condition. The page write mode is illustrated in Figure 40.

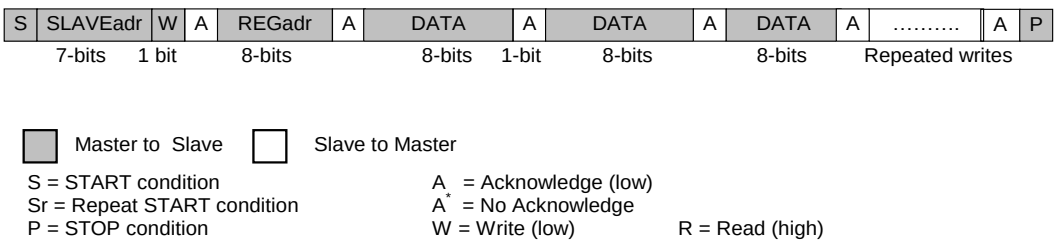


Figure 40: 2-Wire Page Write

Using the control WRITE_MODE a repeated write mode can be enabled. In this mode, the master can execute back-to-back write operations to non-consecutive addresses. This is achieved by transmitting register address and data pairs. The data is stored in the address specified by preceding byte. The repeated write mode is illustrated in Figure 41.

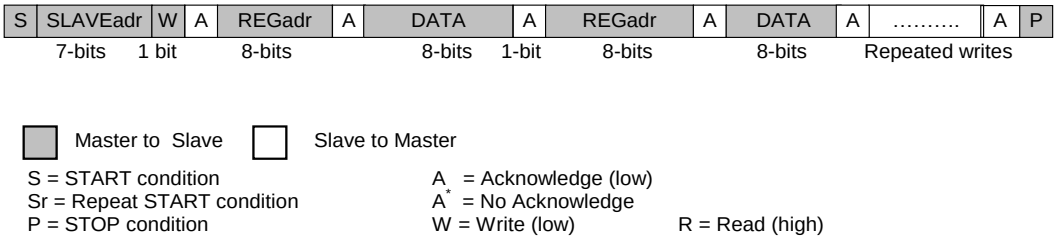


Figure 41: 2-Wire Repeated Write

If a new START or STOP condition occurs within a message, the bus returns to IDLE-mode.

6 Register Map

Register Status / Config	Addr	7	6	5	4	3	2	1	0
STATUS_A	0x0001	Reserved	Reserved	Reserved	Reserved	EXT_OT	SEQUENCING	OVER_TMP	VDD_FLT
STATUS_B	0x0002	Reserved	Reserved	BUCK3_VOUT_SCP	BUCK2_VOUT_SCP	BUCK1_VOUT_SCP	HV_BUCK_SCP	HV_BUCK_UV	HV_BUCK_OV
STATUS_C	0x0003	Reserved	Reserved	BUCK3_VOUT_SCP_DROP_TIMEOUT	BUCK2_VOUT_SCP_DROP_TIMEOUT	BUCK1_VOUT_SCP_DROP_TIMEOUT	Reserved	GPIO_FLAG1	GPIO_FLAG0
EVENT_A	0x0004	Reserved	Reserved	Reserved	Reserved	E_EXT_OT	E_SEQ_RDY	E_OVER_TMP	E_VDD_FLT
EVENT_B	0x0005	Reserved	Reserved	E_BUCK3_VOUT_SCP_FAIL	E_BUCK2_VOUT_SCP_FAIL	E_BUCK1_VOUT_SCP_FAIL	E_HV_BUCK_SCP_FAIL	E_HV_BUCK_UV_FAIL	E_HV_BUCK_OV_FAIL
EVENT_C	0x0006	Reserved	Reserved	E_BUCK3_VOUT_SCP_DROP_TIMEOUT_FAIL	E_BUCK2_VOUT_SCP_DROP_TIMEOUT_FAIL	E_BUCK1_VOUT_SCP_DROP_TIMEOUT_FAIL	Reserved	E_GPIO_FLAG1	E_GPIO_FLAG0
FAULT_LOG	0x0007	Reserved	Reserved	EXTERNAL_FAULT	HVBK_OV_FAULT	HVBK_UV_FAULT	HVBK_SCP_FAULT	OVER_TEMP	VDD_FAULT
FAULT_LOG_1	0x0008	Reserved	Reserved	BUCK3_SCP_DROP_TIMEOUT_FAULT	BUCK2_SCP_DROP_TIMEOUT_FAULT	BUCK1_SCP_DROP_TIMEOUT_FAULT	BUCK3_SCP_FAULT	BUCK2_SCP_FAULT	BUCK1_SCP_FAULT
IRQ_MASK_A	0x0009	Reserved	Reserved	Reserved	Reserved	M_EXT_OT	M_SEQ_RDY	M_OVER_TMP	M_VDD_FLT
IRQ_MASK_B	0x000A	Reserved	Reserved	M_BUCK3_VOUT_SCP_FAIL	M_BUCK2_VOUT_SCP_FAIL	M_BUCK1_VOUT_SCP_FAIL	M_HV_BUCK_SCP_FAIL	M_HV_BUCK_UV_FAIL	M_HV_BUCK_OV_FAIL

Register Status / Config	Addr	7	6	5	4	3	2	1	0
IRQ_MASK_C	0x000B	Reserved	Reserved	M_BUCK3_VOUT_SCP_DROP_TIMEOUT_FAIL	M_BUCK2_VOUT_SCP_DROP_TIMEOUT_FAIL	M_BUCK1_VOUT_SCP_DROP_TIMEOUT_FAIL	Reserved	M_GPIO_FLAG1	M_GPIO_FLAG0
CONTROL_A	0x000C	Reserved	Reserved 1	Reserved 1	Reserved	Reserved 0	Reserved 0	PWR_EN	SYS_EN
CONTROL_B	0x000D	Reserved 0	Reserved 0	WRITE_MODE	Reserved 0	Reserved	Reserved 1	Reserved	Reserved
CONTROL_C	0x000E	Reserved	Reserved	LDO_EN_PULLDOWN	HVLDO_EN_PULLDOWN	MUTELVL_SEL		EN_MUTE	Reserved 0
I2C_BASE_ADDR	0x0010	IF_BASE_ADDR			Reserved	Reserved	Reserved	Reserved	Reserved
GPIO									
Register	Addr	7	6	5	4	3	2	1	0
GPIO_DATA_IN	0x0017	Reserved	Reserved	Reserved	Reserved	Reserved	GPIO_NIRQ_IN	GPIO_IN	
GPIO_DATA_OUT	0x0018	Reserved	Reserved	Reserved	Reserved	GPO_SDA_OUT	GPIO_NIRQ_OUT	GPIO_OUT	
GPIO_0_CONF	0x0019	GPIO_0_FUNC_SEL			GPIO_0_ACTIVE_LOW	GPIO_0_PD	GPIO_0_PU	GPIO_0_PP	GPIO_0_OUT_EN
GPIO_1_CONF	0x001A	GPIO_1_FUNC_SEL			GPIO_1_ACTIVE_LOW	GPIO_1_PD	GPIO_1_PU	GPIO_1_PP	GPIO_1_OUT_EN
GPIO_NIRQ_CONF	0x001B	GPIO_NIRQ_FUNC_SEL			GPIO_NIRQ_ACTIVE_LOW	GPIO_NIRQ_PD	GPIO_NIRQ_PU	GPIO_NIRQ_PP	GPIO_NIRQ_OUT_EN

Register Status / Config	Addr	7	6	5	4	3	2	1	0
GPIO_VBUCK_CONF	0x001C	VBUCK2_USE_2GPIO_SEL	GPO_SDA_ACTIVE_LOW	VBUCK3_GPIO_SEL		VBUCK2_GPIO_SEL		VBUCK1_GPIO_SEL	
GPIO_UP_SEQ_CONF	0x001D	GPIO_1_UP_STEP				GPIO_0_UP_STEP			
GPIO_DN_SEQ_CONF	0x001E	GPIO_1_DN_STEP				GPIO_0_DN_STEP			
GPO_SDA_SEQ_CONF	0x001F	GPO_SDA_DN_STEP				GPO_SDA_UP_STEP			
GPIO_NIRQ_SEQ_CONF	0x0020	GPIO_NIRQ_DN_STEP				GPIO_NIRQ_UP_STEP			
Sequencer									
Register	Addr	7	6	5	4	3	2	1	0
ID_0	0x0021	Reserved	Reserved	Reserved	Reserved	WAIT_ID_ALWAYS	Reserved 0	Reserved 0	Reserved 1
HV_BUCK_STEP	0x0022	HV_BUCK_STDBY_STEP				HV_BUCK_STEP			
BUCK_1_2_STEP	0x0024	BUCK2_STEP				BUCK1_STEP			
BUCK_3_STEP	0x0025	Reserved	Reserved	Reserved	Reserved	BUCK3_STEP			
SEQ_STATUS	0x0026	SEQ_POINTER				WAIT_STEP			

Register Status / Config	Addr	7	6	5	4	3	2	1	0
SEQ_A	0x0027	POWER_END				SYSTEM_END			
SEQ_B	0x0028	Reserved 0	Reserved 1	Reserved 0	Reserved 0	MAX_COUNT			
SEQ_TIMER	0x0029	SEQ_DUMMY				SEQ_TIME			
Supplies									
Register	Addr	7	6	5	4	3	2	1	0
BUCK1_CONF0	0x002A	BUCK1_EN	VBUCK1						
BUCK1_CONF0_ALT	0x002B	Reserved	VBUCK1_ALT						
BUCK1_CONF1	0x002C	BUCK1_PD_DIS	Reserved 0	Reserved 1	Reserved	BUCK1_SYNC_ILIM		BUCK1_MODE	
BUCK2_CONF0	0x002D	BUCK2_EN	VBUCK2						
BrUCK2_CONF0_ALT	0x002E	Reserved	VBUCK2_ALT						
BUCK2_CONF1	0x002F	BUCK2_PD_DIS	Reserved 0	Reserved 1	Reserved	BUCK2_SYNC_ILIM		BUCK2_MODE	
BUCK3_CONF0	0x0030	BUCK3_EN	VBUCK3						

Register Status / Config	Addr	7	6	5	4	3	2	1	0
BUCK3_CONF0_ALT	0x0031	Reserved	VBUCK3_ALT						
BUCK3_CONF1	0x0032	BUCK3_PD_DIS	Reserved 0	Reserved 1	Reserved	BUCK3_SYNC_ILIM		BUCK3_MODE	
HVBUCK_CONF1	0x0033	VHVBUCK							
HVBUCK_CONF2	0x0034	Reserved 1	TON_CTRIM			VHVBUCK_SLEW_RATE			HVBUCK_EN
HVBUCK_CONF3	0x0035	Reserved 1	OV_TH		UV_TH			ITON_SCALE	
HVBUCK_CONF4	0x0036	Reserved	NEG_OC_TH			Reserved	POS_OC_TH		
HVBUCK_VSTDBY	0x0037	Reserved	Reserved	Reserved	Reserved	Reserved	VHVBUCK_STDBY		
HVBUCK_STATUS1	0x0038	Reserved	Reserved	HVBK_PGOOD	HVBK_DCM_STATE	HVBK_SCP_UV	HVBK_OV	LV_VBST_LOW	AVDD_HVBK_POR
Control									
Register	Addr	7	6	5	4	3	2	1	0
WAIT_CONT	0x0039	WAIT_DIR	Reserved 0	Reserved 1	Reserved 1	DELAY_TIME			
StandBy Interface									
Register	Addr	7	6	5	4	3	2	1	0

Register Status / Config	Addr	7	6	5	4	3	2	1	0
STBY_CONF	0x0049	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved 0	Reserved 0	PSC_EN
Test Registers									
Register	Addr	7	6	5	4	3	2	1	0
BUCK1_CONF2	0x005A	BUCK1_VDAC_RANGE	Reserved 0	Reserved 0	Reserved 1	Reserved 1	Reserved 0	Reserved 1	Reserved 0
BUCK1_CONF5	0x005D	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	BUCK1_VRANGE_GAIN
BUCK2_CONF2	0x0063	BUCK2_VDAC_RANGE	Reserved 0	Reserved 0	Reserved 1	Reserved 1	Reserved 0	Reserved 1	Reserved 0
BUCK2_CONF5	0x0066	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	BUCK2_VRANGE_GAIN
BUCK3_CONF2	0x006C	BUCK3_VDAC_RANGE	Reserved 0	Reserved 0	Reserved 1	Reserved 1	Reserved 0	Reserved 1	Reserved 0
BUCK3_CONF5	0x006F	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	BUCK3_VRANGE_GAIN
HVBUCK_CONF5	0x0079	EN_UV	EN_OV	HVBUCK_EN_SCP	Reserved 1	Reserved 0	Reserved 0	Reserved 0	Reserved 0
HVBUCK_CONF6	0x007A	EN_NEG_OC	EN_POS_OC	Reserved	Reserved 0	Reserved 1	Reserved 1	Reserved 0	Reserved 0
HVBUCK_CONF7	0x007B	Reserved	Reserved	Reserved	TON_REF_SEL_DCM			Reserved 0	Reserved 1

Register Status / Config	Addr	7	6	5	4	3	2	1	0
HVBUCK_CONF16	0x0084	Reserved	DRVH_DET_FALL_DLY			Reserved 0	Reserved 1	DRVH_DRV2	
HVBUCK_CONF17	0x0085	DRVH_DRV1_DRV3		DRVHR_DLY3		DRVHR_DLY2		DRVHR_DLY1	
HVBUCK_CONF18	0x0086	Reserved	DRVL_DET_FALL_DLY			Reserved 0	Reserved 1	DRVL_DRV	
HVBUCK_CONF19	0x0087	DRVL_DLY		DRVHF_DLY3		DRVHF_DLY2		DRVHF_DLY1	
HVBUCK_CONF27	0x008F	Reserved 0	Reserved 1	Reserved 1	Reserved 1	Reserved 1	Reserved 1	EN_PULL_LOW	Reserved 0
HVBUCK_CONF29	0x0091	Reserved 0	Reserved 0	Reserved 0	Reserved 1	Reserved 1	Reserved 1	Reserved 0	EN_PWR_SW

6.1 Status and Configuration

6.1.1 Register STATUS_A

Address	Name	POR value	Status
0x0001	STATUS_A	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	EXT_OT	SEQUENCING	OVER_TMP	VDD_FLT

Field Name	Bits	Type	POR	Description
EXT_OT	[3]	RO	0x0	Indicates for external Over temperature Value: Description 0x0 (POR): 0:Normal 0x1: 1:Fault External Over Temp
SEQUENCING	[2]	RO	0x0	Indicates when the Main FSM is busy Value: Description 0x0 (POR): 0:Normal 0x1: 1:Sequence Running
OVER_TMP	[1]	RO	0x0	Indicates an Over temperature on the PMIC Value: Description 0x0 (POR): 0: Normal 0x1: 1:Fault Over Temp
VDD_FLT	[0]	RO	0x0	VDD level Value: Description 0x0 (POR): 0:VDD Fault 0x1: 1:Normal

6.1.2 Register STATUS_B

Address	Name	POR value	Status
0x0002	STATUS_B	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	BUCK3_VOUT_SCP	BUCK2_VOUT_SCP	BUCK1_VOUT_SCP	HV_BUCK_SCP	HV_BUCK_UV	HV_BUCK_OV

Field Name	Bits	Type	POR	Description
BUCK3_VOUT_SCP	[5]	RO	0x0	Buck3 SCP occurs Value: Description 0x0: 0:Buck3 SCP does not occur

Field Name	Bits	Type	POR	Description
				(POR)
				0x1 1:Buck3 SCP occurs
BUCK2_VOUT_SCP	[4]	RO	0x0	Buck2 SCP occurs Value Description 0x0 (POR) 0:Buck2 SCP does not occur 0x1 1:Buck2 SCP occurs
BUCK1_VOUT_SCP	[3]	RO	0x0	Buck1 SCP occurs Value Description 0x0 (POR) 0:Buck1 SCP does not occur 0x1 1:Buck1 SCP occurs
HV_BUCK_SCP	[2]	RO	0x0	HV Buck SCP occurs Value Description 0x0 (POR) 0:HV Buck SCP does not occur 0x1 1:HV Buck SCP occurs
HV_BUCK_UV	[1]	RO	0x0	HV Buck UV occurs Value Description 0x0 (POR) 0:HV Buck UV does not occur 0x1 1:HV Buck UV occurs
HV_BUCK_OV	[0]	RO	0x0	HV Buck OV occurs Value Description 0x0 (POR) 0:HV Buck OV does not occur 0x1 1:HV Buck OV occurs

6.1.3 Register STATUS_C

Address	Name	POR value	Status
0x0003	STATUS_C	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	BUCK3_VOUT_SCP_DROP_TIMEOUT	BUCK2_VOUT_SCP_DROP_TIMEOUT	BUCK1_VOUT_SCP_DROP_TIMEOUT	Reserved	GPIO_FLAG1	GPIO_FLAG0

Field Name	Bits	Type	POR	Description
BUCK3_VOUT_SCP_DROP_TIMEOUT	[5]	RO	0x0	Buck3 SCP drop timeout occurs Value Description 0x0 (POR) 0:Buck3 SCP drop timeout does not occur 0x1 1:Buck3 SCP drop timeout occurs

Field Name	Bits	Type	POR	Description
BUCK2_VOUT_SCP_DROP_TIMEOUT	[4]	RO	0x0	Buck2 SCP drop timeout occurs Value: 0x0 (POR) — 0:Buck2 SCP drop timeout does not occur Value: 0x1 — 1:Buck2 SCP drop timeout occurs
BUCK1_VOUT_SCP_DROP_TIMEOUT	[3]	RO	0x0	Buck1 SCP drop timeout occurs Value: 0x0 (POR) — 0:Buck1 SCP drop timeout does not occur Value: 0x1 — 1:Buck1 SCP drop timeout occurs
GPIO_FLAG1	[1]	RO	0x0	GPIO_1 event flag Value: 0x0 (POR) — 0:Normal Value: 0x1 — 1:Status GPIO_1
GPIO_FLAG0	[0]	RO	0x0	GPIO_0 event flag Value: 0x0 (POR) — 0:Normal Value: 0x1 — 1:Status - GPIO_0

6.1.4 Register EVENT_A

Address	Name	POR value	IRQ event
0x0004	EVENT_A	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	E_EXT_OT	E_SEQ_RDY	E_OVER_TMP	E_VDD_FLT

Field Name	Bits	Type	POR	Description
E_EXT_OT	[3]	RW W1CL	0x0	Event caused by External Temperature rising above threshold Value: 0x0 (POR) — 0:Normal Value: 0x1 — 1:Event External Over Temp
E_SEQ_RDY	[2]	RW W1CL	0x0	Main FSM has performed an up Sequence Value: 0x0 (POR) — 0:Normal Value: 0x1 — 1:Event Sequencing
E_OVER_TMP	[1]	RW W1CL	0x0	Event caused by Temperature rising above threshold Value: 0x0 (POR) — 0:Normal

Field Name	Bits	Type	POR	Description
				0x1 1:Event Over Temp
E_VDD_FLT	[0]	RW W1CL	0x0	Event caused by VDD level dropping below threshold Value: Description 0x0 (POR): 0:Normal 0x1: 1:Event Low VDD

6.1.5 Register EVENT_B

Address	Name	POR value	IRQ event
0x0005	EVENT_B	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	E_BUCK3_VOUT_SCP_FAIL	E_BUCK2_VOUT_SCP_FAIL	E_BUCK1_VOUT_SCP_FAIL	E_HV_BUCK_SCP_FAIL	E_HV_BUCK_UV_FAIL	E_HV_BUCK_OV_FAIL

Field Name	Bits	Type	POR	Description
E_BUCK3_VOUT_SCP_FAIL	[5]	RW W1CL	0x0	Event caused by falling edge of BUCK3_VOUT_SCP signal debounced by 10 us Value: Description 0x0 (POR): 0:Normal 0x1: 1:Event Buck3 Fault
E_BUCK2_VOUT_SCP_FAIL	[4]	RW W1CL	0x0	Event caused by falling edge of BUCK2_VOUT_SCP signal debounced by 10us Value: Description 0x0 (POR): 0:Normal 0x1: 1:Event Buck2 Fault
E_BUCK1_VOUT_SCP_FAIL	[3]	RW W1CL	0x0	Event caused by falling edge of BUCK1_VOUT_SCP signal debounced by 10 us Value: Description 0x0 (POR): 0:Normal 0x1: 1:Event Buck1 Fault
E_HV_BUCK_SCP_FAIL	[2]	RW W1CL	0x0	Event caused by falling edge of HV_BUCK_SCP signal debounced by 10 us Value: Description 0x0 (POR): 0:Normal 0x1: 1:Event HV Buck Fault
E_HV_BUCK_UV_FAIL	[1]	RW W1CL	0x0	Event caused by falling edge of HV_BUCK_UV signal debounced by 10 us Value: Description 0x0 (POR): 0:Normal 0x1: 1:Event HV Buck Fault
E_HV_BUCK_OV_FAIL	[0]	RW W1CL	0x0	Event caused by falling edge of HV_BUCK_OV signal debounced by 10 us Value: Description 0x0 (POR): 0:Normal 0x1: 1:Event HV Buck Fault

6.1.6 Register EVENT_C

Address	Name	POR value	IRQ event
0x0006	EVENT_C	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	E_BUCK3_VOUT_SCP_DROP_TIMEOUT_FAIL	E_BUCK2_VOUT_SCP_DROP_TIMEOUT_FAIL	E_BUCK1_VOUT_SCP_DROP_TIMEOUT_FAIL	Reserved	E_GPIO_FLAG1	E_GPIO_FLAG0

Field Name	Bits	Type	POR	Description
E_BUCK3_VOUT_SCP_DROP_TIMEOUT_FAIL	[5]	RW W1CL	0x0	Event caused by rising edge of BUCK3_VOUT_SCP_DROP_TIMEOUT signal Value: Description 0x0 (POR): 0:Normal 0x1: 1:Event Buck3 Fault
E_BUCK2_VOUT_SCP_DROP_TIMEOUT_FAIL	[4]	RW W1CL	0x0	Event caused by rising edge of BUCK2_VOUT_SCP_DROP_TIMEOUT signal Value: Description 0x0 (POR): 0:Normal 0x1: 1:Event Buck2 Fault
E_BUCK1_VOUT_SCP_DROP_TIMEOUT_FAIL	[3]	RW W1CL	0x0	Event caused by rising edge of BUCK1_VOUT_SCP_DROP_TIMEOUT signal Value: Description 0x0 (POR): 0:Normal 0x1: 1:Event Buck1 Fault
E_GPIO_FLAG1	[1]	RW W1CL	0x0	Event: GPIO_1 event Value: Description 0x0 (POR): 0:Normal 0x1: 1:Event GPIO_1
E_GPIO_FLAG0	[0]	RW W1CL	0x0	Event: GPIO_0 event Value: Description 0x0 (POR): 0:Normal 0x1: 1:Event GPIO_0

6.1.7 Register FAULT_LOG

Address	Name	POR value
0x0007	FAULT_LOG	0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	EXTERNAL_FAULT	HVBK_OV_FAULT	HVBK_UV_FAULT	HVBK_SCP_FAULT	OVER_TEMP	VDD_FAULT

Field Name	Bits	Type	POR	Description
EXTERNAL_FAULT	[5]	RW W1CL	0x0	Power Down by External Power Down(GPIO) Value: 0x0 (POR) = 0:Normal; 0x1 = 1:Fault
HVBK_OV_FAULT	[4]	RW W1CL	0x0	Power Down by HV BUCK Over Voltage Detection Value: 0x0 (POR) = 0:Normal; 0x1 = 1:Fault
HVBK_UV_FAULT	[3]	RW W1CL	0x0	Power Down by HV BUCK Under Voltage Detection Value: 0x0 (POR) = 0:Normal; 0x1 = 1:Fault
HVBK_SCP_FAULT	[2]	RW W1CL	0x0	Power Down by HV BUCK SCP Detection Value: 0x0 (POR) = 0:Normal; 0x1 = 1:Fault
OVER_TEMP	[1]	RW W1CL	0x0	Power Down by Junction Over Temperature Detection Value: 0x0 (POR) = 0:Normal; 0x1 = 1:Fault
VDD_FAULT	[0]	RW W1CL	0x0	Power Down by VDD Under Voltage Detection Value: 0x0 (POR) = 0:Normal; 0x1 = 1:Fault

6.1.8 Register FAULT_LOG_1

Address	Name	POR value
0x0008	FAULT_LOG_1	0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	BUCK3_SCP_DROP_TIMEOUT_FAULT	BUCK2_SCP_DROP_TIMEOUT_FAULT	BUCK1_SCP_DROP_TIMEOUT_FAULT	BUCK3_SCP_FAULT	BUCK2_SCP_FAULT	BUCK1_SCP_FAULT

Field Name	Bits	Type	POR	Description
BUCK3_SCP_DROP_TIMEOUT_FAULT	[5]	RW W1CL	0x0	Power Down by BUCK 3 SCP Drop timeout Detection Value: Description 0x0 (POR): 0:Normal 0x1: 1:Fault
BUCK2_SCP_DROP_TIMEOUT_FAULT	[4]	RW W1CL	0x0	Power Down by BUCK 2 SCP Drop timeout Detection Value: Description 0x0 (POR): 0:Normal 0x1: 1:Fault
BUCK1_SCP_DROP_TIMEOUT_FAULT	[3]	RW W1CL	0x0	Power Down by BUCK 1 SCP Drop timeout Detection Value: Description 0x0 (POR): 0:Normal 0x1: 1:Fault
BUCK3_SCP_FAULT	[2]	RW W1CL	0x0	Power Down by BUCK 3 SCP Detection Value: Description 0x0 (POR): 0:Normal 0x1: 1:Fault
BUCK2_SCP_FAULT	[1]	RW W1CL	0x0	Power Down by BUCK 2 SCP Detection Value: Description 0x0 (POR): 0:Normal 0x1: 1:Fault
BUCK1_SCP_FAULT	[0]	RW W1CL	0x0	Power Down by BUCK 1 SCP Detection Value: Description 0x0 (POR): 0:Normal 0x1: 1:Fault

6.1.9 Register IRQ_MASK_A

Address	Name	POR value	
0x0009	IRQ_MASK_A	0x08	IRQ event mask

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	M_EXT_OT	M_SEQ_RDY	M_OVER_TMP	M_VDD_FLT

Field Name	Bits	Type	POR	Description
M_EXT_OT	[3]	RW OTP	0x1	nIRQ Mask - External Over_temp Value: Description 0x0: 0:nIRQ from External Over_Temp Event 0x1 (POR): 1:Mask nIRQ from External Over_Temp Event
M_SEQ_RDY	[2]	RW OTP	0x0	nIRQ Mask - Main FSM is busy Value: Description 0x0 (POR): 0:nIRQ from Sequencer Event 0x1: 1:Mask nIRQ from Sequencer Event
M_OVER_TMP	[1]	RW OTP	0x0	nIRQ Mask - Over_temp Value: Description 0x0 (POR): 0:nIRQ from Over Temp Event 0x1: 1:Mask nIRQ from Over Temp Fault Event
M_VDD_FLT	[0]	RW OTP	0x0	nIRQ_Mask - VDD level Value: Description 0x0 (POR): 0:nIRQ from VDD Fault Event 0x1: 1:Mask nIRQ from VDD Fault Event

6.1.10 Register IRQ_MASK_B

Address	Name	POR value	
0x000A	IRQ_MASK_B	0x00	IRQ event mask

7	6	5	4	3	2	1	0
Reserved	Reserved	M_BUCK3_VOUT_SCP_FAIL	M_BUCK2_VOUT_SCP_FAIL	M_BUCK1_VOUT_SCP_FAIL	M_HV_BUCK_SCP_FAIL	M_HV_BUCK_UV_FAIL	M_HV_BUCK_OV_FAIL

Field Name	Bits	Type	POR	Description
M_BUCK3_VOUT_SCP_FAIL	[5]	RW OTP	0x0	nIRQ Mask BUCK3_VOUT_SCP fail event Value: Description 0x0 (POR): 0:nIRQ from Buck3 Event 0x1: 1:Mask nIRQ from Buck3 Event

Field Name	Bits	Type	POR	Description
M_BUCK2_VOUT_SCP_FAIL	[4]	RW OTP	0x0	nIRQ Mask BUCK2_VOUT_SCP fail event Value: Description 0x0 (POR): 0:nIRQ from Buck2 Event 0x1: 1:Mask nIRQ from Buck2 Event
M_BUCK1_VOUT_SCP_FAIL	[3]	RW OTP	0x0	nIRQ Mask BUCK1_VOUT_SCP fail event Value: Description 0x0 (POR): 0:nIRQ from Buck1 Event 0x1: 1:Mask nIRQ from Buck1 Event
M_HV_BUCK_SCP_FAIL	[2]	RW OTP	0x0	nIRQ Mask HV_BUCK_SCP fail event Value: Description 0x0 (POR): 0:nIRQ from HV Buck Event 0x1: 1:Mask nIRQ from HV Buck Event
M_HV_BUCK_UV_FAIL	[1]	RW OTP	0x0	nIRQ Mask HV_BUCK_UV fail event Value: Description 0x0 (POR): 0:nIRQ from HV Buck Event 0x1: 1:Mask nIRQ from HV Buck Event
M_HV_BUCK_OV_FAIL	[0]	RW OTP	0x0	nIRQ Mask HV_BUCK_OV fail event Value: Description 0x0 (POR): 0:nIRQ from HV Buck Event 0x1: 1:Mask nIRQ from HV Buck Event

6.1.11 Register IRQ_MASK_C

Address	Name	POR value	IRQ event mask
0x000B	IRQ_MASK_C	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	M_BUCK3_VOUT_SCP_DROP_TIMEOUT_FAIL	M_BUCK2_VOUT_SCP_DROP_TIMEOUT_FAIL	M_BUCK1_VOUT_SCP_DROP_TIMEOUT_FAIL	Reserved	M_GPIO_FLAG1	M_GPIO_FLAG0

Field Name	Bits	Type	POR	Description
M_BUCK3_VOUT_SCP_DROP_TIMEOUT_FAIL	[5]	RW OTP	0x0	nIRQ Mask BUCK3_VOUT_SCP_DROP_TIMEOUT fail event Value: Description 0x0 (POR): 0:nIRQ from Buck3 Event 0x1: 1:Mask nIRQ from Buck3

Field Name	Bits	Type	POR	Description
				Event
M_BUCK2_VOUT_SCP_DROP_TIMEOUT_FAIL	[4]	RW OTP	0x0	nIRQ Mask BUCK2_VOUT_SCP_DROP_TIMEOUT fail event Value: Description 0x0 (POR): 0:nIRQ from Buck2 Event 0x1: 1:Mask nIRQ from Buck2 Event
M_BUCK1_VOUT_SCP_DROP_TIMEOUT_FAIL	[3]	RW OTP	0x0	nIRQ Mask BUCK1_VOUT_SCP_DROP_TIMEOUT fail event Value: Description 0x0 (POR): 0:nIRQ from Buck1 Event 0x1: 1:Mask nIRQ from Buck1 Event
M_GPIO_FLAG1	[1]	RW OTP	0x0	nIRQ Mask for GPIO_1 event Value: Description 0x0 (POR): 0:nIRQ from GPIO_1 Event 0x1: 1:Mask nIRQ from GPIO_1 Event
M_GPIO_FLAG0	[0]	RW OTP	0x0	nIRQ Mask for GPIO_0 event Value: Description 0x0 (POR): 0:nIRQ from GPIO_0 Event 0x1: 1:Mask nIRQ from GPIO_0 Event

6.1.12 Register CONTROL_A

Address	Name	POR value	
0x000C	CONTROL_A	0x63	System control

7	6	5	4	3	2	1	0
Reserved	Reserved 1	Reserved 1	Reserved	Reserved 0	Reserved 0	PWR_EN	SYS_EN

Field Name	Bits	Type	POR	Description
PWR_EN	[1]	RW OTP	0x1	POWER State target control bit Value: Description 0x0: 0:Low 0x1 (POR): 1:High

SYS_EN	[0]	RW OTP	0x1	SYSTEM State target control bit Value: 0x0 — 0:Low Value: 0x1 (POR) — 1:High

6.1.13 Register CONTROL_B

Address	Name	POR value	
0x000D	CONTROL_B	0x24	System control

7	6	5	4	3	2	1	0
Reserved 0	Reserved 0	WRITE_MODE	Reserved 0	Reserved	Reserved 1	Reserved	Reserved

Field Name	Bits	Type	POR	Description
WRITE_MODE	[5]	RW OTP	0x1	I^2C Write Mode Value: 0x0 — 0: Page Write Mode Value: 0x1 (POR) — 1: Repeated Write Mode

6.1.14 Register CONTROL_C

Address	Name	POR value	
0x000E	CONTROL_C	0x34	System control

7	6	5	4	3	2	1	0
Reserved	Reserved	LDO_EN_PULLDOWN	HVLDO_EN_PULLDOWN	MUTELVL_SEL		EN_MUTE	Reserved 0

Field Name	Bits	Type	POR	Description
LDO_EN_PULLDOWN	[5:5]	RW OTP	0x1	Enable output pull down function Value: 0x0 — 00: Disable Value: 0x1 (POR) — 01: Enable
HVLDO_EN_PULLDOWN	[4:4]	RW OTP	0x1	Enable output pull down function Value: 0x0 — 00: Disable Value: 0x1 (POR) — 01: Enable
MUTELVL_SEL	[3:2]	RW OTP	0x1	Mute Threshold Selection Value: 0x0 — 00: 8.53V Value: 0x1 (POR) — 01: 8.13V

Field Name	Bits	Type	POR	Description
				0x2 10: 7.43V 0x3 11: 6.83V
EN_MUTE	[1:1]	RW OTP	0x0	Enable mute function Value / Description 0x0 (POR) 00: Disable 0x1 01: Enable

6.1.15 Register I2C_BASE_ADDR

Address	Name	POR value
0x0010	I2C_BASE_ADDR	0x80

7	6	5	4	3	2	1	0
IF_BASE_ADDR			Reserved	Reserved	Reserved	Reserved	Reserved

Field Name	Bits	Type	POR	Description
IF_BASE_ADDR	[7:5]	RW OTP	0x4	3 MSB of the I²C Interfaces Base Address XXX10000 10010010 = 0x92 write address of HS (I²C) IF 10010011 = 0x93 read address of HS (I²C) IF Value / Description 0x0 0:0x10 0x1 1:0x30 0x2 2:0x50 0x3 3:0x70 0x4 (POR) 4:0x90 0x5 5:0xB0 0x6 6:0xD0 0x7 7:0xF0

6.2 GPIO

6.2.1 Register GPIO_DATA_IN

Address	Name	POR value
0x0017	GPIO_DATA_IN	0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	GPIO_NIRQ_IN	GPIO_IN	

Field Name	Bits	Type	POR	Description
GPIO_NIRQ_IN	[2]	RO	0x0	GPIO_NIRQ input data Value: Description 0x0 (POR):
GPIO_IN	[1:0]	RO	0x0	GPIO input data Value: Description 0x0 (POR):

6.2.2 Register GPIO_DATA_OUT

Address	Name	POR value
0x0018	GPIO_DATA_OUT	0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	GPO_SDA_OUT	GPIO_NIRQ_OUT	GPIO_OUT	

Field Name	Bits	Type	POR	Description
GPO_SDA_OUT	[3]	RW OTP	0x0	GPO_SDA output data Value: Description 0x0 (POR):
GPIO_NIRQ_OUT	[2]	RW OTP	0x0	GPIO_NIRQ output data Value: Description 0x0 (POR):
GPIO_OUT	[1:0]	RW OTP	0x0	GPIO output data Value: Description 0x0 (POR):

6.2.3 Register GPIO_0_CONF

Address	Name	POR value
0x0019	GPIO_0_CONF	0x00

7	6	5	4	3	2	1	0
GPIO_0_FUNC_SEL			GPIO_0_ACTIVE_LOW	GPIO_0_PD	GPIO_0_PU	GPIO_0_PP	GPIO_0_OUT_EN

Field Name	Bits	Type	POR	Description
GPIO_0_FUNC_SEL	[7:5]	RW OTP	0x0	Gpio Function Select Value: Description 0x0 (POR): 0: Pure GPIO 0x1: 1: Power Sequencer Control, GPO 0x2: 2: External Interrupt, GPI 0x3: 3: External Power Down, GPI 0x4: 4: Loop GPIO_NIRQ Input as output 0x5: 5: Mute 0x6: 6: NA 0x7: 7: NA
GPIO_0_ACTIVE_LOW	[4]	RW OTP	0x0	Active Low Value: Description 0x0 (POR): 0: Default (active high) 0x1: 1: Active Low
GPIO_0_PD	[3]	RW OTP	0x0	Pull Down Value: Description 0x0 (POR): 0: Pull down disable 0x1: 1: Pull down enable
GPIO_0_PU	[2]	RW OTP	0x0	Pull Up Value: Description 0x0 (POR): 0: Pull up disable 0x1: 1: Pull up enable
GPIO_0_PP	[1]	RW OTP	0x0	Push Pull Value: Description 0x0 (POR): 0: Open Drain 0x1: 1: Push-Pull
GPIO_0_OUT_EN	[0]	RW OTP	0x0	Output Enable Value: Description 0x0 (POR): 0: GPI

Field Name	Bits	Type	POR	Description	
				0x1	1: GPO

6.2.4 Register GPIO_1_CONF

Address	Name	POR value
0x001A	GPIO_1_CONF	0x00

7	6	5	4	3	2	1	0
GPIO_1_FUNC_SEL			GPIO_1_ACTIVE_LOW	GPIO_1_PD	GPIO_1_PU	GPIO_1_PP	GPIO_1_OUT_EN

Field Name	Bits	Type	POR	Description	
GPIO_1_FUNC_SEL	[7:5]	RW OTP	0x0	GPIO Function Select	
				Value	Description
				0x0 (POR)	0: Pure GPIO
				0x1	1: Power Sequencer Control, GPO
				0x2	2: External Interrupt, GPI
				0x3	3: External Power Down, GPI
				0x4	4: Loop GPIO_0 Input as output
				0x5	5: Mute
				0x6	6: NA
				0x7	7: NA
GPIO_1_ACTIVE_LOW	[4]	RW OTP	0x0	Active Low	
				Value	Description
				0x0 (POR)	0: Default (active high)
				0x1	1: Active Low
GPIO_1_PD	[3]	RW OTP	0x0	Pull Down	
				Value	Description
				0x0 (POR)	0: Pull down disable
				0x1	1: Pull down enable
GPIO_1_PU	[2]	RW OTP	0x0	Pull Up	
				Value	Description
				0x0 (POR)	0: Pull up disable
				0x1	1: Pull up enable
GPIO_1_PP	[1]	RW OTP	0x0	Push Pull	
				Value	Description
				0x0 (POR)	0: Open Drain
				0x1	1: Push-Pull
GPIO_1_OUT_EN	[0]	RW	0x0	Output Enable	

Field Name	Bits	Type	POR	Description
		OTP		Value / Description 0x0 (POR): 0: GPI 0x1: 1: GPO

6.2.5 Register GPIO_NIRQ_CONF

Address	Name	POR value
0x001B	GPIO_NIRQ_CONF	0x00

7	6	5	4	3	2	1	0
GPIO_NIRQ_FUNC_SEL			GPIO_NIRQ_ACTIVE_LOW	GPIO_NIRQ_PD	GPIO_NIRQ_PU	GPIO_NIRQ_PP	GPIO_NIRQ_OUT_EN

Field Name	Bits	Type	POR	Description
GPIO_NIRQ_FUNC_SEL	[7:5]	RW OTP	0x0	GPIO Function Select Value / Description 0x0 (POR): 0: NIRQ, GPO 0x1: 1: Power Sequencer Control, GPO 0x2: 2: Pure GPIO 0x3: 3: NA 0x4: 4: Loop GPIO_1 Input as output 0x5: 5: Mute 0x6: 6: NA 0x7: 7: NA
GPIO_NIRQ_ACTIVE_LOW	[4]	RW OTP	0x0	Active Low Value / Description 0x0 (POR): 0: Default (active high) 0x1: 1: Active Low
GPIO_NIRQ_PD	[3]	RW OTP	0x0	Pull Down Value / Description 0x0 (POR): 0: Pull down disable 0x1: 1: Pull down enable
GPIO_NIRQ_PU	[2]	RW OTP	0x0	Pull Up Value / Description 0x0 (POR): 0: Pull up disable 0x1: 1: Pull up enable
GPIO_NIRQ_PP	[1]	RW OTP	0x0	Push Pull Value / Description 0x0: 0: Open Drain

Field Name	Bits	Type	POR	Description
				(POR)
				0x1: 1: Push-Pull
GPIO_NIRQ_OUT_EN	[0]	RW OTP	0x0	Output Enable Value: Description 0x0 (POR): 0: GPI 0x1: 1: GPO

6.2.6 Register GPIO_VBUCK_CONF

Address	Name	POR value
0x001C	GPIO_VBUCK_CONF	0x00

7	6	5	4	3	2	1	0
VBUCK2_USE_2GPIO_SEL	GPO_SDA_ACTIVE_LOW	VBUCK3_GPIO_SEL		VBUCK2_GPIO_SEL		VBUCK1_GPIO_SEL	

Field Name	Bits	Type	POR	Description
VBUCK2_USE_2GPIO_SEL	[7]	RW OTP	0x0	Buck2 use both GPIO_1, GPIO_0 to select the VBUCK_ALT, Buck1,3 will lost VBUCK_SEL function. Case({gpio_1, gpio_0}) 2'b00 : VBUCK2; 2'b01 : VBUCK2_ALT; 2'b10 : VBUCK1_ALT; 2'b11 : VBUCK3_ALT; Value: Description 0x0 (POR): 0: Disable 0x1: 1: Enable
GPO_SDA_ACTIVE_LOW	[6]	RW OTP	0x0	SDA use as GPO Active Low Value: Description 0x0 (POR): 0: Default (active high) 0x1: 1: Active Low
VBUCK3_GPIO_SEL	[5:4]	RW OTP	0x0	Over-ride VBUCK3 value with VBUCK2_ALT Value: Description 0x0 (POR): 00: Do Not Over-ride the value 0x1: 01: Over-ride the value when GPIO_0 is high 0x2: 10: Over-ride the value when GPIO_1 is high 0x3: 11: Over-ride the value when NIRQ is high
VBUCK2_GPIO_SEL	[3:2]	RW OTP	0x0	Over-ride VBUCK2 value with VBUCK2_ALT Value: Description 0x0 (POR): 00: Do Not Over-ride the value 0x1: 01: Over-ride the value when GPIO_0 is high

Field Name	Bits	Type	POR	Description
				0x2: 10: Over-ride the value when GPIO_1 is high 0x3: 11: Over-ride the value when NIRQ is high
VBUCK1_GPIO_SEL	[1:0]	RW OTP	0x0	Over-ride VBUCK1 value with VBUCK1_ALT Value / Description 0x0 (POR): 00: Do Not Over-ride the value 0x1: 01: Over-ride the value when GPIO_0 is high 0x2: 10: Over-ride the value when GPIO_1 is high 0x3: 11: Over-ride the value when NIRQ is high

6.2.7 Register GPIO_UP_SEQ_CONF

Address	Name	POR value
0x001D	GPIO_UP_SEQ_CONF	0x00

7	6	5	4	3	2	1	0
GPIO_1_UP_STEP				GPIO_0_UP_STEP			

Field Name	Bits	Type	POR	Description
GPIO_1_UP_STEP	[7:4]	RW OTP	0x0	Power Up Sequencer STEP for GPIO_1 Value / Description 0x0 (POR):
GPIO_0_UP_STEP	[3:0]	RW OTP	0x0	Power Up Sequencer STEP for GPIO_0 Value / Description 0x0 (POR):

6.2.8 Register GPIO_DN_SEQ_CONF

Address	Name	POR value
0x001E	GPIO_DN_SEQ_CONF	0x00

7	6	5	4	3	2	1	0
GPIO_1_DN_STEP				GPIO_0_DN_STEP			

Field Name	Bits	Type	POR	Description
GPIO_1_DN_STEP	[7:4]	RW OTP	0x0	Power Down Sequencer STEP for GPIO_1 Value: 0x0 (POR) — Description:
GPIO_0_DN_STEP	[3:0]	RW OTP	0x0	Power Dn Sequencer STEP for GPIO_0 Value: 0x0 (POR) — Description:

6.2.9 Register GPO_SDA_SEQ_CONF

Address	Name	POR value
0x001F	GPO_SDA_SEQ_CONF	0x00

7	6	5	4	3	2	1	0
GPO_SDA_DN_STEP				GPO_SDA_UP_STEP			

Field Name	Bits	Type	POR	Description
GPO_SDA_DN_STEP	[7:4]	RW OTP	0x0	Power Down Sequencer STEP for GPO_SDA Value: 0x0 (POR) — Description:
GPO_SDA_UP_STEP	[3:0]	RW OTP	0x0	Power Up Sequencer STEP for GPO_SDA Value: 0x0 (POR) — Description:

6.2.10 Register GPIO_NIRQ_SEQ_CONF

Address	Name	POR value
0x0020	GPIO_NIRQ_SEQ_CONF	0x00

7	6	5	4	3	2	1	0
GPIO_NIRQ_DN_STEP				GPIO_NIRQ_UP_STEP			

Field Name	Bits	Type	POR	Description
GPIO_NIRQ_DN_STEP	[7:4]	RW OTP	0x0	Power Down Sequencer STEP for GPIO_NIRQ Value: 0x0 (POR) — Description:
GPIO_NIRQ_UP_STEP	[3:0]	RW OTP	0x0	Power Up Sequencer STEP for GPIO_NIRQ Value: 0x0 (POR) — Description:

6.3 Sequencer

6.3.1 Register ID_0

Address	Name	POR value
0x0021	ID_0	0x01

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	WAIT_ID_ALWAYS	Reserved 0	Reserved 0	Reserved 1

Field Name	Bits	Type	POR	Description
WAIT_ID_ALWAYS	[3]	RW OTP	0x0	WAIT_ID Configuration: 0: Only Perform the WAIT_ID Step on First Use of Sequencer, 1: Perform the WAIT_ID Step on Subsequent Uses of Sequencer. Value: Description 0x0 (POR): 0:First Use 0x1: 1:Always

6.3.2 Register HV_BUCK_STEP

Address	Name	POR value
0x0022	HV_BUCK_STEP	0x00

7	6	5	4	3	2	1	0
HV_BUCK_STDBY_STEP				HV_BUCK_STEP			

Field Name	Bits	Type	POR	Description
HV_BUCK_STDBY_STEP	[7:4]	RW OTP	0x0	Power Sequencer Time for HV Buck STDBY Voltage change Value: Description 0x0 (POR):
HV_BUCK_STEP	[3:0]	RW OTP	0x0	Power Sequencer Time for HV Buck Value: Description 0x0 (POR):

6.3.3 Register BUCK_1_2_STEP

Address	Name	POR value
0x0024	BUCK_1_2_STEP	0x00

7	6	5	4	3	2	1	0
BUCK2_STEP				BUCK1_STEP			

Field Name	Bits	Type	POR	Description
BUCK2_STEP	[7:4]	RW OTP	0x0	Power Sequencer Time forBUCK2 Value: Description 0x0 (POR):
BUCK1_STEP	[3:0]	RW OTP	0x0	Power Sequencer Time forBUCK1 Value: Description 0x0 (POR):

6.3.4 Register BUCK_3_STEP

Address	Name	POR value
0x0025	BUCK_3_STEP	0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	BUCK3_STEP			

Field Name	Bits	Type	POR	Description
BUCK3_STEP	[3:0]	RW OTP	0x0	Power Sequencer Time forBUCK3 Value: Description 0x0 (POR):

6.3.5 Register SEQ_STATUS

Address	Name	POR value
0x0026	SEQ_STATUS	0x00

7	6	5	4	3	2	1	0
SEQ_POINTER				WAIT_STEP			

Field Name	Bits	Type	POR	Description
SEQ_POINTER	[7:4]	RW	0x0	Actual Pointer Position (Time Slot) of Power Sequencer Value: Description 0x0 (POR):
WAIT_STEP	[3:0]	RW	0x0	Power Sequencer Time for Wait Step

		OTP		Value: 0x0 (POR) — Description:

6.3.6 Register SEQ_A

Address	Name	POR value
0x0027	SEQ_A	0x96

7	6	5	4	3	2	1	0
POWER_END				SYSTEM_END			

Field Name	Bits	Type	POR	Description
POWER_END	[7:4]	RW OTP	0x9	OTP Pointer - Last Supply of Domain POWER Value: 0x9 (POR) — Description:
SYSTEM_END	[3:0]	RW OTP	0x6	OTP Pointer - Last Supply of Domain SYSTEM Value: 0x6 (POR) — Description:

6.3.7 Register SEQ_B

Address	Name	POR value
0x0028	SEQ_B	0x49

7	6	5	4	3	2	1	0
Reserved 0	Reserved 1	Reserved 0	Reserved 0	MAX_COUNT			

Field Name	Bits	Type	POR	Description
MAX_COUNT	[3:0]	RW OTP	0x9	OTP Pointer - Last Supply of Domain POWER1 Value: 0x9 (POR) — Description:

6.3.8 Register SEQ_TIMER

Address	Name	POR value
0x0029	SEQ_TIMER	0x3D

7	6	5	4	3	2	1	0
SEQ_DUMMY				SEQ_TIME			

Field Name	Bits	Type	POR	Description
SEQ_DUMMY	[7:4]	RW OTP	0x3	Time for empty Sequence slots

Value	Description
0x0	0000: 32usec
0x1	0001: 64usec
0x2	0010: 96usec
0x3 (POR)	0011: 128usec
0x4	0100: 160usec
0x5	0101: 192usec
0x6	0110: 224usec
0x7	0111: 256usec
0x8	1000: 288usec
0x9	1001: 384usec
0x10	1010: 448usec
0x11	1011: 512usec
0x12	1100: 1.024msec
0x13	1101: 2.048msec
0x14	1110: 4.096msec
0x15	1111: 8.192msec

Field Name	Bits	Type	POR	Description
SEQ_TIME	[3:0]	RW OTP	0xd	Time for each non-empty Sequence slot

Value	Description
0x0	0000: 32usec
0x1	0001: 64usec
0x2	0010: 96usec
0x3	0011: 128usec
0x4	0100: 160usec
0x5	0101: 192usec
0x6	0110: 224usec
0x7	0111: 256usec
0x8	1000: 288usec
0x9	1001: 384usec
0x10	1010: 448usec
0x11	1011: 512usec
0x12	1100: 1.024msec
0x13	1101: 2.048msec

				0x14	1110: 4.096msec
				0x15	1111: 8.192msec

6.4 Supplies

6.4.1 Register BUCK1_CONF0

Address	Name	POR value
0x002A	BUCK1_CONF0	0x50

7	6	5	4	3	2	1	0
BUCK1_EN	VBUCK1						

Field Name	Bits	Type	POR	Description
BUCK1_EN	[7]	RW OTP	0x0	BUCK Enable Value: Description 0x0 (POR): 0:Disabled 0x1: 1:Enabled
VBUCK1	[6:0]	RW OTP	0x50	Buck Target Voltage. Vout = (1+vrange_gain)*(((0.8*vdac_range)+0.6)+0.003125*2*VBuck[6:0]) Value: Description 0x0:

6.4.2 Register BUCK1_CONF0_ALT

Address	Name	POR value
0x002B	BUCK1_CONF0_ALT	0x50

7	6	5	4	3	2	1	0
Reserved	VBUCK1_ALT						

Field Name	Bits	Type	POR	Description
VBUCK1_ALT	[6:0]	RW OTP	0x50	ALT. Buck Target Voltage. Vout = (1+vrange_gain)*(((0.8*vdac_range)+0.6)+0.003125*2*VBuck[6:0]) Value: Description 0x0:

6.4.3 Register BUCK1_CONF1

Address	Name	POR value
0x002C	BUCK1_CONF1	0x29

7	6	5	4	3	2	1	0
BUCK1_PD_DIS	Reserved 0	Reserved 1	Reserved	BUCK1_SYNC_ILIM		BUCK1_MODE	

Field Name	Bits	Type	POR	Description
BUCK1_PD_DIS	[7]	RW OTP	0x0	Pull down disable Value: 0x0 (POR) – 0: Enable PD in OFF Mode 0x1 – 1: Disable PD in OFF Mode
BUCK1_SYNC_ILIM	[3:2]	RW OTP	0x2	BUCK Current Limit: 0x0 – 00: 3230mA 0x1 – 01: 5130mA 0x2 (POR) – 10: 6960mA 0x3 – 11: 8790mA
BUCK1_MODE	[1:0]	RW OTP	0x1	BUCK Operating Mode: 0x0 – 00: Sleep Mode (PFM) 0x1 (POR) – 01: Automatic Mode 0x2 – 10: Synchronous Mode (PWM) 0x3 – 11: Reserved

6.4.4 Register BUCK2_CONF0

Address	Name	POR value
0x002D	BUCK2_CONF0	0x50

7	6	5	4	3	2	1	0
BUCK2_EN	VBUCK2						

Field Name	Bits	Type	POR	Description
BUCK2_EN	[7]	RW OTP	0x0	BUCK Enable Value: 0x0 (POR) – 0:Disabled 0x1 – 1:Enabled
VBUCK2	[6:0]	RW OTP	0x50	Buck Target Voltage. Vout = (1+vrange_gain)*(((0.8*vdac_range)+0.6)+0.003125*2*VBuck[6:0])

				Value	Description
				0x0	

6.4.5 Register BUCK2_CONF0_ALT

Address	Name	POR value
0x002E	BUCK2_CONF0_ALT	0x50

7	6	5	4	3	2	1	0
Reserved	VBUCK2_ALT						

Field Name	Bits	Type	POR	Description
VBUCK2_ALT	[6:0]	RW OTP	0x50	ALT. Buck Target Voltage. Vout = (1+vrange_gain)*(((0.8*vdac_range)+0.6)+0.003125*2*VBuck[6:0]) Value: 0x0 — Description:

6.4.6 Register BUCK2_CONF1

Address	Name	POR value
0x002F	BUCK2_CONF1	0x29

7	6	5	4	3	2	1	0
BUCK2_PD_DIS	Reserved 0	Reserved 1	Reserved	BUCK2_SYNC_ILIM		BUCK2_MODE	

Field Name	Bits	Type	POR	Description
BUCK2_PD_DIS	[7]	RW OTP	0x0	Pull down disable 0x0 (POR): 0: Enable PD in OFF Mode 0x1: 1: Disable PD in OFF Mode
BUCK2_SYNC_ILIM	[3:2]	RW OTP	0x2	BUCK Current Limit: 0x0: 00: 1496mA 0x1: 01: 2393mA 0x2 (POR): 10: 3291mA 0x3: 11: 4189mA
BUCK2_MODE	[1:0]	RW OTP	0x1	BUCK Operating Mode: 0x0: 00: Sleep Mode (PFM) 0x1 (POR): 01: Automatic Mode 0x2: 10: Synchronous Mode (PWM)

				0x3	11: Reserved

6.4.7 Register BUCK3_CONF0

Address	Name	POR value
0x0030	BUCK3_CONF0	0x50

7	6	5	4	3	2	1	0
BUCK3_EN	VBUCK3						

Field Name	Bits	Type	POR	Description
BUCK3_EN	[7]	RW OTP	0x0	BUCK Enable Value: Description 0x0 (POR): 0:Disabled 0x1: 1:Enabled
VBUCK3	[6:0]	RW OTP	0x50	Buck Target Voltage. Vout = (1+vrange_gain)*(((0.8*vdac_range)+0.6)+0.003125*2*VBuck[6:0]) Value: Description 0x0:

6.4.8 Register BUCK3_CONF0_ALT

Address	Name	POR value
0x0031	BUCK3_CONF0_ALT	0x50

7	6	5	4	3	2	1	0
Reserved	VBUCK3_ALT						

Field Name	Bits	Type	POR	Description
VBUCK3_ALT	[6:0]	RW OTP	0x50	ALT. Buck Target Voltage. Vout = (1+vrange_gain)*(((0.8*vdac_range)+0.6)+0.003125*2*VBuck[6:0]) Value: Description 0x0:

6.4.9 Register BUCK3_CONF1

Address	Name	POR value
0x0032	BUCK3_CONF1	0x29

7	6	5	4	3	2	1	0
BUCK3_PD_DIS	Reserved 0	Reserved 1	Reserved	BUCK3_SYNC_ILIM		BUCK3_MODE	

Field Name	Bits	Type	POR	Description
BUCK3_PD_DIS	[7]	RW OTP	0x0	Pull down disable Value: 0x0 (POR) — 0: Enable PD in OFF Mode 0x1 — 1: Disable PD in OFF Mode
BUCK3_SYNC_ILIM	[3:2]	RW OTP	0x2	BUCK Current Limit: 0x0 — 00: 1496mA 0x1 — 01: 2393mA 0x2 (POR) — 10: 3291mA 0x3 — 11: 4189mA
BUCK3_MODE	[1:0]	RW OTP	0x1	BUCK Operating Mode: 0x0 — 00: Sleep Mode (PFM) 0x1 (POR) — 01: Automatic Mode 0x2 — 10: Synchronous Mode (PWM) 0x3 — 11: Reserved

6.4.10 Register HVBUCK_CONF1

Address	Name	POR value
0x0033	HVBUCK_CONF1	0x00

7	6	5	4	3	2	1	0
VHVBUCK							

Field Name	Bits	Type	POR	Description
VHVBUCK	[7:0]	RW OTP	0x0	Buck output voltage select and the value will provide to DAC DAC output: 0V to 1.275V, 5mV/step, 8 bit, 255 steps allowed min target hvbk_dac<7:0> =10100000 (DEC=160, 0.8V) allowed max target hvbk_dac<7:0> =11111111 (DEC=255, 1.275V) DVC slew rate is accounted in hvbk_dac<7:0> Value: 0x0 (POR) — 000000: 0V

				0x1	000001: 0.005V
				0x2	000010: 0.01V
				...	...
				0xFF	111111: 1.275V

6.4.11 Register HVBUCK_CONF2

Address	Name	POR value
0x0034	HVBUCK_CONF2	0xC2

7	6	5	4	3	2	1	0
Reserved 1	TON_CTRIM			VHVBUCK_SLEW_RATE			HVBUCK_EN

Field Name	Bits	Type	POR	Description
TON_CTRIM	[6:4]	RW OTP	0x4	Setting bits for switching frequency adjustment (change Ton charging cap). Setting range: 167kHz to 1.25MHz, nominal 500kHz. Value: Description 0x0: 000: 1.25MHz 0x1: 001: 1MHz 0x2: 010: 833kHz 0x3: 011: 625kHz 0x4 (POR): 100: 500kHz 0x5: 101: 357kHz 0x6: 110: 250kHz 0x7: 111: 167kHz
VHVBUCK_SLEW_RATE	[3:1]	RW OTP	0x1	HV BUCK slew rate: Value: Description 0x0: 000: 1.5625mV/us 0x1 (POR): 001: 3.125mV/us 0x2: 010: 4.6875mV/us 0x3: 011: 6.25mV/us 0x4: 100: 7.8125mV/us 0x5: 101: 9.375mV/us 0x6: 110: 10.9375mV/us 0x7: 111: 12.5mV/us
HVBUCK_EN	[0]	RW OTP	0x0	HV Buck enable Value: Description 0x0 (POR): 0: Disable 0x1: 1: Enable

6.4.12 Register HVBUCK_CONF3

Address	Name	POR value
0x0035	HVBUCK_CONF3	0xD3

7	6	5	4	3	2	1	0
Reserved 1	OV_TH		UV_TH			ITON_SCALE	

Field Name	Bits	Type	POR	Description
OV_TH	[6:5]	RW OTP	0x2	OV threshold Value: 0x0 — 00: (105%~107.5%)*DAC_out 0x1 — 01: (110%~112.5%)*DAC_out 0x2 (POR) — 10: (115%~120%)*DAC_out 0x3 — 11: (125%~130%)*DAC_out
UV_TH	[4:2]	RW OTP	0x4	UV threshold Value: 0x0 — 000: 95%*DAC_out 0x1 — 001: 92.5%*DAC_out 0x2 — 010: 90%*DAC_out 0x3 — 011: 87.5%*DAC_out 0x4 (POR) — 100: 85%*DAC_out 0x5 — 101: 80%*DAC_out 0x6 — 110: 75%*DAC_out 0x7 — 111: 70%*DAC_out
ITON_SCALE	[1:0]	RW OTP	0x3	Ton width based on Vout to fix switching frequency (e.g. 500kHz) Value: 0x0 — 00: Vout=0.8V~1.275V 0x1 — 01: Vout=1.6V~2.55V 0x2 — 10: Vout=2.4V~3.825V 0x3 (POR) — 11: Vout=4V~6.375V

6.4.13 Register HVBUCK_CONF4

Address	Name	POR value
0x0036	HVBUCK_CONF4	0x04

7	6	5	4	3	2	1	0
Reserved	NEG_OC_TH			Reserved	POS_OC_TH		

Field Name	Bits	Type	POR	Description
NEG_OC_TH	[6:4]	RW OTP	0x0	Negative OC/zero-crossing threshold, V(SW_HVBK)-V(PGND) when low-side MOS is turned on

<table>
<tr><td></td><td></td><td></td><td></td><td><table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0 (POR)</td><td>000: 0mV</td></tr><tr><td>0x1</td><td>001: 10mV</td></tr><tr><td>0x2</td><td>010: 20mV</td></tr><tr><td>0x3</td><td>011: 40mV</td></tr><tr><td>0x4</td><td>100: 60mV</td></tr><tr><td>0x5</td><td>101: 80mV</td></tr><tr><td>0x6</td><td>110: 120mV</td></tr><tr><td>0x7</td><td>111: 160mV</td></tr></table></td></tr>
<tr><td>POS_OC_TH</td><td>[2:0]</td><td>RW OTP</td><td>0x4</td><td>Positive OC threshold, V(PGND)-V(SW_HVBK) when low-side MOS is turned on<table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0</td><td>000: 90mV</td></tr><tr><td>0x1</td><td>001: 120mV</td></tr><tr><td>0x2</td><td>010: 150mV</td></tr><tr><td>0x3</td><td>011: 180mV</td></tr><tr><td>0x4 (POR)</td><td>100: 210mV</td></tr><tr><td>0x5</td><td>101: 240mV</td></tr><tr><td>0x6</td><td>110: 270mV</td></tr><tr><td>0x7</td><td>111: 300mV</td></tr></table></td></tr>
</table>

6.4.14 Register HVBUCK_VSTDBY

Address	Name	POR value
0x0037	HVBUCK_VSTDBY	0x07

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	VHVBUCK_STDBY		

Field Name	Bits	Type	POR	Description
VHVBUCK_STDBY	[2:0]	RW OTP	0x7	HV Buck output voltage select in standby mode. DAC output: 0.66V to 0.96V Value: 0x0 — 0000: set DAC=0.76V, Vout=3.8V 0x1 — 0001: set DAC=0.78V, Vout=3.9V 0x2 — 0010: set DAC=0.8V, Vout=4V 0x3 — 0011: set DAC=0.82V, Vout=4.1V 0x4 — 0100: set DAC=0.84V, Vout=4.2V 0x5 — 0101: set DAC=0.86V, Vout=4.3V 0x6 — 0110: set DAC=0.88V, Vout=4.4V 0x7 (POR) — 0111: set DAC=0.9V, Vout=4.5V

6.4.15 Register HVBUCK_STATUS1

Address	Name	POR value
0x0038	HVBUCK_STATUS1	0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	HVBK_PGOOD	HVBK_DCM_STATE	HVBK_SCP_UV	HVBK_OV	LV_VBST_LOW	AVDD_HVBK_POR

Field Name	Bits	Type	POR	Description
HVBK_PGOOD	[5]	RO	0x0	Report HV buck Vout >92.5% target Vout Value: 0x0 (POR)
HVBK_DCM_STATE	[4]	RO	0x0	HV Buck DCM state indicator Value: 0x0 (POR)
HVBK_SCP_UV	[3]	RO	0x0	HV buck SCP/UV detection result Value: 0x0 (POR)
HVBK_OV	[2]	RO	0x0	HV buck OV detection result Value

Field Name	Bits	Type	POR	Description
				0x0 (POR)
LV_VBST_LOW	[1]	RO	0x0	Report LV_VBST_low to digital Value: Description 0x0 (POR)
AVDD_HVBK_POR	[0]	RO	0x0	Report AVDD_HVBK POR to digital Value: Description 0x0 (POR)

6.5 Control

6.5.1 Register WAIT_CONT

Address	Name	POR value
0x0039	WAIT_CONT	0x3B

7	6	5	4	3	2	1	0
WAIT_DIR	Reserved 0	Reserved 1	Reserved 1	DELAY_TIME			

Field Name	Bits	Type	POR	Description
WAIT_DIR	[7]	RW OTP	0x0	Value: 0x0 (POR) — 0: Wait during Power-Up Sequence Value: 0x1 — 1: Wait during Power-Up and Power-Down Sequence
DELAY_TIME	[3:0]	RW OTP	0xb	OUT32K and RTC internal clock delay when in timer mode Value: 0x0 — 0000: 0usec Value: 0x1 — 0001: 540us Value: 0x2 — 0010: 1.0msec Value: 0x3 — 0011: 2.0msec Value: 0x4 — 0100: 4.1msec Value: 0x5 — 0101: 8.2msec Value: 0x6 — 0110: 16.4msec Value: 0x7 — 0111: 32.8msec Value: 0x8 — 1000: 65.5msec Value: 0x9 — 1001: 131msec Value: 0x10 — 1010: 262msec Value: 0x11 — 1011: 524msec Value: 0x12 — 1100: 1.0sec Value: 0x13 — 1101: 2.1sec Value: 0x14 — 1110: 4.2sec Value: 0x15 — 1111: 8.4sec

6.6 Standby Interface

6.6.1 Register STBY_CONF

Address	Name	POR value
0x0049	STBY_CONF	0x00

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved 0	Reserved 0	PSC_EN

Field Name	Bits	Type	POR	Description
PSC_EN	[0]	RW OTP	0x0	Stand-By Controller feature enable default to disabled requires Host or OTP to enable Value: 0x0 (POR) = 0:Disable; 0x1 = 1:Enable

6.7 Test Registers

6.7.1 Register BUCK1_CONF2

Address	Name	POR value
0x005A	BUCK1_CONF2	0x1A

7	6	5	4	3	2	1	0
BUCK1_VDAC_RANGE	Reserved 0	Reserved 0	Reserved 1	Reserved 1	Reserved 0	Reserved 1	Reserved 0

Field Name	Bits	Type	POR	Description
BUCK1_VDAC_RANGE	[7]	RW OTP	0x0	Voltage DAC range Value: Description 0x0 (POR): 0.6V-1.4V 0x1: 1.4V-2.2V

6.7.2 Register BUCK1_CONF5

Address	Name	POR value
0x005D	BUCK1_CONF5	0x00

7	6	5	4	3	2	1	0
Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	BUCK1_VRANGE_GAIN

Field Name	Bits	Type	POR	Description
BUCK1_VRANGE_GAIN	[0]	RW OTP	0x0	Set 2x gain onBUCK1 for VOUT>2.4V Value: Description 0x0 (POR): 0:1x Gain 0x1: 1:2x Gain

6.7.3 Register BUCK2_CONF2

Address	Name	POR value
0x0063	BUCK2_CONF2	0x1A

7	6	5	4	3	2	1	0
BUCK2_VDAC_RANGE	Reserved 0	Reserved 0	Reserved 1	Reserved 1	Reserved 0	Reserved 1	Reserved 0

Field Name	Bits	Type	POR	Description
BUCK2_VDAC_RANGE	[7]	RW OTP	0x0	Voltage DAC range Value: Description 0x0: 0.6V-1.4V

				(POR)	
				0x1	1.4V-2.2V

6.7.4 Register BUCK2_CONF5

Address	Name	POR value
0x0066	BUCK2_CONF5	0x00

7	6	5	4	3	2	1	0
Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	BUCK2_VRANGE_GAIN

Field Name	Bits	Type	POR	Description	
BUCK2_VRANGE_GAIN	[0]	RW OTP	0x0	Set 2x gain onBUCK2 for VOUT>2.4V	
				Value	Description
				0x0 (POR)	0:1x Gain
				0x1	1:2x Gain

6.7.5 Register BUCK3_CONF2

Address	Name	POR value
0x006C	BUCK3_CONF2	0x1A

7	6	5	4	3	2	1	0
BUCK3_VDAC_RANGE	Reserved 0	Reserved 0	Reserved 1	Reserved 1	Reserved 0	Reserved 1	Reserved 0

Field Name	Bits	Type	POR	Description	
BUCK3_VDAC_RANGE	[7]	RW OTP	0x0	Voltage DAC range	
				Value	Description
				0x0 (POR)	0.6V-1.4V
				0x1	1.4V-2.2V

6.7.6 Register BUCK3_CONF5

Address	Name	POR value
0x006F	BUCK3_CONF5	0x00

7	6	5	4	3	2	1	0
Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	BUCK3_VRANGE_GAIN

Field Name	Bits	Type	POR	Description
BUCK3_VRANGE_GAIN	[0]	RW	0x0	Set 2x gain onBUCK3 for VOUT>2.4V

		OTP		Value: 0x0 (POR) — Description: 0:1x Gain Value: 0x1 — Description: 1:2x Gain

6.7.7 Register HVBUCK_CONF5

Address	Name	POR value
0x0079	HVBUCK_CONF5	0xF0

7	6	5	4	3	2	1	0
EN_UV	EN_OV	HVBUCK_EN_SCP	Reserved 1	Reserved 0	Reserved 0	Reserved 0	Reserved 0

Field Name	Bits	Type	POR	Description
EN_UV	[7]	RW OTP	0x1	Enable UV detection, During soft start, DVC, and soft stop with 50us extension, UV detection is disabled Value: 0x0 — Description: 0: disable UV detection Value: 0x1 (POR) — Description: 1: enable UV detection
EN_OV	[6]	RW OTP	0x1	Enable OV detection, During soft start, DVC, and soft stop with 50us extension, OV detection is disabled Value: 0x0 — Description: 0: disable OV detection Value: 0x1 (POR) — Description: 1: enable OV detection
HVBUCK_EN_SCP	[5]	RW OTP	0x1	Enable Vout short detection Value: 0x0 — Description: 0: Disable Vout short detection and reaction Value: 0x1 (POR) — Description: 1: Enable Vout short detection

6.7.8 Register HVBUCK_CONF6

Address	Name	POR value
0x007A	HVBUCK_CONF6	0xCC

7	6	5	4	3	2	1	0
EN_NEG_OC	EN_POS_OC	Reserved	Reserved 0	Reserved 1	Reserved 1	Reserved 0	Reserved 0

Field Name	Bits	Type	POR	Description
EN_NEG_OC	[7]	RW OTP	0x1	Enable negative OC/zero-crossing detection Value: 0x0 — 0: disable negative OC detection Value: 0x1 (POR) — 1: enable negative OC detection
EN_POS_OC	[6]	RW OTP	0x1	Enable positive OC detection Value: 0x0 — 0: disable positive OC detection Value: 0x1 (POR) — 1: enable positive OC detection

6.7.9 Register HVBUCK_CONF7

Address	Name	POR value
0x007B	HVBUCK_CONF7	0x19

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	TON_REF_SEL_DCM			Reserved 0	Reserved 1

Field Name	Bits	Type	POR	Description
TON_REF_SEL_DCM	[4:2]	RW OTP	0x6	When loop enters DCM (with hvbk_dcm_th), change Ton Value: 0x0 — 000: DCM Ton=60%*(CCM Ton) Value: 0x1 — 001: DCM Ton=80%*(CCM Ton) Value: 0x2 — 010: DCM Ton=100%*(CCM Ton) Value: 0x3 — 011: DCM Ton=110%*(CCM Ton) Value: 0x4 — 100: DCM Ton=120%*(CCM Ton) Value: 0x5 — 101: DCM Ton=130%*(CCM Ton) Value: 0x6 (POR) — 110: DCM Ton=140%*(CCM Ton) Value: 0x7 — 111: DCM Ton=150%*(CCM Ton)

6.7.10 Register HVBUCK_CONF16

Address	Name	POR value
0x0084	HVBUCK_CONF16	0x37

7	6	5	4	3	2	1	0
Reserved	DRVH_DET_FALL_DLY			Reserved 0	Reserved 1	DRVH_DRV2	

Field Name	Bits	Type	POR	Description
DRVH_DET_FALL_DLY	[6:4]	RW OTP	0x3	Filter time of DRVH=low detection Value / Description 0x0: 000: 0nS 0x1: 001: 5nS 0x2: 010: 10nS 0x3 (POR): 011: 15nS 0x4: 100: 20nS 0x5: 101: 25nS 0x6: 110: 35nS 0x7: 111: 55nS Value / Description 0x0: 000: 0nS 0x1: 001: 5nS 0x2: 010: 10nS 0x3 (POR): 011: 15nS 0x4: 100: 20nS 0x5: 101: 25nS 0x6: 110: 35nS 0x7: 111: 55nS
DRVH_DRV2	[1:0]	RW OTP	0x3	DRVH driving capability during rising interval T2 Value / Description 0x0: 00: x1 0x1: 01: x2 0x2: 10: x3 0x3 (POR): 11: x4

6.7.11 Register HVBUCK_CONF17

Address	Name	POR value
0x0085	HVBUCK_CONF17	0x55

7	6	5	4	3	2	1	0
DRVH_DRV1_DRV3		DRVHR_DLY3		DRVHR_DLY2		DRVHR_DLY1	

Field Name	Bits	Type	POR	Description
DRVH_DRV1_DRV3	[7:6]	RW OTP	0x1	DRVH driving capability during rising interval T1 and T3 Value: Description 0x0: 00: x1 0x1 (POR): 01: x2 0x2: 10: x3 0x3: 11: x4
DRVHR_DLY3	[5:4]	RW OTP	0x1	DRVH rising interval of T3 Value: Description 0x0: 00: 0nS 0x1 (POR): 01: 10nS 0x2: 10: 20nS 0x3: 11: 30nS
DRVHR_DLY2	[3:2]	RW OTP	0x1	DRVH rising interval of T2 Value: Description 0x0: 00: 3nS 0x1 (POR): 01: 6nS 0x2: 10: 9nS 0x3: 11: 12nS
DRVHR_DLY1	[1:0]	RW OTP	0x1	DRVH rising interval of T1 Value: Description 0x0: 00: 0nS 0x1 (POR): 01: 2nS 0x2: 10: 4nS 0x3: 11: 6nS

6.7.12 Register HVBUCK_CONF18

Address	Name	POR value
0x0086	HVBUCK_CONF18	0x36

7	6	5	4	3	2	1	0
Reserved	DRVL_DET_FALL_DLY			Reserved 0	Reserved 1	DRVL_DRV	

Field Name	Bits	Type	POR	Description
DRVL_DET_FALL_DLY	[6:4]	RW OTP	0x3	Filter time of DRVL=low detection Value: Description 0x0: 000: 0nS 0x1: 001: 5nS 0x2: 010: 10nS 0x3 (POR): 011: 15nS 0x4: 100: 20nS 0x5: 101: 25nS 0x6: 110: 35nS 0x7: 111: 55nS
DRVL_DRV	[1:0]	RW OTP	0x2	DRVL driving capability during rising and falling edges Value: Description 0x0: 00: x1 0x1: 01: x2 0x2 (POR): 10: x3 0x3: 11: x4

6.7.13 Register HVBUCK_CONF19

Address	Name	POR value
0x0087	HVBUCK_CONF19	0x54

7	6	5	4	3	2	1	0
DRVL_DLY		DRVHF_DLY3		DRVHF_DLY2		DRVHF_DLY1	

Field Name	Bits	Type	POR	Description
DRVL_DLY	[7:6]	RW OTP	0x1	DRVL rising and falling interval definition Value: Description 0x0: 00: 5nS 0x1 (POR): 01: 10nS 0x2: 10: 15nS 0x3: 11: 20nS
DRVHF_DLY3	[5:4]	RW OTP	0x1	DRVH falling interval of T3 Value: Description 0x0: 00: 5nS 0x1 (POR): 01: 10nS 0x2: 10: 15nS 0x3: 11: 20nS
DRVHF_DLY2	[3:2]	RW OTP	0x1	DRVH falling interval of T2 Value: Description 0x0: 00: 3nS 0x1 (POR): 01: 6nS 0x2: 10: 9nS 0x3: 11: 12nS
DRVHF_DLY1	[1:0]	RW OTP	0x0	DRVH falling interval of T1 Value: Description 0x0 (POR): 00: 0nS 0x1: 01: 2nS 0x2: 10: 4nS 0x3: 11: 6nS

6.7.14 Register HVBUCK_CONF27

Address	Name	POR value
0x008F	HVBUCK_CONF27	0x7E

7	6	5	4	3	2	1	0
Reserved 0	Reserved 1	Reserved 1	Reserved 1	Reserved 1	Reserved 1	EN_PULL_LOW	Reserved 0

Field Name	Bits	Type	POR	Description
EN_PULL_LOW	[1]	RW OTP	0x1	Turn on low-side MOS when HV buck is off Value: 0x0 — 0: disable, always hvbk_pull_low_SW_HVBK=0 Value: 0x1 (POR) — 1: enable, hvbk_pull_low_SW_HVBK=1 when HV buck is off (before HV buck is turned on and after HV buck is turned off after DAC count to 0x0 plus hvbk_fccm_extend)

6.7.15 Register HVBUCK_CONF29

Address	Name	POR value
0x0091	HVBUCK_CONF29	0x1D

7	6	5	4	3	2	1	0
Reserved 0	Reserved 0	Reserved 0	Reserved 1	Reserved 1	Reserved 1	Reserved 0	EN_PWR_SW

Field Name	Bits	Type	POR	Description
EN_PWR_SW	[0]	RW OTP	0x1	Enable of power switching Value: 0x0 — 0: always turn off power switch between VINBK1 pin (HV buck output) and AVDD_HVBK pin. hvbk_sw_vinbk1=0 Value: 0x1 (POR) — 1: turn on power switch between VINBK1 pin (HV buck output) and AVDD_HVBK pin (hvbk_sw_vinbk1=1) after hvbk_pgood=1 for 1ms.

7 Application Information

7.1 Component Selection

7.1.1 Capacitors

Ref	Value	Tol.	Size [mm]	Height [mm]	Temp. Char.	Rating [V]	Part Number
AVDD	1 x 10 µF	±10 %	2012	1.45	X7R	10	C2012X7R1A106K125AC
AVDD_HVBK	1 x 10 µF	±10 %	2012	1.45	X7R	10	C2012X7R1A106K125AC
LDO5V	1 x 4.7 µF	±10 %	2012	1	X7R	10	C2012X7R1A475K085AC
LDO2P5V	1 x 1 µF	±10 %	1608	0.9	X7R	6.3	GRM188R70J105KA01D
VIN_Supply	1 x 100 nF	±10 %	1608	0.9	X7R	50	GRM188R71H104KA93D
	1 x 10 µF	±10 %	2012	1.45	X5R	35	C2012X5R1V106K125AC
VBuck1, VBuck2, VBuck3,	1 x 100 nF	±10 %	1608	0.9	X7R	50	GRM188R71H104KA93D
	1 x 10 µF	±10 %	2012	1.45	X5R	35	C2012X5R1V106K125AC
	2 × 47 µF	±20 %	2012	1.45	X5R	10	GRM21BR61A476ME15
HVBuck	2 x 100 nF	±10 %	1608	0.9	X7R	50	GRM188R71H104KA93D
	1 x 100 nF	±10 %	1608	0.9	X7R	16	GRM188R71C104KA01D
	4 x 10 µF	±20 %	3225	2.8	X7R	35	GJ832ER7YA106KA12
	10 × 47 µF	±20 %	2012	1.45	X5R	10	GRM21BR61A476ME15

7.1.2 Inductors

Ref	Value	ISAT [A]	IRMS [A]	DCR (typ) [mΩ]	Size (W×L×H) [mm]	Part Number
Buck1, Buck2, Buck3	1.5 µH	11.5	11	9.7	7.1×6.5×3	TDK SPM6530T -1R5M
		11.5	11	9.7	7.1×6.5×3	TDK SPM6530T -1R5M
		11.5	11	9.7	7.1×6.5×3	TDK SPM6530T -1R5M
HVBuck	1.5 µH	51	28	2.3	12.8x13.8x6.5	Cyntec CMLS136E-1R5MS

7.1.3 Resistors

Ref	Value	Tol.	Size [mm]	Height [mm]	Temp. Char.	Rating [W]	Part Number
HVBuck	0R	Jumper	1608	0.55	Jumper	0.1	RC0603JR-070RL
	24.9K	±1 %	1608	0.55	±100 ppm/°C	0.1	RC0603FR-0724K9L
	100K	±1 %	1608	0.55	±100 ppm/°C	0.1	RC0603FR-07100K9L

7.1.4 MOSFET

Ref	RDSON at VGS=4.5 V (mOhm)	Size (W×L×H) [mm]	VDS Rating [V]	Part Number
HVBuck	3.6	5.3x6.15x1	40	AON6232

7.2 PCB Layout Guide

7.2.1 LVBUCK converter

- Put all the power components Cin, L and Cout as close to chip as possible.
- Make the trace SWBK as thick and short as possible for lower parasitic impedances and lower EMI.
- Keep the trace FB_BK away from noisy trace for example: SWBK. And the start point of the FB_BK trace should be capacitor pad.
- Make the PGND loop trace as thick and short as possible to minimize the parasitic impedances.
- Make sure the power trace to load is thick enough or not too long when using the remote sensing topology. The parasitic inductance of the power trace should be lower than the equation as below.

$$\frac{1}{2\pi\sqrt{L_p \times C_{load}}} > 5 \times (unit\ gain\ bandwidth)$$

where the unit gain bandwidth is around 100KHz for PV88080 LVBUCKs. For example, if the Cload is 4.7µF, the Lp should lower than 21nH.

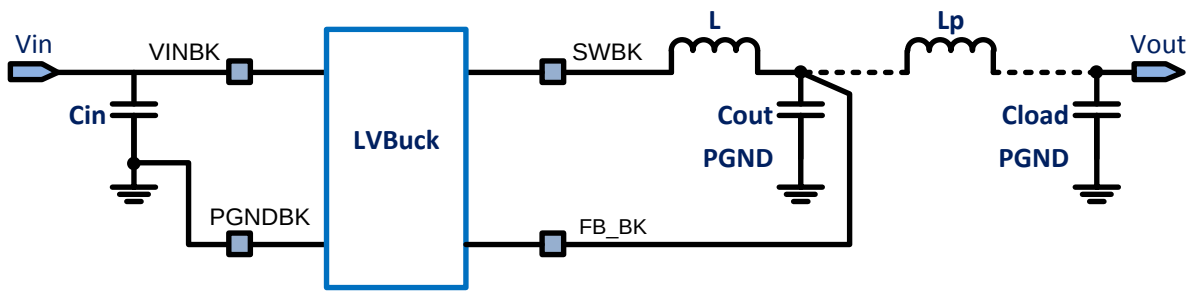


Figure 42: LVBUCK Converter Block

7.2.2 HVBUCK controller

- Put the capacitors CBST and CAVDD_HV as close to the chip as possible.
- Put the feedback divider RFB1 and RFB2 and feedforward capacitor CFF close to the chip.
- Keep the trace FBBK and FB_HVBK away from noisy trace for example: DRVH, DRVL, SW_HVBK. And the start point of the FBBK trace should be Cout capacitor pad.
- Put all the power components Cin, M1, M2, L and Cout as close as possible to minimize the power loop. And make sure all the power trace be thick and short.
- Do not cross over the trace DRVH with DRVL, adding GND between them.
- Do not cross over the trace DRVL with SW_HVBK, adding GND between them.

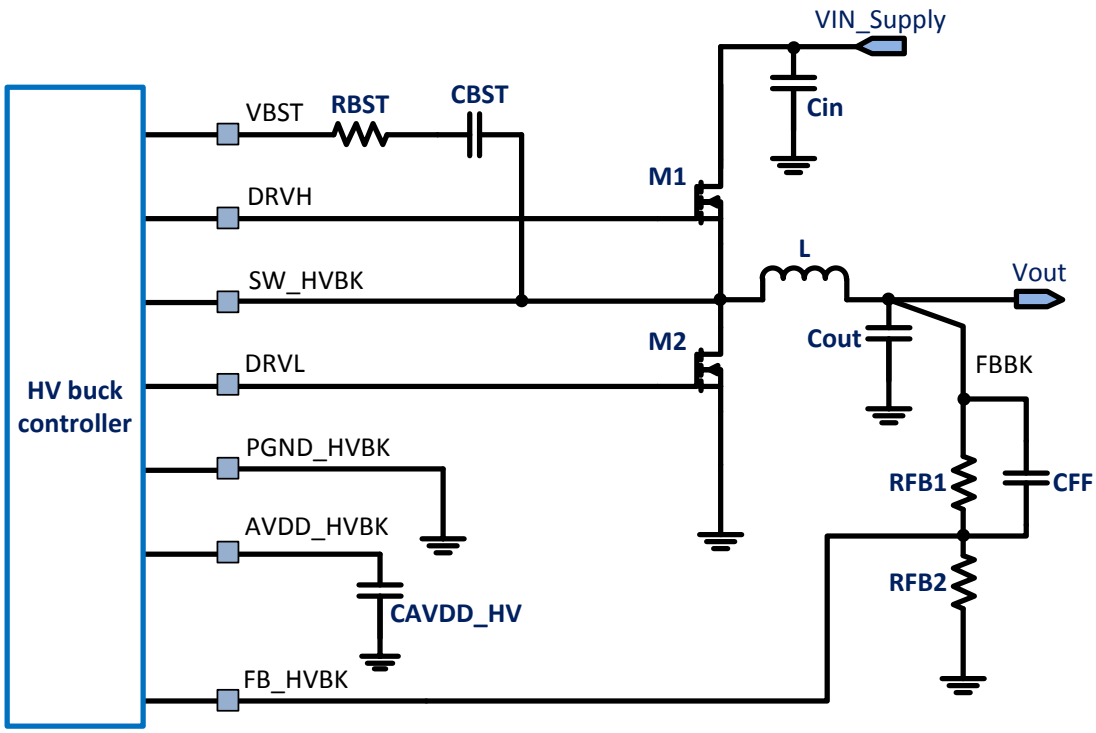


Figure 43: HVBUCK Controller Block

7.2.3 Other Stages

- Put the capacitors CHVLDO_in, CLDO_out, CAVDD_in and CLDO2_out as close to the chip as possible.
- Keep the I2C trace away from noisy trace, adding GND between SDA and SCL trace.
- Keep the trace GPIO2 away from noisy trace and keep RT as close to the chip when it be set to thermal sensing mode.
- Do not connect AGND to PGND directly. Using a 0R resistor or bead to connect them would be better.

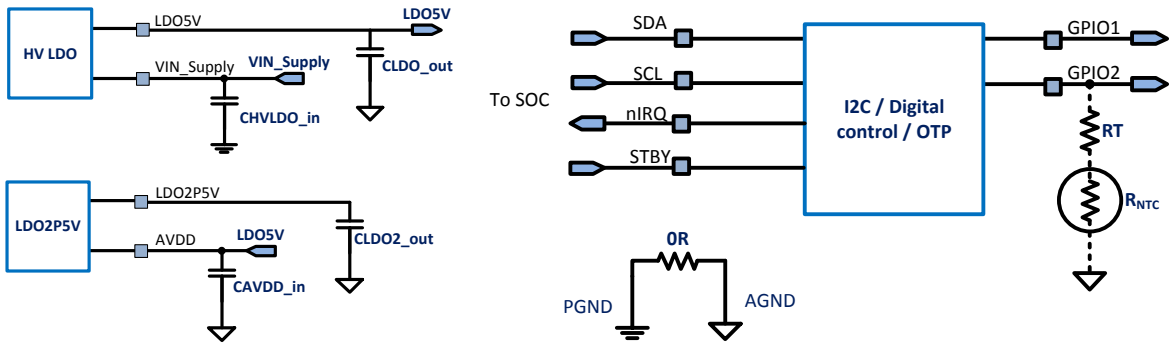


Figure 44: Analog and Digital Block

7.2.4 PCB Layout Reference

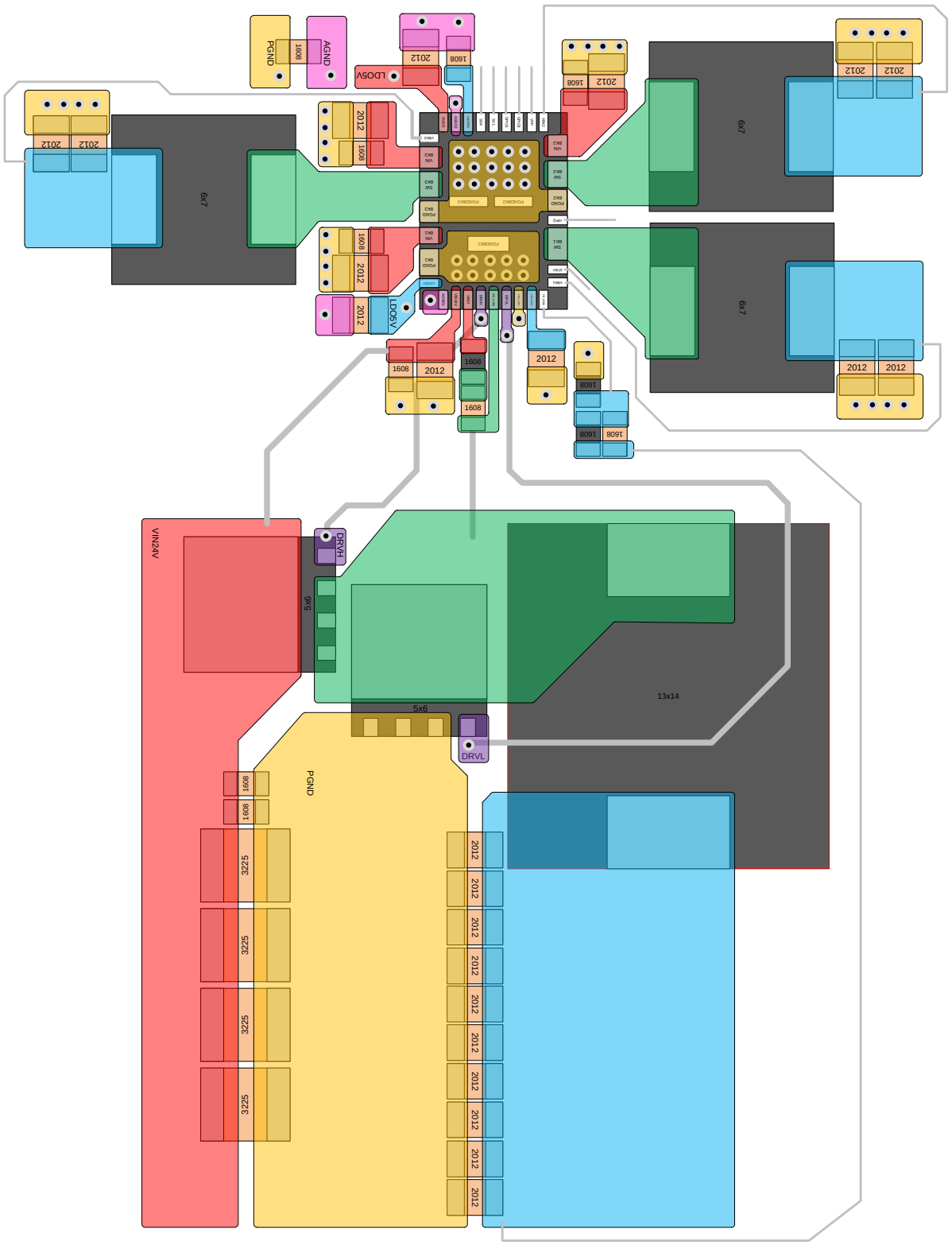
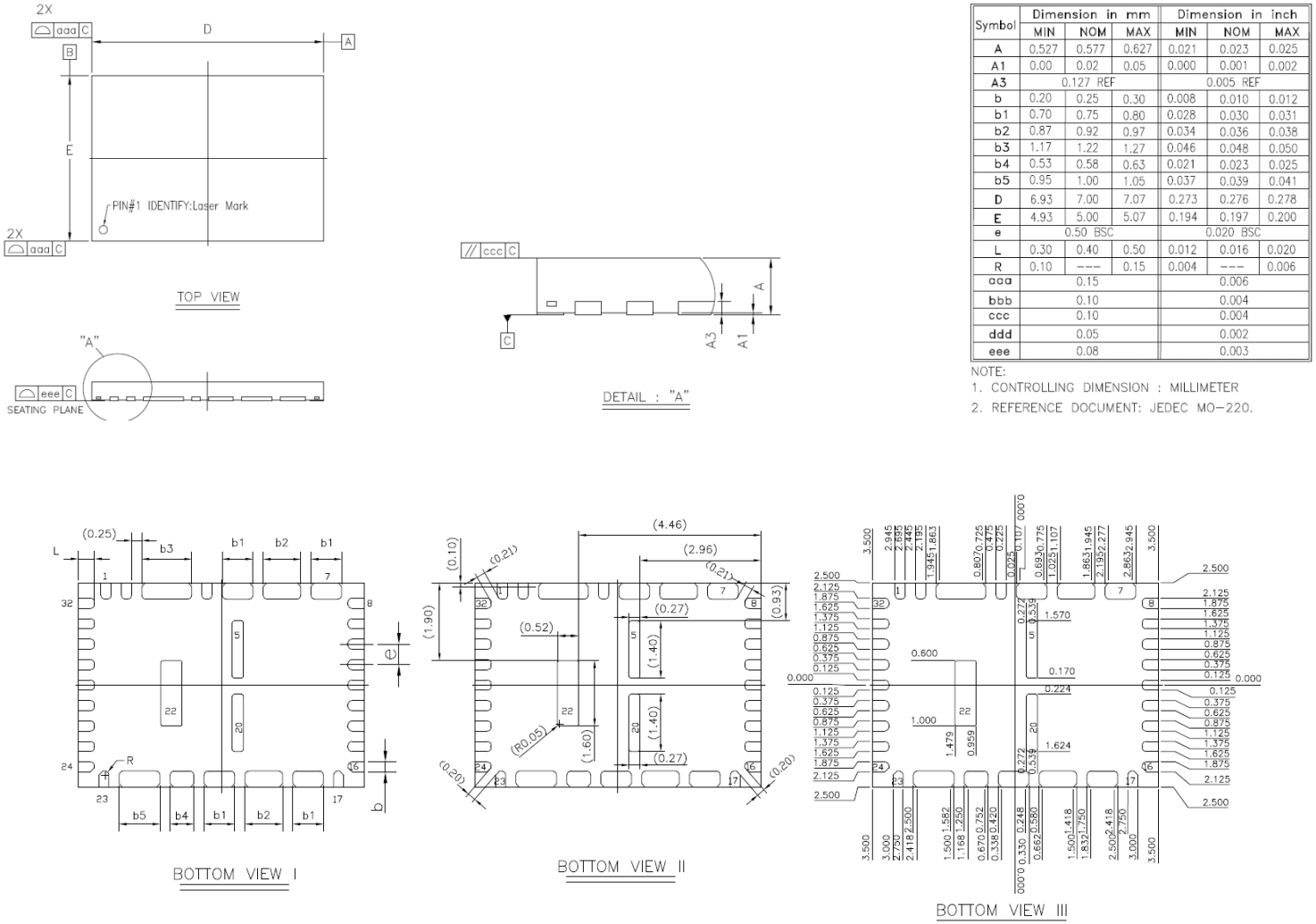


Figure 45: PCB Layout

8 Package Outline Drawing



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.527	0.577	0.627	0.021	0.023	0.025
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.127 REF			0.005 REF	
b	0.20	0.25	0.30	0.008	0.010	0.012
b1	0.70	0.75	0.80	0.028	0.030	0.031
b2	0.87	0.92	0.97	0.034	0.036	0.038
b3	1.17	1.22	1.27	0.046	0.048	0.050
b4	0.53	0.58	0.63	0.021	0.023	0.025
b5	0.95	1.00	1.05	0.037	0.039	0.041
D	6.93	7.00	7.07	0.273	0.276	0.278
E	4.93	5.00	5.07	0.194	0.197	0.200
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
R	0.10	---	0.15	0.004	---	0.006
aaa		0.15			0.006	
bbb		0.10			0.004	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 46: PV88080 Package Outline Drawing

9 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. The xxx represents a placeholder for the specific OTP variant. For details and availability, please consult Dialog Semiconductor's customer support portal or your local sales representative.

Table 24: Ordering Information

Part Number (Note 1)	Package Information	Package Description	Pack Outline
PV88080-xxxFR1	32 pin FC-MQFN	Waffle Tray	Figure 46
PV88080-xxxFR2	32 pin FC-MQFN	Tape and Reel	Figure 46

Note 1 xxx is the OTP variant. Please refer the detail information in OTP variant application note.

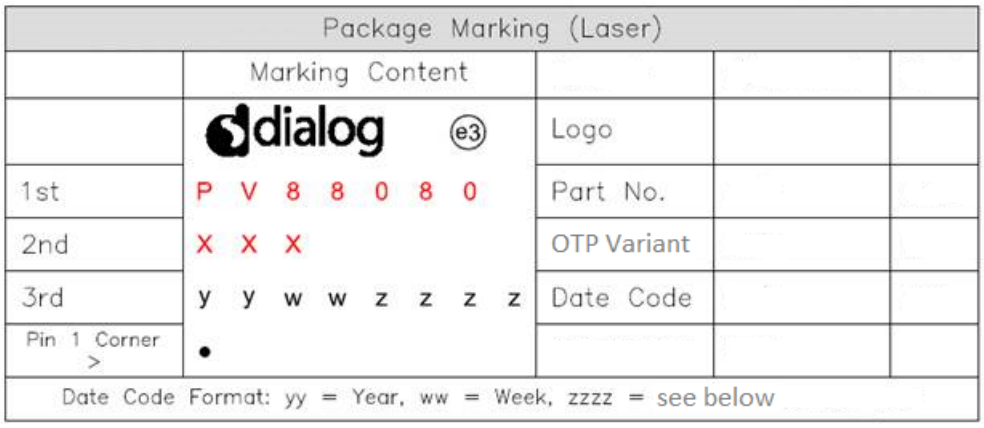


Figure 47: PV88080 Package Marking

Where zzzz = first z is wafer fab, second z is assembly supplier, third and fourth z are unique lot identifiers.

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
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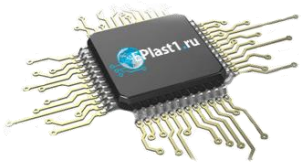

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